A Second Life for Flash With Page Isolation

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Flash Memory – we still depend on it

- **Sustainability** and Reliability
- Endurance limitation: wear-out by using (Program/Erase cycling)

thedrive.com

40 YEARS PC

Tesla Asked to Recall 158,000 Vehicles Over Flash Memory Failure

An issue with Model S and Model X flash memory storage can cause the media control unit to fail.

By Stephanie Mlot January 14, 2021

https://www.pcmag.com/news/tesla-asked-to-recall-158000-vehicles-over-flash-memory-failure

Problem

- System-level and Device-level mitigation techniques
  - over-provisioning, wear-leveling, read-retry, etc. – Active or Passive Recovery
- Can "bad" blocks be reused?

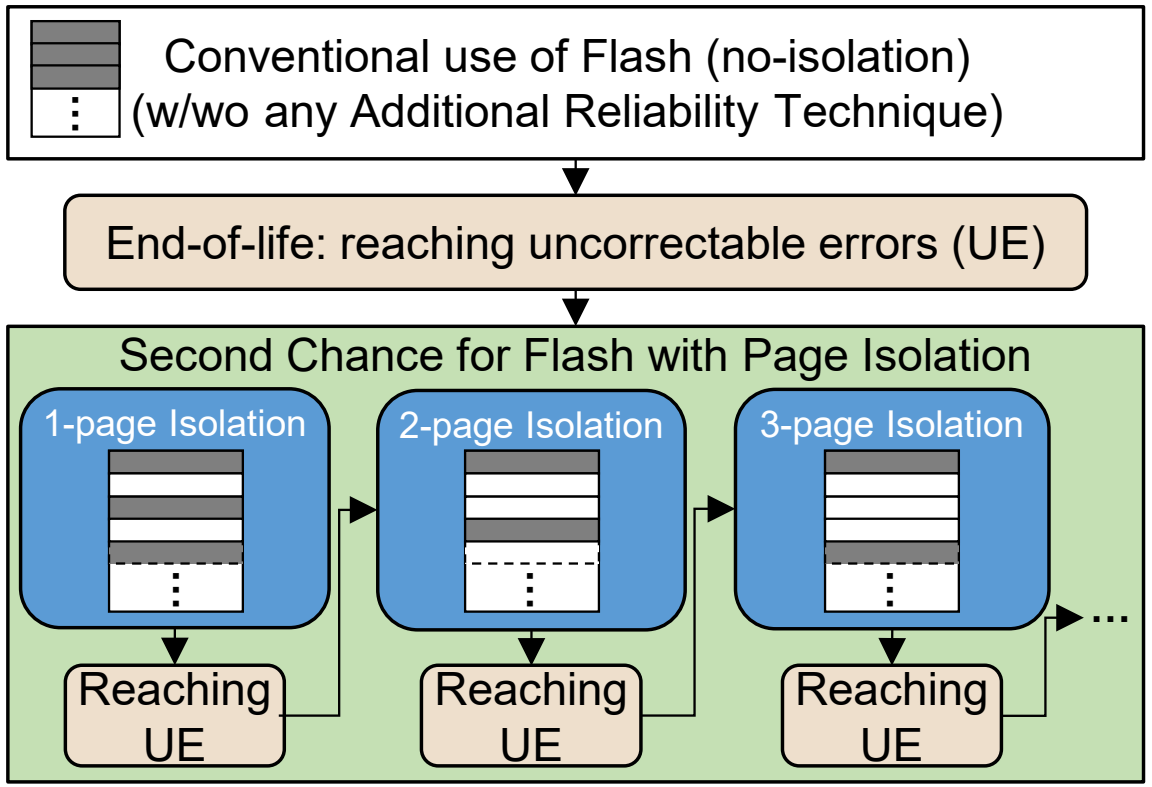
Solution

Page Isolation: enables the use of pages after life

https://www.tesla.com/support/8gb-emmc-recall-frequently-asked-questions

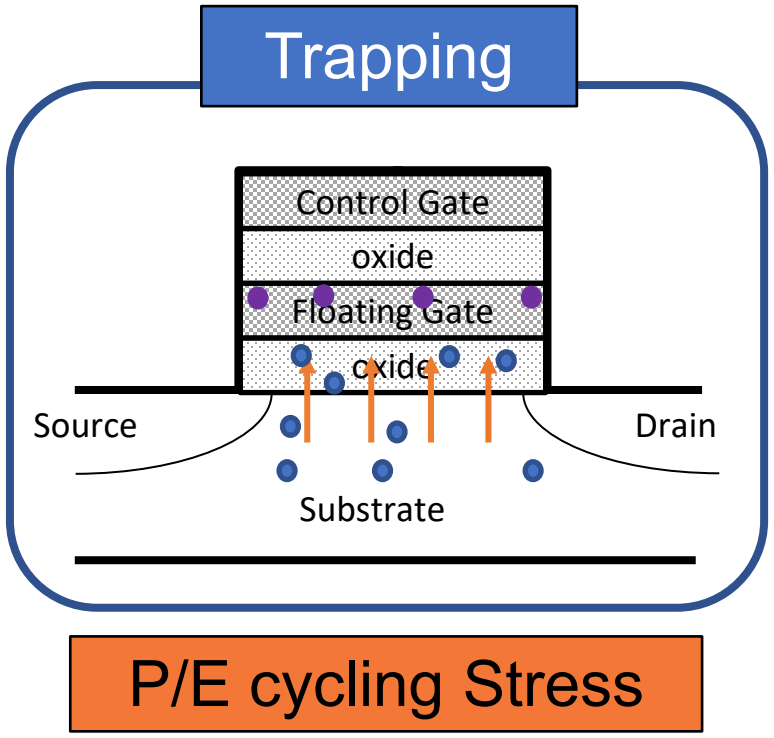
Outline

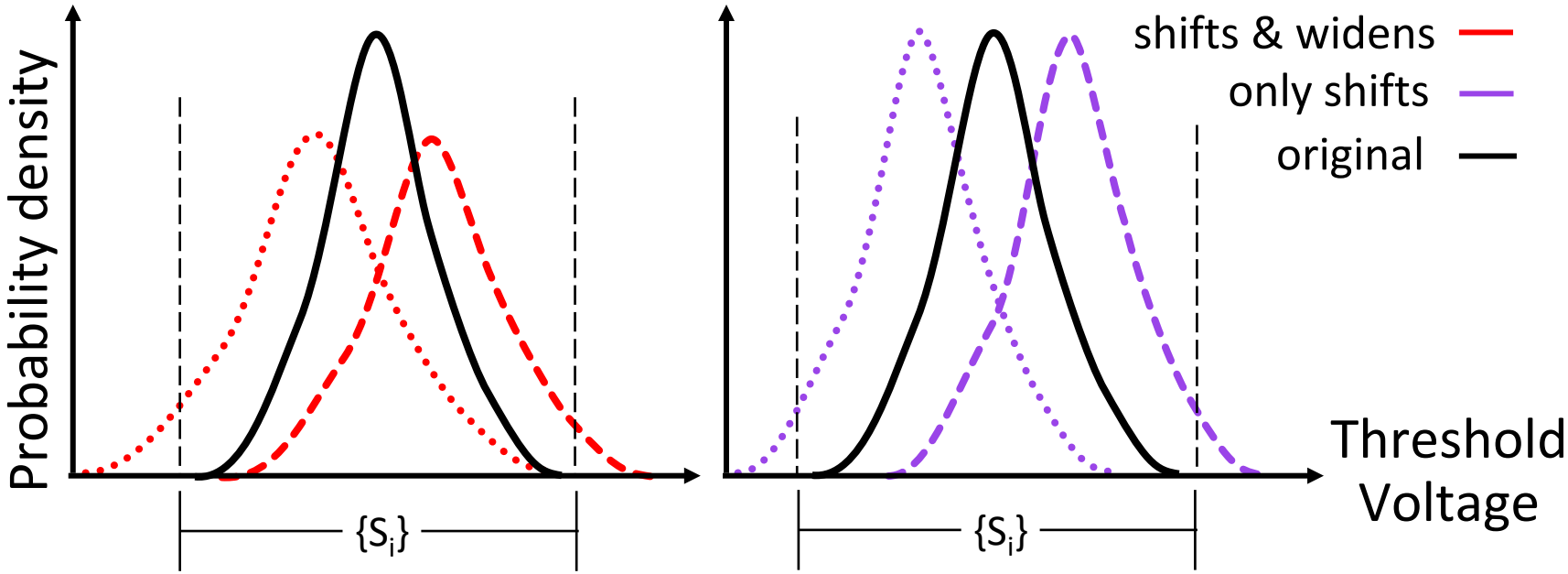
- We like Flash Memory
- [Device] Reliability of Flash
- [Circuit] Program Interference
- **Page Isolation**
- Experimental Results
- [System] SSD FTL Implementation
- Conclusion



Reliability of Flash

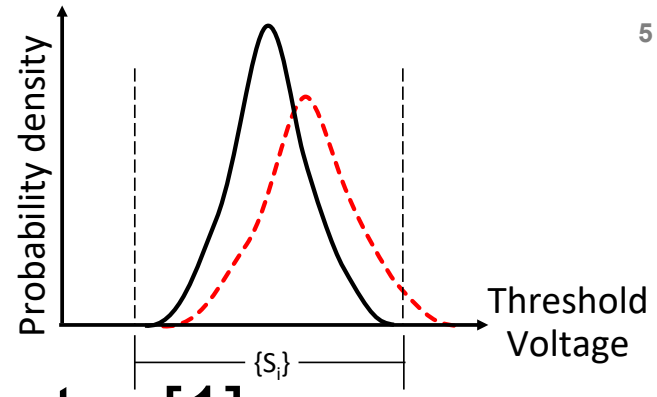
- Electrons are forcibly moved during Program and Erase operations
- Stress shifts and widens or only shifts threshold voltage pdf

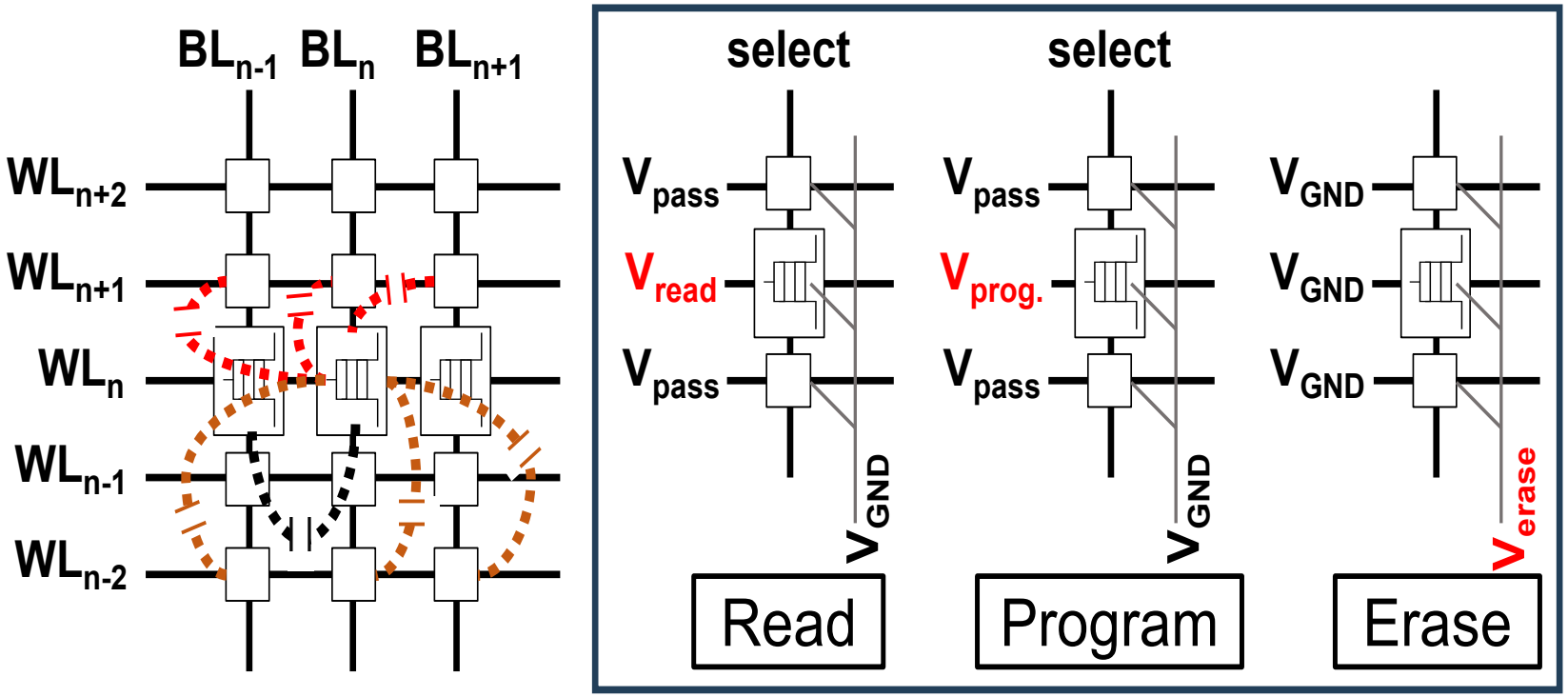


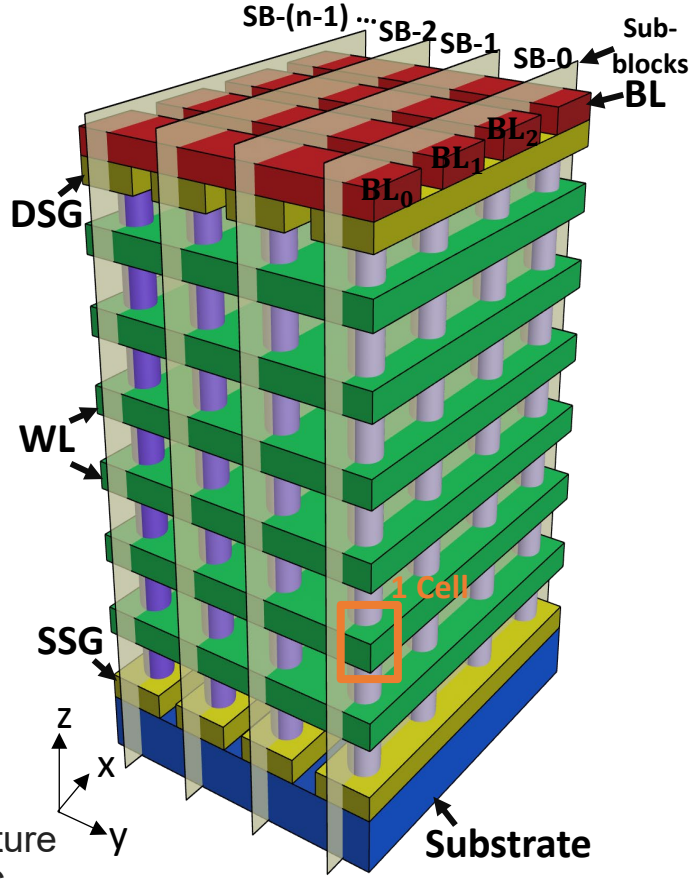


Programming Interference

- Cells are not independent
- Cell-to-cell interference is reported as dominant factor [1]





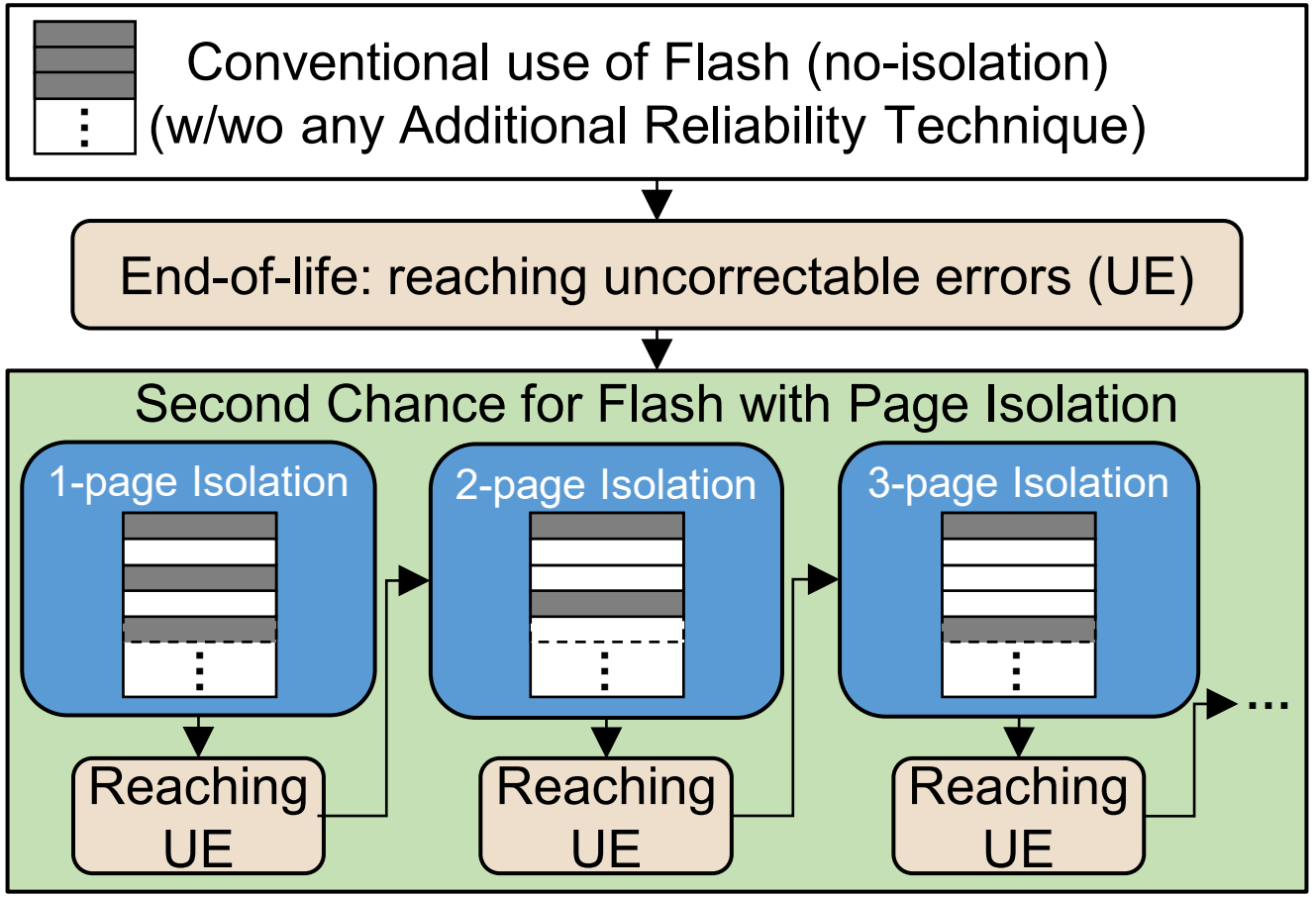


[1] Park, Ki-Tae, et al. "A zeroing cell-to-cell interference page architecture with temporary LSB storing and parallel MSB program scheme for MLC NAND flash memories." *IEEE JSSC 2008*

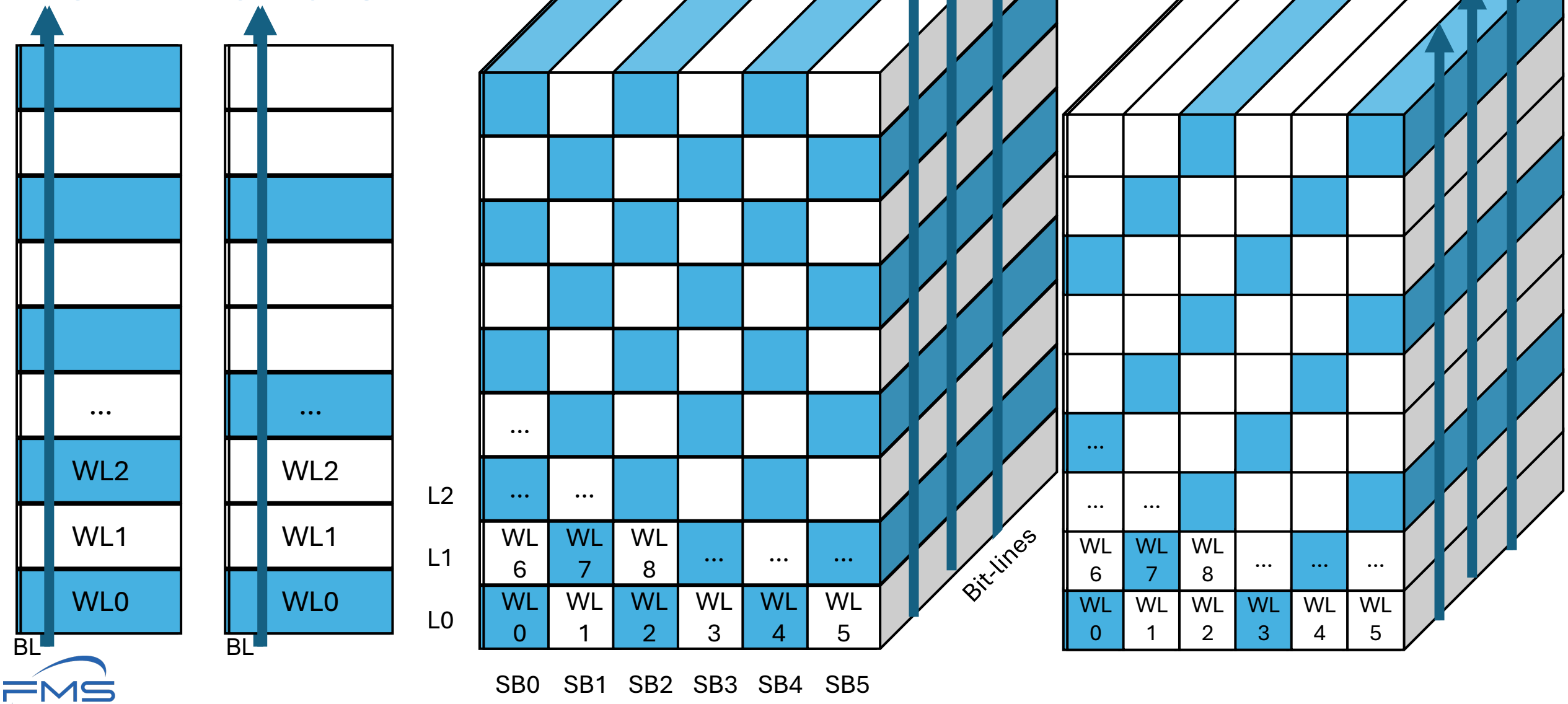
Page Isolation

Idea:

- Using some pages for isolation to mititgate page interference (and read disturb)
- Enables usage of blocks (pages) otherwise declared as «bad»
- Calibrate read current for low_level-to-high_level errors

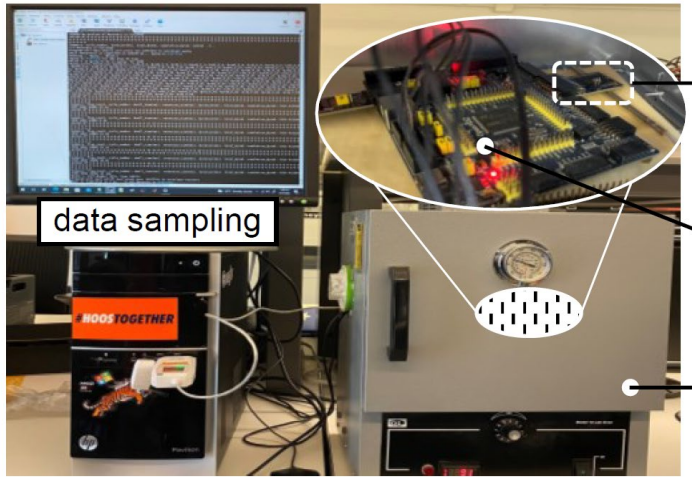


Page Isolation for 2D and 3D

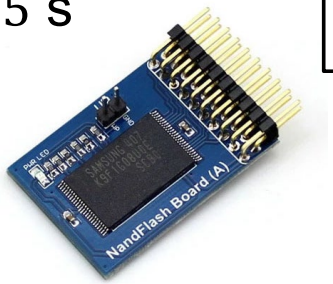


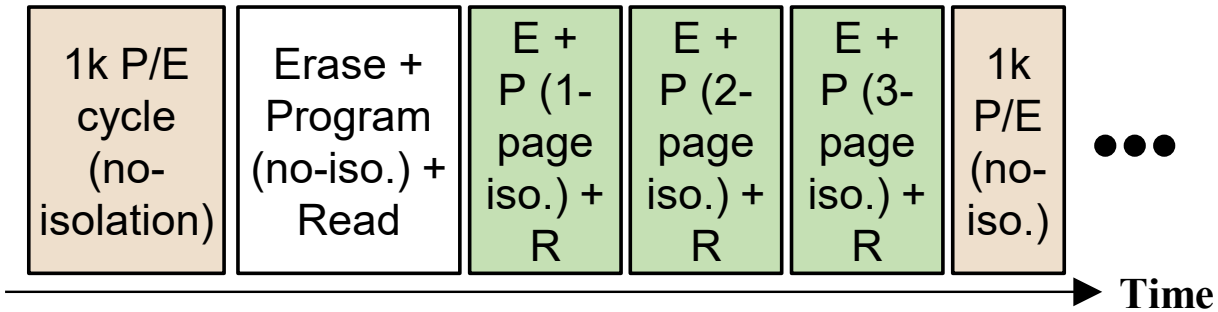
Experimental Setup

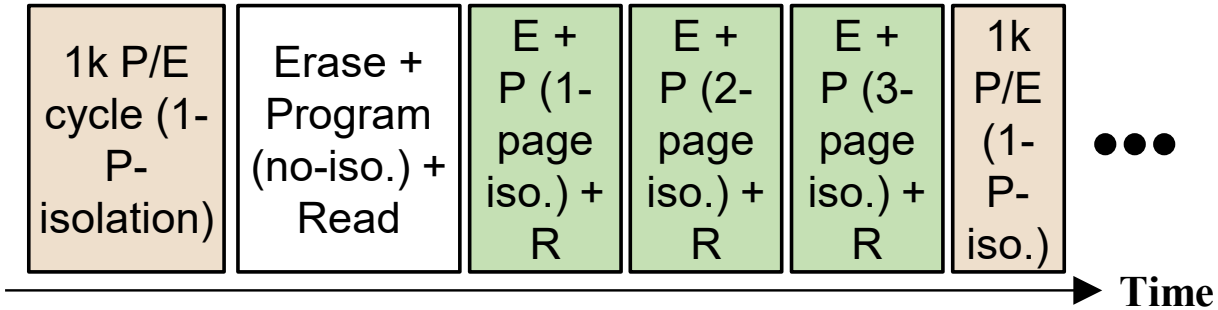
- 2D SLC NAND – floating gate
- 3D TLC NAND – charge trap
- no-ECC and no read-retry
- Data-0 and Random Data
- Tested at different temperatures

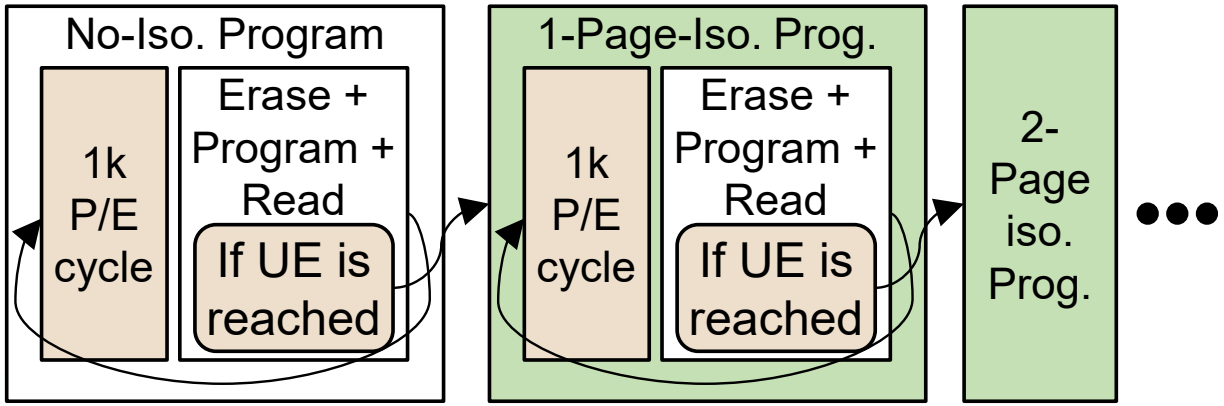


ECC-limit:
1 bit / (512+16 Byte)
dwell time:
1.5 s



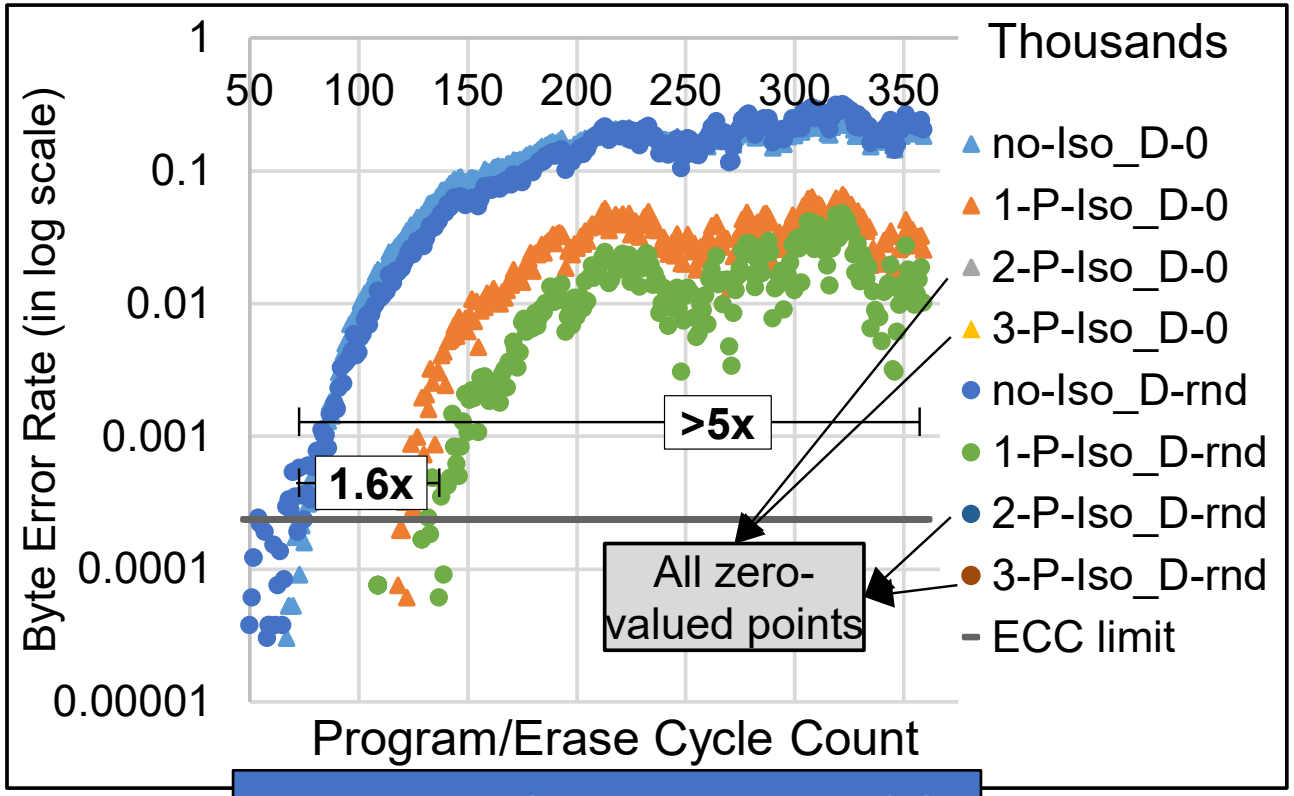




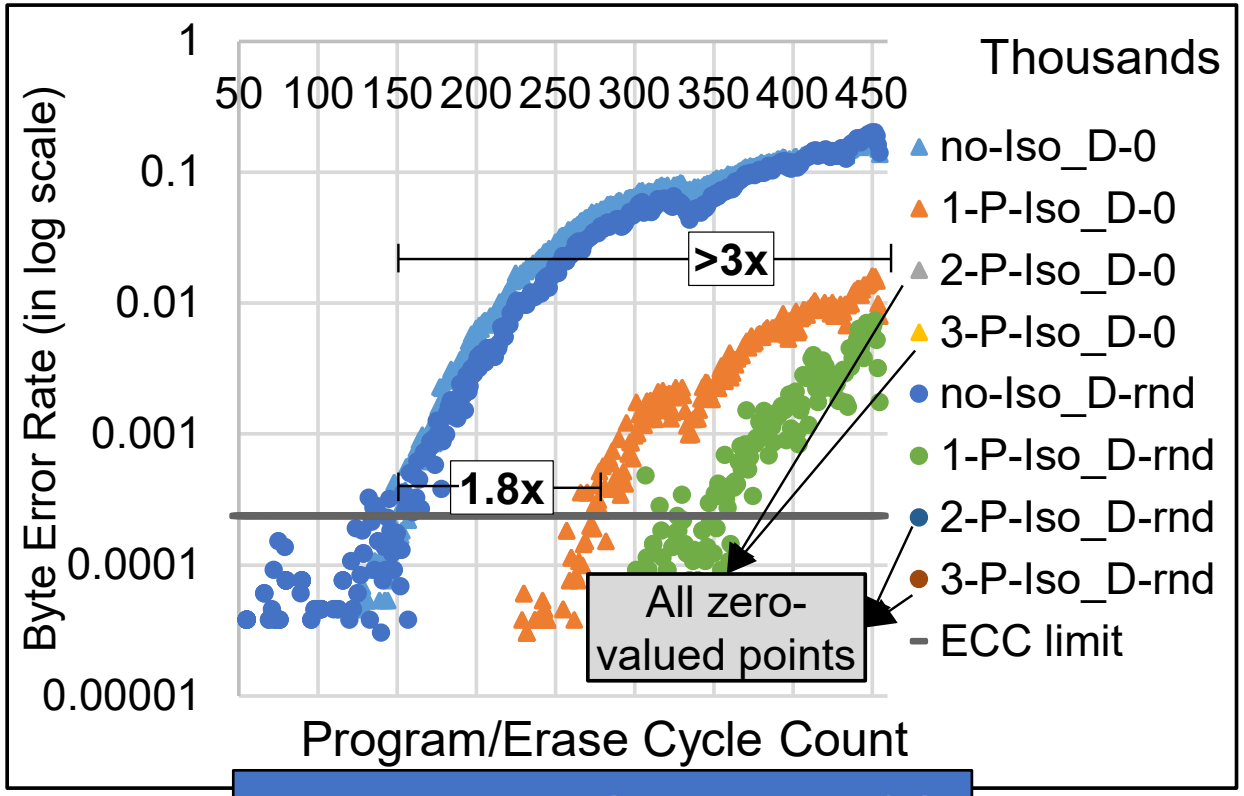


Page Isolation Enhances Reliability – 2D

- Page isolation reduces the error rate
- Presents additional the lifetime



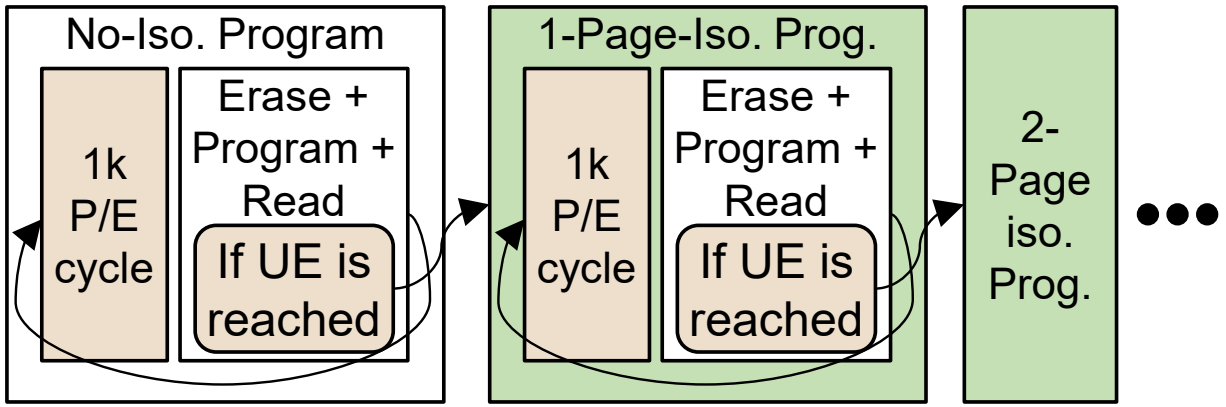
Regular Cycling at 50ºC

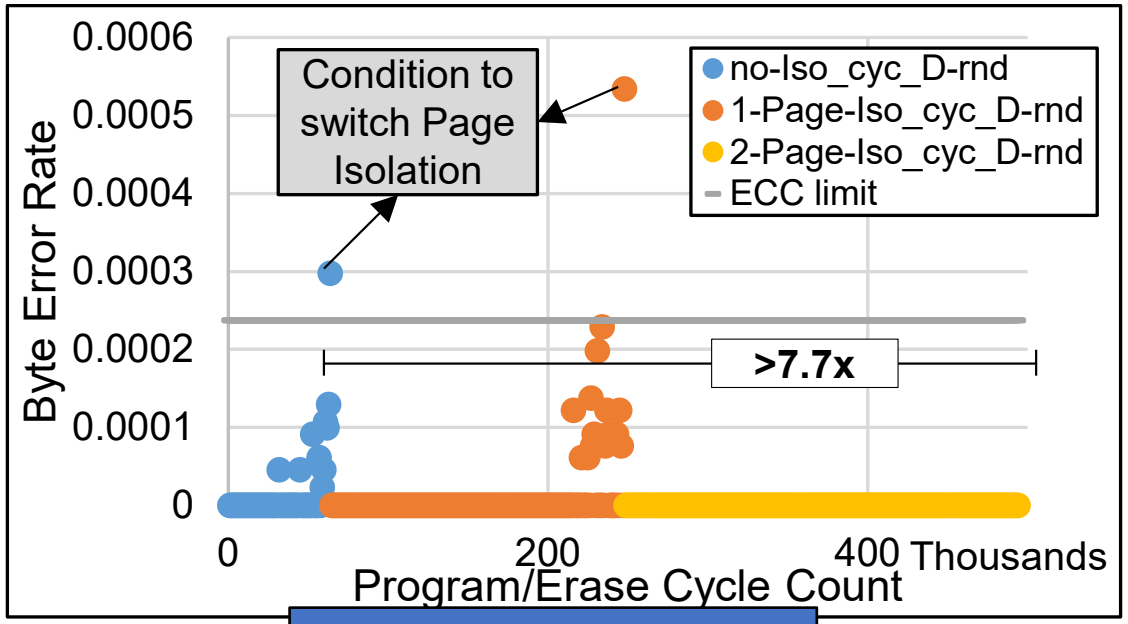


1-Page-Iso Cyc. at 50ºC

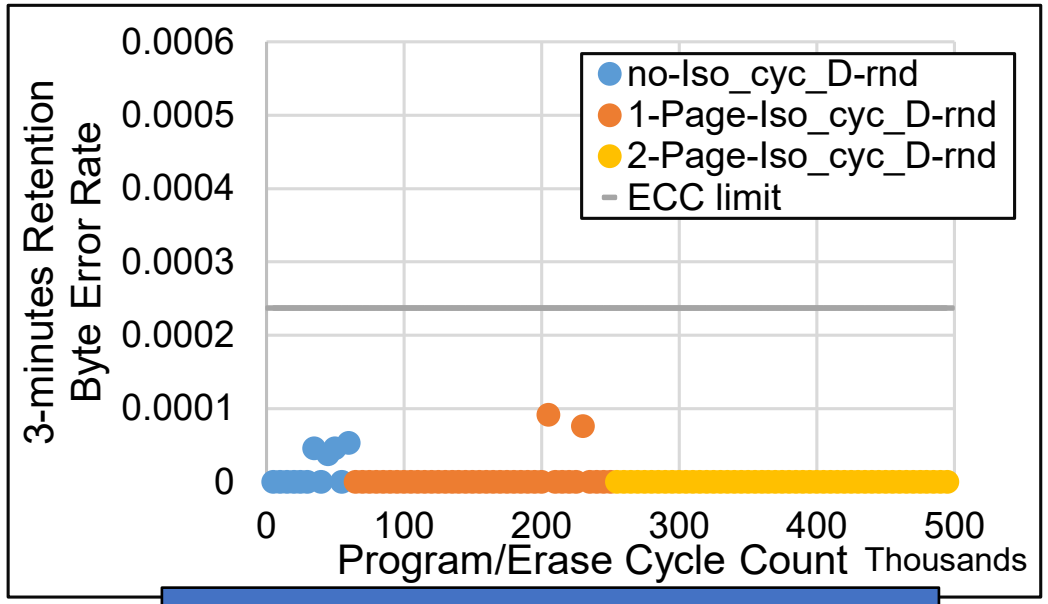
Life After Death with Page Isolation – 2D

- 50% of pages gets 3.5x extra life
- 33% of gets more than 7.7x





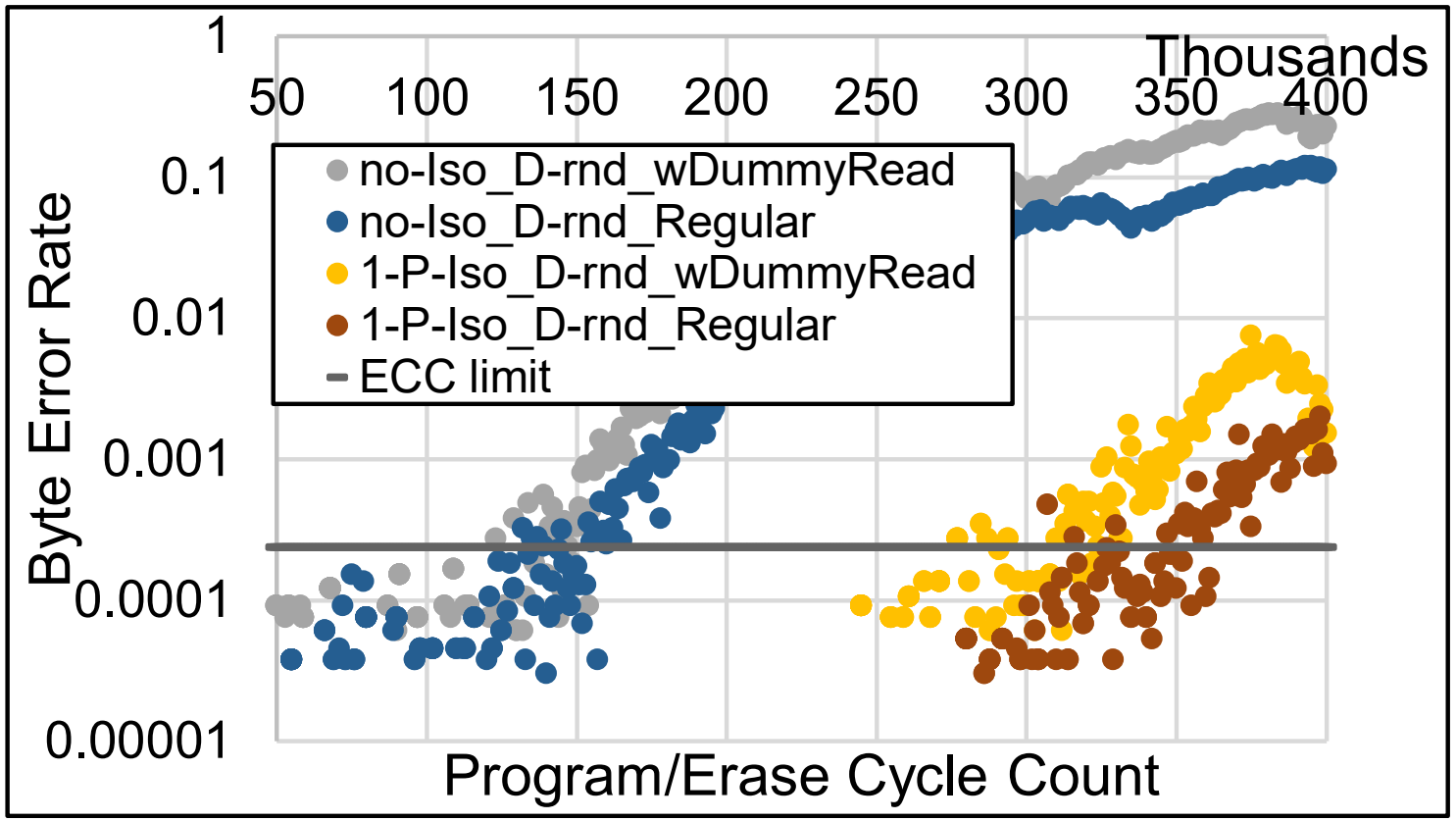
Time-0 at 50ºC



3-min Retention at 50ºC

Read Disturb vs Program Interference – 2D

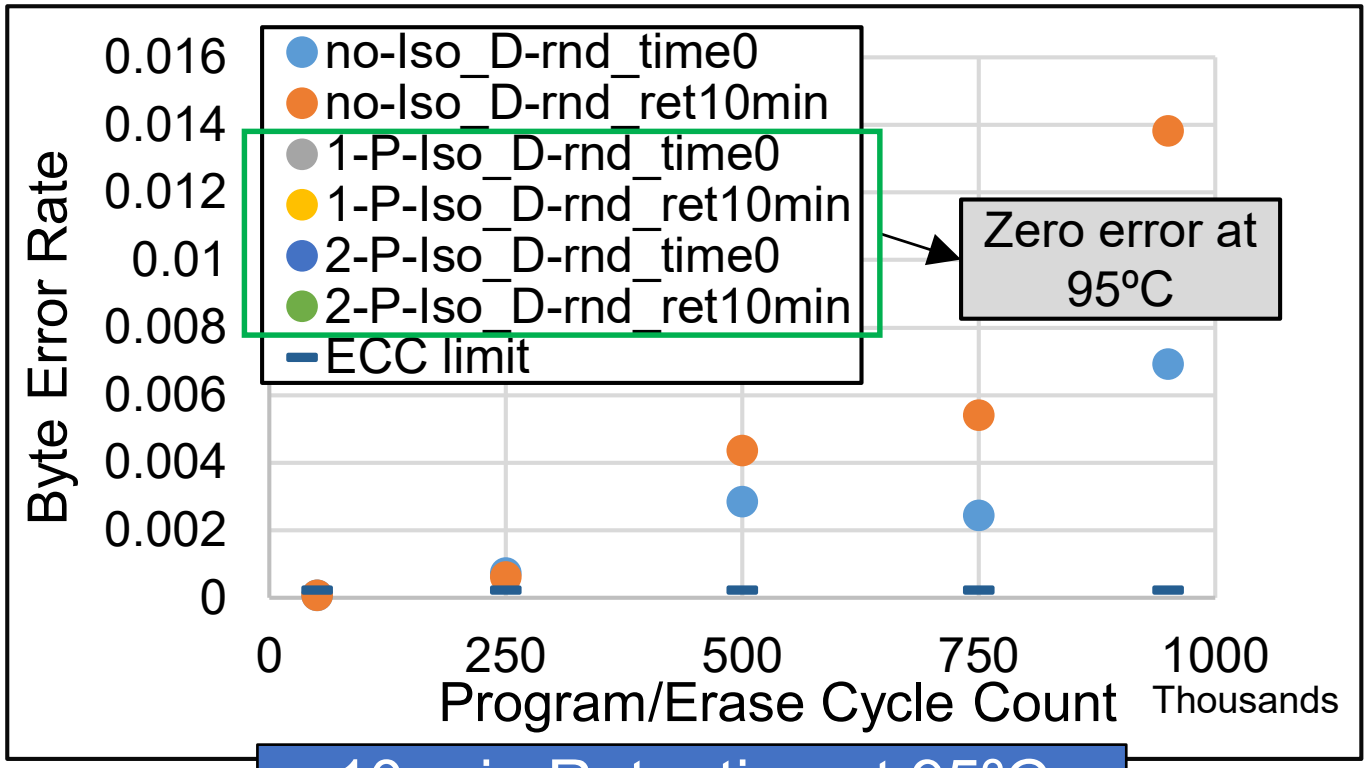
- 2.4x lifetime improvement with Read Disturb mitigation
- 2.3x lifetime improvement with equalized Read Disturb



1-Page-Iso Cycling at 50ºC

Retention and High Temperature – 2D

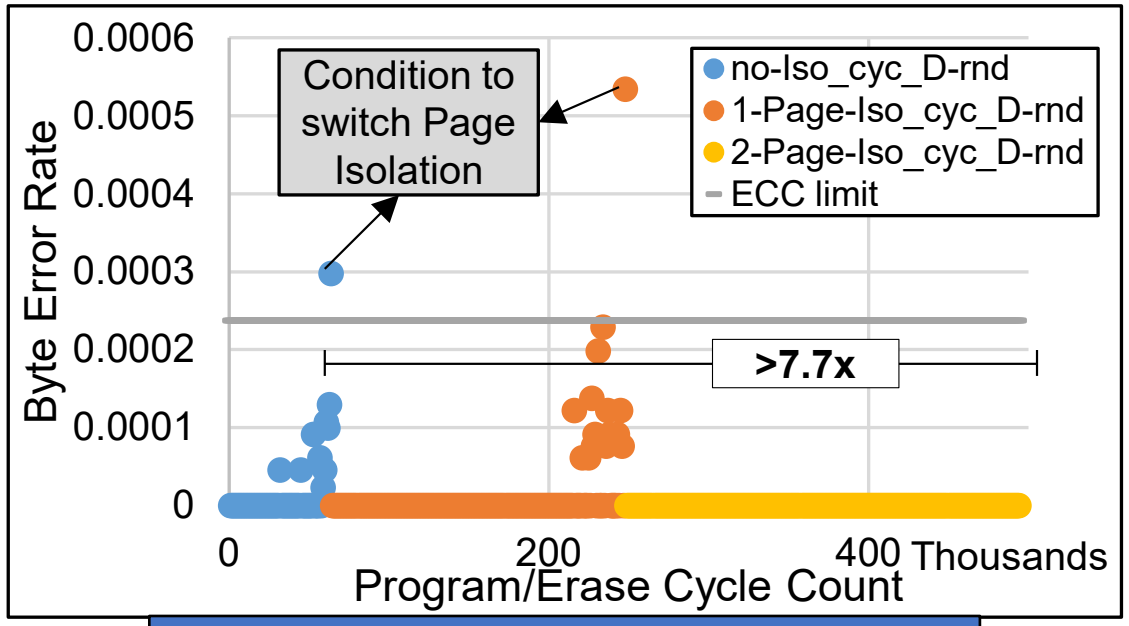
- Low (zero) error rate even at high temperature retention error



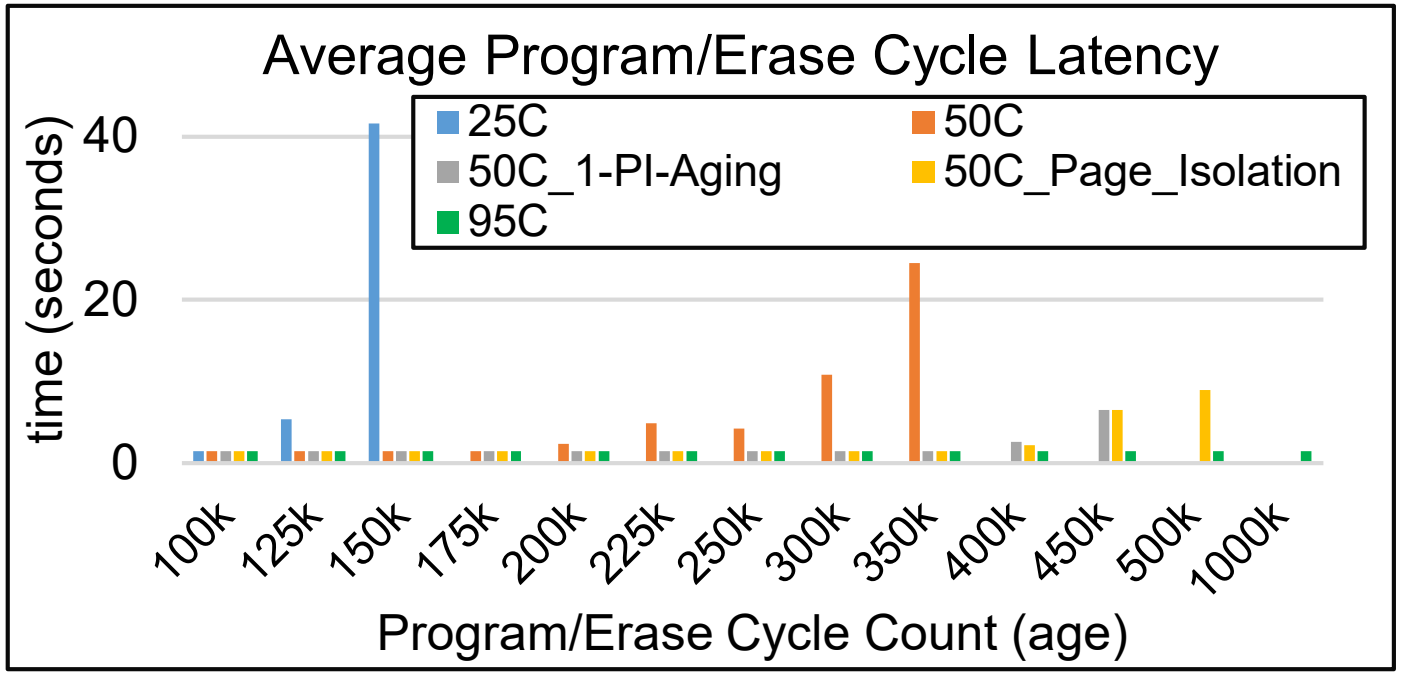
10-min Retention at 95ºC
Regular Cycling at 95ºC

It still ages: Cycling Latency – 2D

- 7.7x translates to 6.6x lifetime improvement for performance demanding applications

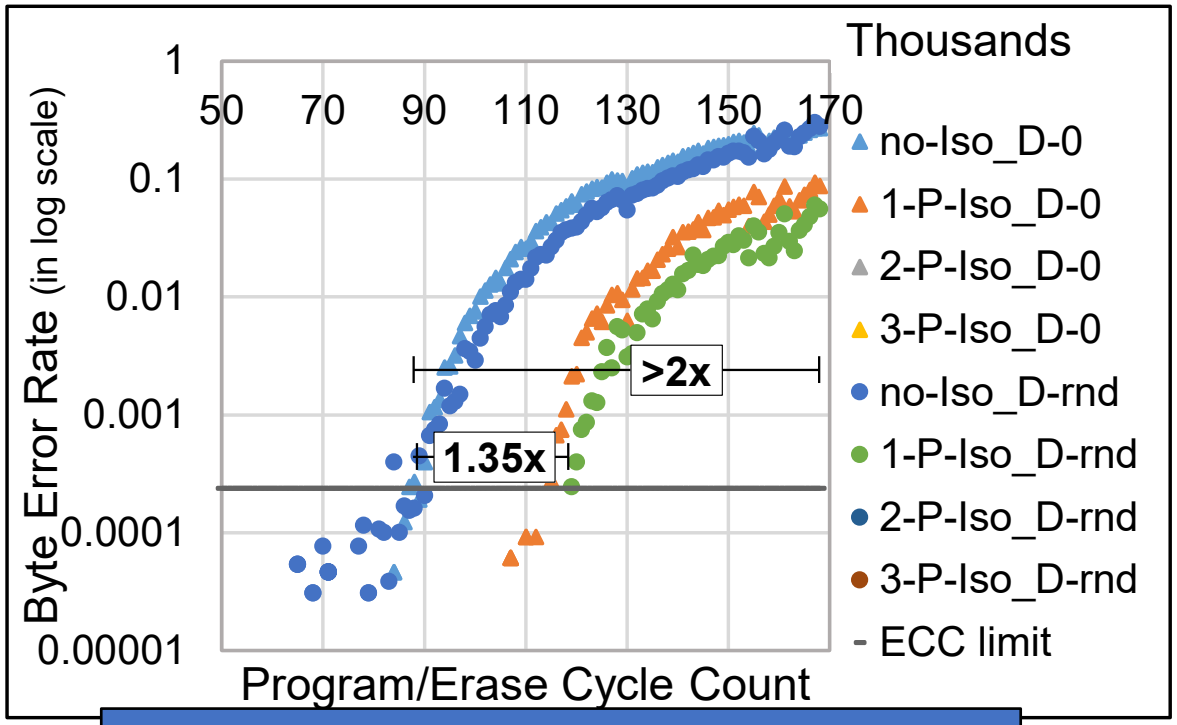


Page Isolation at 50ºC

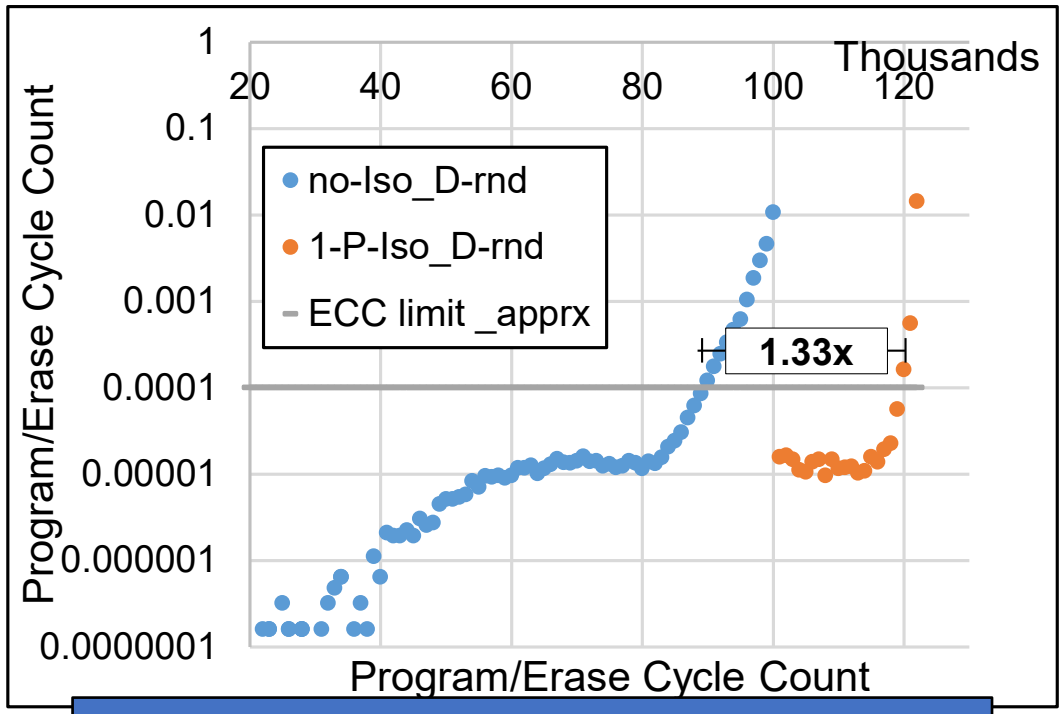


Life After Death with Page Isolation – 3D vs 2D (wip)

- 3D benefits Page Isolation less than 2D because of higher dependency – Increasing number of isolation page is needed



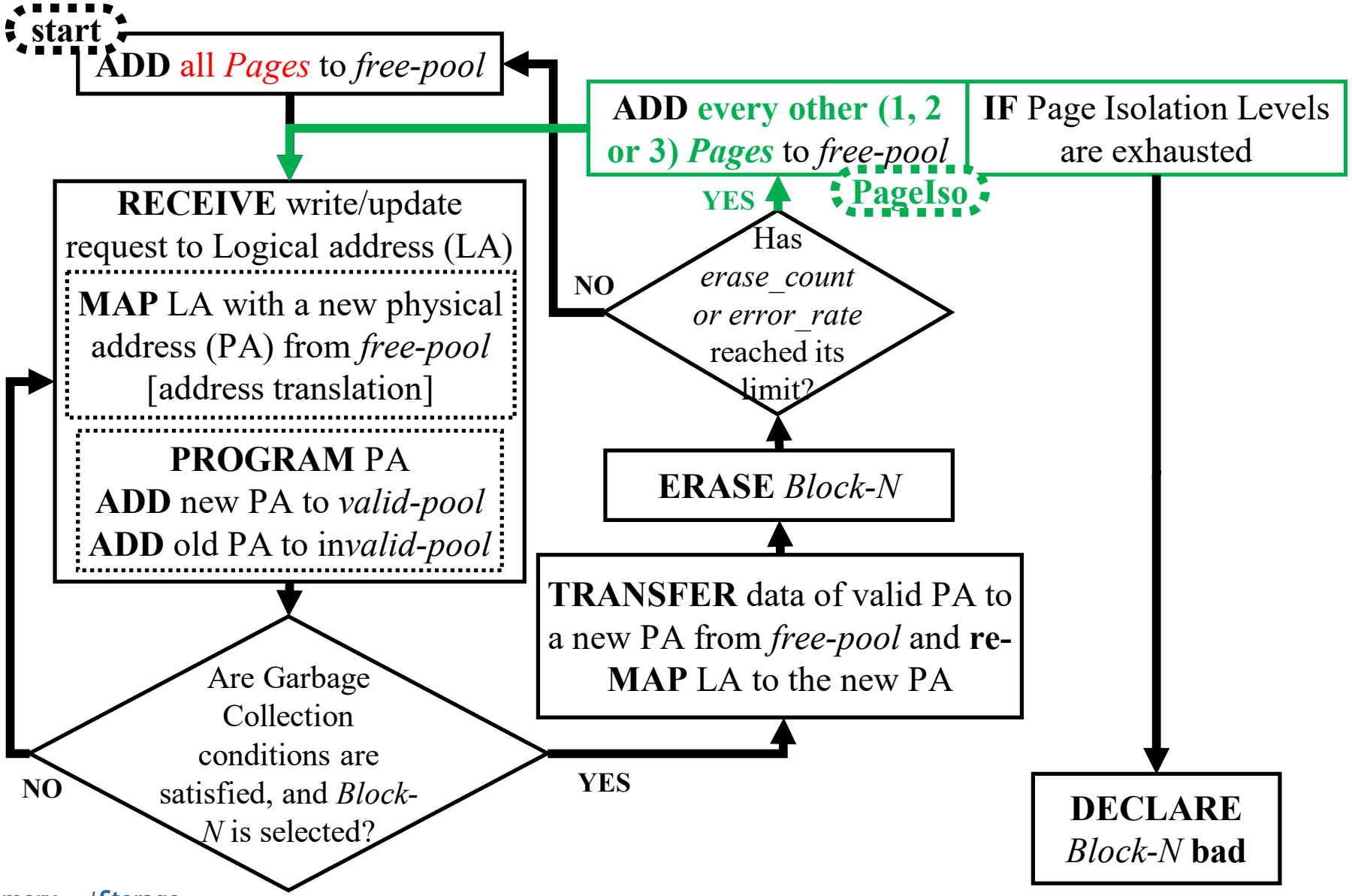
2D - Regular Cycling at **25ºC**



3D - Regular Cycling at **25ºC**

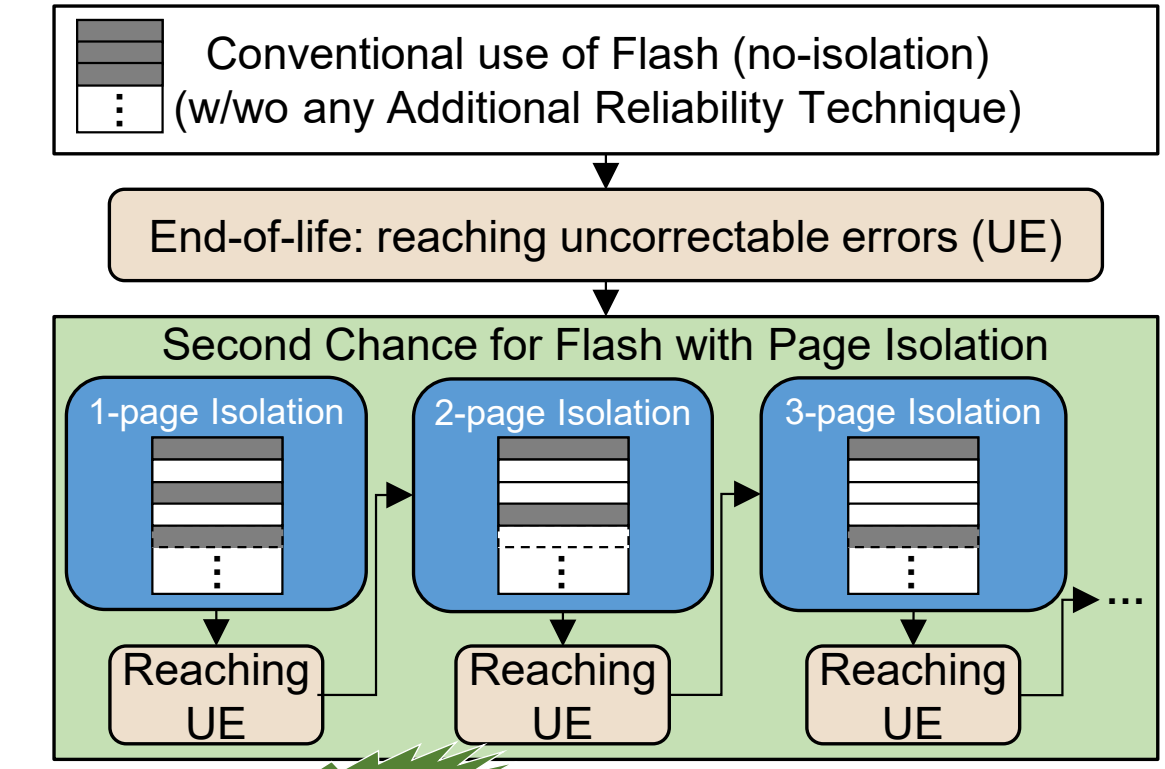
Time-0

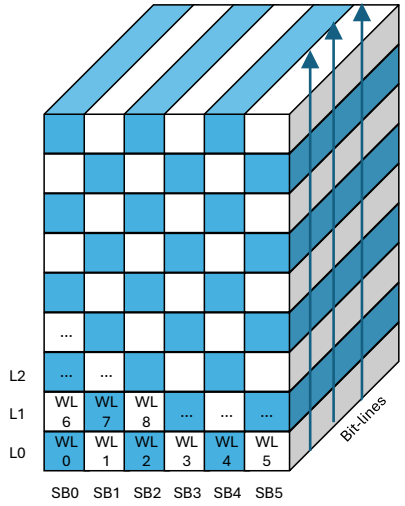
SSD FTL (Flash Translation Layer) Implementation



Conclusion

- Page Isolation:
  - For already aged blocks
  - At 50ºC, 3.5x lifetime for half of the capacity
    - >6x lifetime for 1/3 of the capacity
    - At 25ºC -> 1.3x
  - Easy to implement in SSD FTL
  - Reduces the capacity loss, which happens due to reliability (and the waste)





Acknowledgment

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