An Ultra-low-power LDPC Decoder Application in SLC Mode

Name: Mao-Ruei Li, PhD.

Title: Project Deputy Manager

Silicon Motion Technology Corp.

Legal Notice and Disclaimer

- The content of this document including, but not limited to, concepts, ideas, figures and architectures is furnished for informational use only, is subject to change without notice, and should not be construed as a commitment by Silicon Motion Inc. and its affiliates. Silicon Motion Inc. assumes no responsibility or liability for any errors or inaccuracies that may appear in the informational content contained in this document.
- Nothing in these materials is an offer to sell any of the components or devices referenced herein.
- Silicon Motion Inc. may have patents, patent applications, trademarks, copyrights, or other intellectual property rights covering subject matter in this document. Except as expressly provided in any written license agreement from Silicon Motion, Inc., the furnishing of this document does not give you any license to these patents, trademarks, copyrights, or other intellectual property.
- © 2025 Silicon Motion Inc. or its affiliates. All Rights Reserved.
- Silicon Motion, the Silicon Motion logo, MonTitan™, the MonTitan™ logo are trademarks or registered trademarks of Silicon Motion Inc.

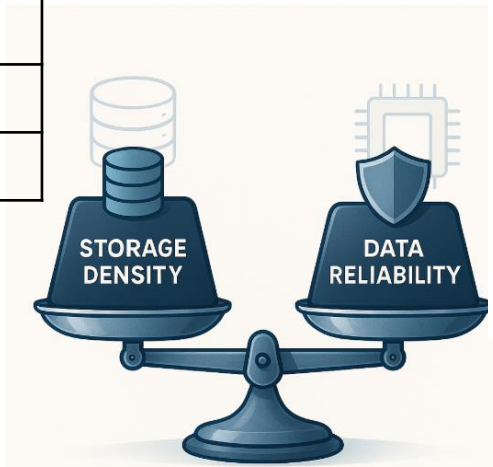
Outline

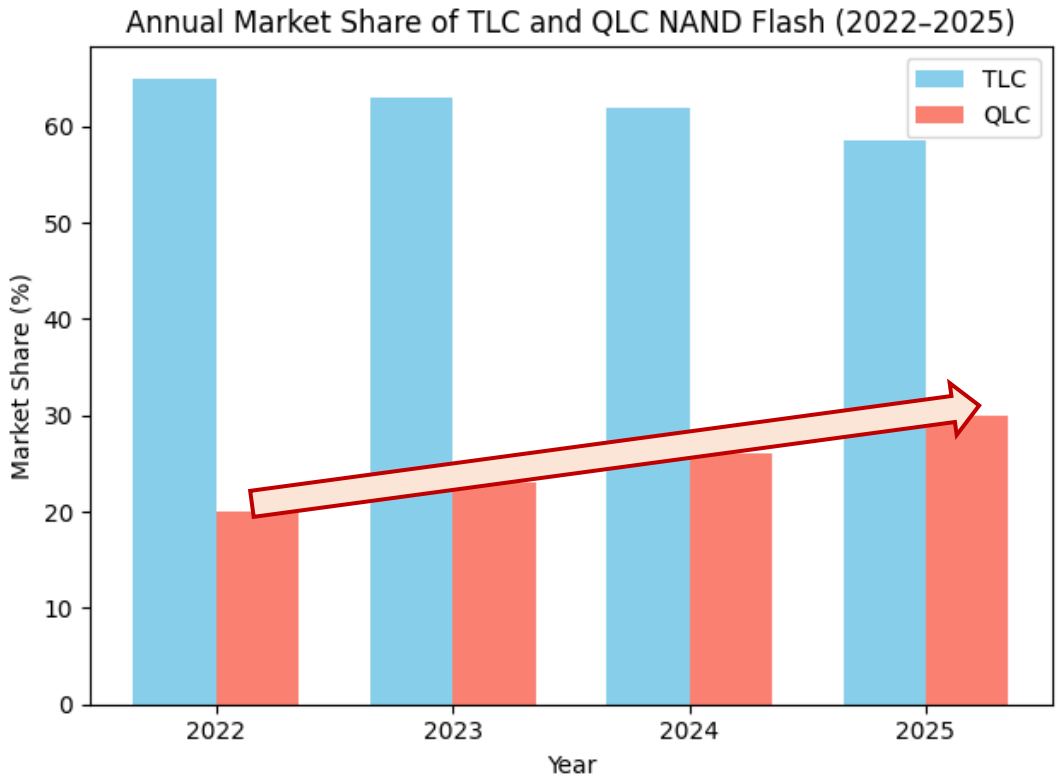
- Background
  - NAND Development
  - SLC-mode Error Characterization
- SMI Solution: SLC-mode Decoder
  - Ultra-low-power LDPC Decoder
  - Performance
- Application: SLC mode decoder with dynamic SLC

NAND Flash Trend

- QLC NAND Flash is becoming more common
  - Higher storage density
  - Lower cost
- QLC root cause: Density vs Reliability

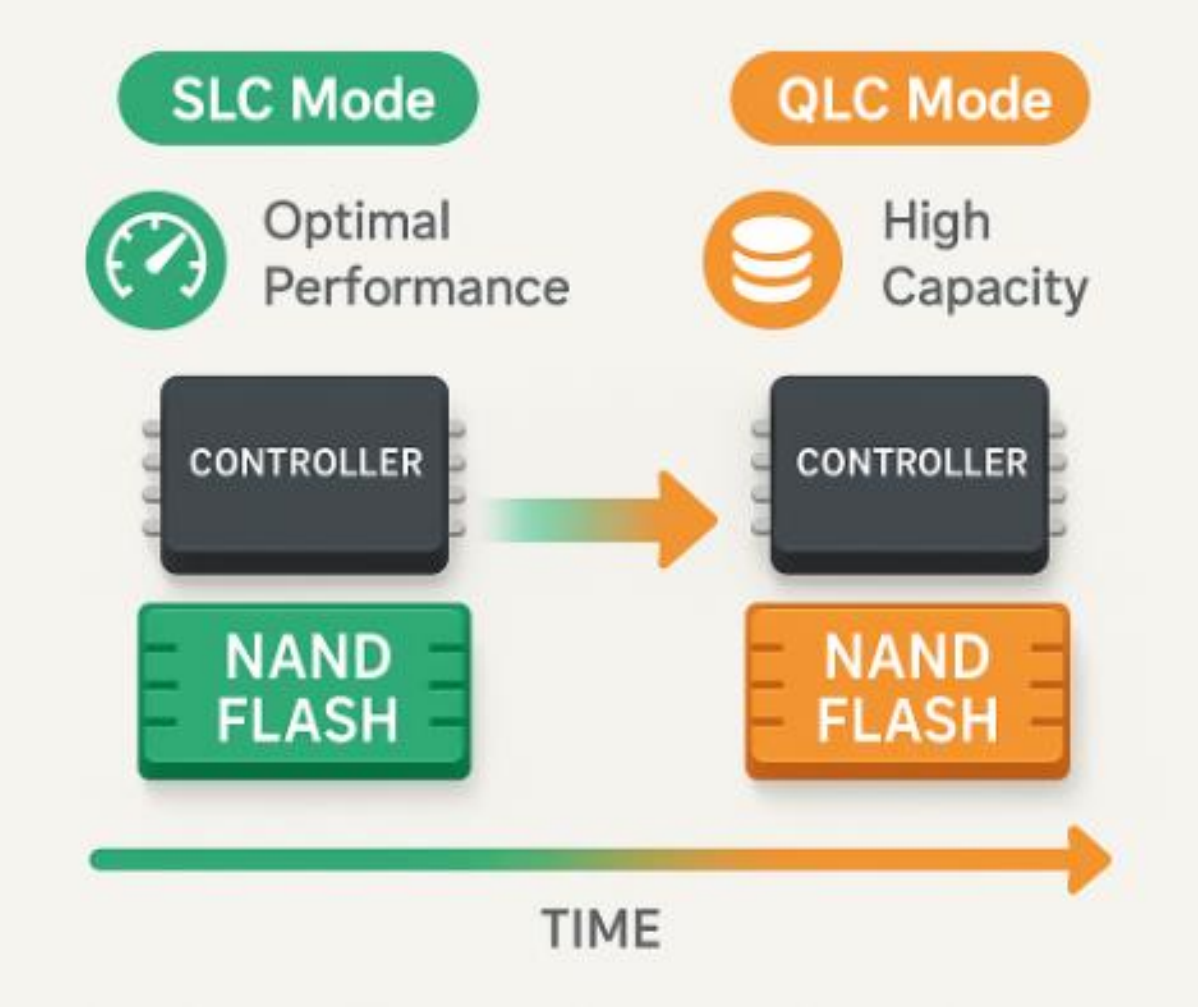
	Write latency	Read latency	PE cycle
SLC	0.5ms	10us	>100K
MLC	1.2ms	50us	10K
TLC	2.4ms	100us	3K
QLC	10-20ms	150-200us	~1K





SLC Mode (pseudo-SLC)

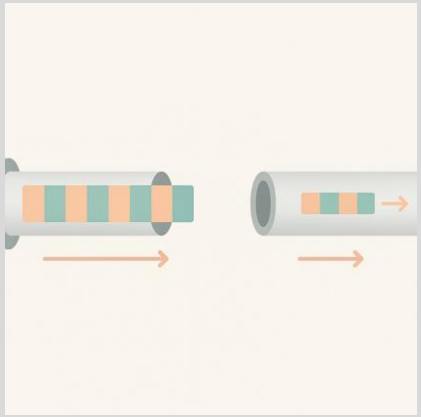
- SLC mode reduces the number of bits stored in each cell to one.
  - Reduce the amount of stored bits in each cell
  - Increase the reliability and lifetime
  - Decrease read/write latency



SLC Mode Decoder

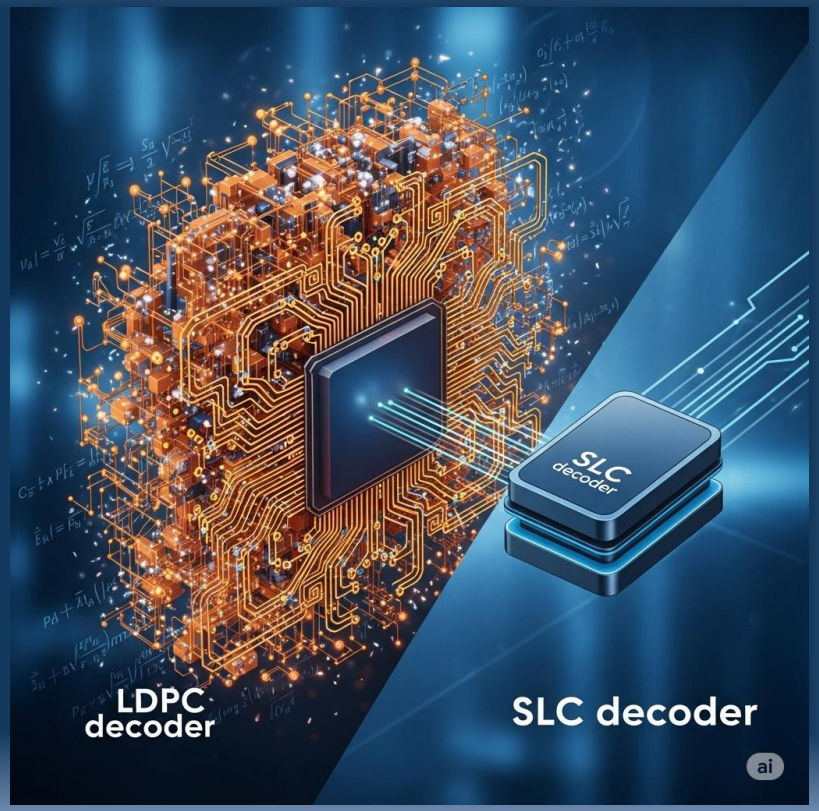
Traditional SLC-aware methods

Less accurate reads/program to reduce array busy time.



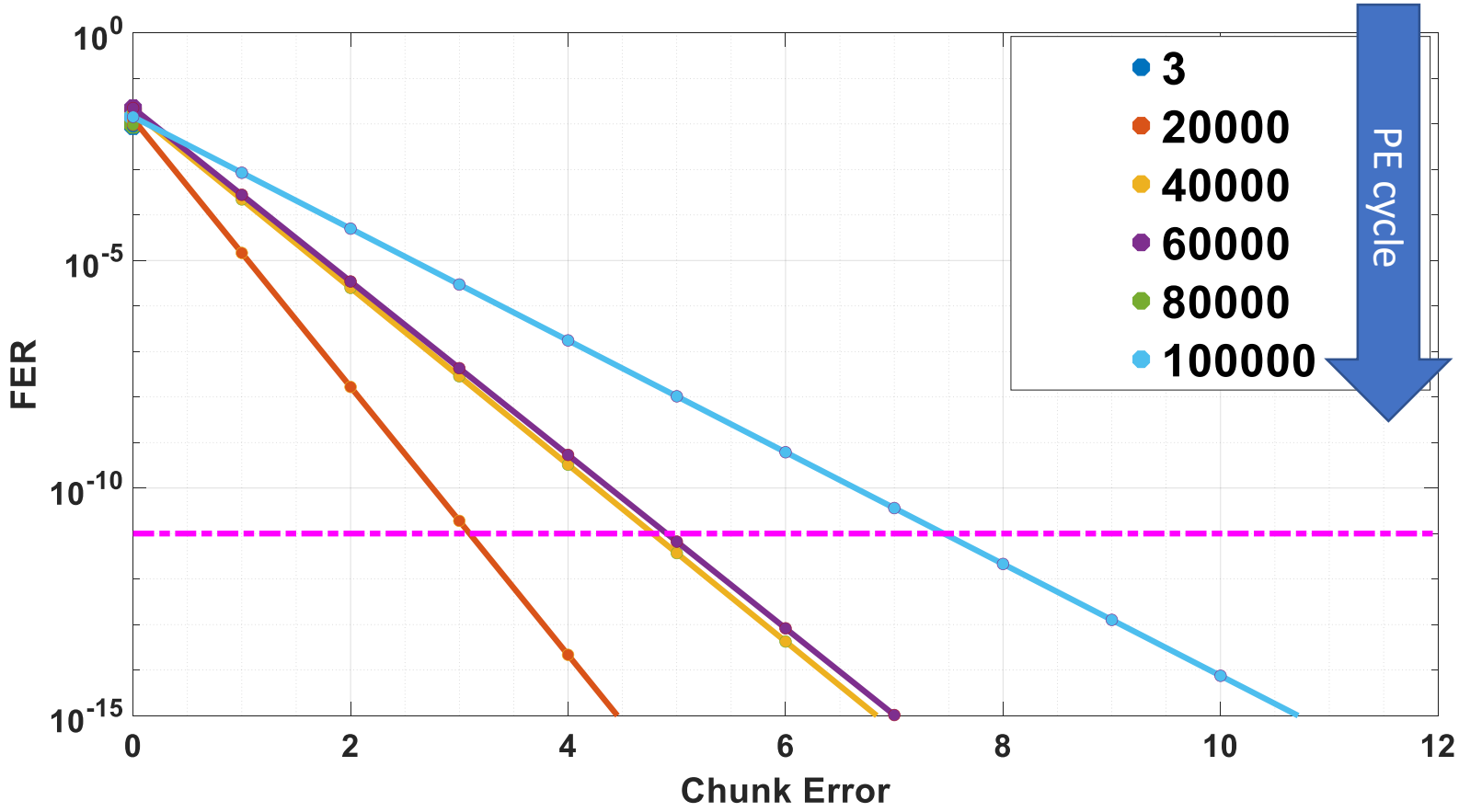
Higher LDPC code rate to improve NAND IF efficiency.

True SLC-aware methods



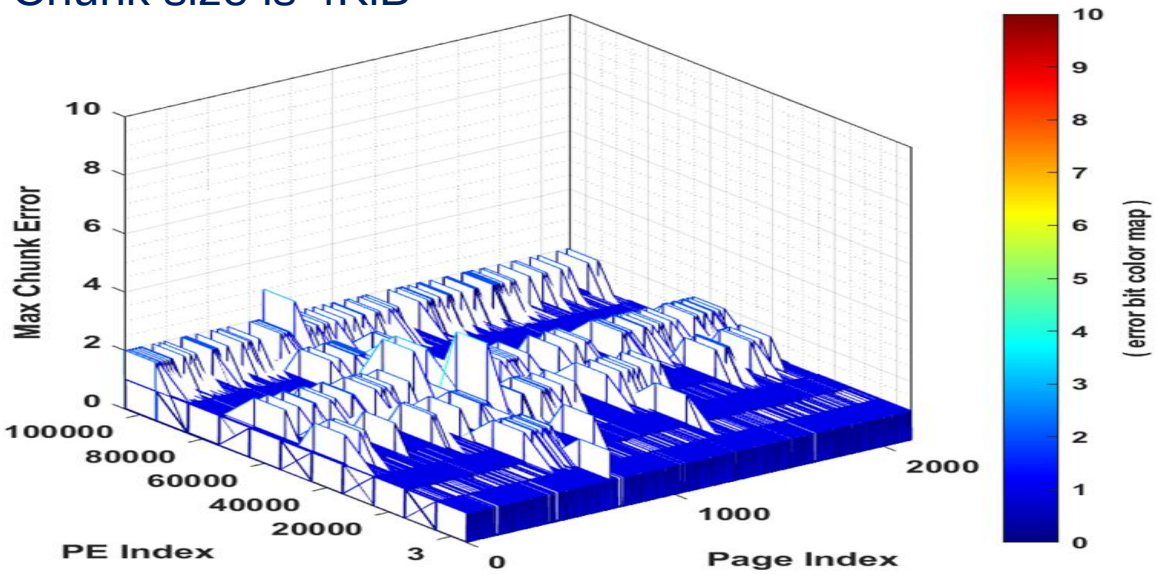
SLC Error Characterization

- Keep very low error bit number through life-time

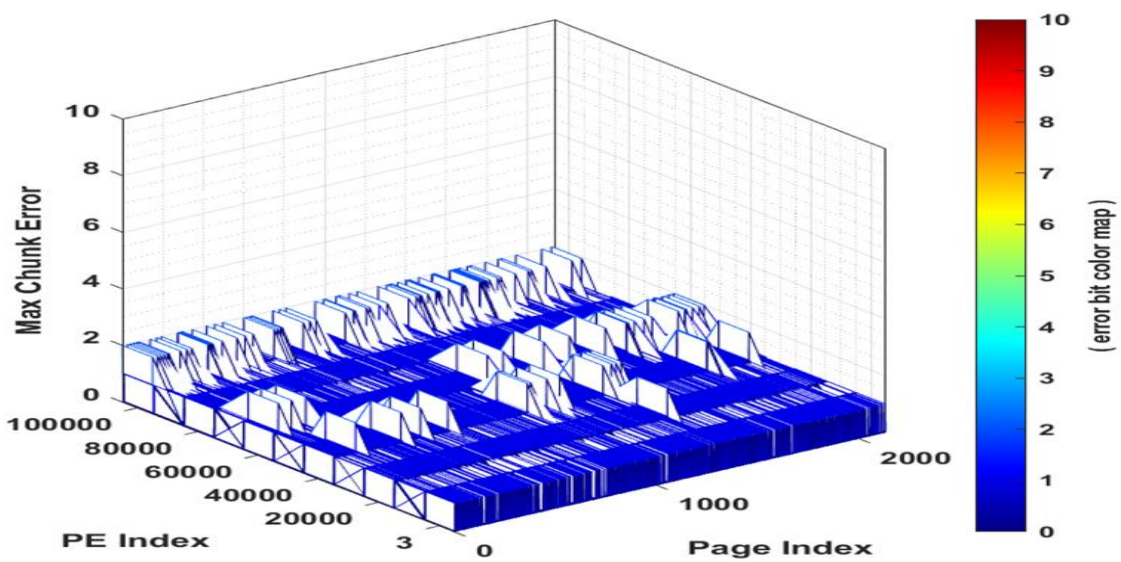


SLC Error Characterization

Chunk size is 4KiB



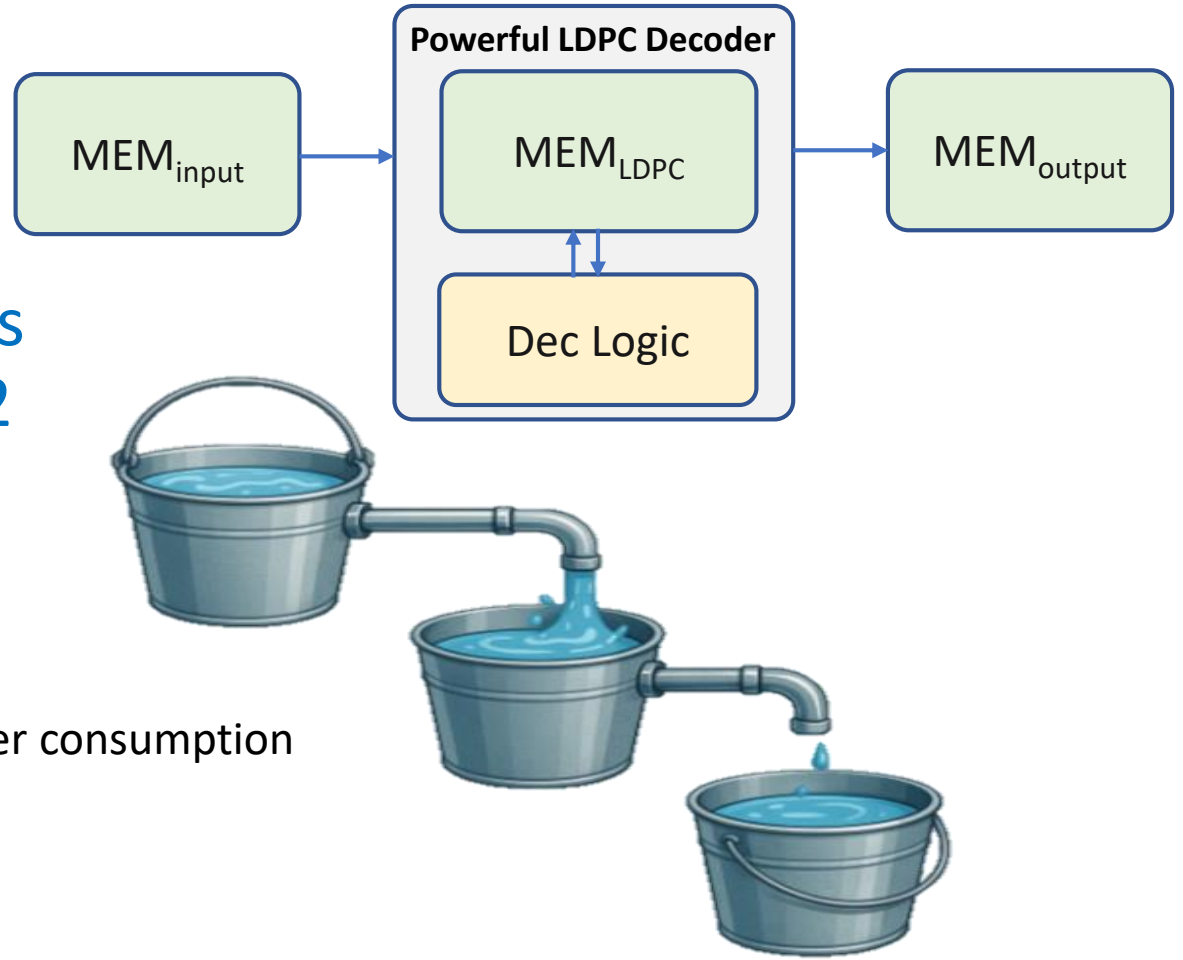
Normal read



Best read

Conventional LDPC Decoder in SLC mode

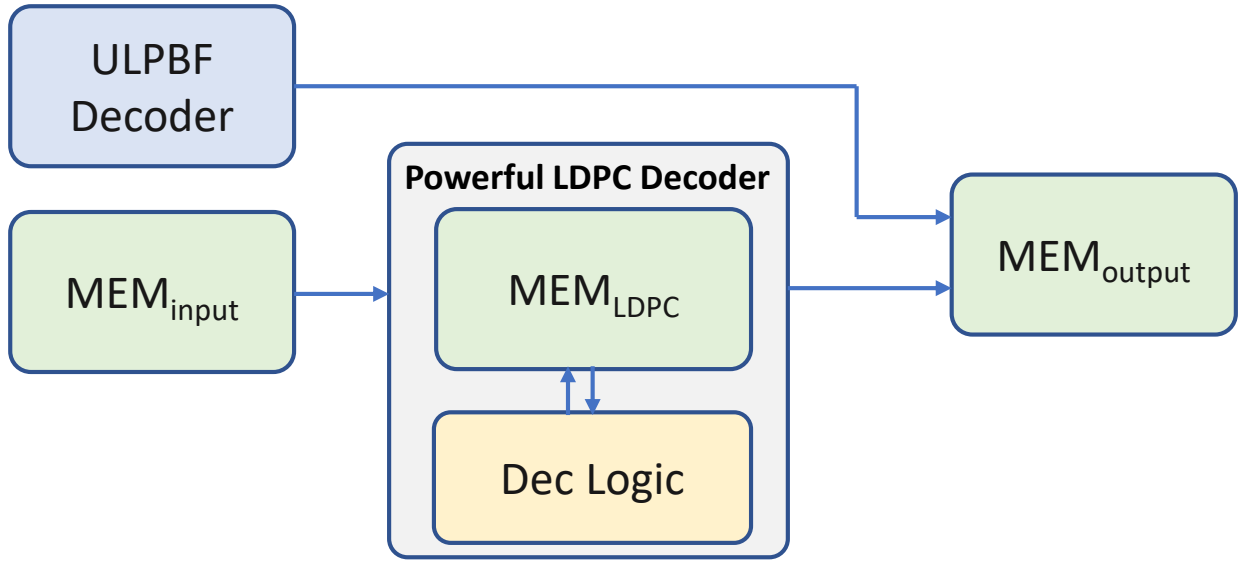
- At least three memory blocks are required to be moved during the decoding process.
- The powerful LDPC decoder calculates the syndrome and decodes within 1-2 iterations.



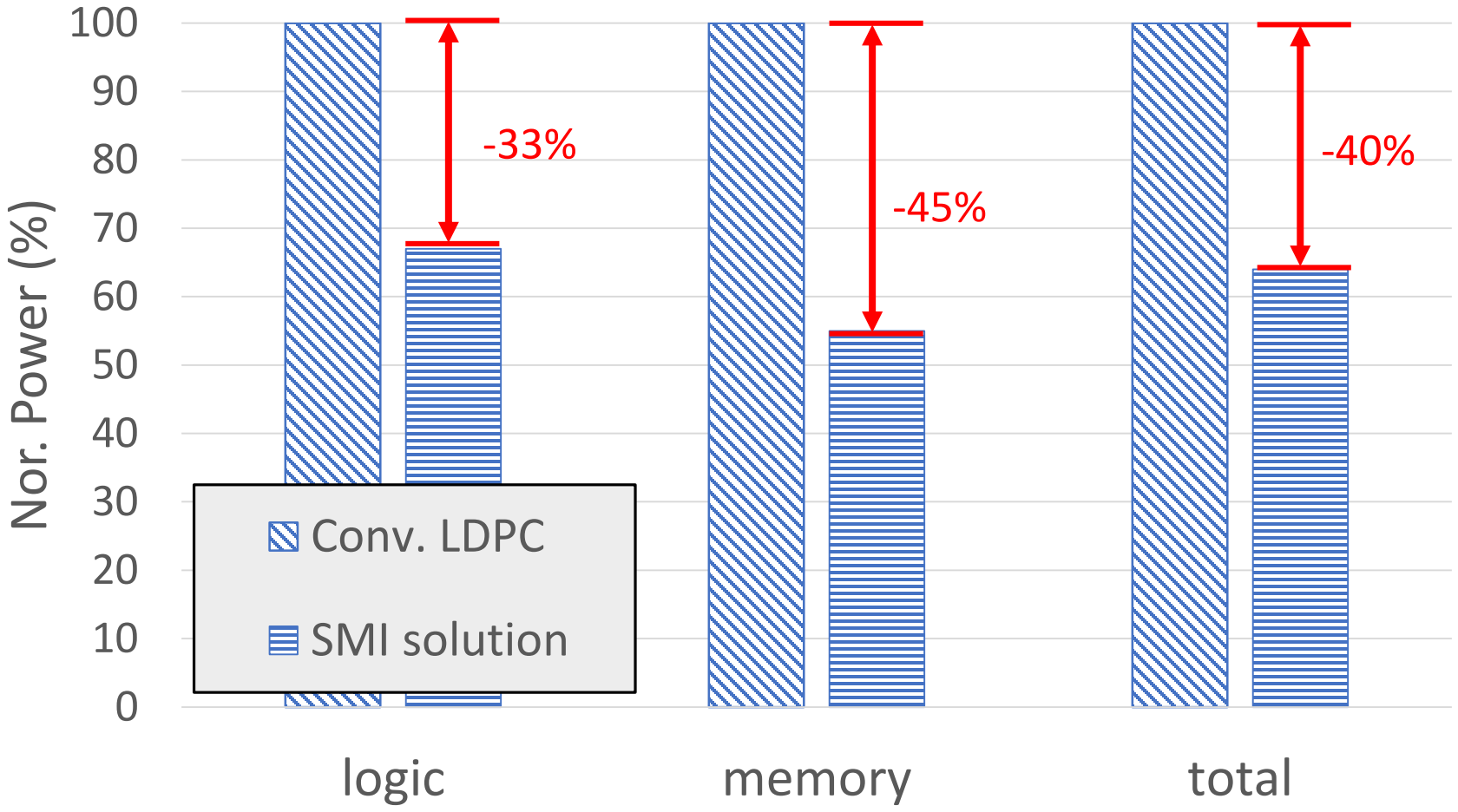
60% memory power consumption

SMI SLC Mode Solution

- Ultra-low power bit flipping decoder only provide the limited correction capacity.
  - Only 10bit correction ability
- Advantages:
  - Reduce memory power on data transfer
  - Reduce logic dynamic power
- The activation rate of powerful LDPC decoder is 5.08×10^{-9}

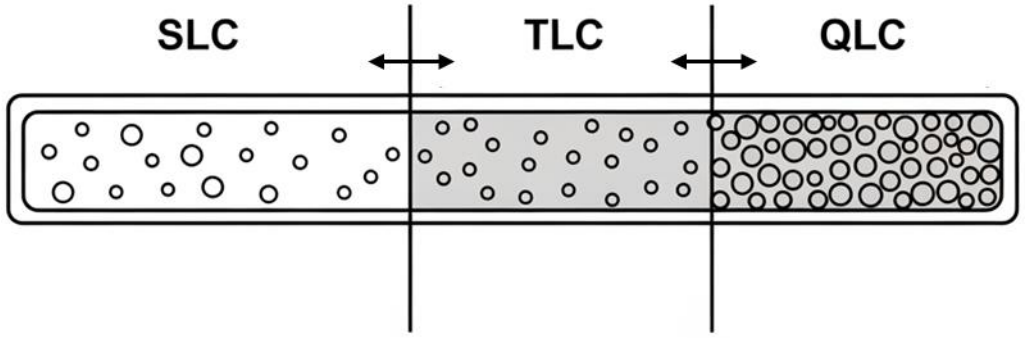


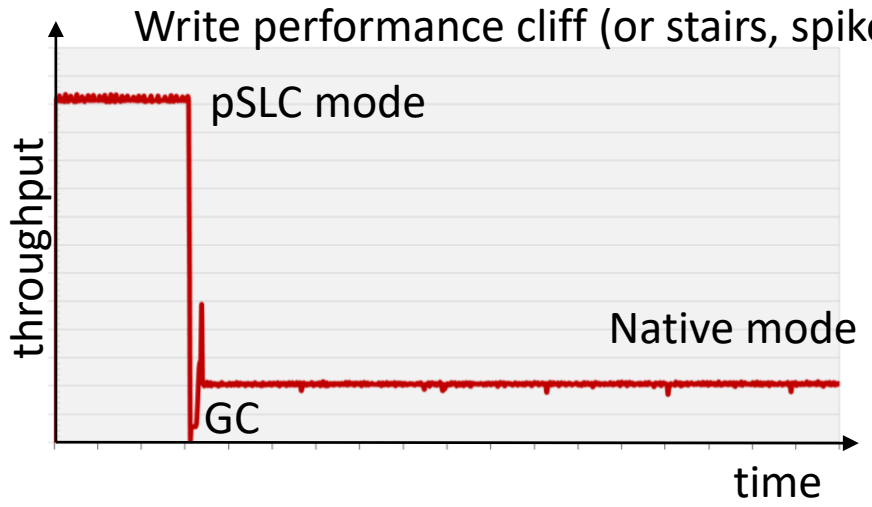
Comparison and Performance



Leverage The SLC-aware Decoder

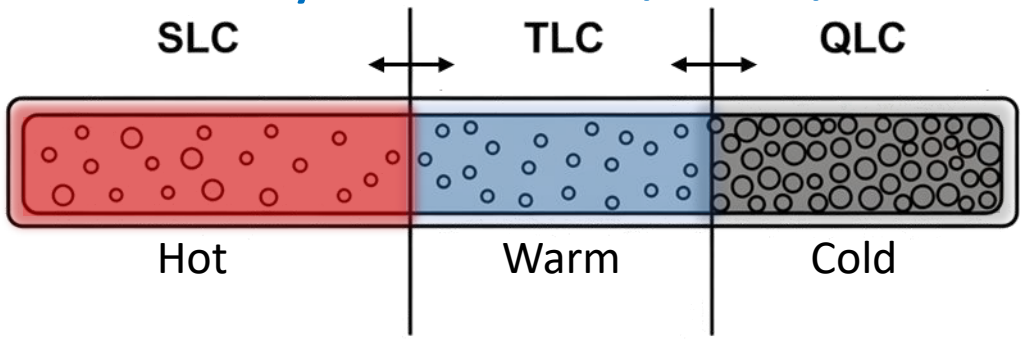
- Dynamic SLC / TLC / QLC





Read-hot data strategy with SLC-mode Decoder

- Smart dynamic SLC / TLC / QLC



Impact on **Read-Hot Data Strategy** with SLC-aware decoder

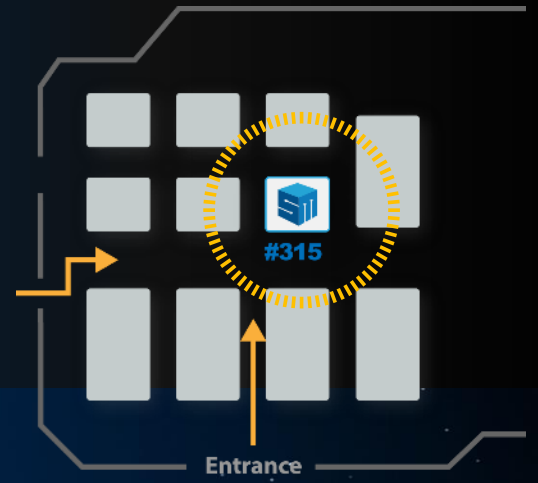
To	From SLC	From TLC	From QLC
SLC	Enhanced "Always-Hot" Tiering	More Frequent & Efficient Read Promotion	Strategic High-Impact Promotion
TLC	More Precise De-staging	Less Pressure on In-Tier GC	Efficient Warm-Up Promotion
QLC	Aggressive Cold Data Flushing	Clearer Tier Boundaries	No Direct Impact

Scan to learn more!

Meet us at booth

#315

SiliconMotion



Smart Storage in Motion: From Silicon Innovation to AI Transformation Across all Spectrums!