An Ultra-low-power LDPC Decoder Application in SLC Mode

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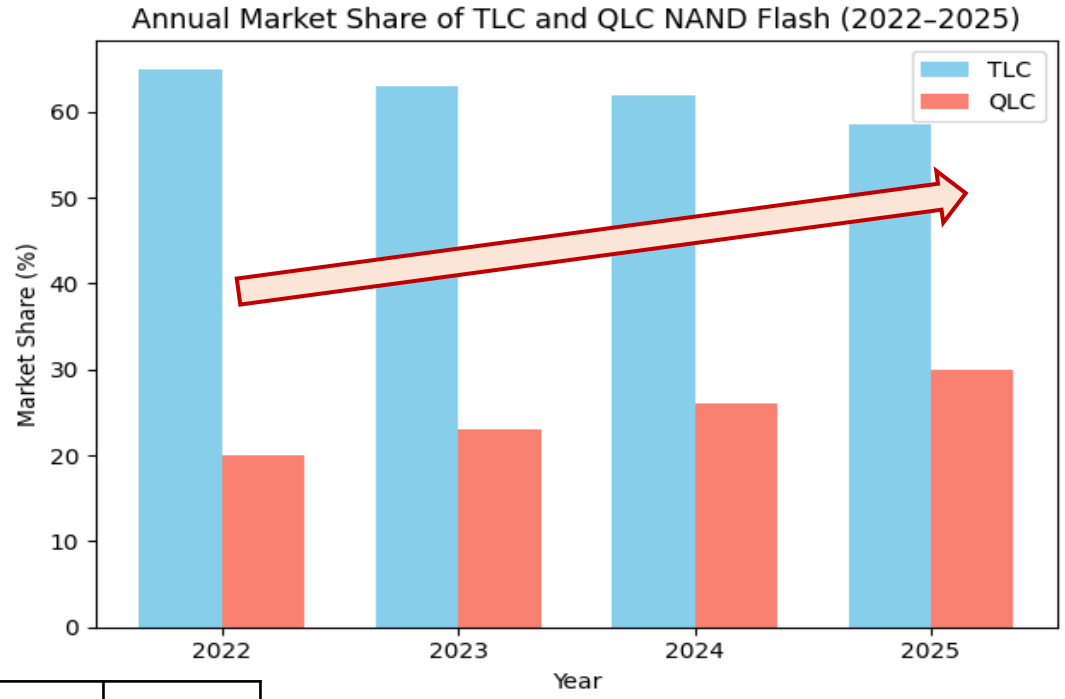
Outline

- Background
  - NAND Development
  - SLC-mode Error Characterization
- SMI Solution: SLC-mode Decoder
  - Ultra-low-power LDPC Decoder
- Performance

NAND Flash Trend

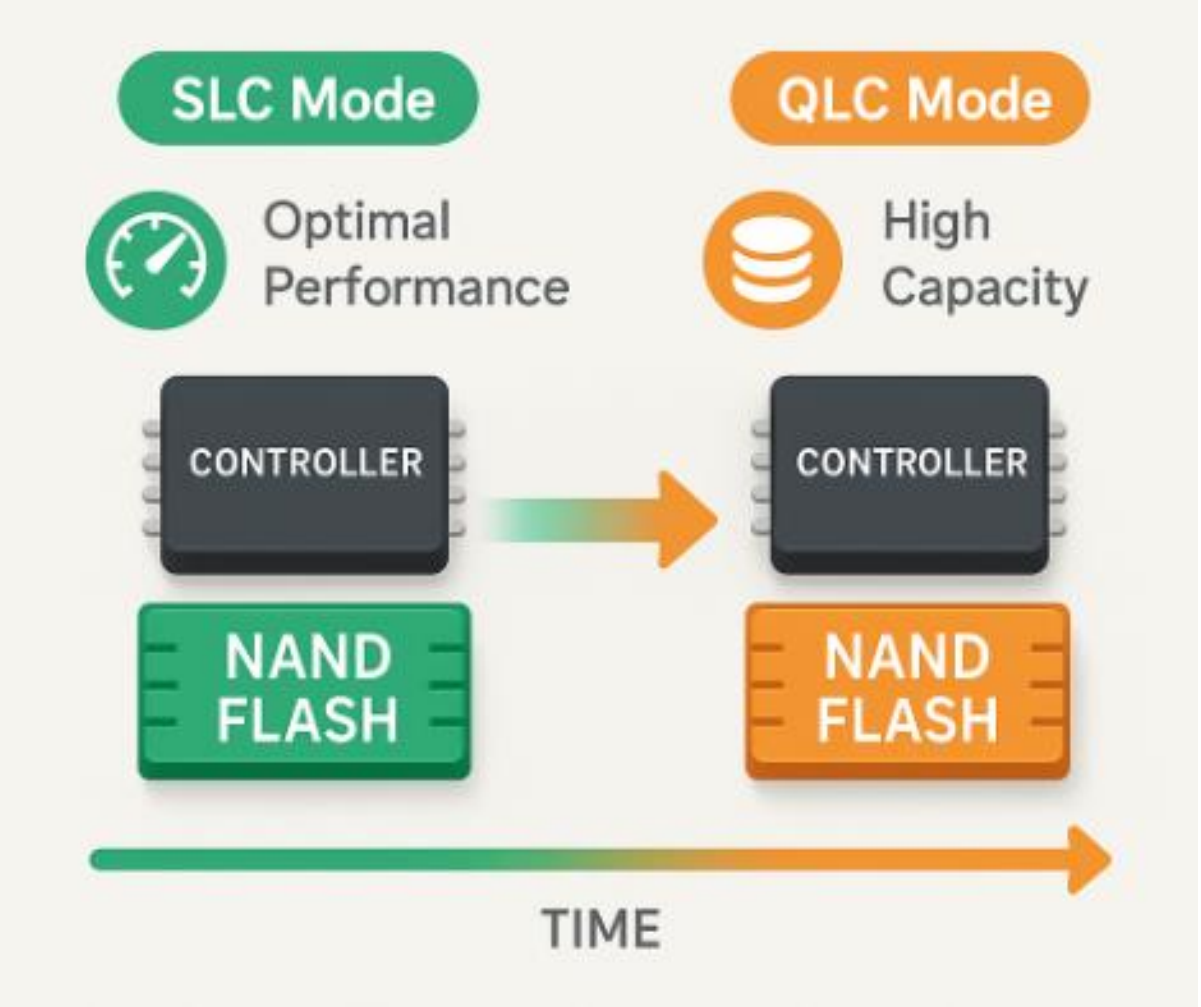
- QLC NAND Flash is becoming more common
  - Higher storage density
  - Lower cost
- QLC root cause:



	Write latency	Read latency	PE cycle
SLC	0.5ms	10us	>100K
MLC	1.2ms	50us	10K
TLC	2.4ms	100us	3K
QLC	10-20ms	150-200us	~1K

SLC Mode (pseudo-SLC)

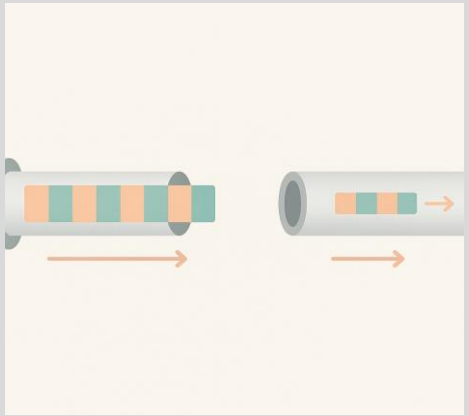
- SLC mode reduces the number of bits stored in each cell to one.
  - Reduce the amount of stored bits in each cell
  - Increase the reliability and lifetime
  - Decrease read/write latency



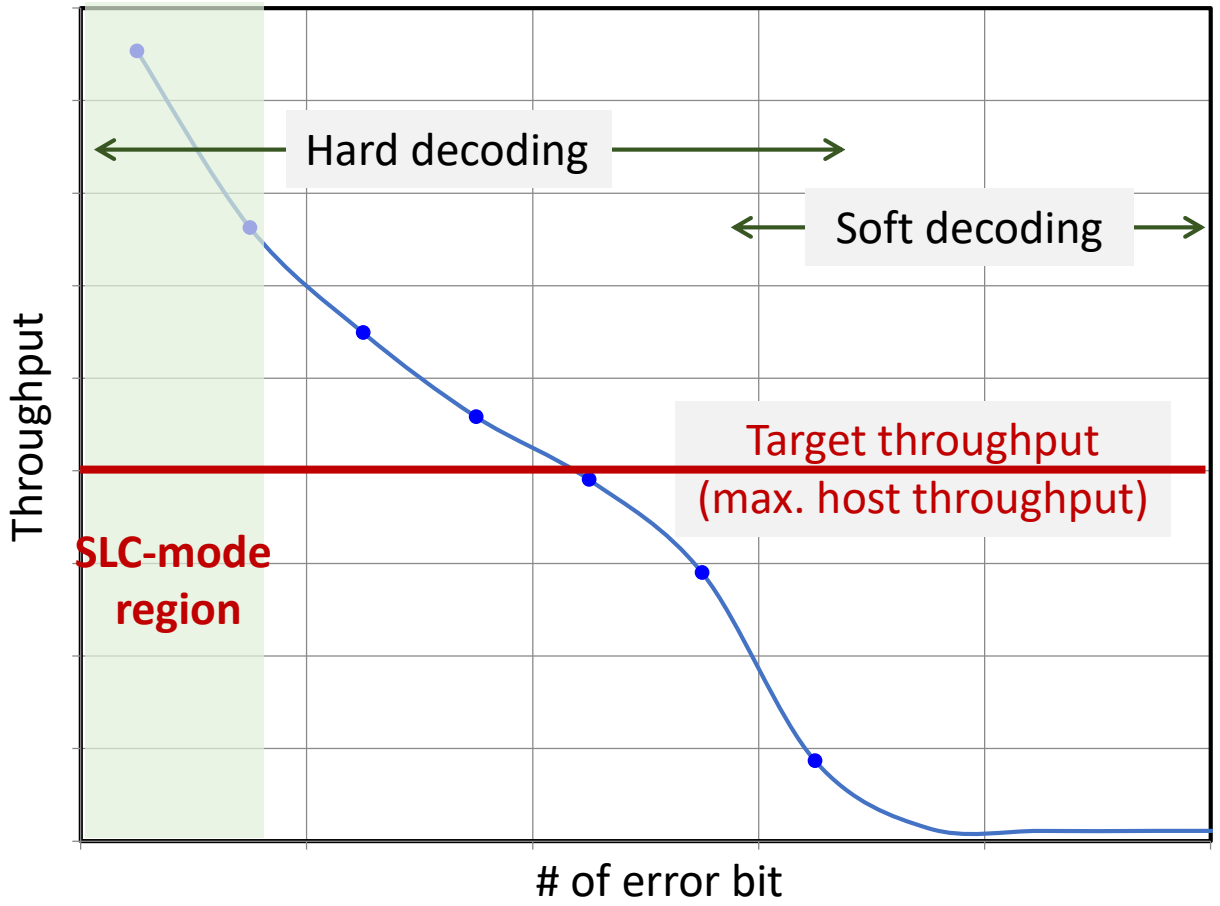
About SLC Mode Technique

Traditional SLC-aware methods

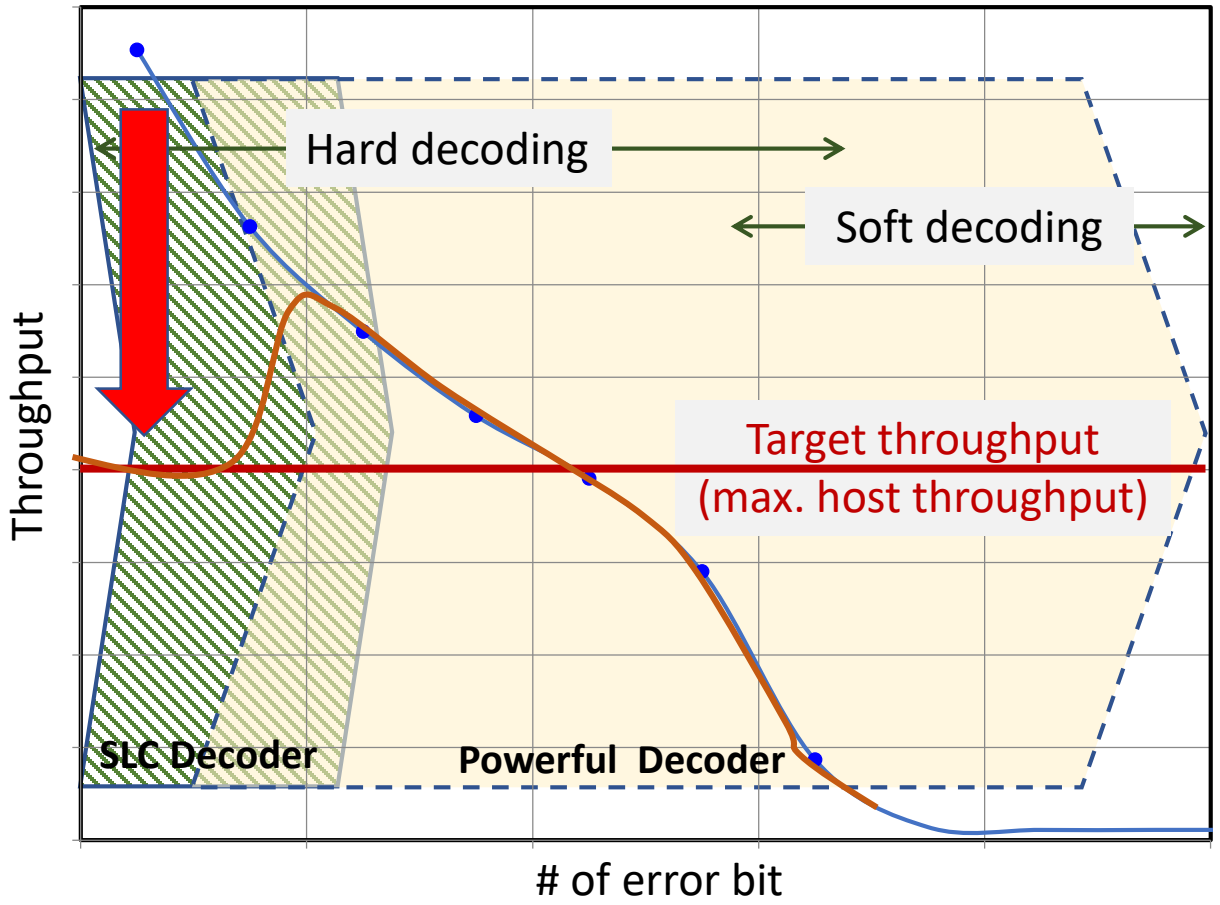
Less accurate reads/program to reduce array busy time.



Higher LDPC code rate to improve NAND IF efficiency.

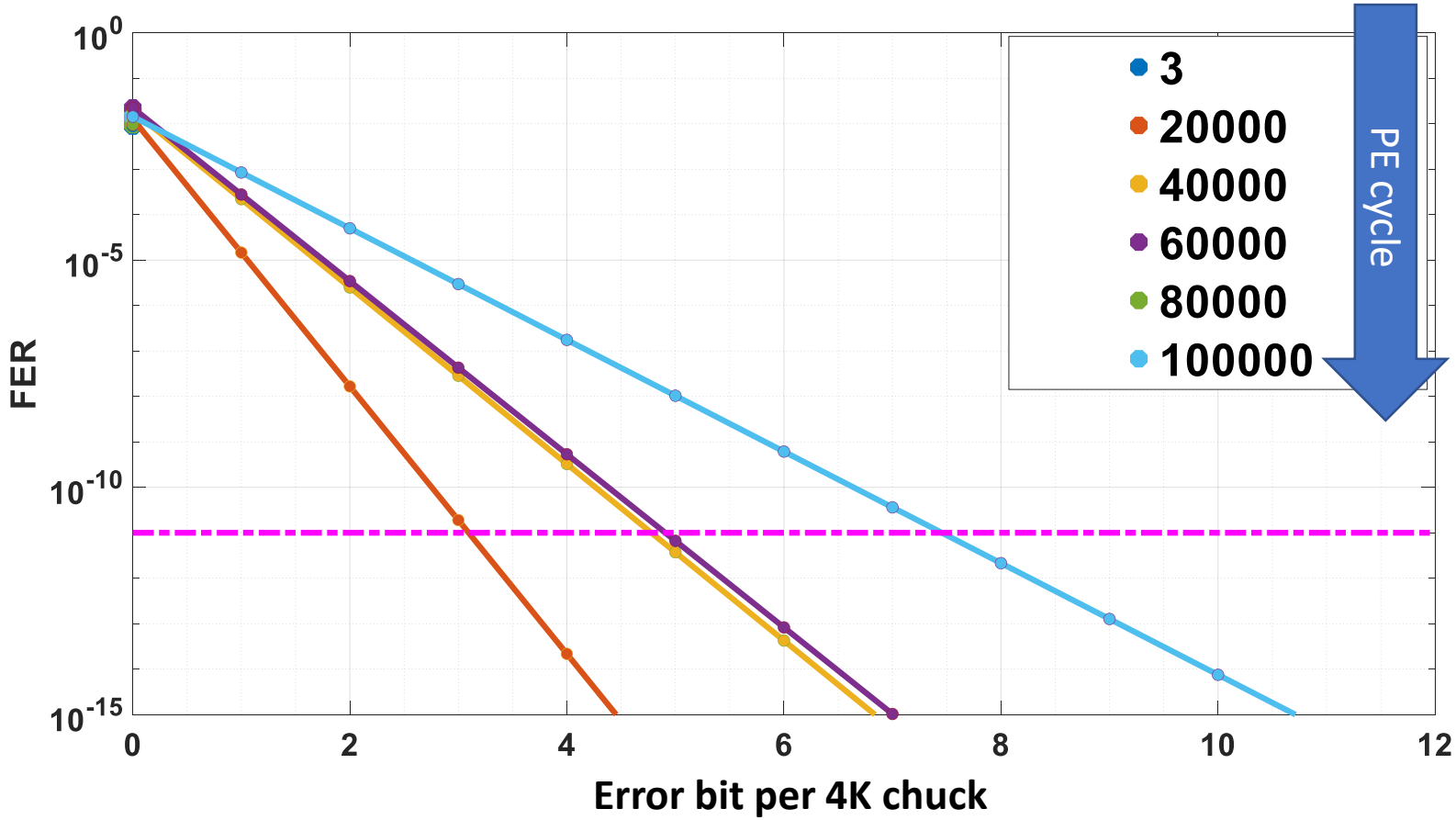


SLC Decoder Solution



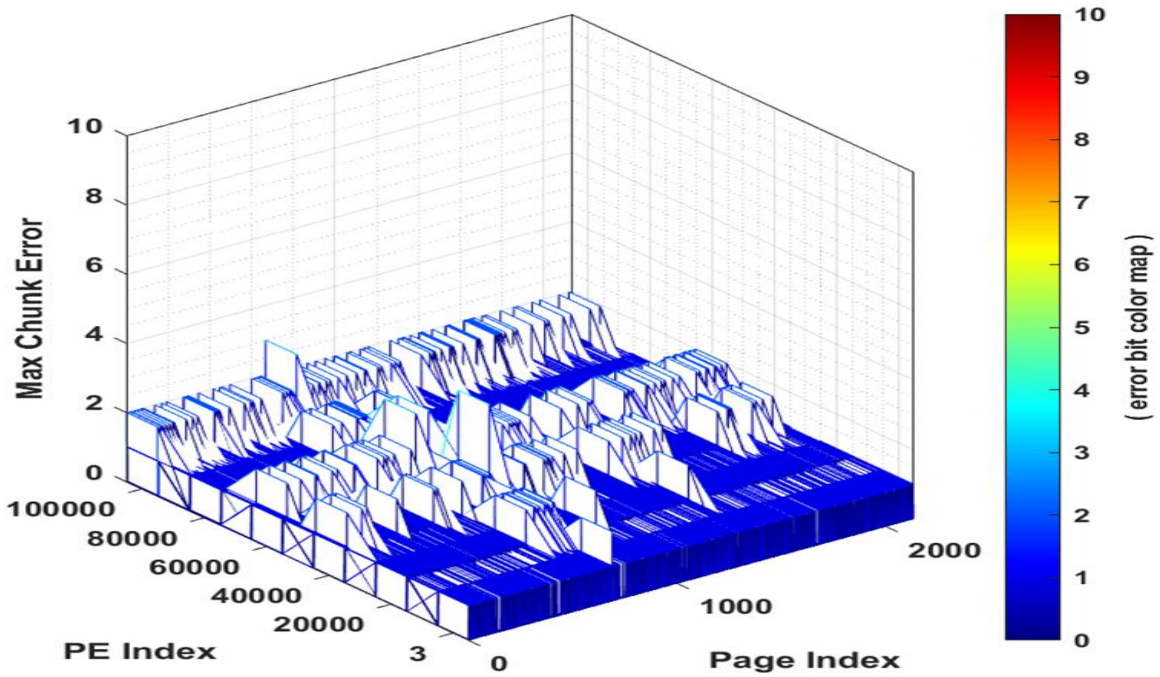
SLC Error Characterization

- Keep very low error bit number through life-time

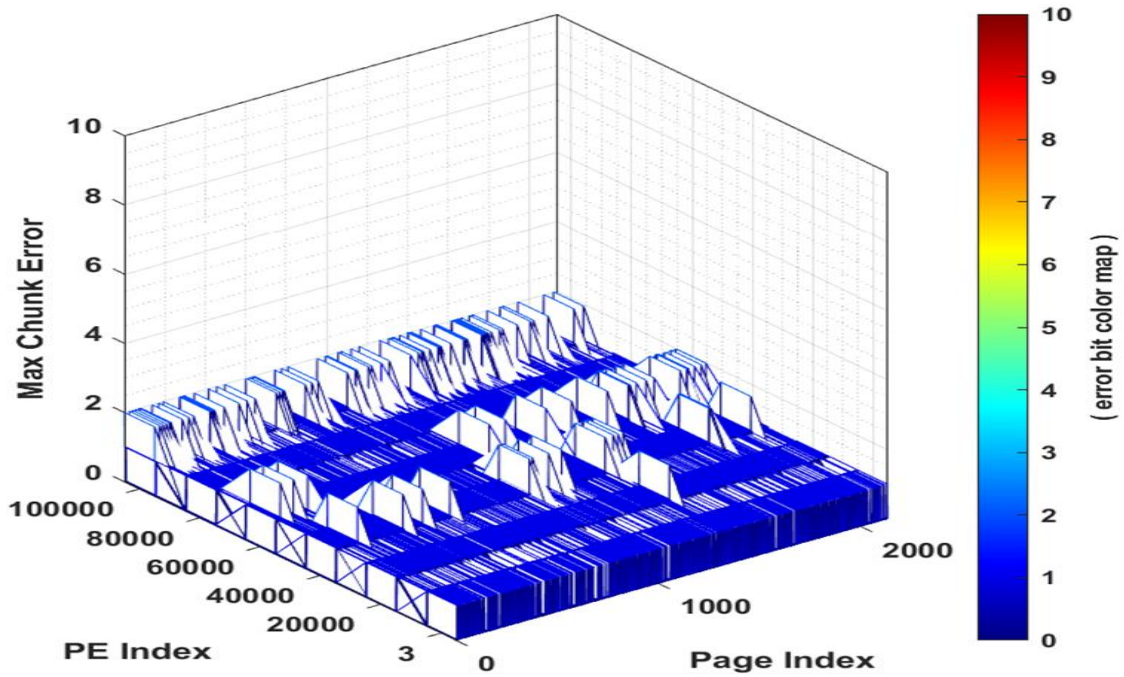


SLC Error Characterization

Chunk size is 4KiB

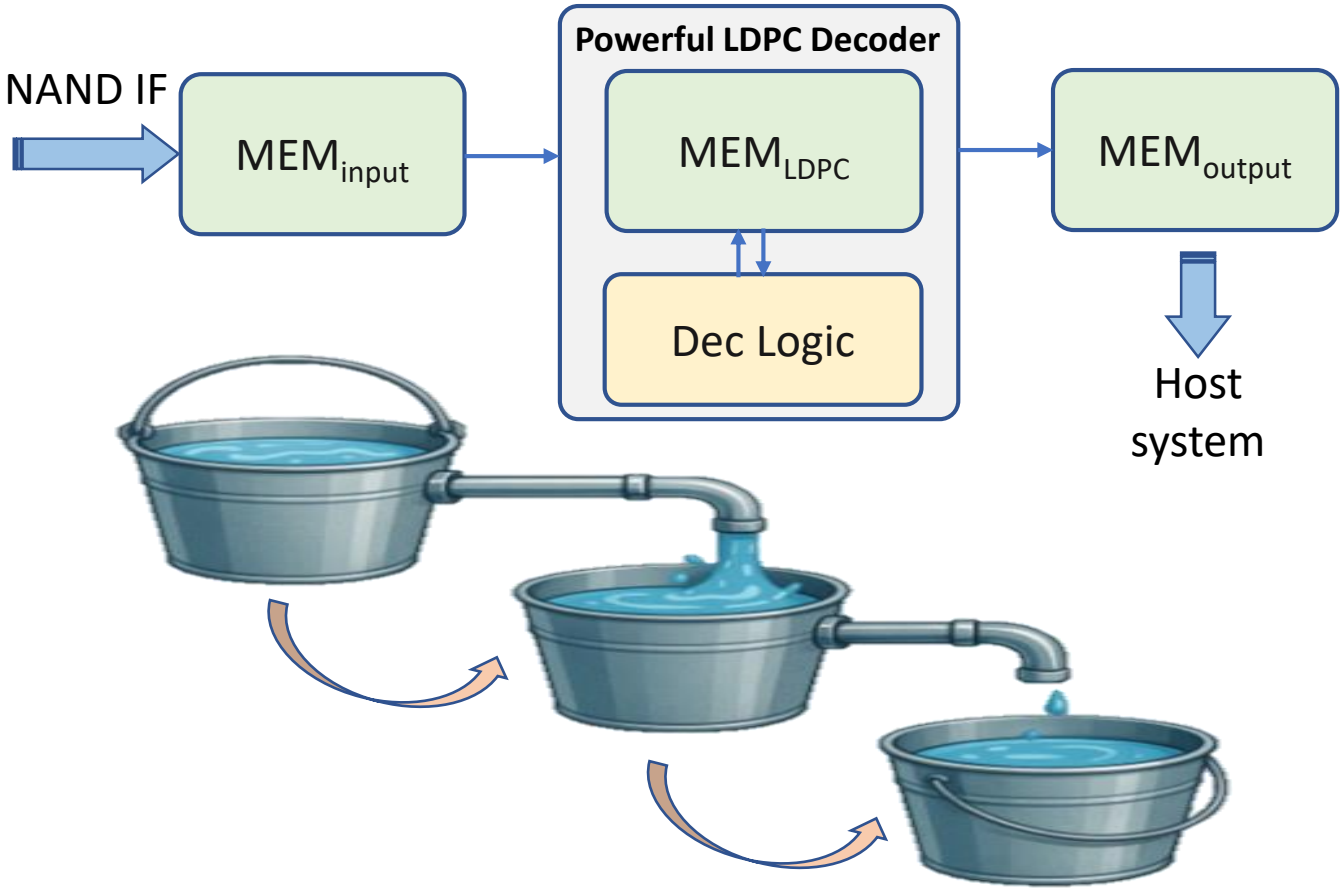


Normal read



Best read

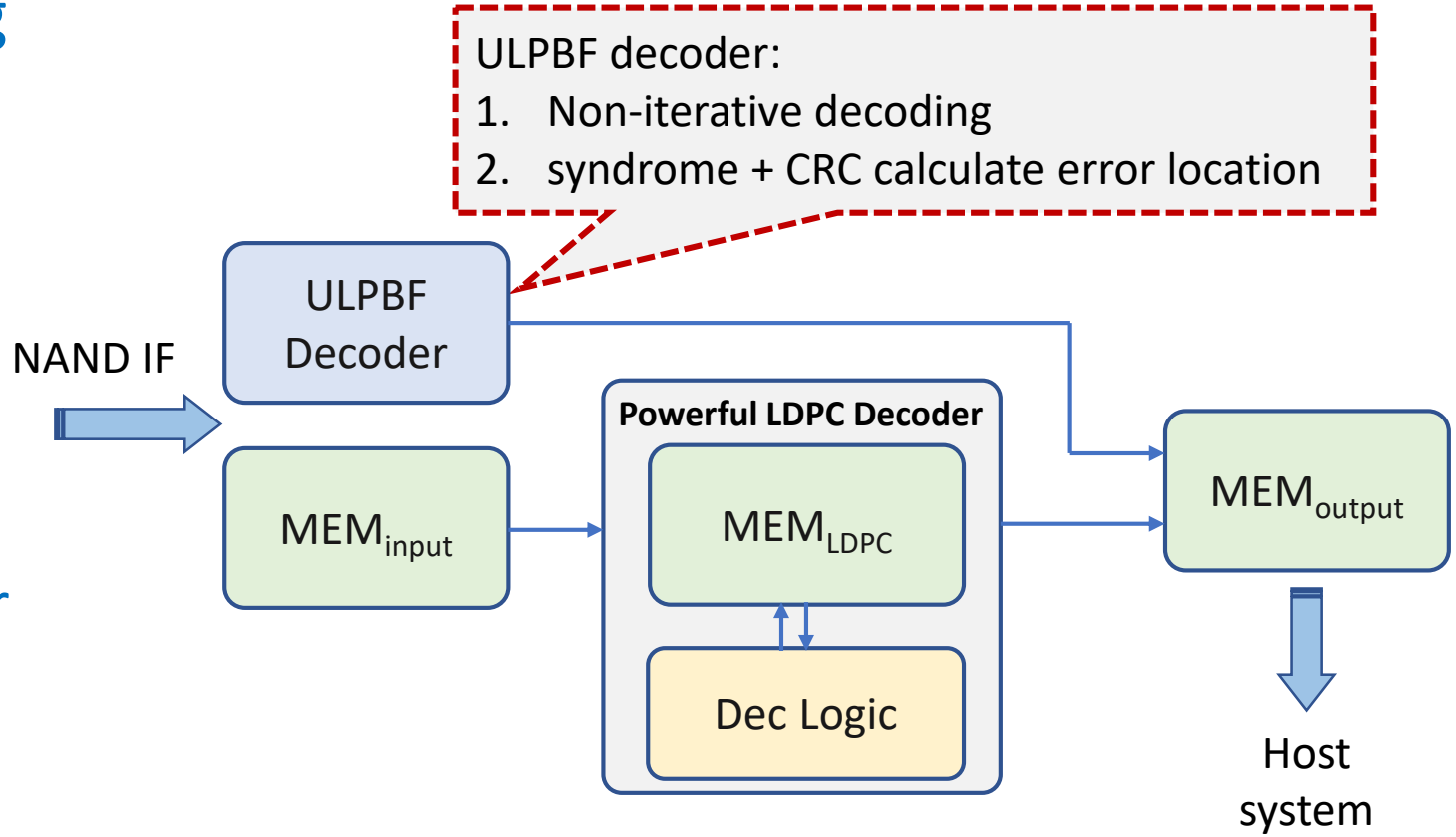
Conventional LDPC Decoder in SLC mode



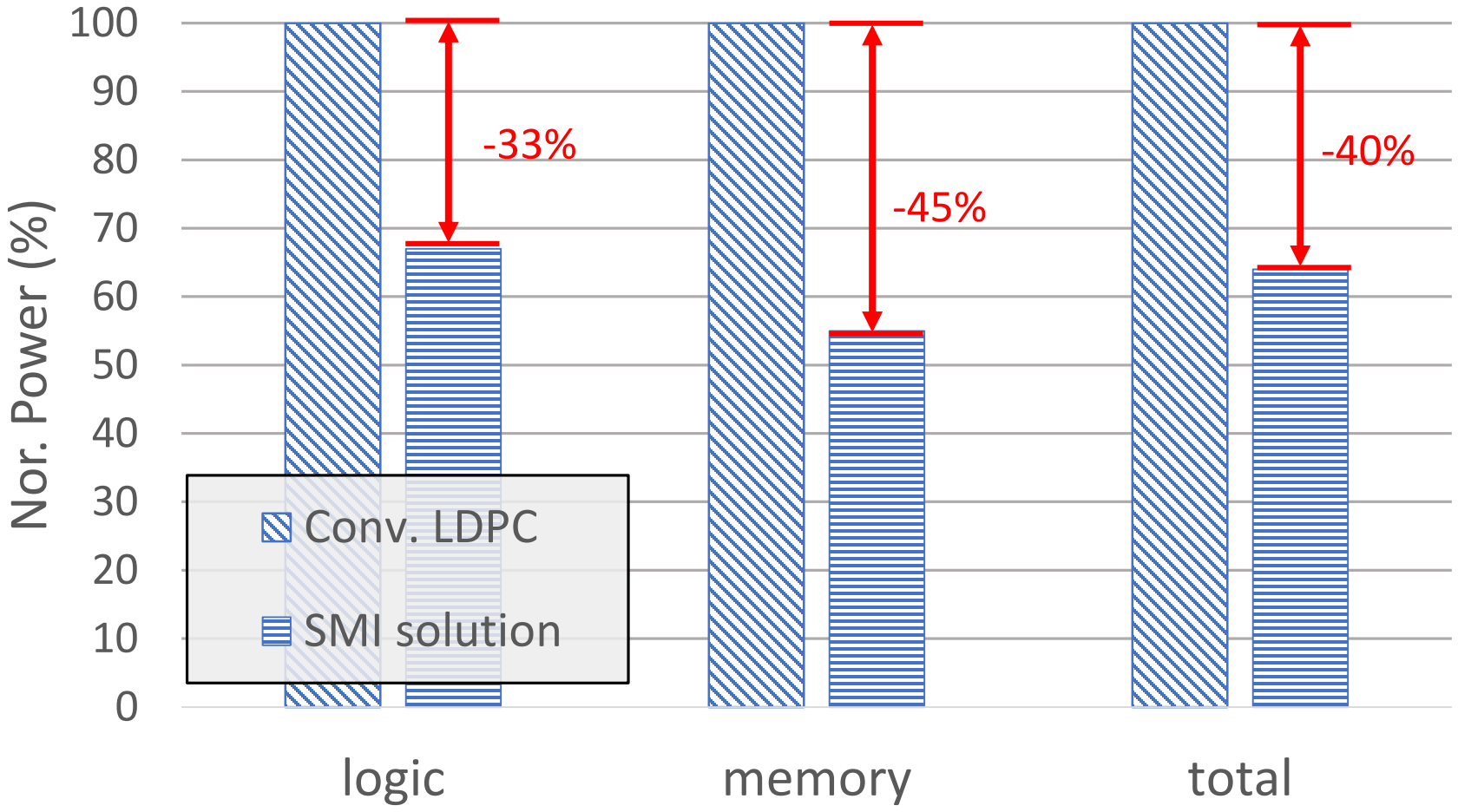
- Three memory blocks are required.
- In SLC mode region, only 1-2 iterations are required.
  - 60% power consumption in data transfer

SMI SLC Mode Solution

- Ultra-low power bit flipping (ULPBF) decoder only provide the limited correction capacity.
- Advantages:
  - Reduce memory power on data transfer
  - Reduce logic dynamic power
- The activation rate of powerful LDPC decoder is $5.08x10^{-9}$



Comparison in Power consumption



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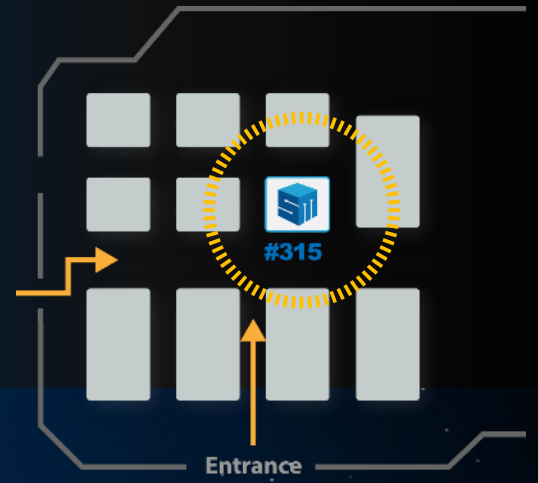

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