An Ultra-low-power LDPC Decoder Application in SLC Mode

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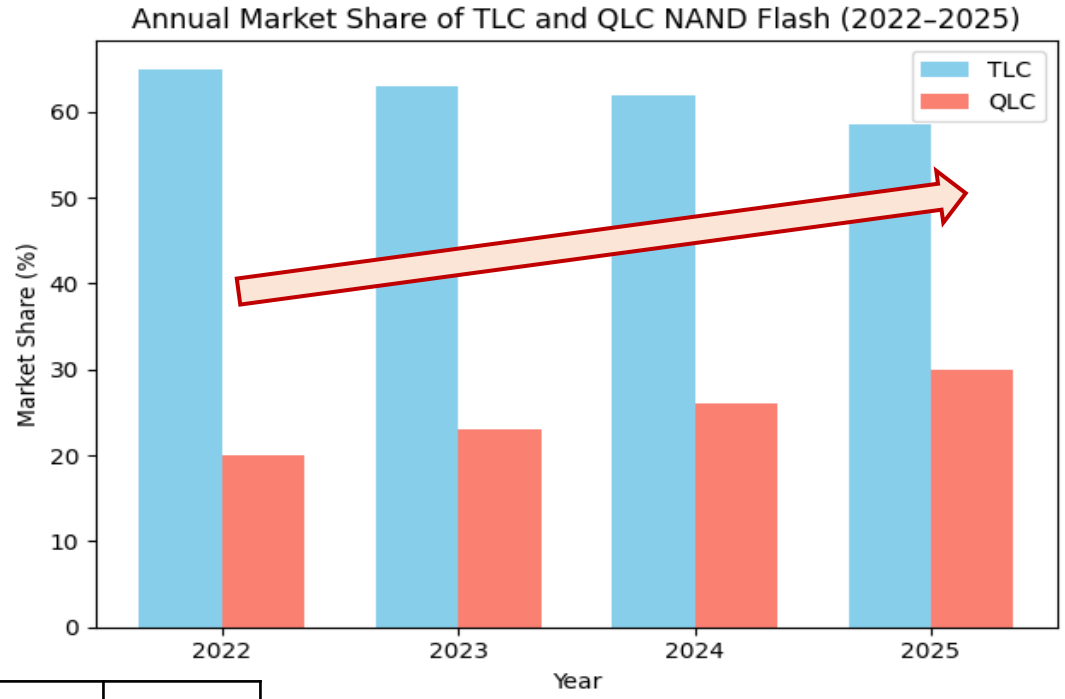
Outline

- Background
  - NAND Development
  - SLC-mode Error Characterization
- SMI Solution: SLC-mode Decoder
  - Ultra-low-power LDPC Decoder
- Performance and summary

NAND Flash Trend

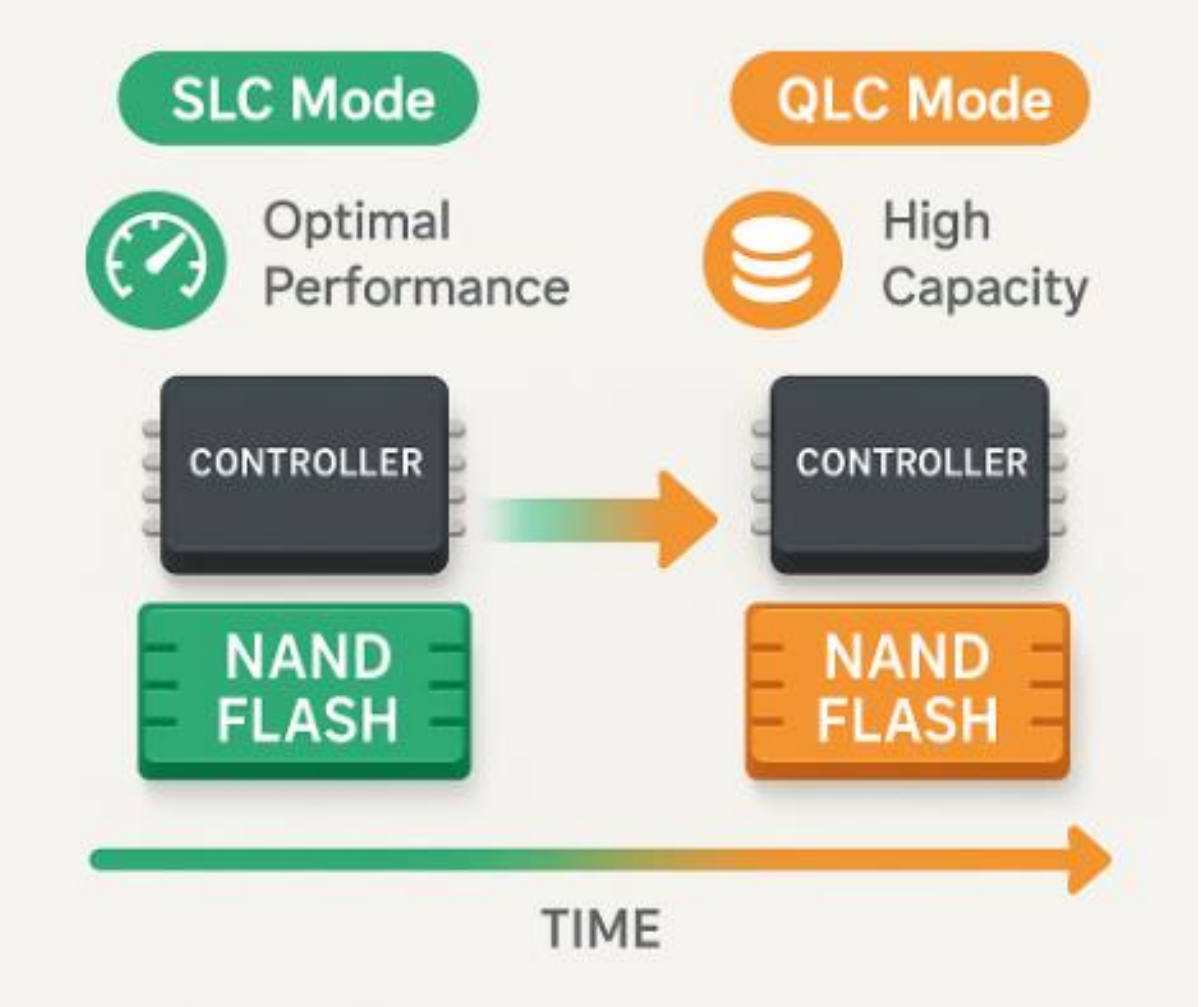
- QLC NAND Flash is becoming more common
  - Higher storage density
  - Lower cost
- QLC root cause:



	Write latency	Read latency	PE cycle
SLC	0.5ms	10us	>100K
MLC	1.2ms	50us	10K
TLC	2.4ms	100us	3K
QLC	10-20ms	150-200us	~1K

SLC Mode (Pseudo-SLC)

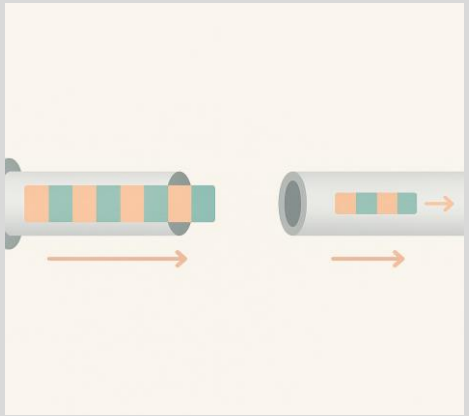
- SLC mode reduces the number of bits stored in each cell to one
  - Reduce the amount of stored bits in each cell
  - Increase the reliability and lifetime
  - Decrease read/write latency



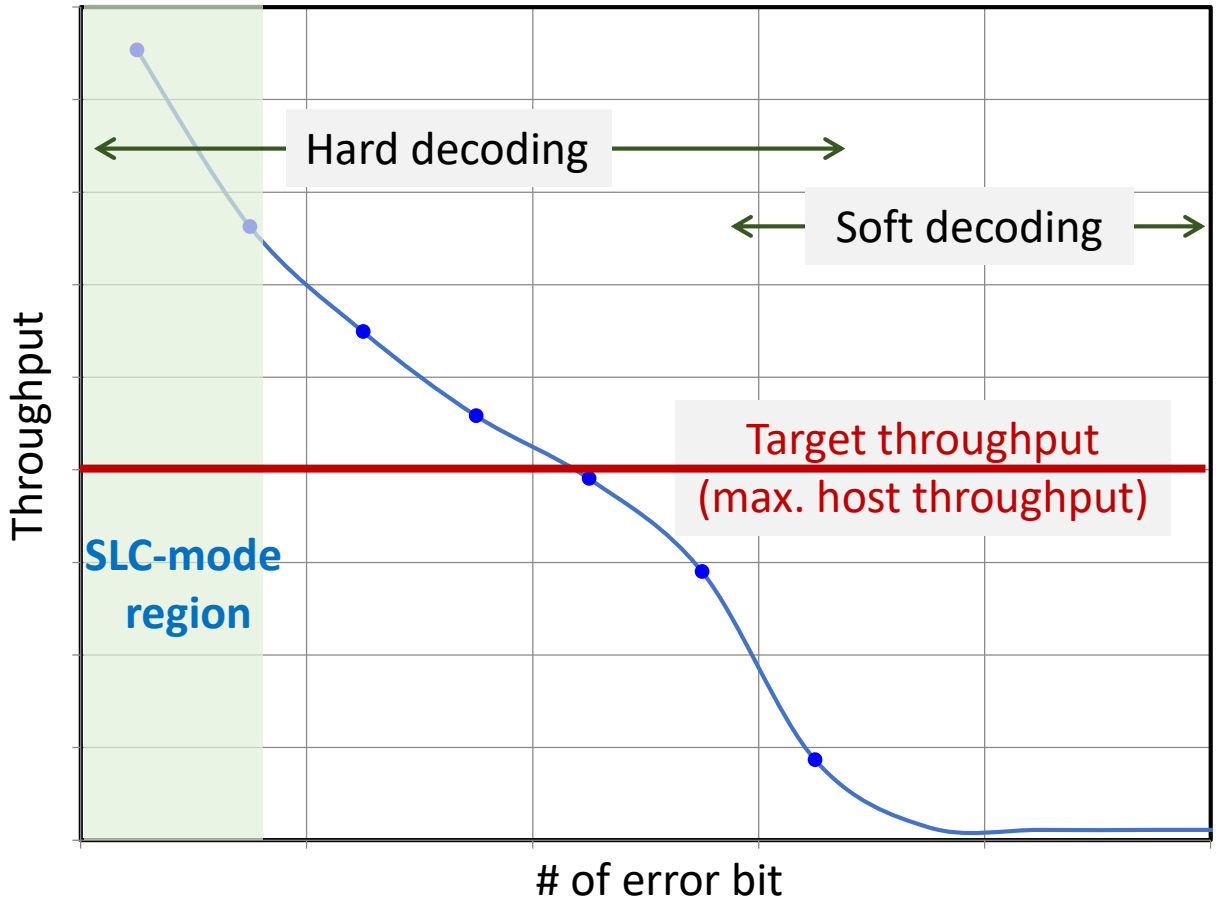
About SLC Mode Technique

Traditional SLC-aware methods

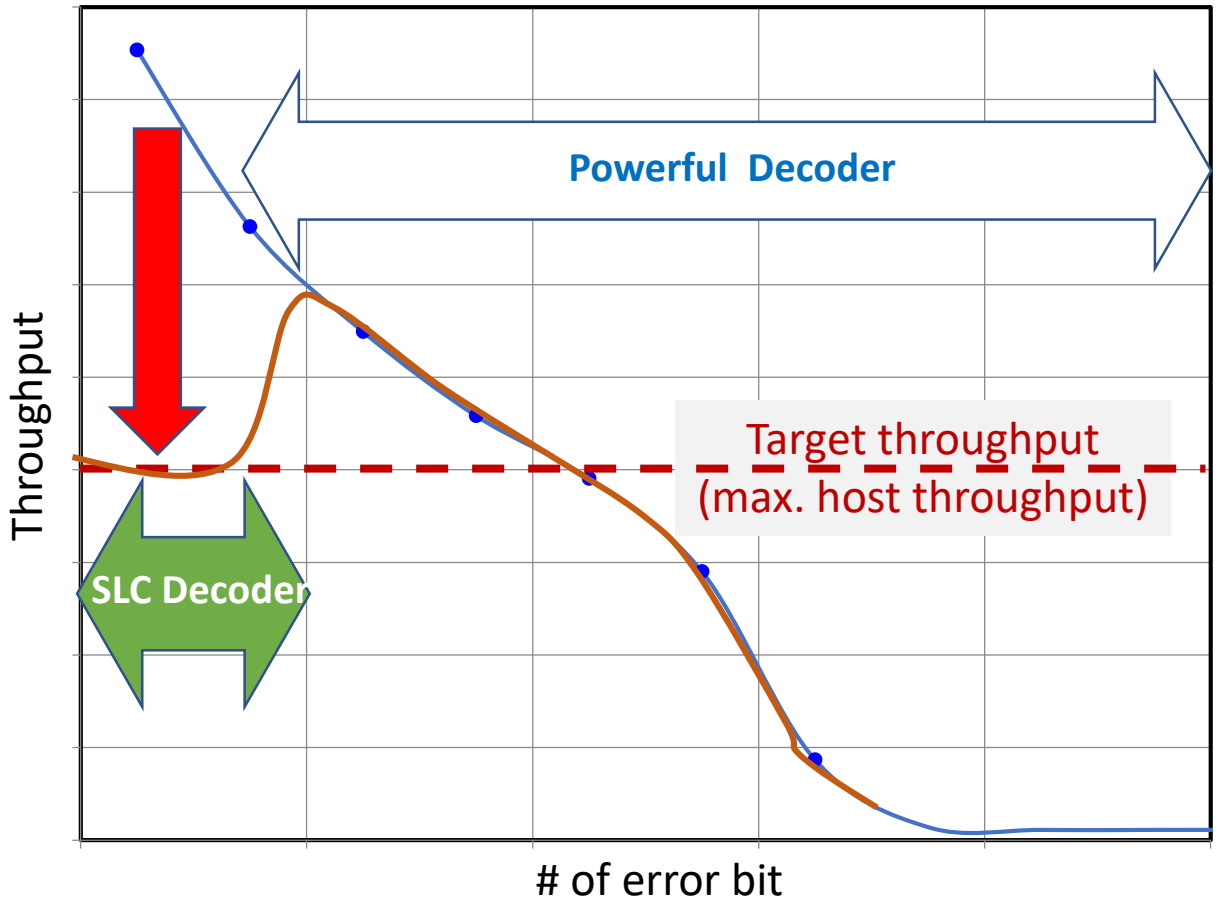
Less accurate reads/program to reduce array busy time.



Higher LDPC code rate to improve NAND IF efficiency.

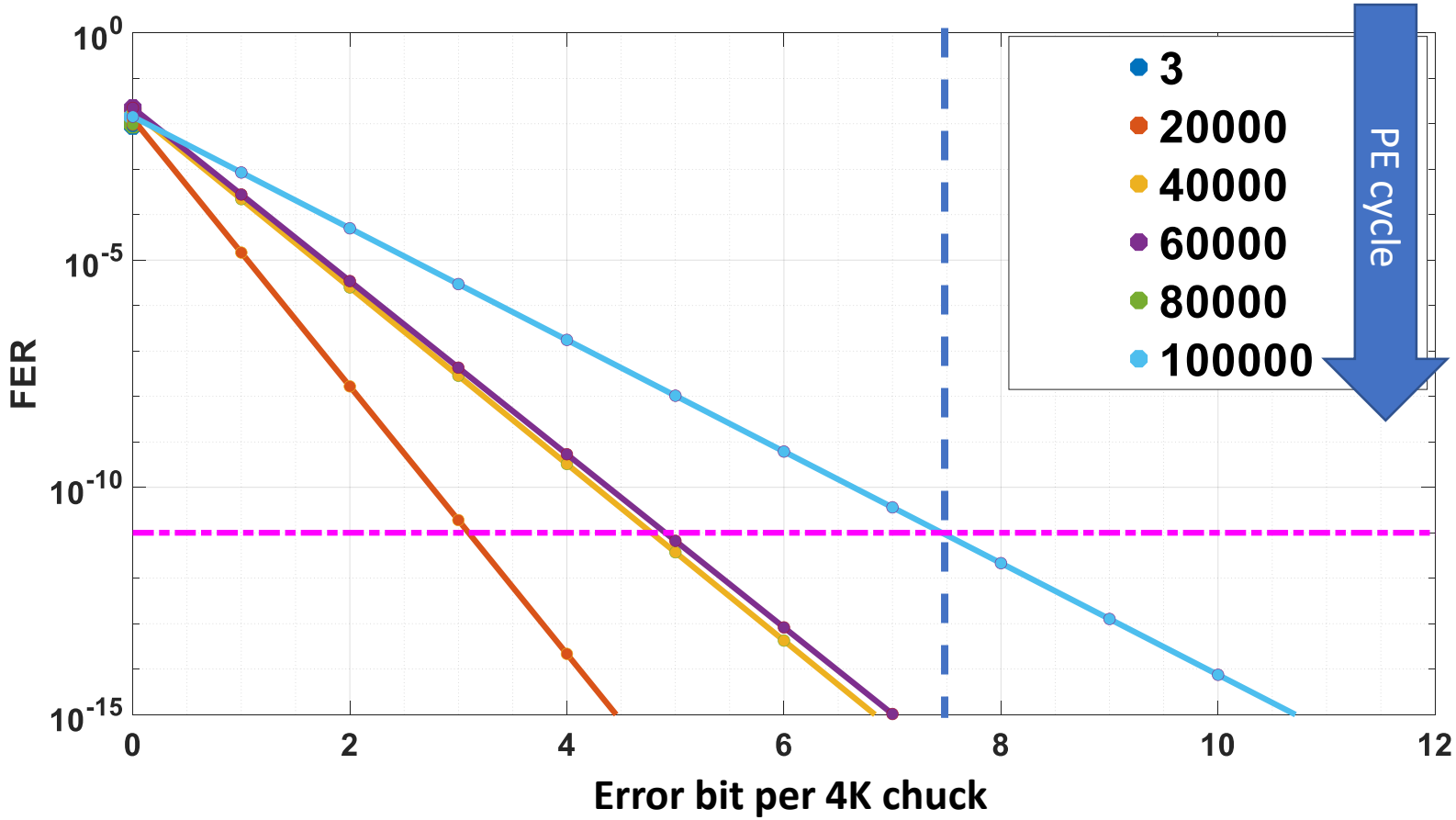


SLC Decoder Solution



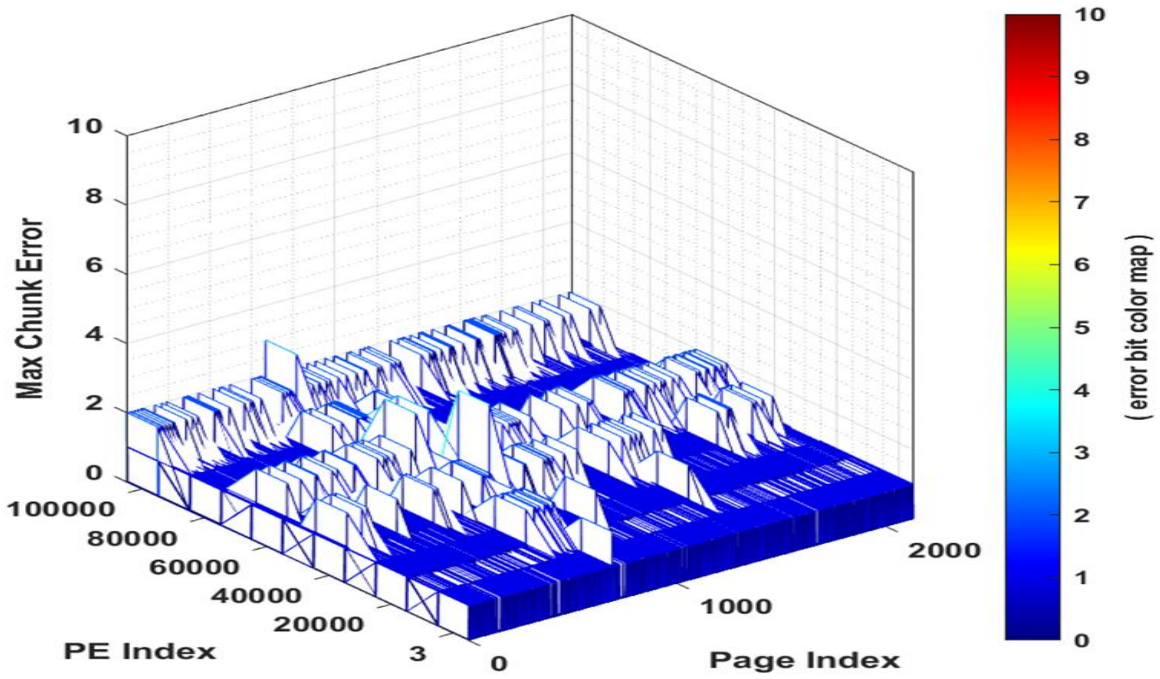
SLC Error Characterization

- Keep very low error bit number through life-time

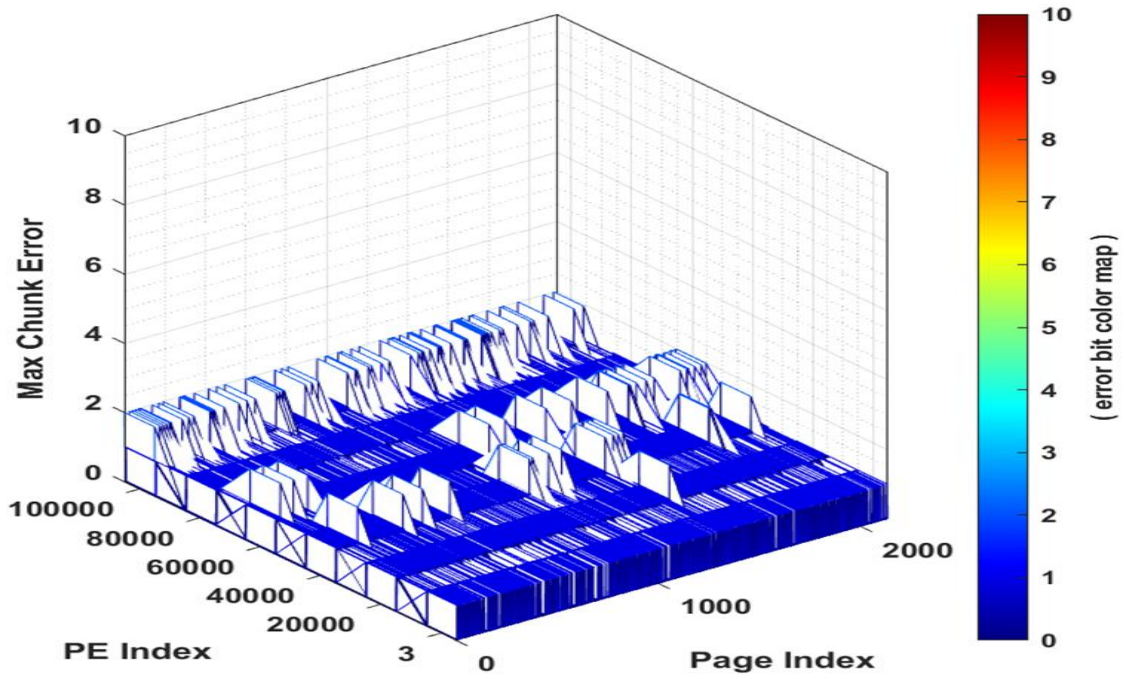


SLC Error Characterization

Chunk size is 4KiB



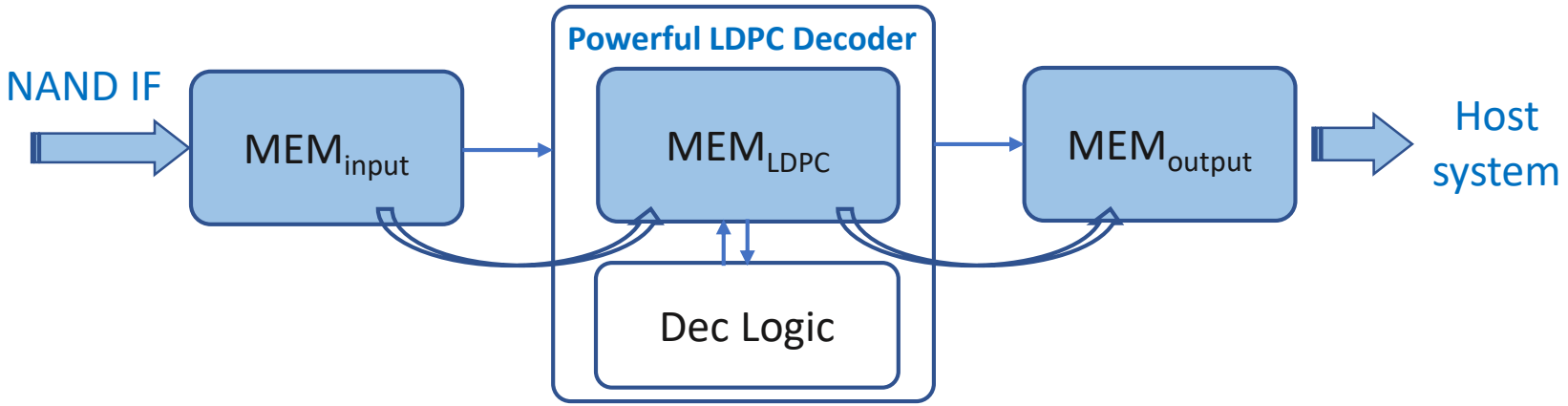
Normal read



Best read

Conventional LDPC Decoder in SLC Mode

- Three memory blocks are required
- In SLC mode region, only 1-2 iterations are required



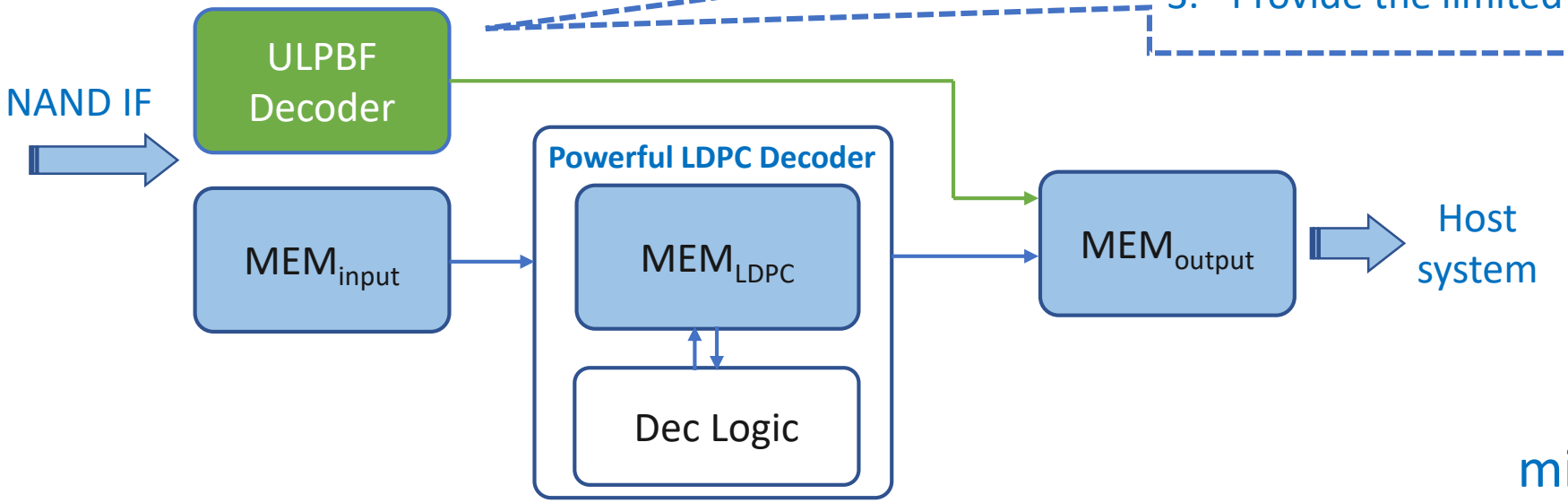
60%

power consumption in data transfer

SMI SLC Mode Solution

- Use the ultra-low power bit flipping (ULPBF) algorithm
- Advantages
  - Reduce memory power on data transfer
  - Reduce logic dynamic power

ULPBF decoder:
1. Non-iterative decoding
2. syndrome + CRC calculate error location
3. Provide the limited correction capacity



5.08x10^{-9}
miss rate in SLC mode

Performance and Summary

- Performance results

-33%	-45%	-40%	+5%
Logic dynamic power	Memory power	Total power	Area

- The dual-decoder approach selects the most power efficiency decoding path
- A simple decoding algorithm ULPBF has lower complexity and just enough throughput to the target

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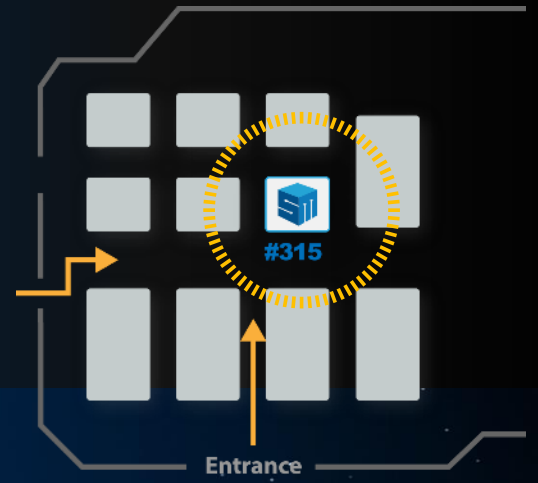

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