

How EDSFF exceeds for PCIe[®] 5.0 and 6.0

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Background



U.2 has been the primary form factor for HDDs for 15 years

- 1 form factor supporting multiple interfaces (SAS, PCIe)



EDSFF is a newer (~7 years)

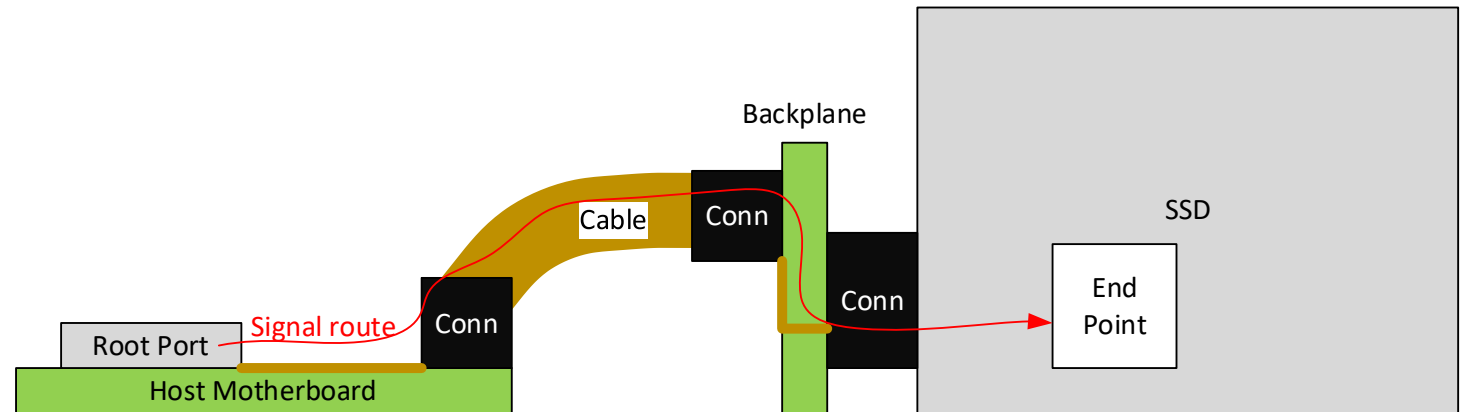
- 4 form factors for different applications
- Same card edge interconnect
- Same electrical specs for all devices

When looking at PCIe® 6.0, where are the issues?

Insertion loss budget with 3 connector topology

- PCB routing budget includes PCB loss (1 dB/in), via transitions, and AC cap loss
- Not much flexibility at 32 GT/s extremely limited at 64GT/s
- Both EDSFF and U.2 limited in this topology
 - If more budget is needed, either lower loss material or re-timers which add cost

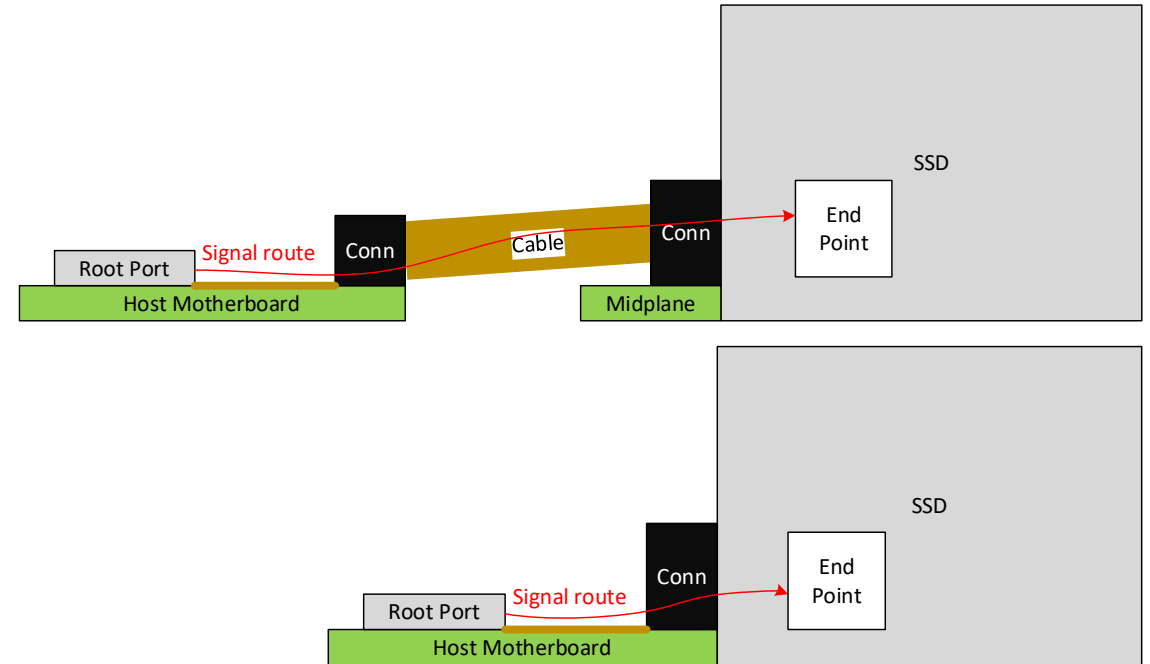
Spec	EDSFF		U.2	
Pcie revision	5.0 (32GT/s)	6.0 (64 GT/s)	5.0 (32GT/s)	6.0 (64 GT/s)
Nyquist	16 GHz	16 GHz	16 GHz	16 GHz
Loss target	36 dB	32 dB	36 dB	32 dB
Root complex @nyquist	9 dB	8 dB	9 dB	8 dB
1M mated cable @nyquist	7.5 dB	7 dB	7.5 dB	7 dB
Device connector @nyquist	1 dB	0.75 dB	0.75 dB	No spec
Device @nyquist	7 dB	6 dB	6.5 dB	No spec
PCB routing budget @nyquist	11.5 dB	10.25 dB	12.25 dB	10.25* dB



*Assumed same values for EDSFF and U.2 for Gen 6.0

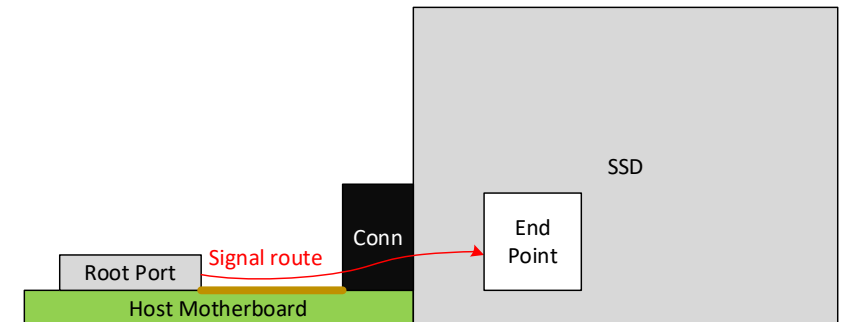
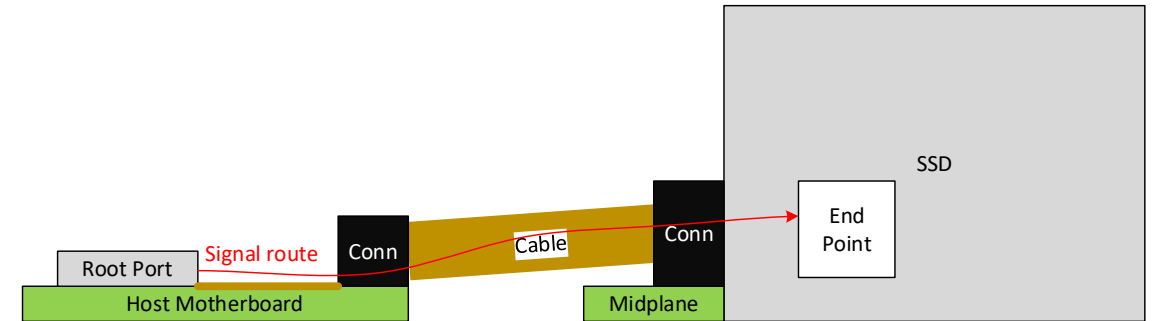
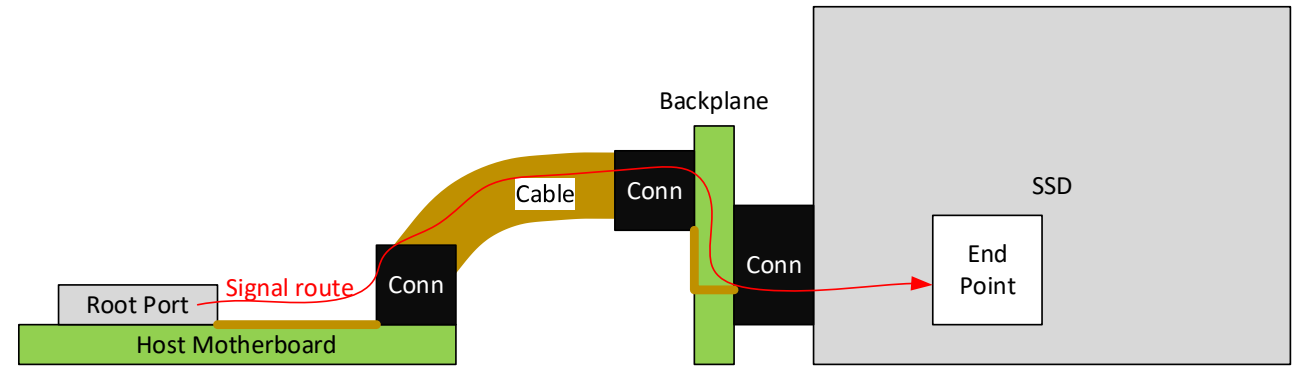
Reducing insertion loss with EDSFF

- EDSFF also supports 2 and 1 connector topologies
 - 2+ dB gained
 - SNIA SFF-TA-1016 hybrid connector
 - SNIA SFF-TA-1035 style B connector
- The 1 connector topology eliminates cabling
 - 6+ dB gained
 - SFF-TA-1002 orthogonal connector



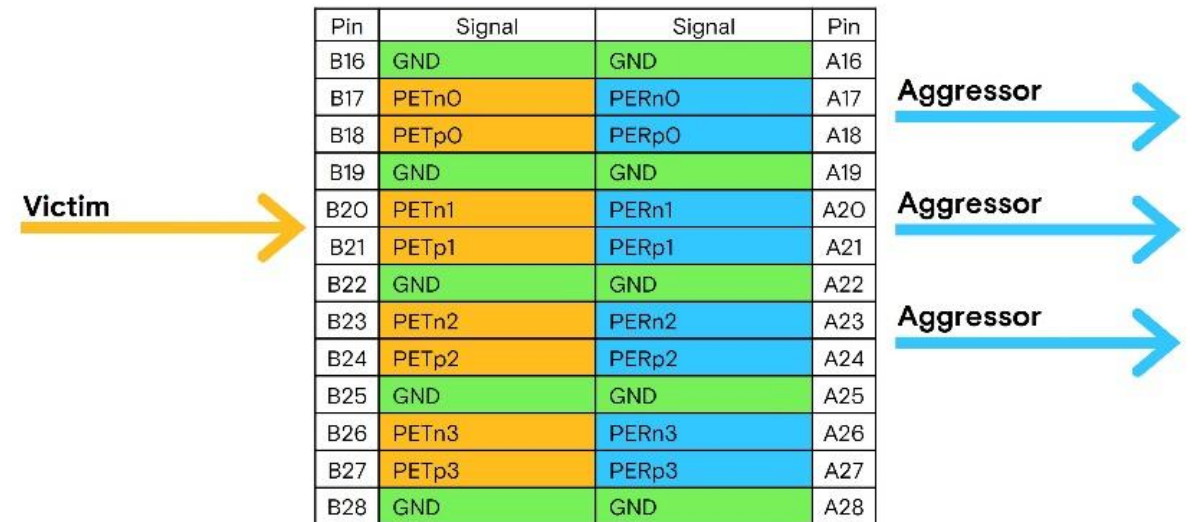
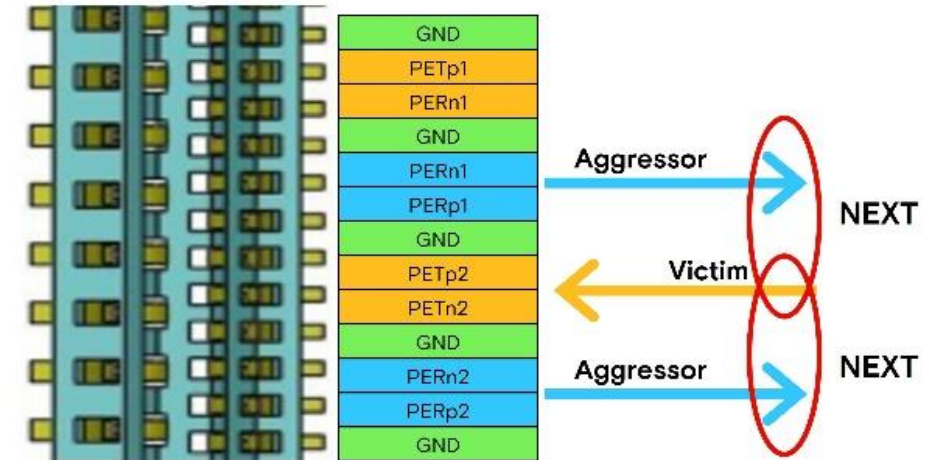
Return loss

- Return loss is impacted by impedance discontinuities
- U.2 has a 2-piece connector vs. EDSFF having a card edge
 - EDSFF has less transitions = better return loss
 - U.2 on device side also has impacts to routing making the problem worse
- With EDSFF 1 and 2 connector topologies, several additional discontinuities are eliminated
 - Less connector transitions
 - Less vias
- Both of these also have the benefit of requiring less



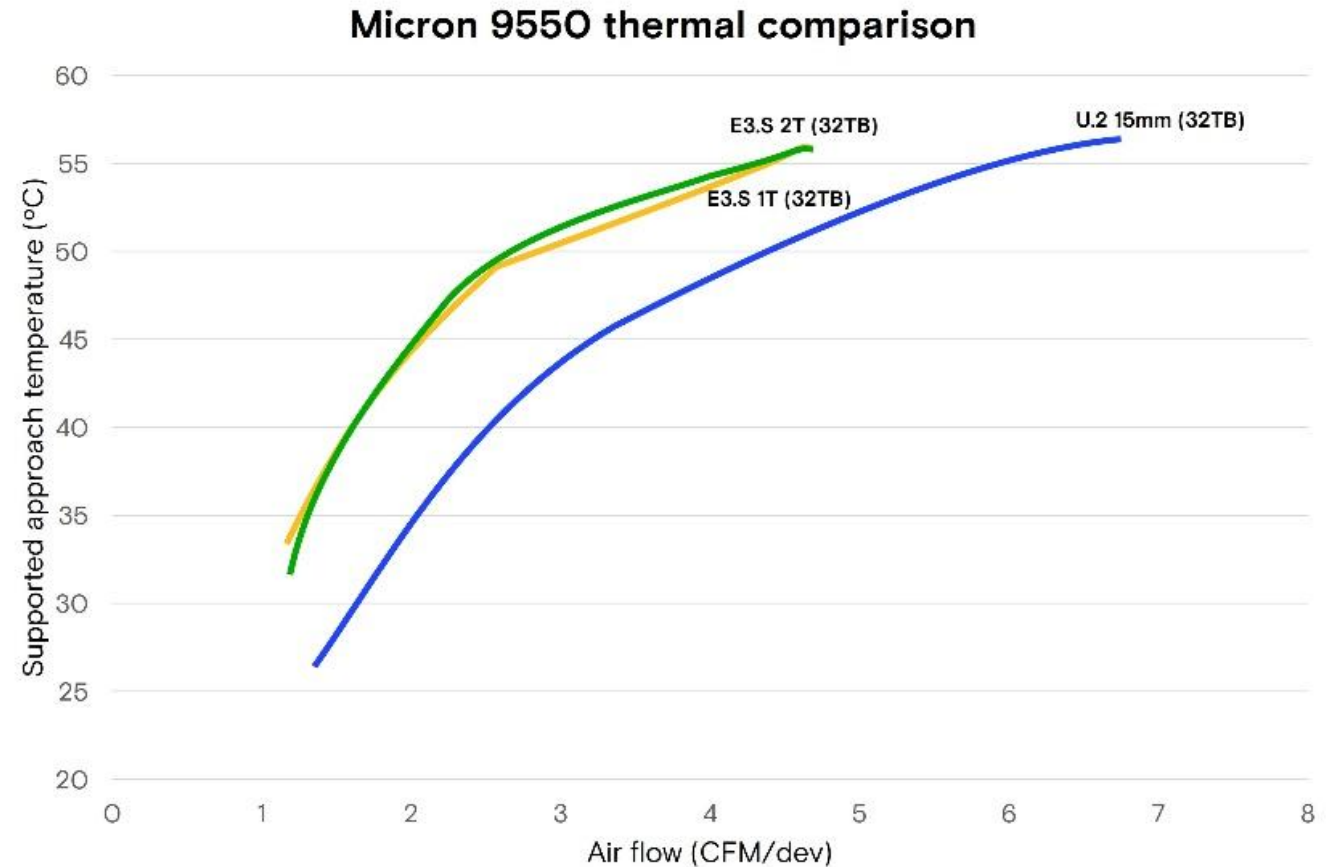
Crosstalk

- Significant challenge with PCIe 6.0 having lower SNR
- U.2 pin design not optimal for Near End Cross Talk (NEXT) due to TX and RX pins being interleaved
- EDSFF NEXT is much better due to having TX and RX on opposite sides of the connector and card edge



Power/thermals

- EDSFF E3.S is very similar in dimensions to U.2
- E3.S requires less volume of air to cool at the same capacity and power as U.2 regardless of approach temp
- E3.S is more efficient at passing airflow through the SSD
 - Fewer components/connectors impeding airflow



Summary

- For PCIe 5.0 and 6.0
 - EDSFF provides more options for improving insertion loss at a lower cost
 - EDSFF has better return loss
 - EDSFF has better crosstalk performance
 - EDSFF has better thermal capability
- Recommend moving away from U.2 to EDSFF for future host systems



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