PGM Efficiency Improvement method for QLC device

PRESENTER

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SK hynix

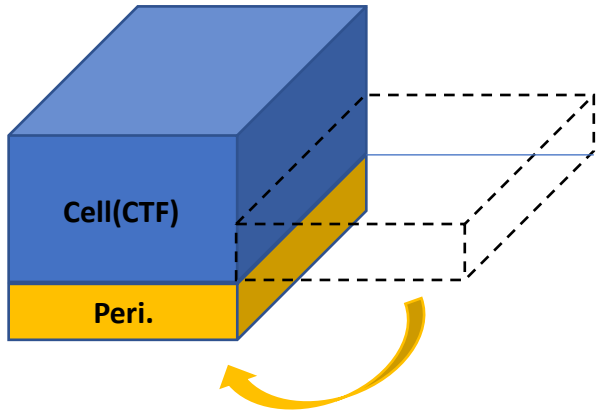
Agenda

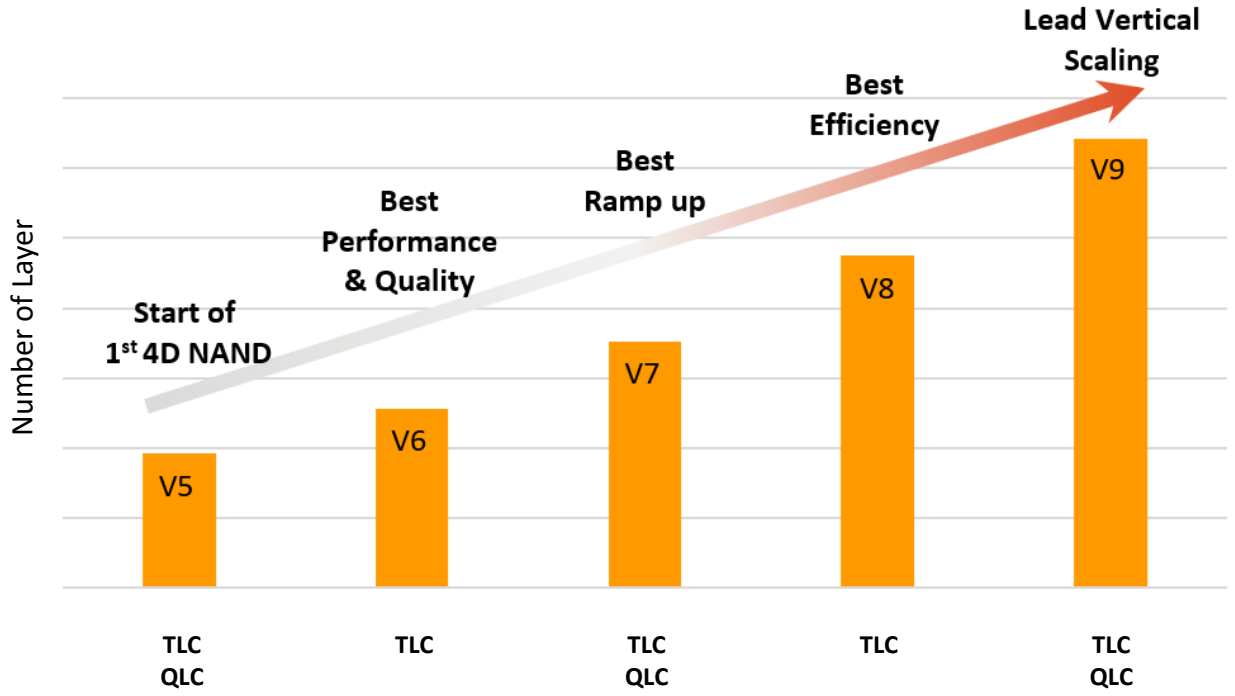
- SK Hynix NAND Tech Platform Scaling
- Challenges of Stacking
- Methods to Improve Program Efficiency
- Concept of a New Method to Improve Program Efficiency and Results
- Summary

SK Hynix NAND Tech Platform Scaling

- SK Hynix's been mass-producing 4D PUC up to the 5th generation, utilizing highly matured CTF technology
- Also developed QLC NAND, starting with the first generation of 4D PUC

4D Peri Under Cell (PUC)



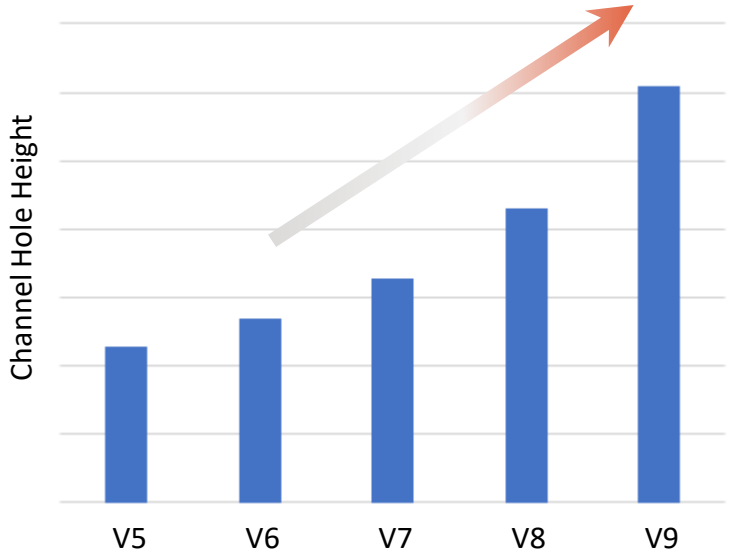


Challenges of Stacking

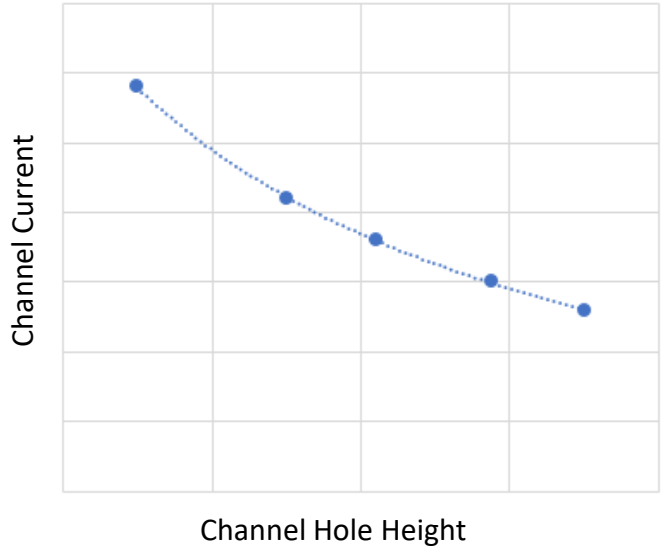
- The total height of the channel hole has increased with the addition of multiple layers
- To secure channel current, the vertical gate pitch should be reduced

→ Cell characteristic will be deteriorated

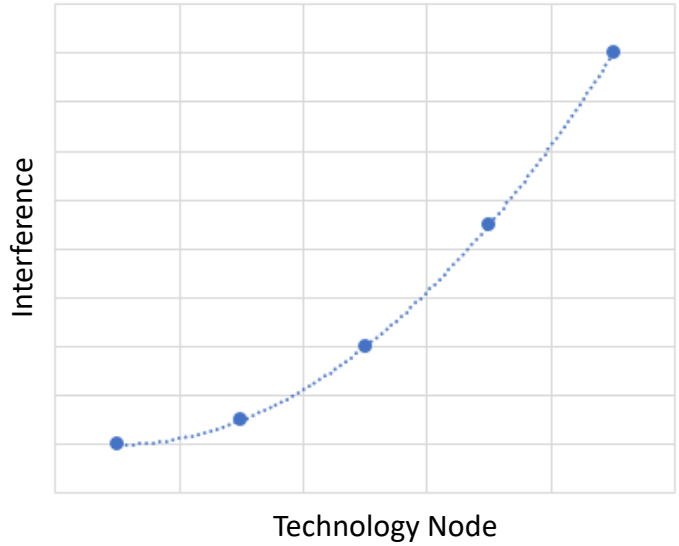
Channel Hole Height



Channel Current



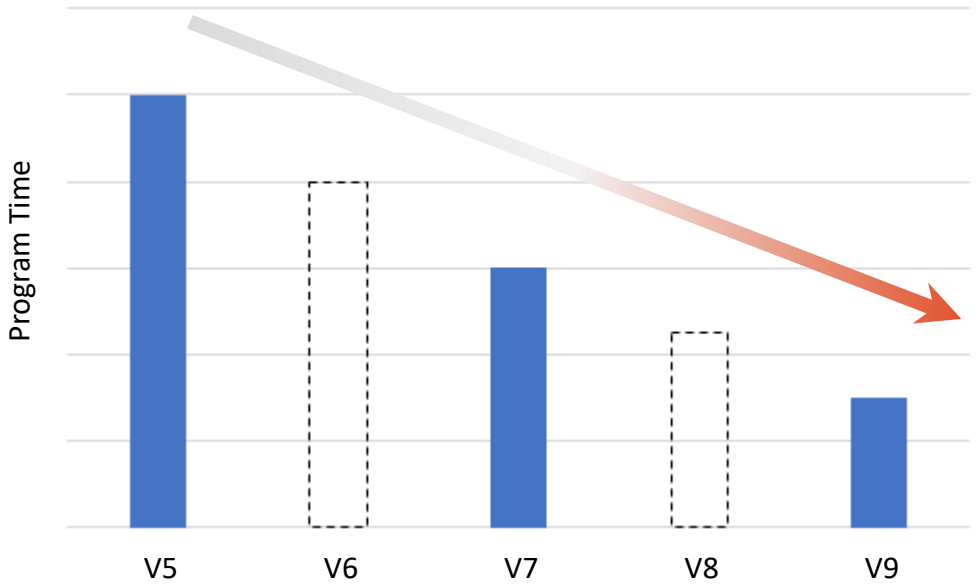
Interference between word lines



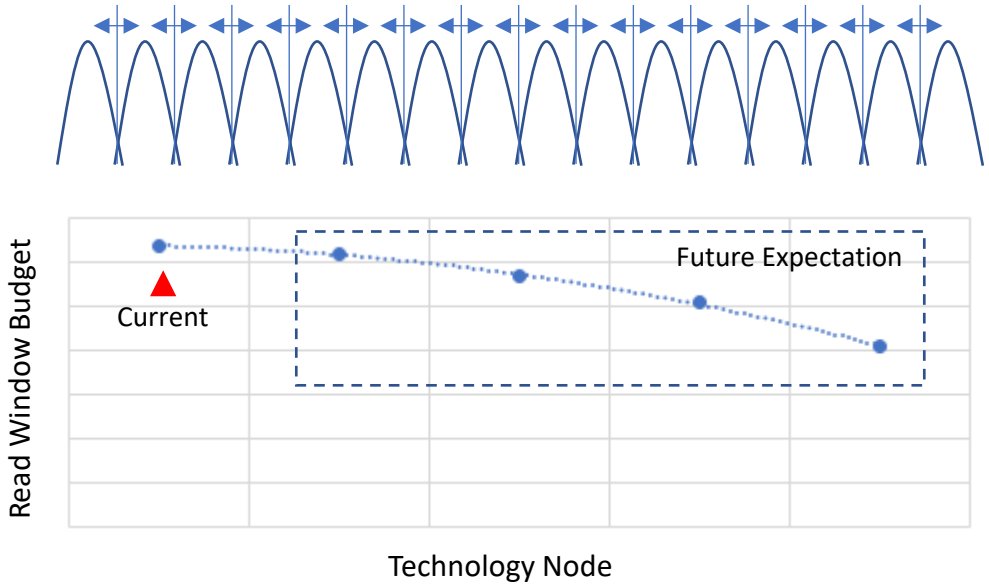
QLC Program Time and Read Window Expectation

- QLC program time is becoming shorter as generations progress
- Due to these circumstances, a reduction in the read window is anticipated in future tech.

Program Time at QLC mode

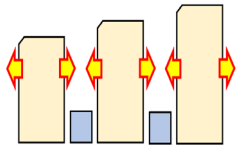
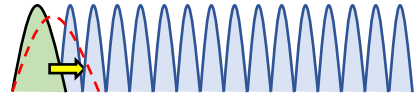
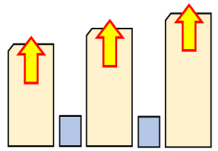
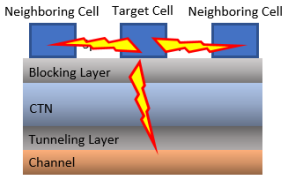
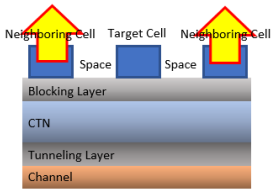
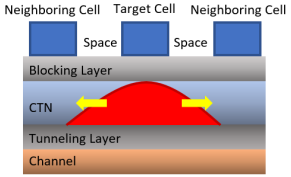


Read Window Budget Expectation



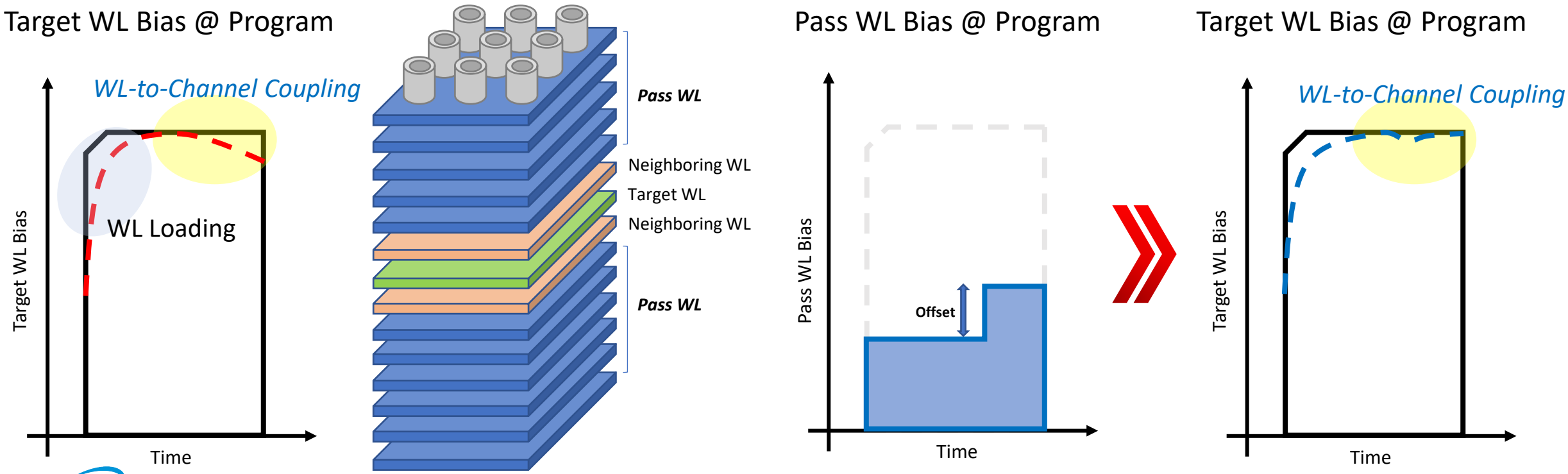
Methods to Improve Program Efficiency

- There are various approaches to improving program efficiency, but there are also challenges involved

Program Efficiency Improvement Methods		Challenges	
Process	WL Resistivity Improvement	Cost, Vertical gate pitch	
Design	Pump Capacity/Efficiency	Chip Size, Power Consumption	
Algorithm	Program Net-time Control 	Program Disturbance Degradation 	
	Program Pulse Bias Control 	WL to WL Breakdown / WL to Channel Breakdown 	
	Neighboring WL Control 	Lateral Charge Spreading 	

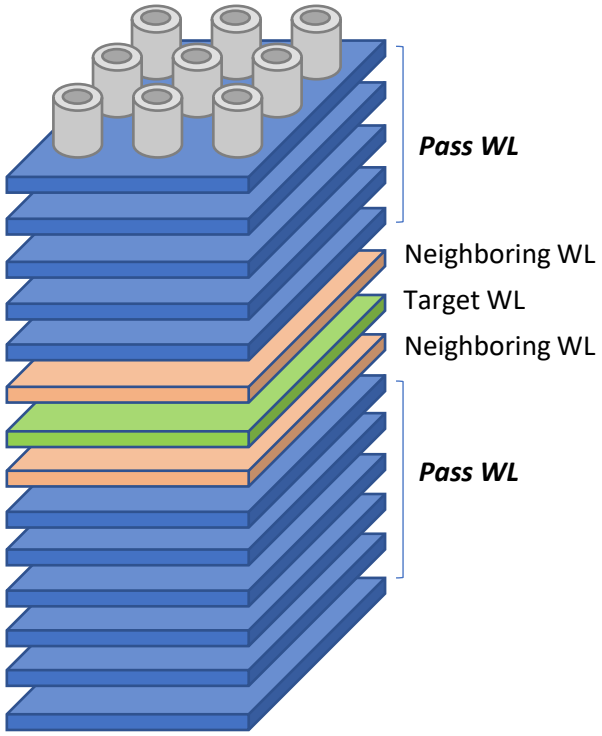
Another Way to Improve Program Efficiency

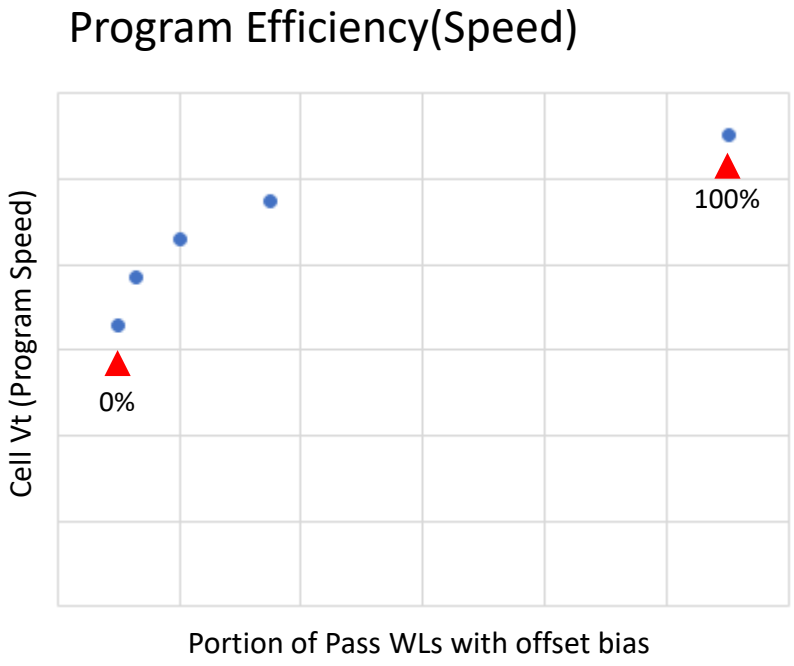
- Program efficiency has degraded due to word line (WL) loading and WL-to-Channel coupling
- WL-to-channel coupling is caused by the drop in channel potential during a program pulse
- To compensate for the WL-to-Channel coupling, the bias on the pass WLs needs to be offset at program pulse

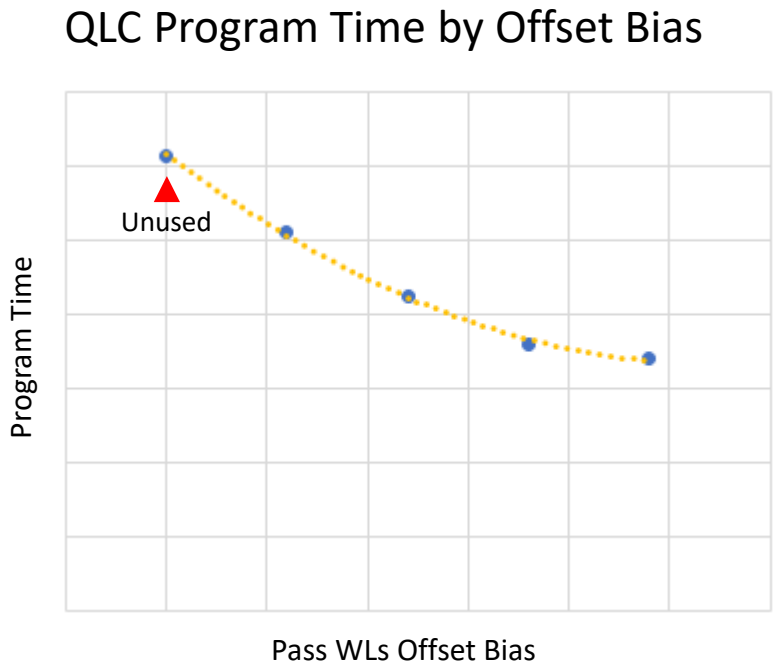


Results

- Increasing the portion of Pass WL with applied offset bias enhances program efficiency
- As the offset bias is increased, the QLC program time decreases, and saturation is observed beyond a certain offset bias







Summary

- As more layers are introduced in NAND flash memory, reducing vertical gate pitch helps address channel current but may negatively impact cell characteristics and program performance
- Various methods are available to improve program efficiency, each with its own advantages and disadvantages
- One effective strategy is to adjust the bias of the Pass WLs during program operations
- Using this method, mitigate the effects of program efficiency reduction caused by WL-to-channel coupling

PGM Efficiency Improvement Method for QLC device

Questions?

Talk to us in the hallway or at the SK Hynix Booth!

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