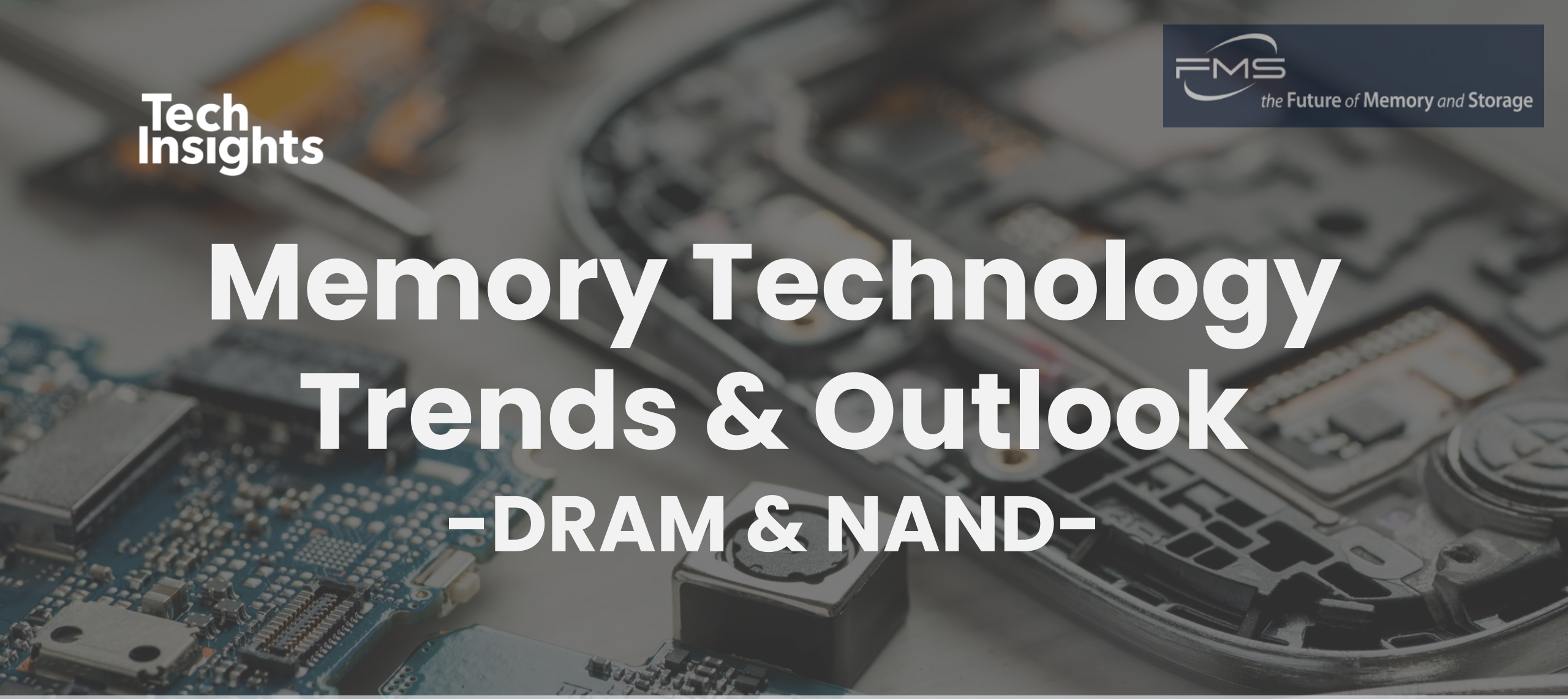


Tech Insights

FMS the Future of Memory and Storage

Memory Technology Trends & Outlook

-DRAM & NAND-

FMS 2025

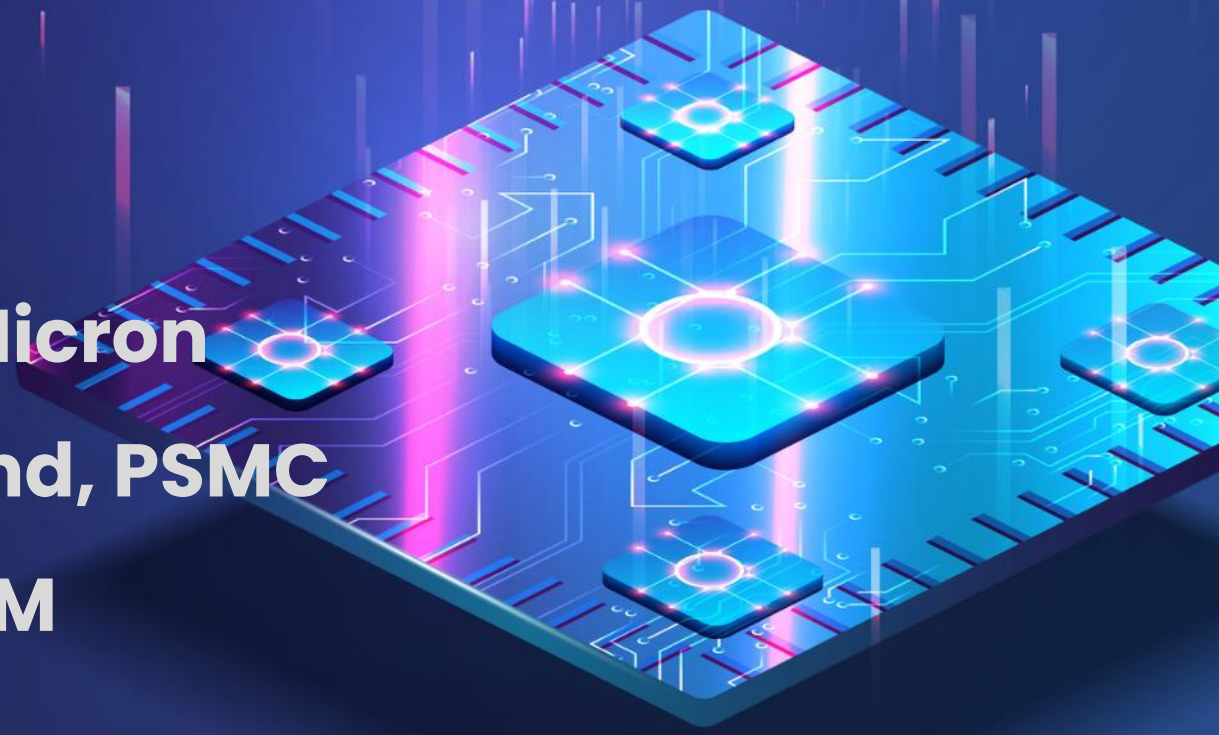
Dr. Jeongdong Choe
Senior Technical Fellow, SVP
www.techinsights.com

FMS
the Future of Memory and Storage

Session 1

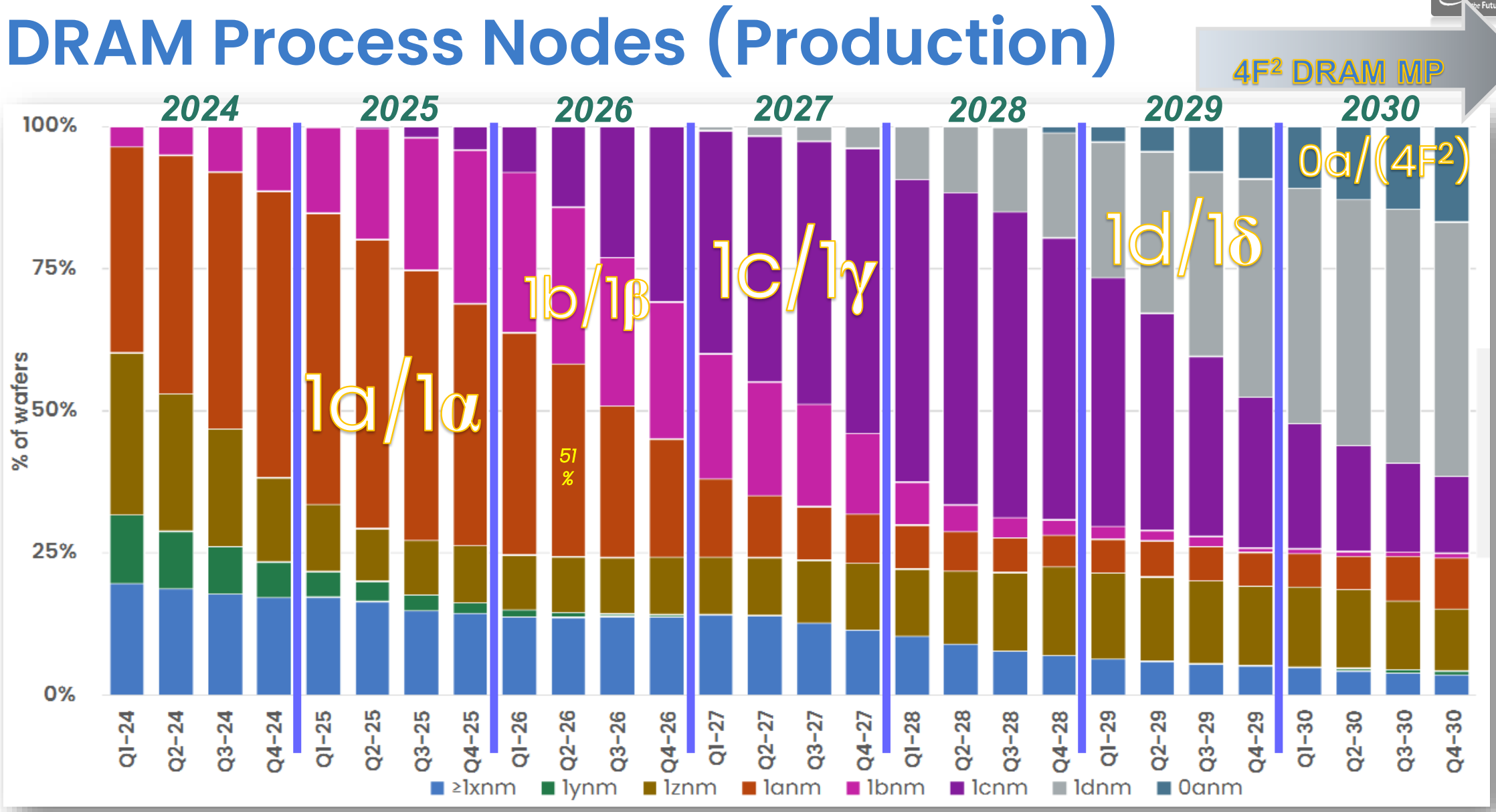
➢ DRAM

- DRAM Market
- Samsung, SK hynix, Micron
- CXMT, Nanya, Winbond, PSMC
- DDR/LPDDR/GDDR/HBM



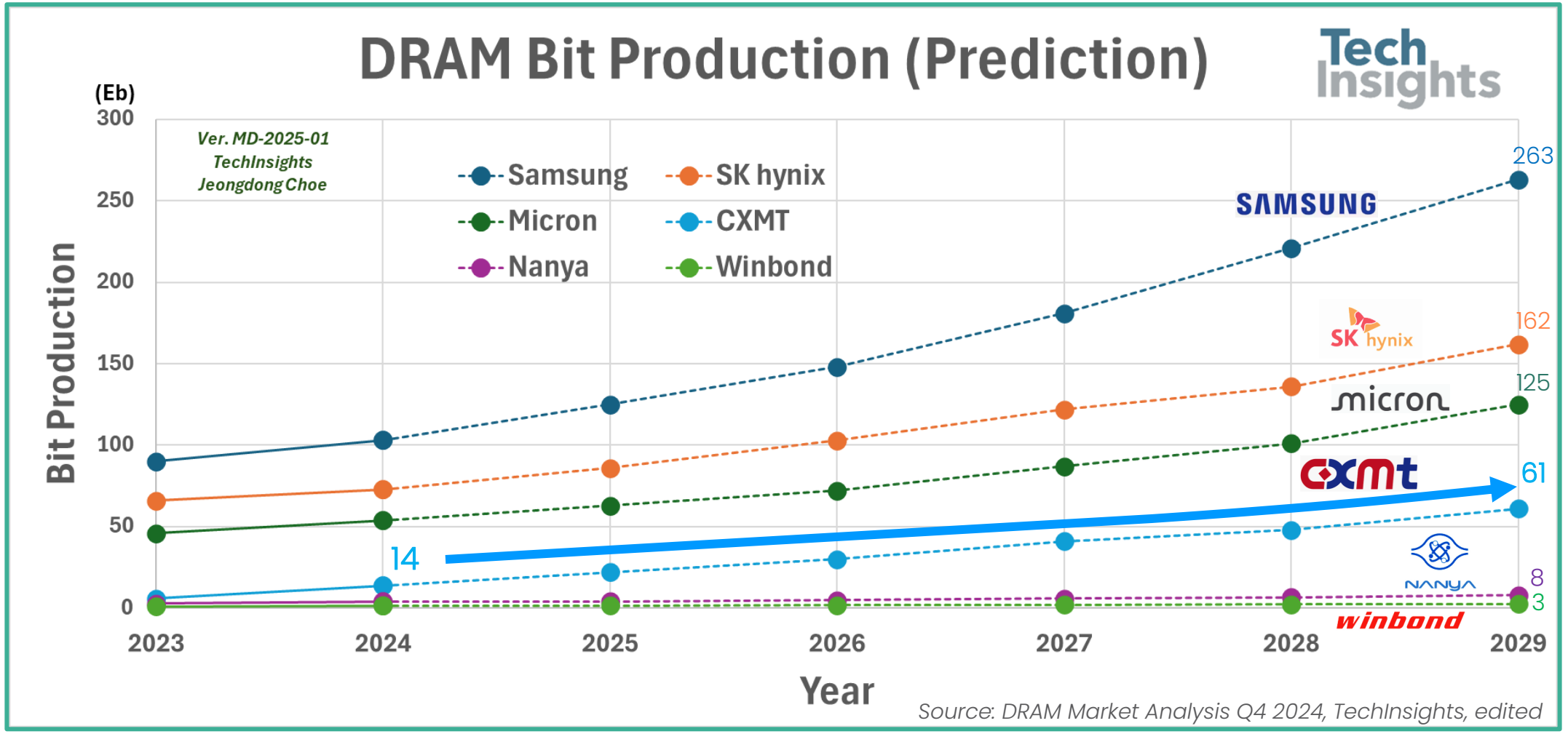
Tech Insights

DRAM Process Nodes (Production)



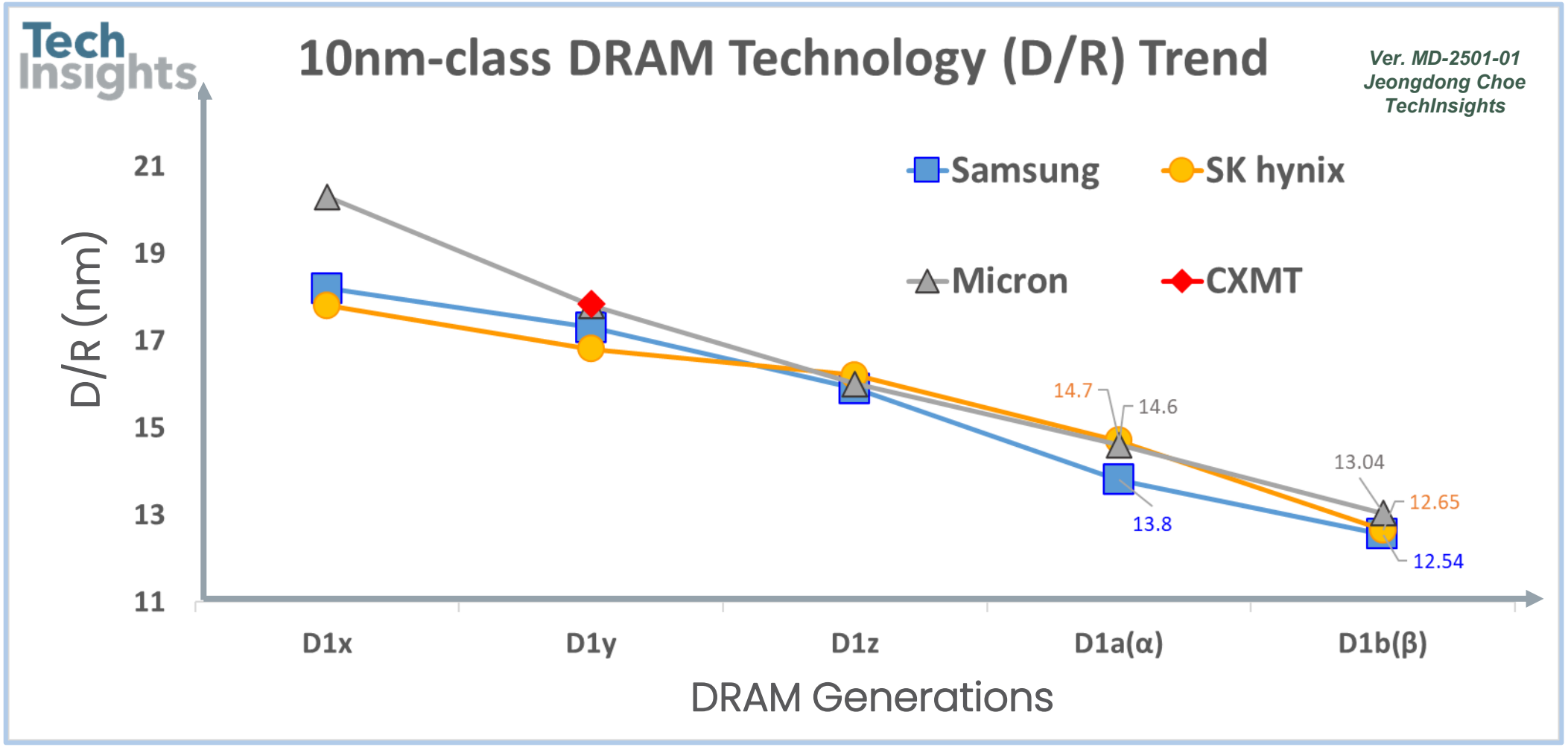
Source: DRAM Market Analysis Q2 2025, TechInsights

DRAM Bit Production (Expected)

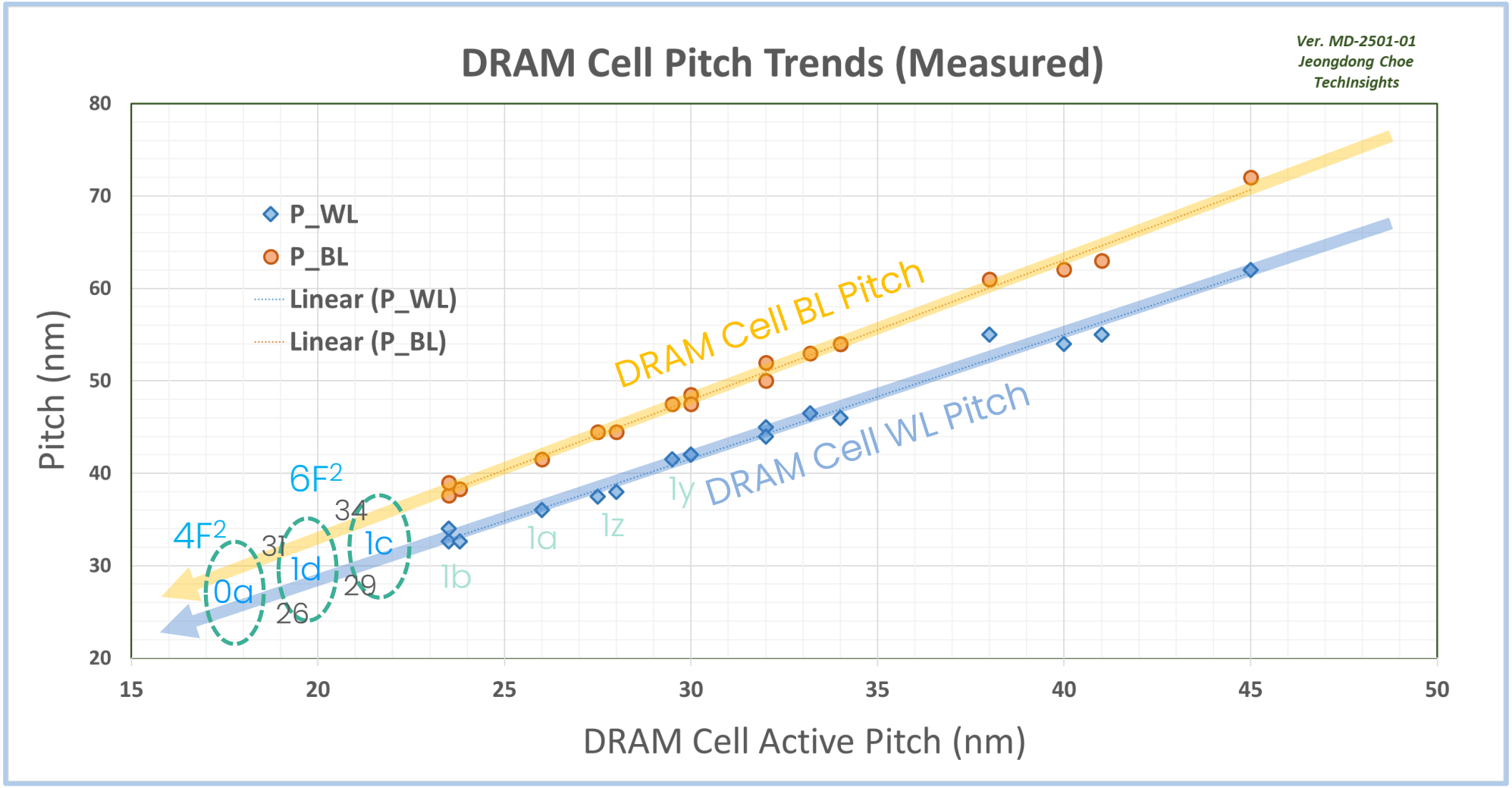


Source: DRAM Market Analysis Q4 2024, TechInsights, edited

DRAM Technology Node (D/R, F)



DRAM Pitch Trends: WL, BL



D1b(D1β) DRAM Cell: Samsung *vs.* SK hynix *vs.* Micron

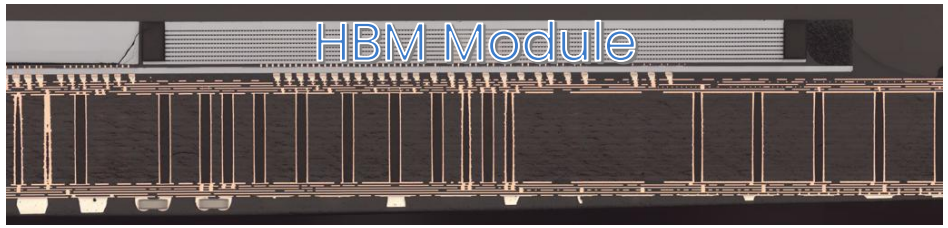
Items	Samsung D1b	SK hynix D1b	Micron D1β
Die Size/Ex. Device	36.68 mm^2/LPDDR5X 16Gb, Samsung (6.55 mm × 5.60 mm)	37.98 mm^2/DDR5 16Gb, SK hynix (6.47 mm × 5.87 mm)	36.78 mm^2/LPDDR5 16Gb, Micron (7.02 mm × 5.24 mm)
Bit Density	446.67 Mb/mm^2	431.40 Mb/mm^2	435.0 Mb/mm^2
Cell size	0.00123 μm^2	0.00125 μm^2	0.00133 μm^2
WL (Cell Gate) Materials	TiN/Poly	TiN/Poly	TiN/Poly
Active Island Length	85 nm	84 nm	92 nm
Pitch (Act/WL/BL) Measured	23.5 nm/32.6 nm/37.6 nm	23.4 nm/33.1 nm/37.9 nm	24.0 nm/34.0 nm/39.0 nm
Feature Size [F, D/R]	12.5 nm	12.6 nm	13.1 nm
Interconnection to BL	M1	M1	M1/M2
Peri-Gate Pitch (Smallest)	100 nm	130 nm	108 nm
Cell SNLP Shape	Circle	Circle	Circle
SNC Etch	Likely, SAC	Likely, SAC	Likely, SAC
Top Plate Materials	SiGe 230 nm on TiN	W/SiGe 54 nm/95 nm on TiN	W/SiGe 100 nm/88 nm on TiN
Cap. Dielectrics Detected	HfO/ZrO/ZrAlO (NbO)	ZrO/HfAlO/ZrAlO/HfAlO/ZrAlO	ZrO/HfAlZrO/HfZrO/AlO
Cap. MESH Photo/Etch Pattern	Circle/Triangle	Circle/Triangle	Oval/Hexagonal
Number of Metal Layers	6 (1 W, 4 Cu, 1 Al) + RDL	5 (1 W, 3 Cu, 1 Al) + RDL	7 (2 W, 4 Cu, 1 Al) + RDL

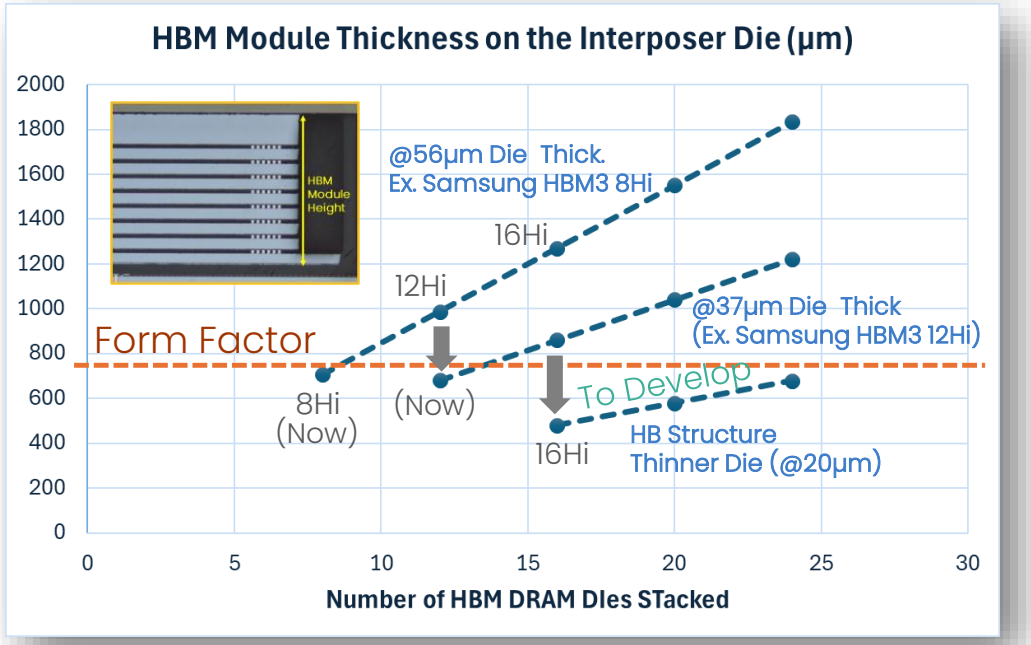
CXMT DRAM: G4

Items	CXMT G1	CXMT G3	CXMT G4
Die Size/Ex. Device	79.20 mm^2 (7.12 mm × 10.99 mm) CXMT CXDQ3A8AM-CG 1 GB DDR4 Device (8 Gb Die)	44.66 mm^2 (4.87 mm × 9.17 mm) CXMT CXDB6CCDM-MA 8 GB LPDDR4X Device (8 Gb Die)	66.99 mm^2 (8.19 mm × 8.18 mm) Gloway 16GBx2 (32GB) DDR5-6000 2 GB DDR5 Device **(16 Gb Die)**
Bit Density	0.101 Gb/mm^2	0.179 Gb/mm^2	0.239 Gb/mm^2
Cell size	0.0044 μm^2	0.0025 μm^2	0.0020 μm^2
Feature Size	23.8 nm	18.0 nm	16.0 nm
Pitch (Act/WL/BL)Measured	45.0 nm/61.0 nm/72.0 nm	34.0 nm/46.6 nm/54.2 nm	29.8 nm/41.7 nm/47.9 nm
Relative Generation (Samsung/SK hynix/Micron)	D2y	D1x	D1z
Cell Gate Materials	W/(TiN)	W/(TiN)	Poly-Si/TiN
Cap. Dielectrics	ZrO/ZrAlO	ZrO/ZrAlO	ZrO/HfO/ZrO/HfO/ZrAlO

Hybrid Bonding for HBM Application

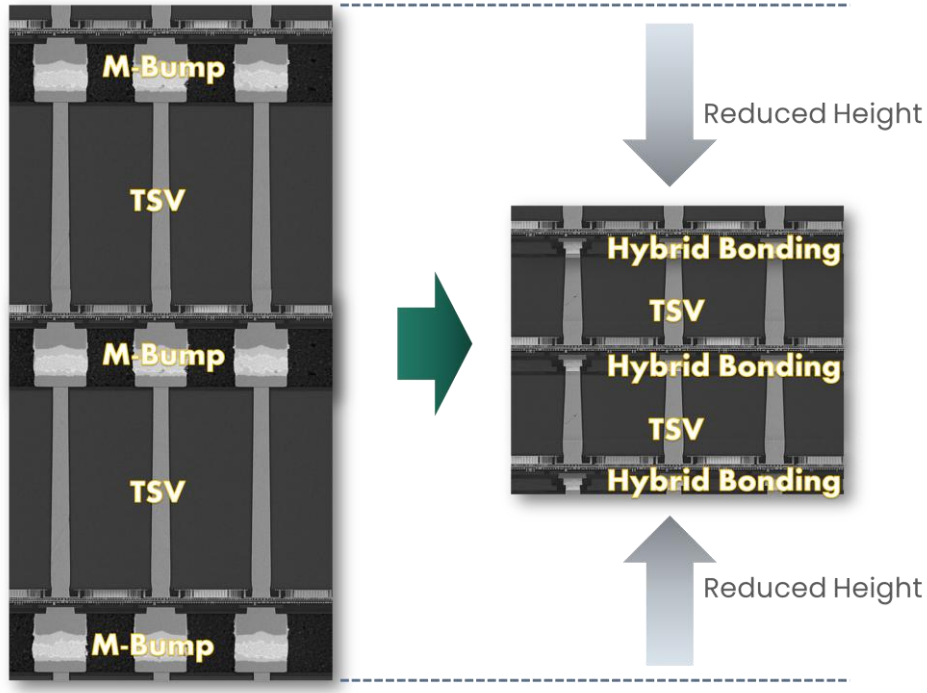
✓ Due to limited HBM module height (Form Factor), HB structures with thinner dies are required





Gap-fill Structure

Gapless Structure
(with Thinner Dies)



FMS the Future of Memory and Storage

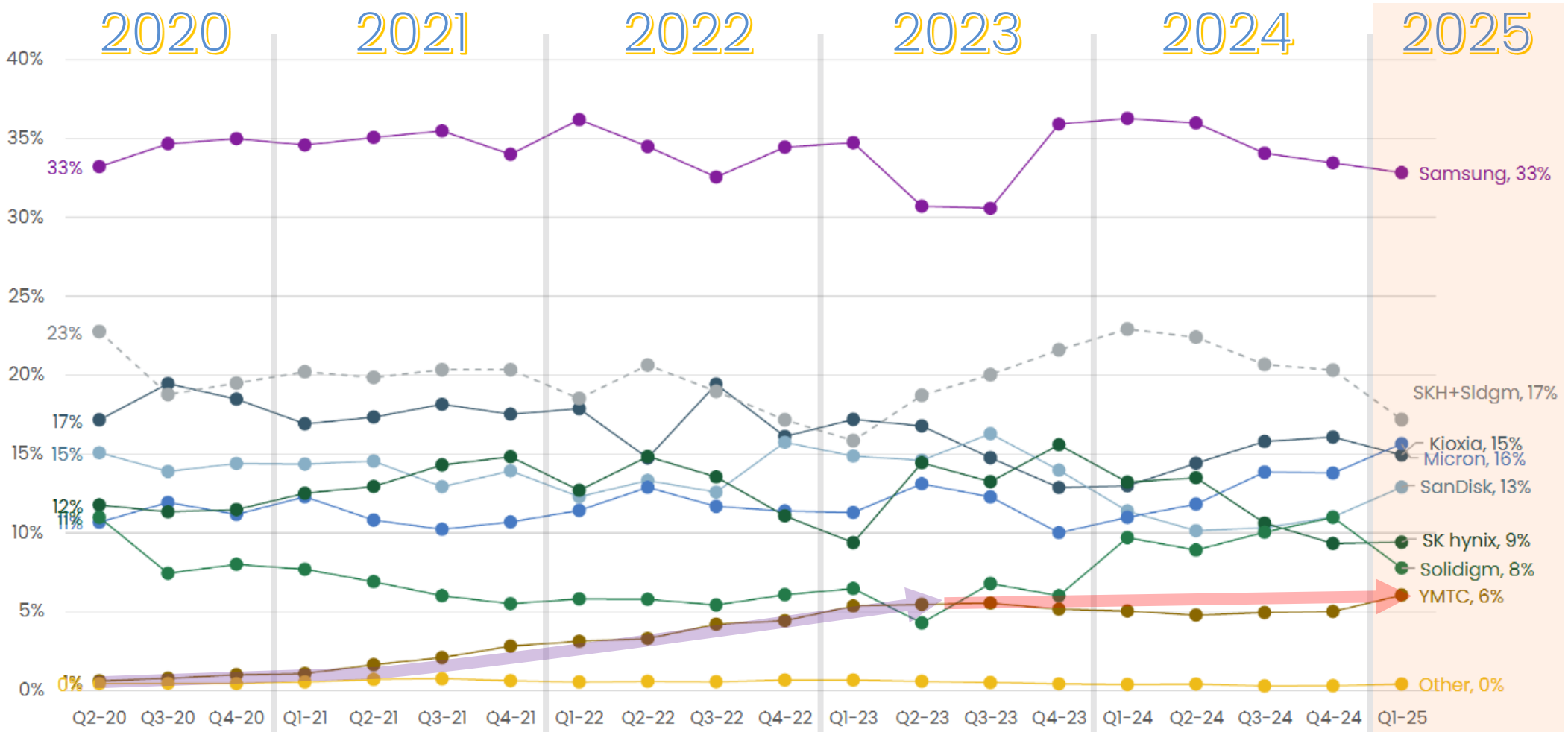
Session 2

➢ 3D NAND

- NAND Market
- Samsung, SK hynix/Solidigm
- Micron, KIOXIA, SanDisk, YMTC
- 2xxL/2yyL, Hybrid Bonding

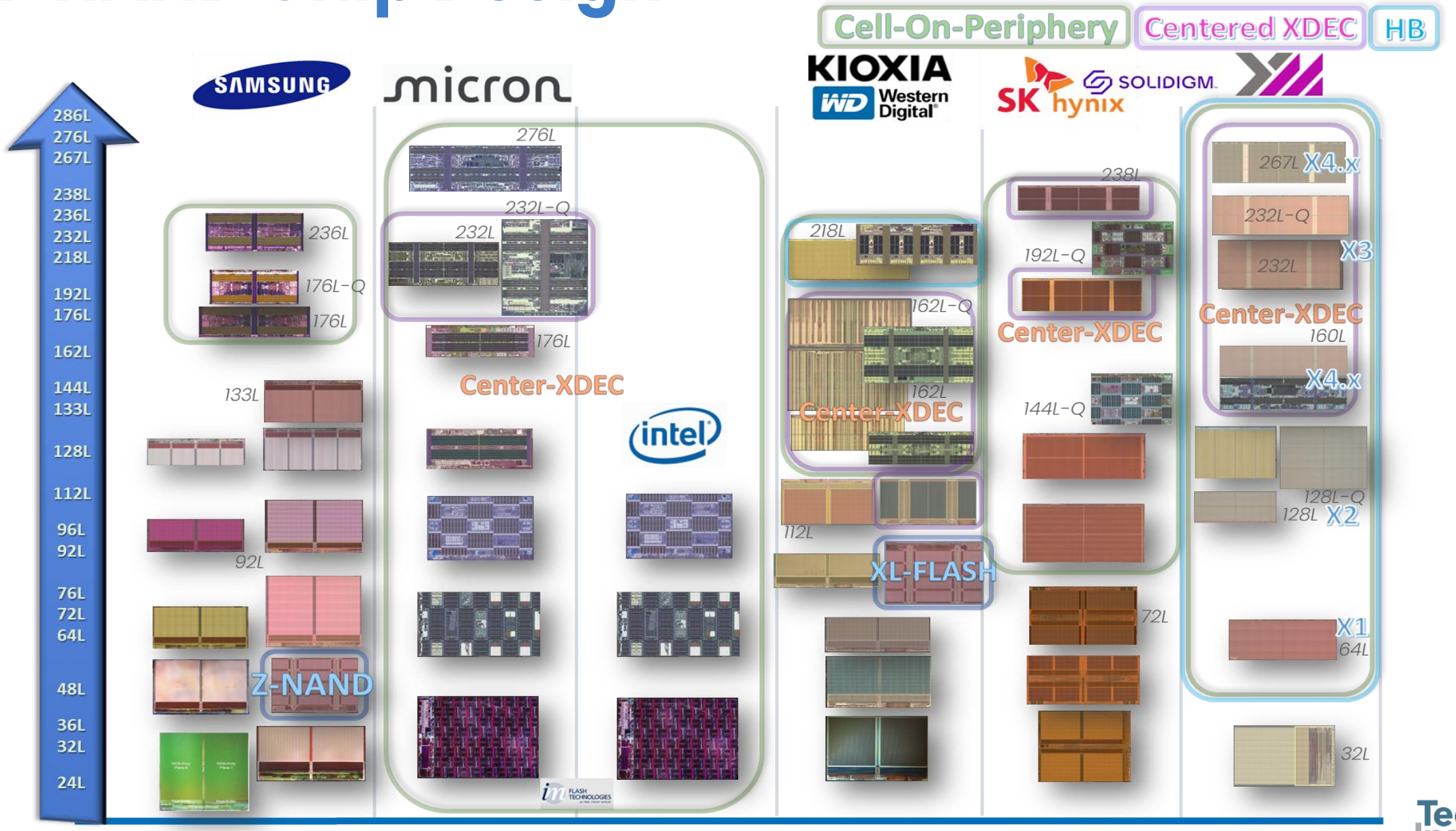
Tech Insights

NAND Market Share (Revenue)

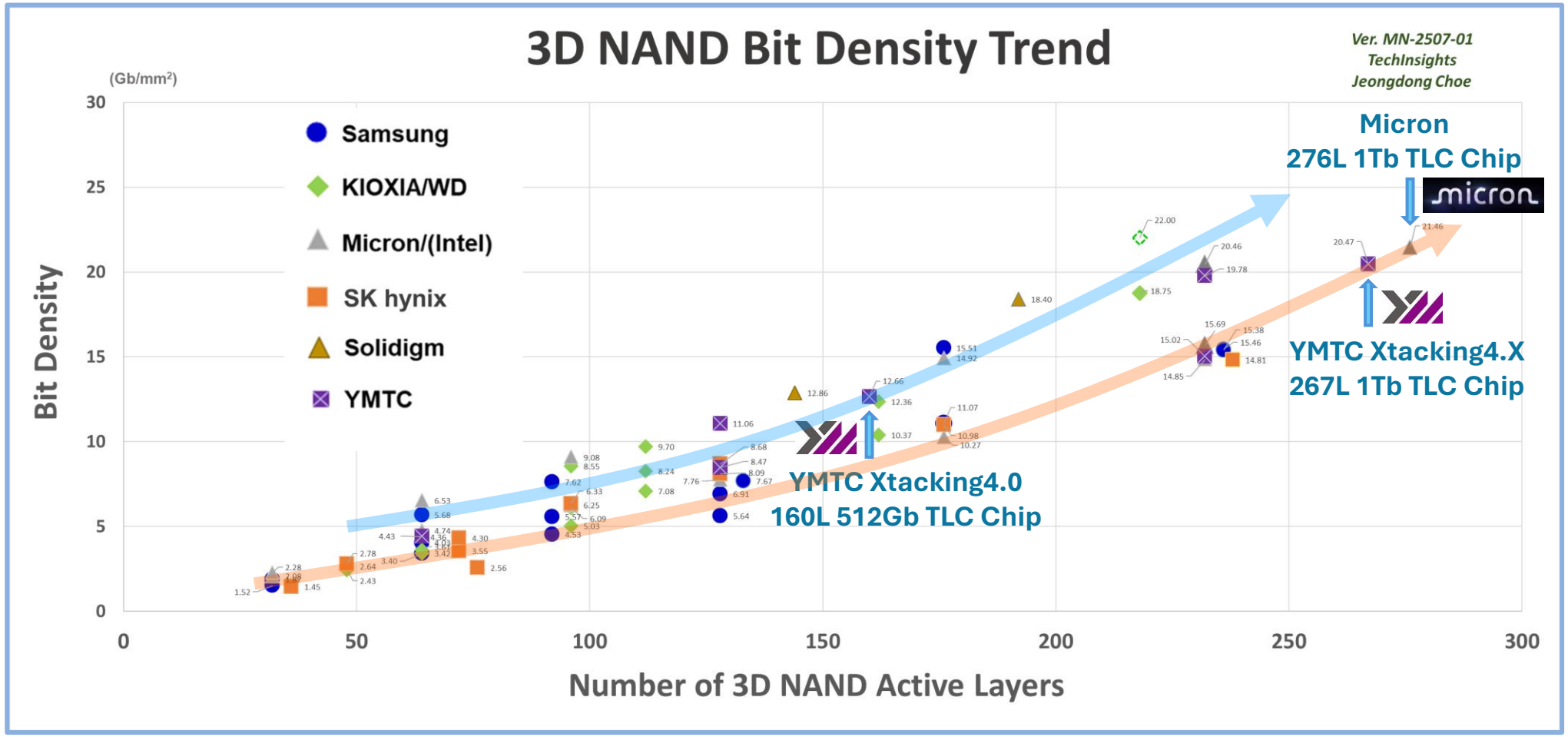


Source: NAND Market Analysis Q2 2025, TechInsights

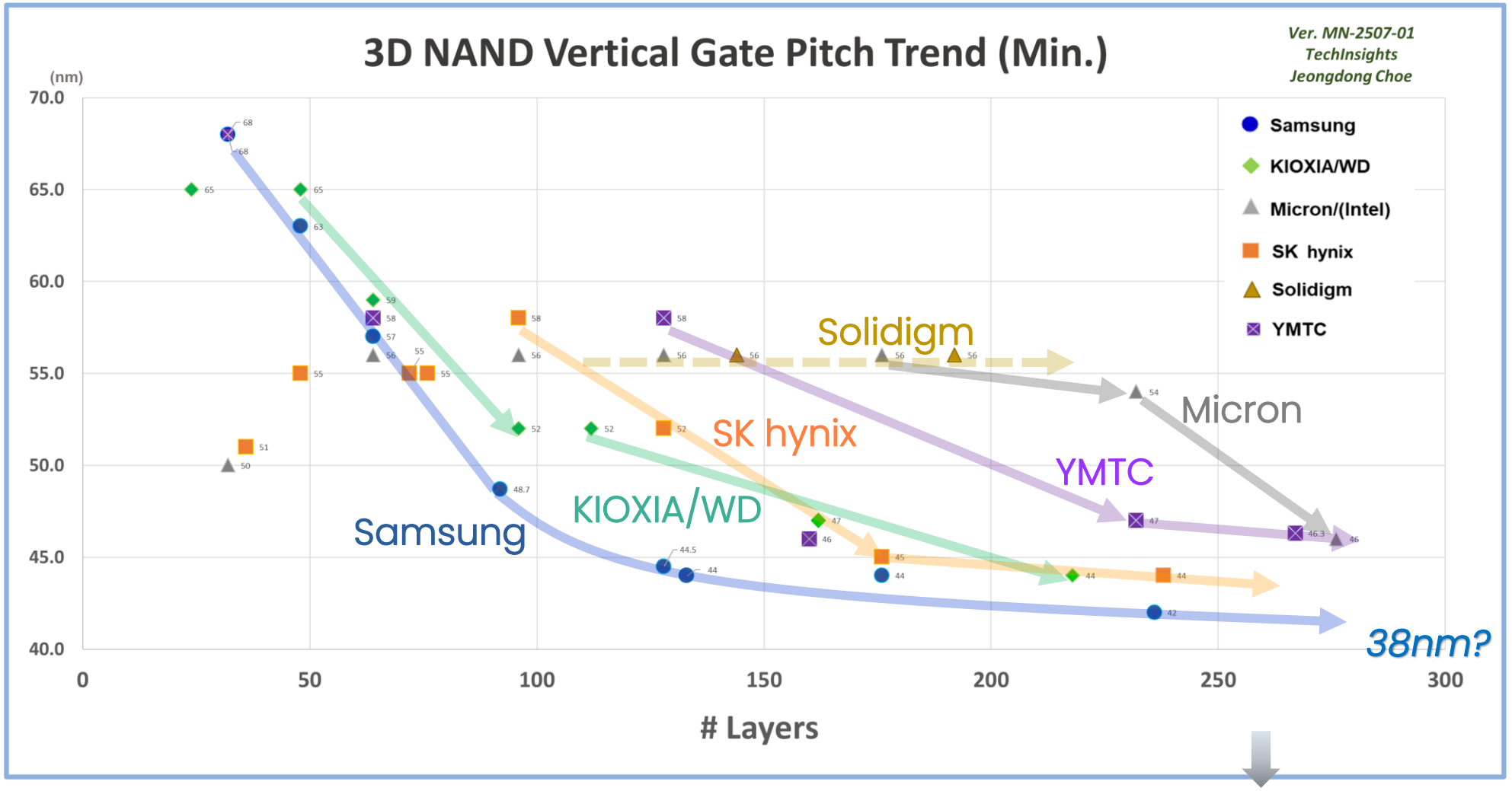
3D NAND Chip Design



3D NAND Bit Density Trend (TLC, QLC)

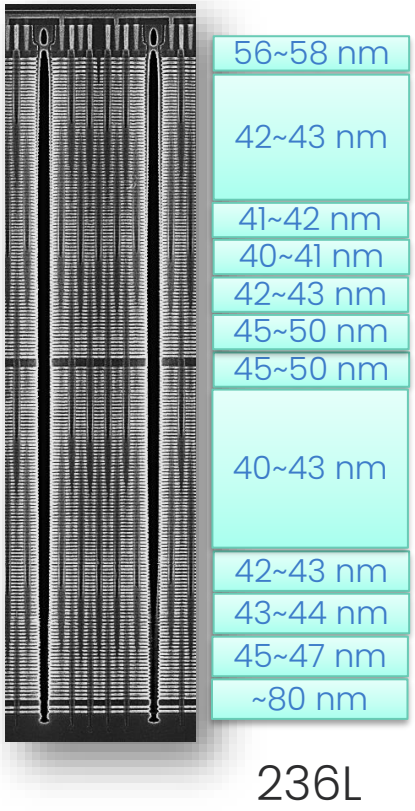


3D NAND Min. Vertical Gate Pitch Trend



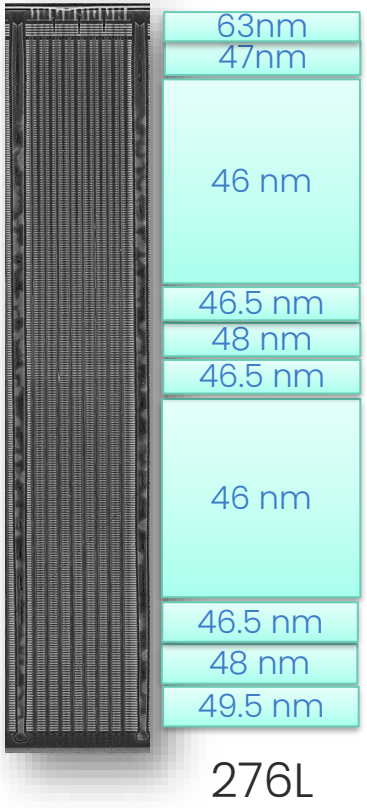
Mold Thickness Engineering (Measured)

- Samsung



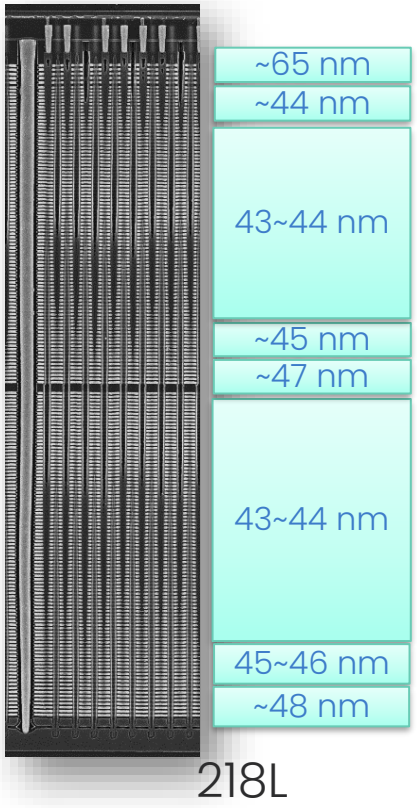
236L

- Micron



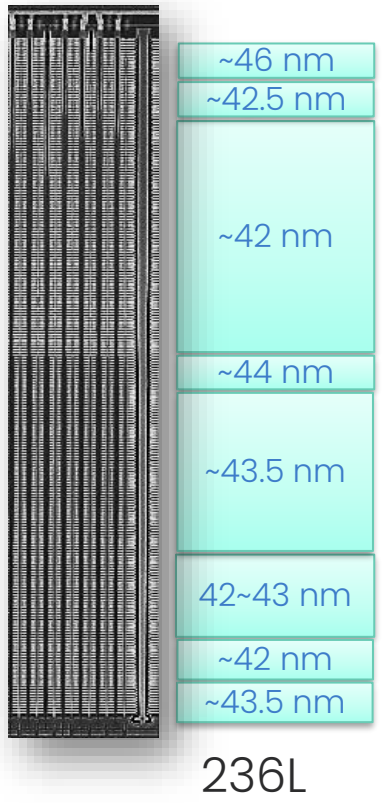
276L

- KIOXIA



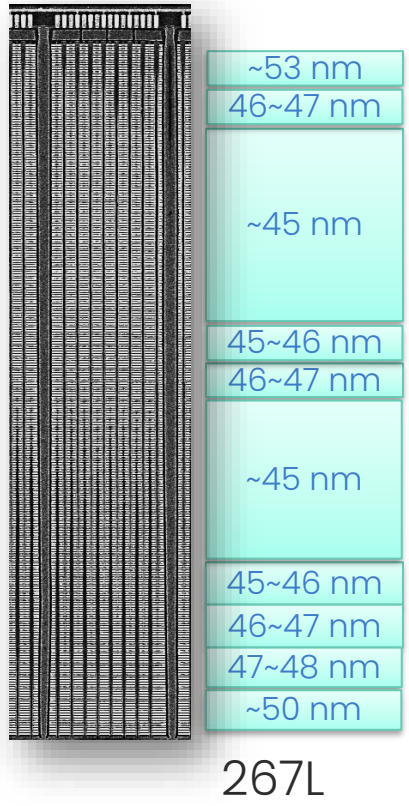
218L

- SK hynix



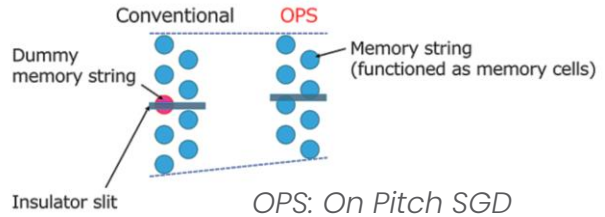
236L

- YMTC



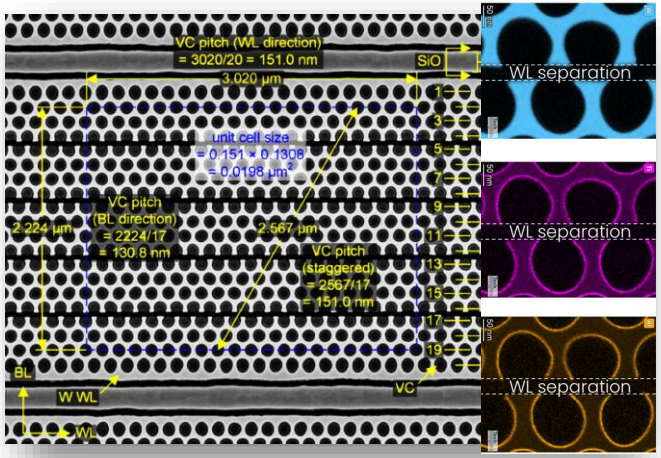
267L

Vertical Channel Holes: OPS Design



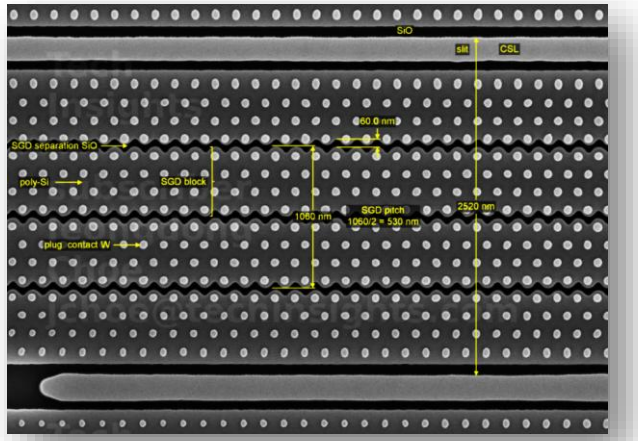
OPS: On Pitch SGD

KIOXIA 20 Holes (No dummy VC)



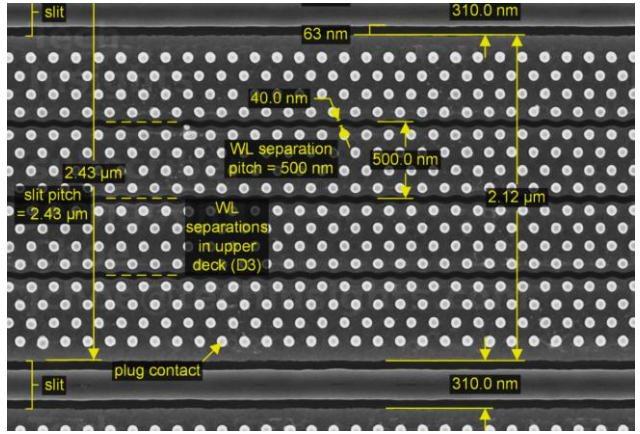
Ex. KIOXIA 218L
Active #VC: 20
Slit Pitch 3.07 μm
VCP: 130.8 nm (BL direction)

YMTC 16 Holes (No dummy VCs)



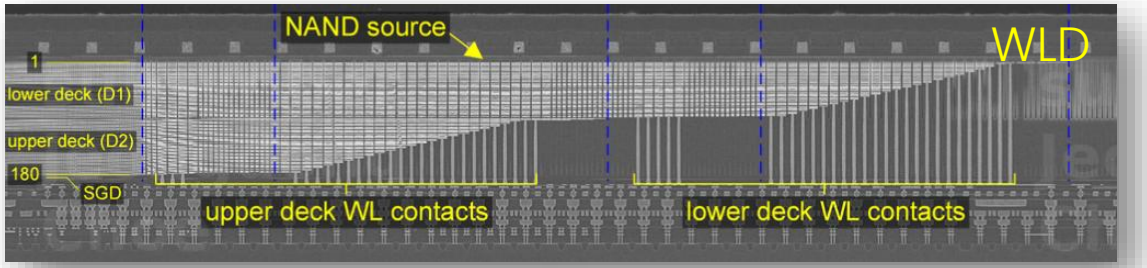
Ex. YMTC 267L
Active #VC: 16
Slit Pitch 2.52 μm
VCP: 132.0 nm (BL direction)

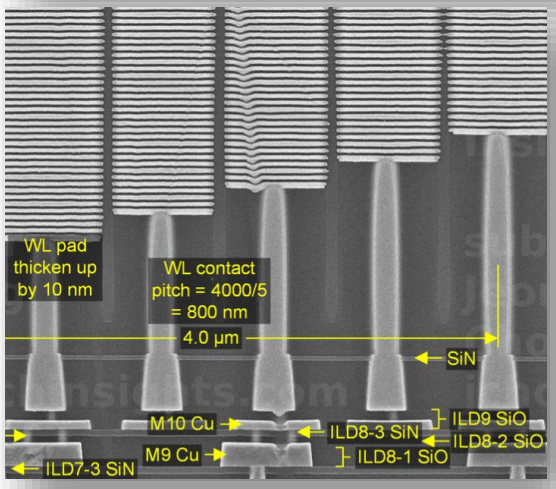
Micron 16 Holes (No dummy VCs)



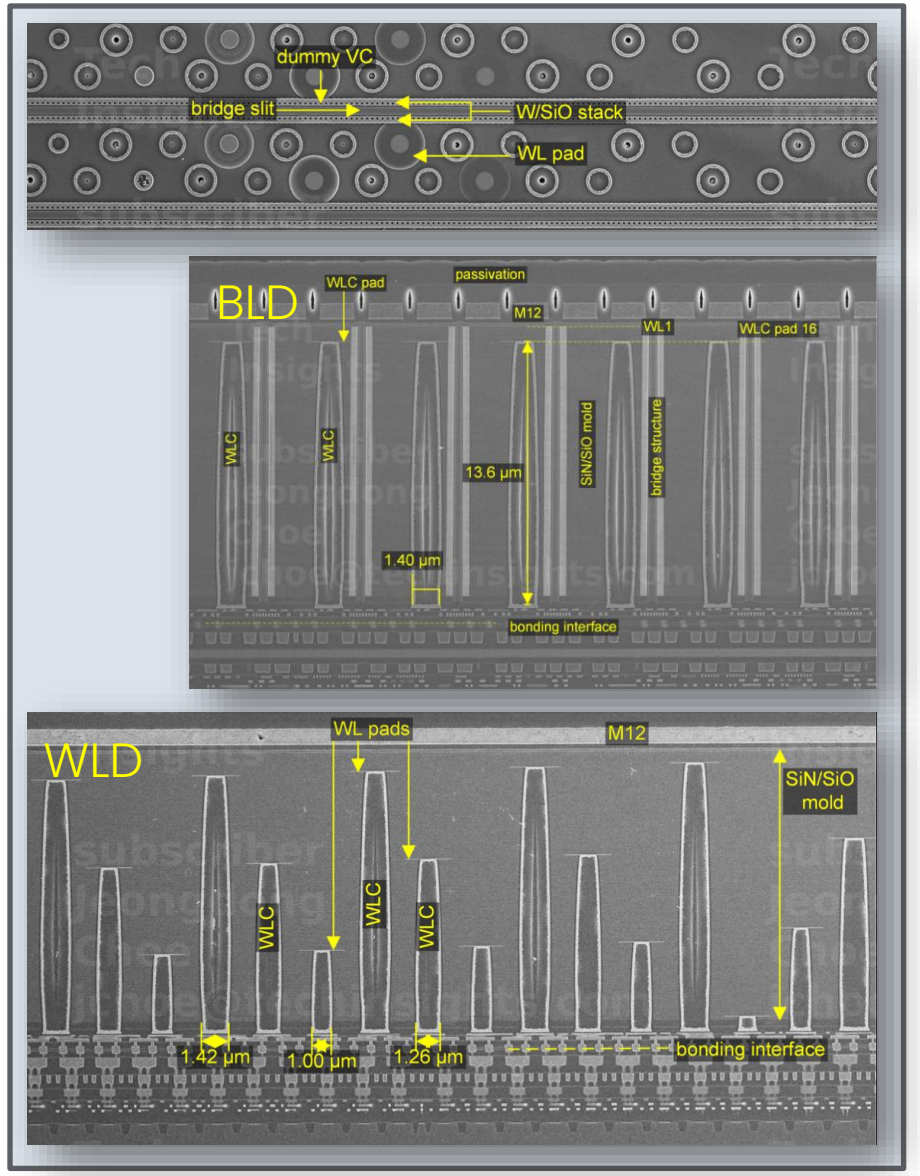
Ex. Micron 276L
Active #VC: 16
Slit Pitch 2.43 μm
VCP: 125.0 nm (BL direction)

Stairless WLC (YMTC 276L)



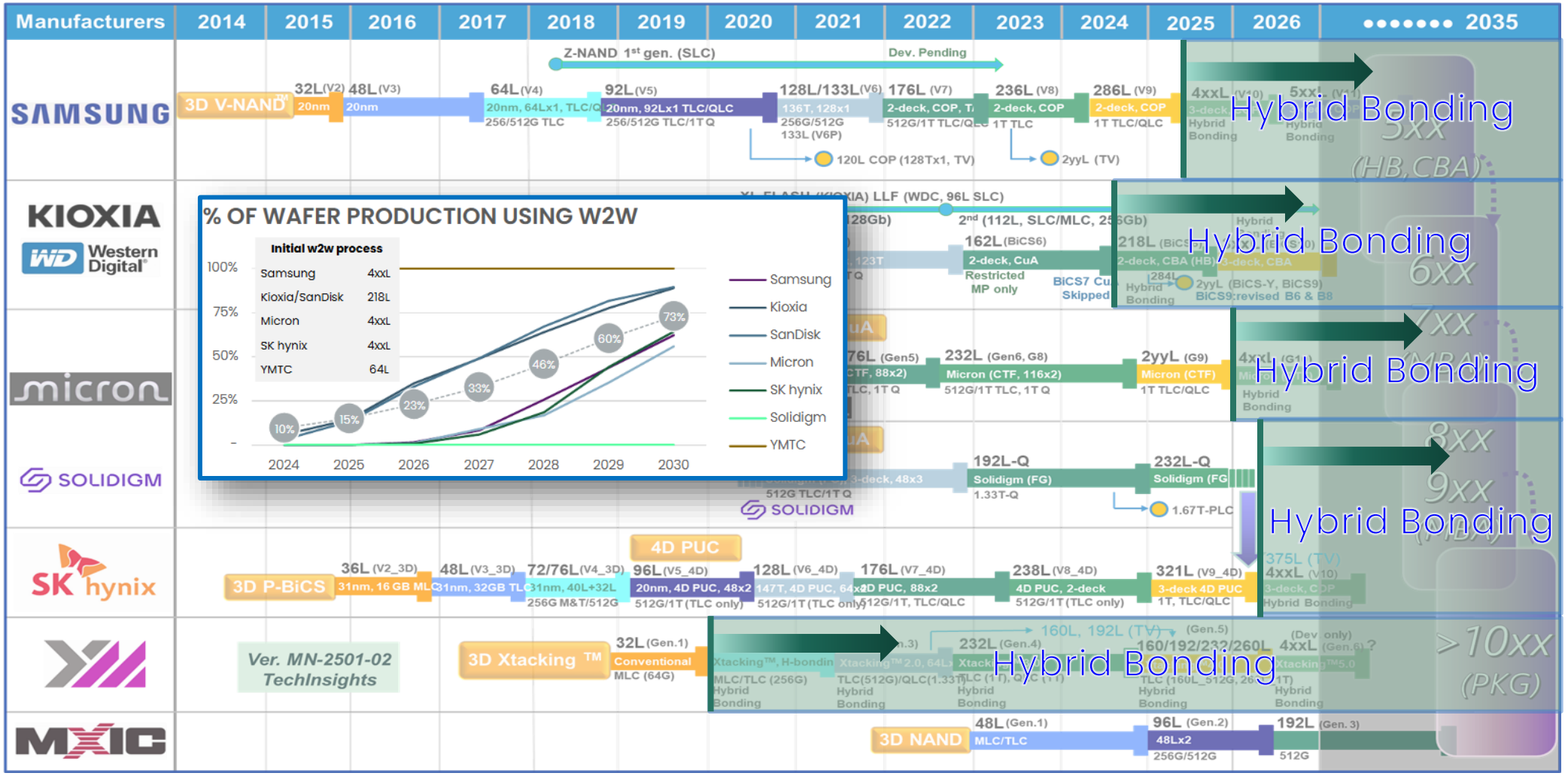


Conventional Staircase Structure



Stairless WLC Structure

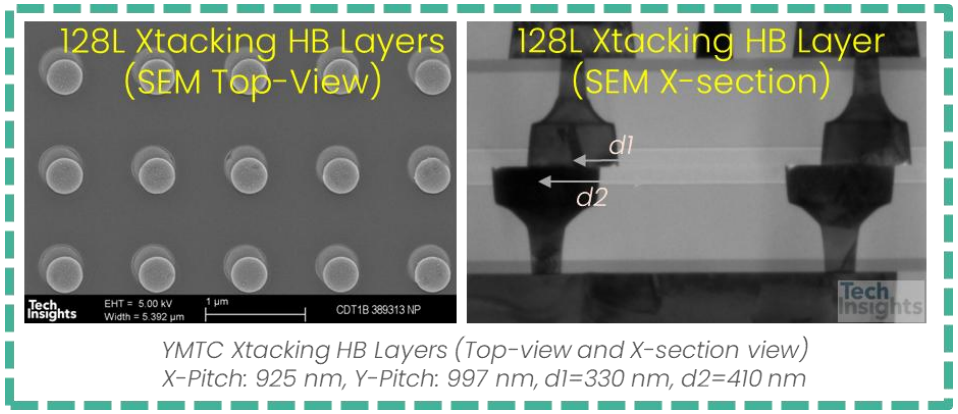
Hybrid Bonding Memory (NAND) Adoption



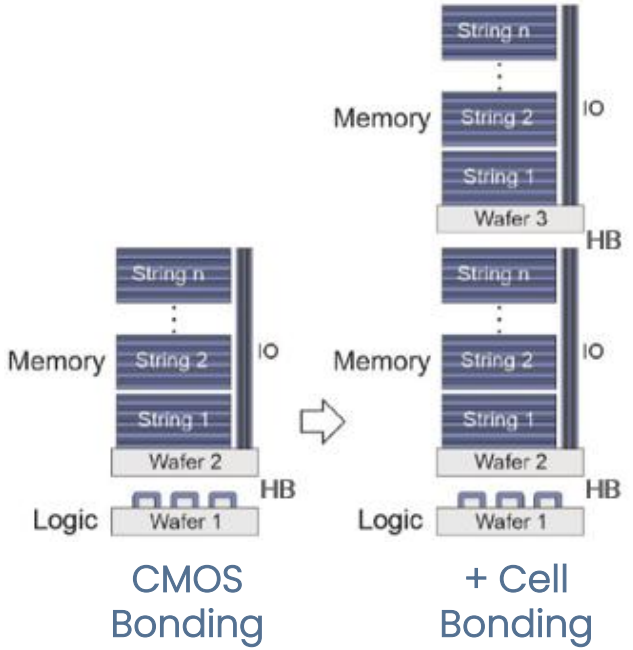
3D NAND Hybrid Bonding (HB) Application

- **3D NAND Array-to-Logic HB Chip with High Density and Higher Performance**

  - ✓ W2W format (YMTC Xtacking 1.0/2.0/3.0/4.0 HB 3D NAND Products, KIOXIA BiCS8 CBA 218L Products)
  - ✓ 3D NAND peripheral circuitry prepared on a wafer separately from a multi-stack processed array wafer
  - ✓ More solid logic transistors with well VT controlled, more flexible applications
  - ✓ Challenges: alignment, local uniformity, mechanical stress, topography/CMP dishing voids, cleanliness, Smaller pitches



YMTC Xtacking HB Layers (Top-view and X-section view)
X-Pitch: 925 nm, Y-Pitch: 997 nm, d1=330 nm, d2=410 nm



Tech Insights

www.techinsights.com