

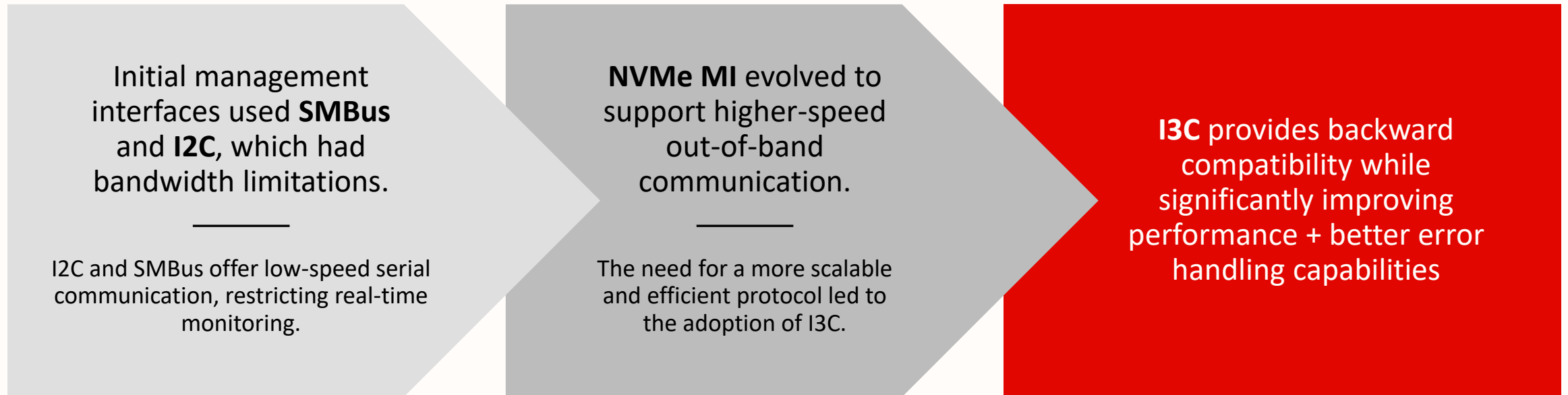


Efficient Management of NVMe SSDs using I3C

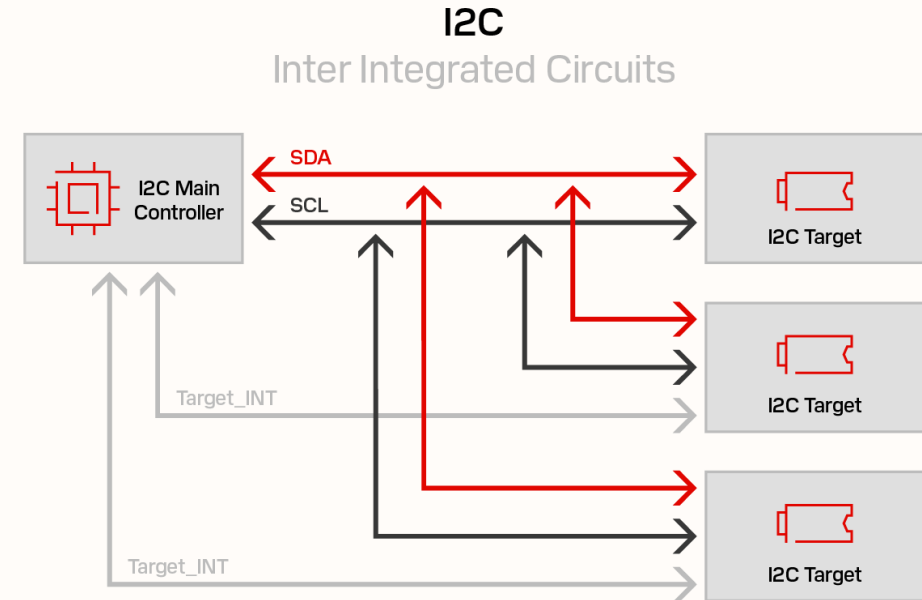
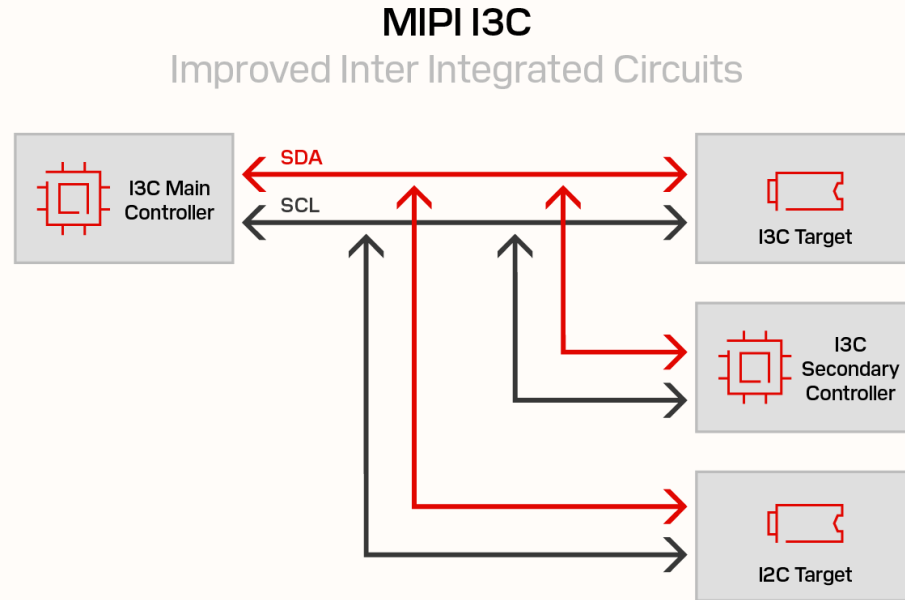
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Large Fleets of SSD's Pushed the Limits of I2C



What is I3C?



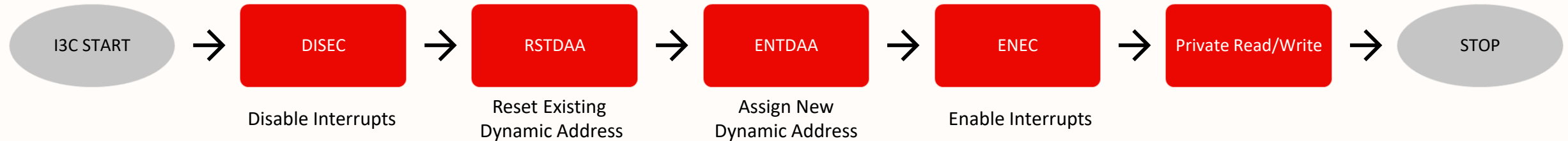
- I3C is a next-generation interface designed by MIPI Alliance for advanced communication.
- It improves upon I2C by offering lower power consumption and higher data rates.
- Supports dynamic addressing and multi-drop capability, reducing bus congestion.
- Allows for in-band interrupts, reducing pin count, polling overhead and improving efficiency.
- Provides robust error handling and enhanced security for critical applications.

I3C Communication

I3C communication flow

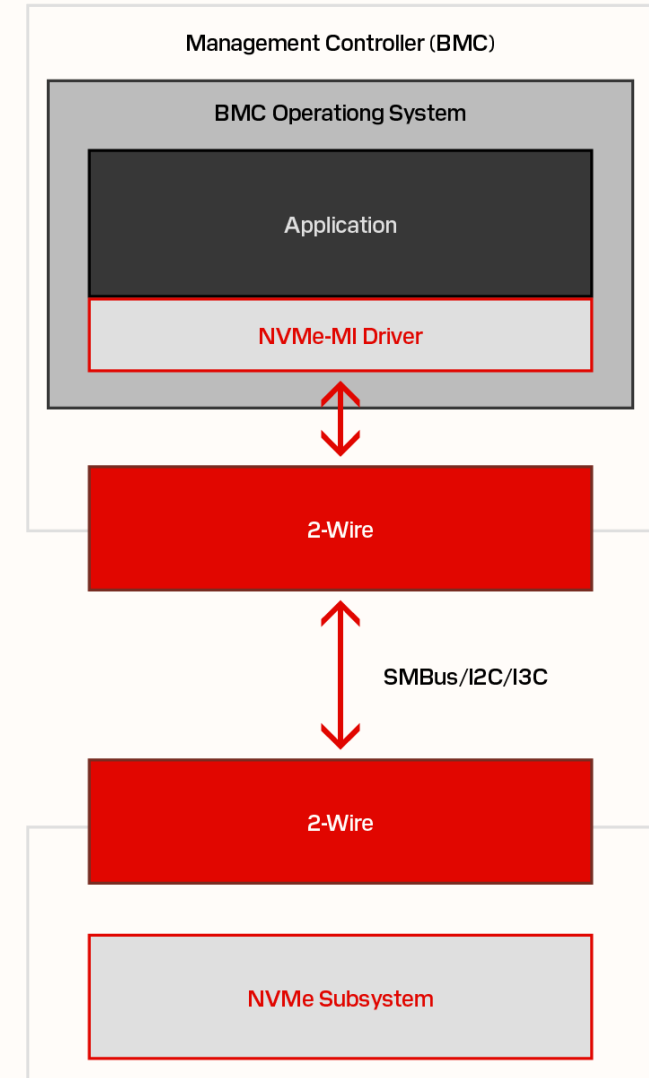


Detailed I3C communication flow

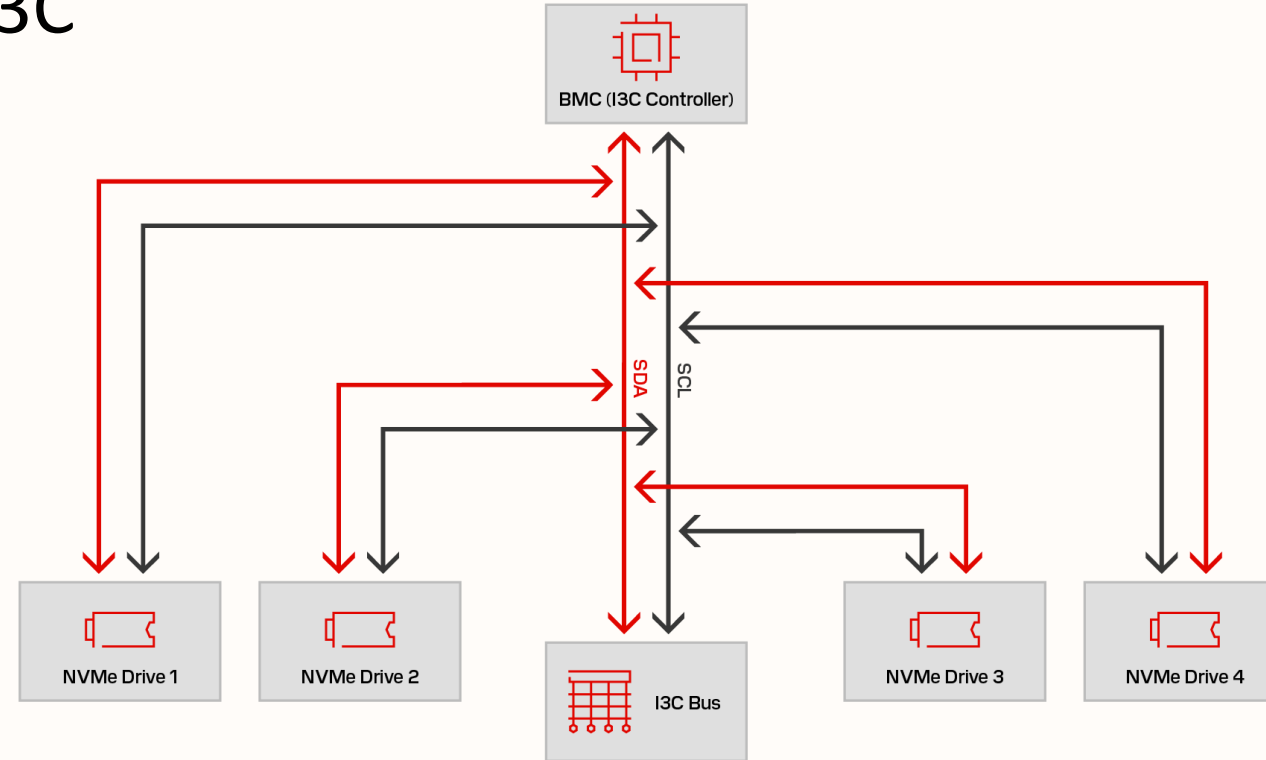


Introduction to NVMe MI

- NVMe Management Interface (MI) enables out-of-band communication for SSD monitoring and control.
- Helps manage SSD parameters like health, temperature, and firmware updates.
- Used in data centers and enterprise storage solutions for better SSD lifecycle management.
- Provides mechanisms for remote diagnostics and predictive maintenance.
- Supports firmware updates without impacting normal SSD operations.



NVMe MI over I3C



- NVMe MI over I3C leverages I3C's high-speed and multi-drop capabilities for SSD management.
- Reduces command latency, improving the responsiveness of SSD telemetry.
- Enables real-time health monitoring without impacting storage performance.
- Supports dynamic device discovery and hot-plug capability, optimized for high-density storage array configurations in data centers.
- Minimizes power consumption compared to traditional interfaces, increasing efficiency.
- Higher bandwidth also allows sideband security to be improved with larger keys for post-quantum cryptography and device logs to be read over I3C

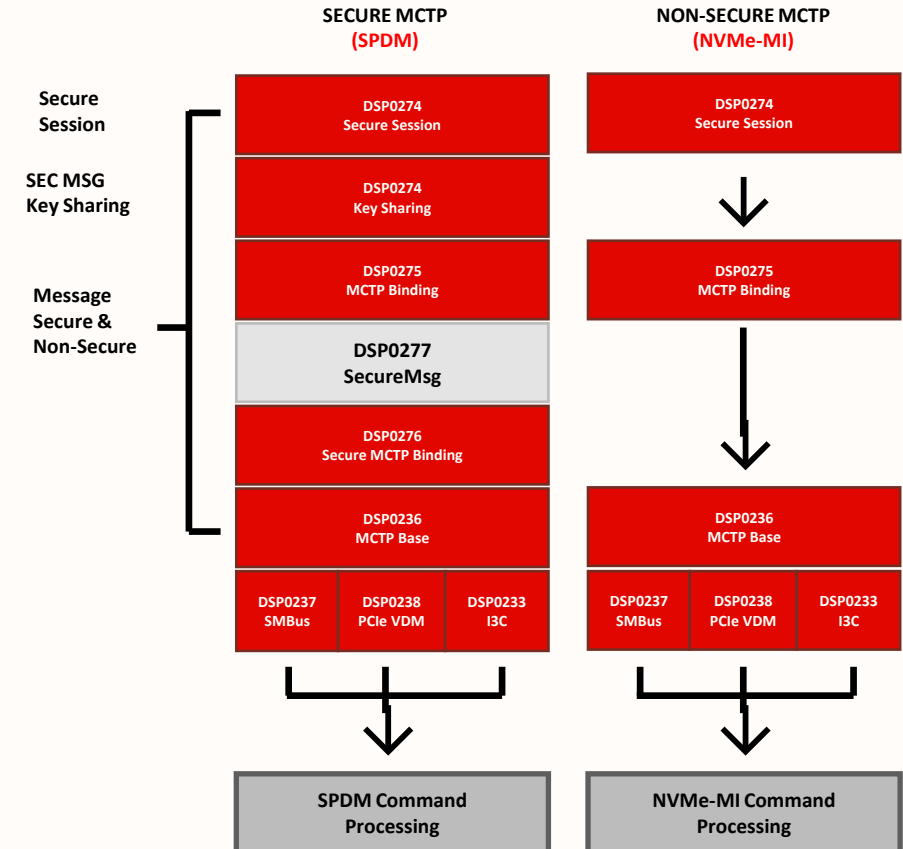
Comparison – NVMe MI over I2C vs. I3C

Feature	I2C	I3C
Bus Speed	100 kHz, 400 kHz, 1 mHz	Up to 12.5 mHz SDR, 25mHz HDR
Pull Up Resistors	External	Built in
Signaling	Open Drain	Push Pull & Open Drain
Voltage Range	Variable (1V8, 3V3, 5V) M.2 : 1V8 , EDSFF, U.2 : 3v3	1V2, 1V8, 3V3 M.2 , EDSFF, U.2 : 1V8
Addressing	Static 7 bit/10 bit Addresses are determined or selected by HW	Dynamic 7 bit Controller allocates address to each Target
Interrupts (IBI)	External	In Band
Hot Join	No	Yes
Active Controllers allowed	1+	1
Clock Stretching	Yes	No
Common Command Codes (CCC)	No	Yes
High Data Rate (HDR) Modes	No	Optional
IO Pads	I2C special pads – 50ns Spike Filter	Standard Pads. No Spike Filter. 4MA Drive



NVMe MI over I3C – Architecture Overview

- Architecture involves an I3C controller (host) communicating with multiple SSDs as I3C targets.
- Key management applications such as NVMe MI or SPDM (Security Protocol and Data Model) run over MCTP, which abstracts the different sideband transports
- Each MCTP binding is unique for the various sideband interfaces (SMBus, I3C, PCIe VDM)
- SSD firmware implements MCTP for I3C and interprets MCTP message payloads and processes MI or SPDM commands accordingly.



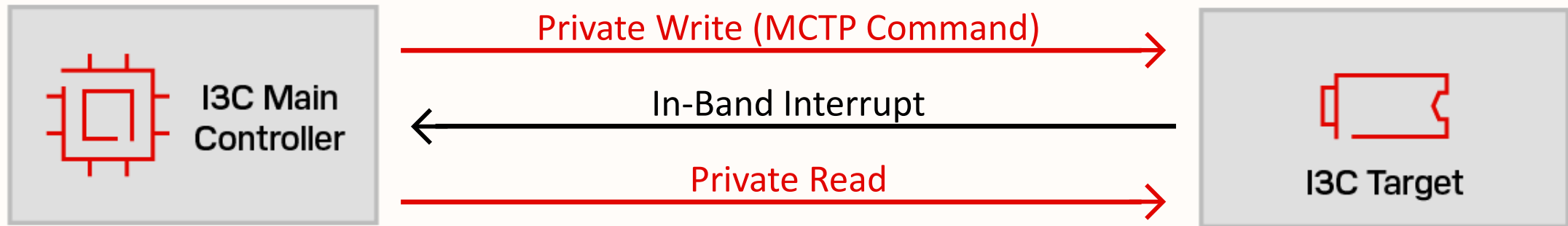


MCTP (Management Component Transport Protocol)

MCTP is a transport protocol designed for platform management communications

Provides message-based transport with packet integrity and sequencing

Uses in-band messaging to exchange data



Major Difference from I2C: No switching of roles between Controller and Target, when target has the requested packet, it sends out an IBI

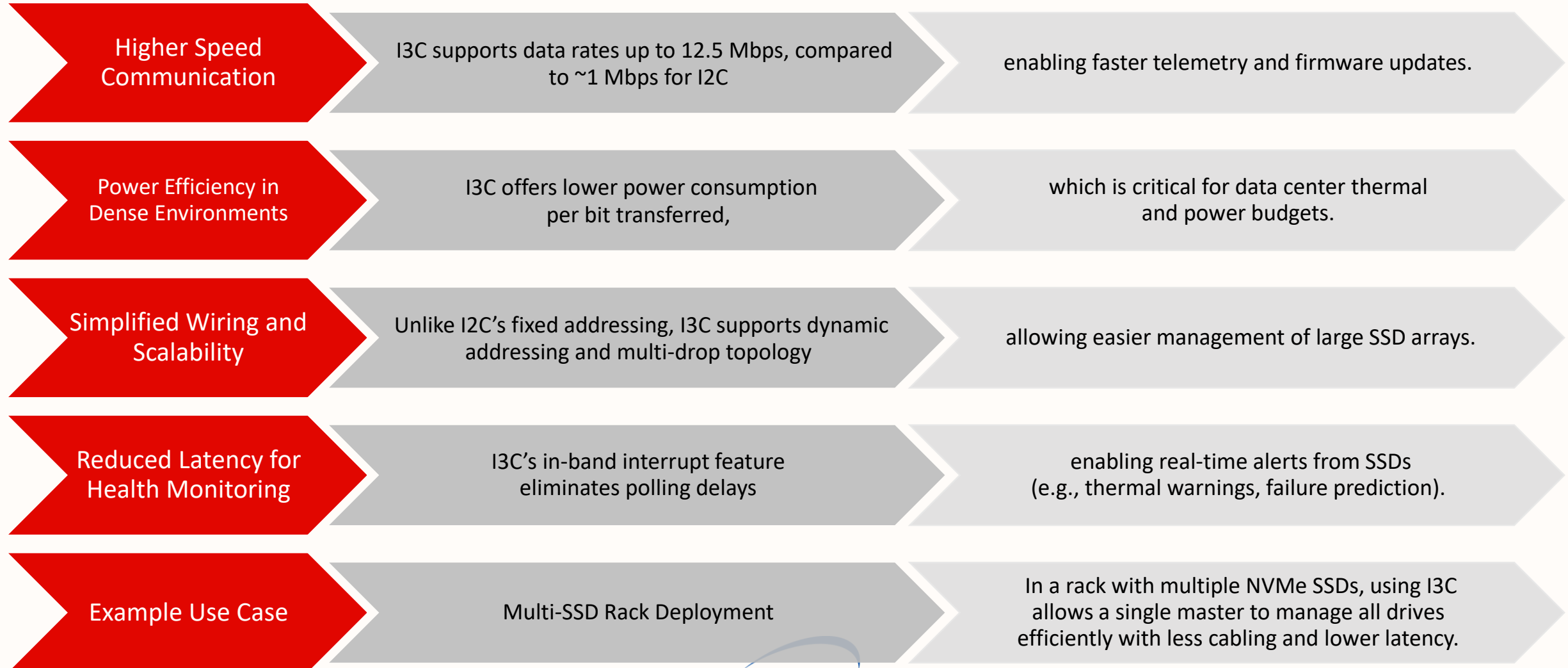


Implementation in SSDs

- SSD firmware must support NVMe MI and SPDM commands over MCTP/I3C for compatibility.
- Host systems require an I3C master controller for communication.
- The controller must integrate a dedicated I3C IP core within the ASIC to enable protocol-level support.
- Requires modifications in SSD firmware to handle I3C-specific MCTP messaging.
- I3C interface is integrated alongside the primary data path to allow non-intrusive out-of-band monitoring.
- Implementation of NVMe MI commands for efficient management in enterprise storage solutions.



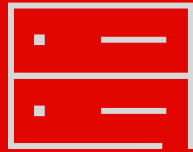
Real-World Examples – Why Shift to I3C?



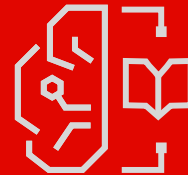


Industry Adoption & Applications

- NVMe specifications now include support for MI over I3C.
- Companies are investing in this technology.
- Adoption expected to grow in hyperscale data centers and cloud storage.
- Ongoing efforts to standardize I3C for broader storage applications.
- Future SSD firmware updates will further enhance MI capabilities.



Data Centers: Optimizing SSD management and remote diagnostics



AI/ML workloads: Real-time monitoring of storage performance.



High-performance computing: Managing large-scale SSD deployments



Challenges and Limitations

- Legacy systems still rely on I2C/SMBus, requiring gradual migration.
- Firmware and hardware updates needed for widespread adoption.
- Potential compatibility issues with older SSDs.
- Industry-wide standardization and interoperability need further development.
- Cost considerations in upgrading infrastructure to support I3C.

Takeaways

For Firmware Engineers

Reduced firmware complexity with faster command execution and improved error handling mechanisms.

For System Architects

Easier integration into high-density storage designs with fewer limitations than legacy SMBus or I2C.

For Data Center Operators

Enables real-time telemetry access for predictive maintenance and proactive SSD replacement, reducing downtime.

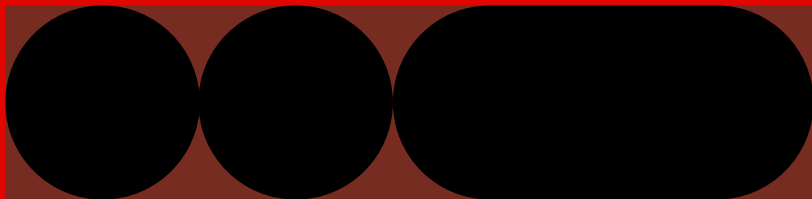
For Embedded Developers

A familiar protocol (backward compatible with I2C) but with modern features that streamline SSD integration.

Conclusion

I3C isn't just an upgrade it's an enabler for smarter, faster, and more efficient SSD management at scale.

“START” “REPEAT” “1988/2025”



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