Composable Infrastructure Leverages CXL for Memory Sharing and Benchmark Results

Brian Pan
H3 Platform

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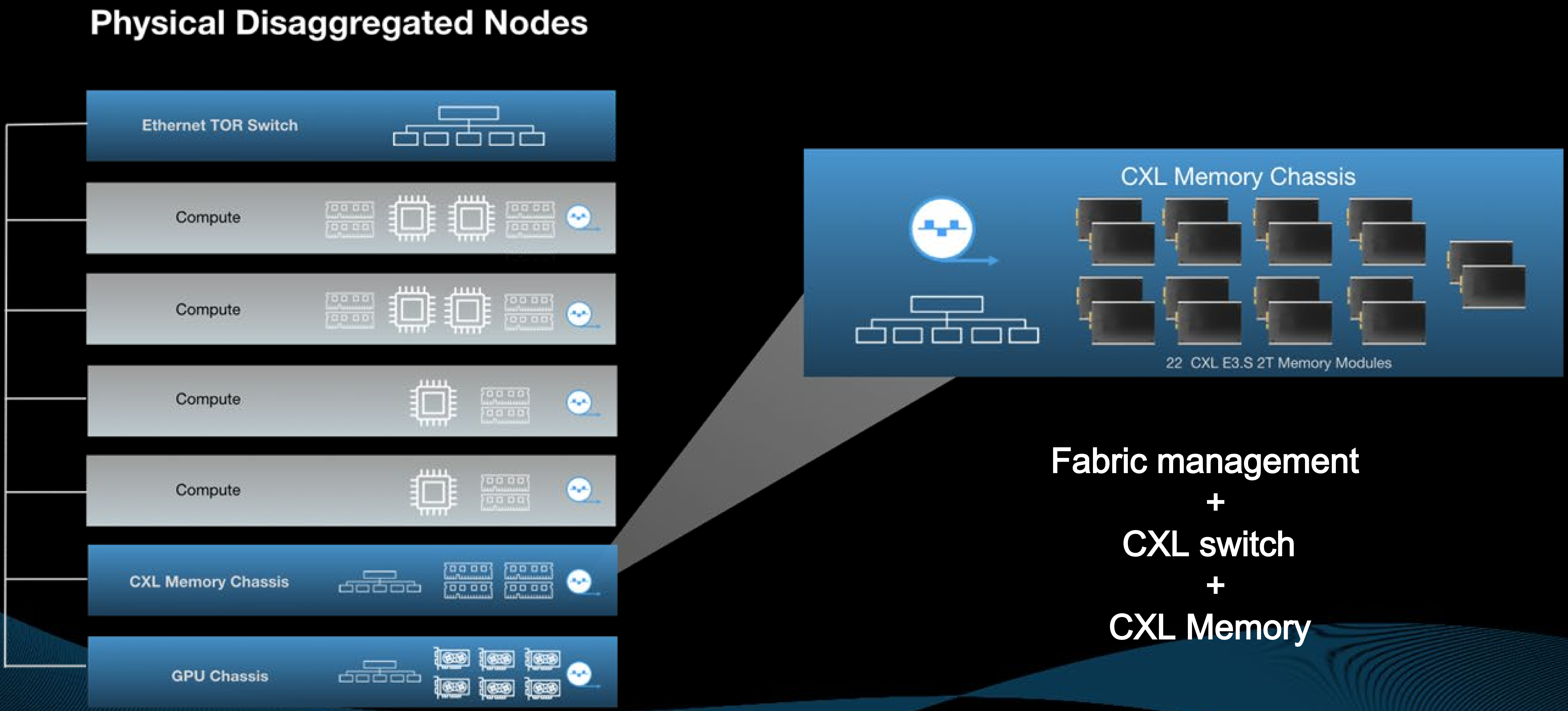
Composable CXL Infrastructure



Fabric management
+
CXL switch
+
CXL Memory

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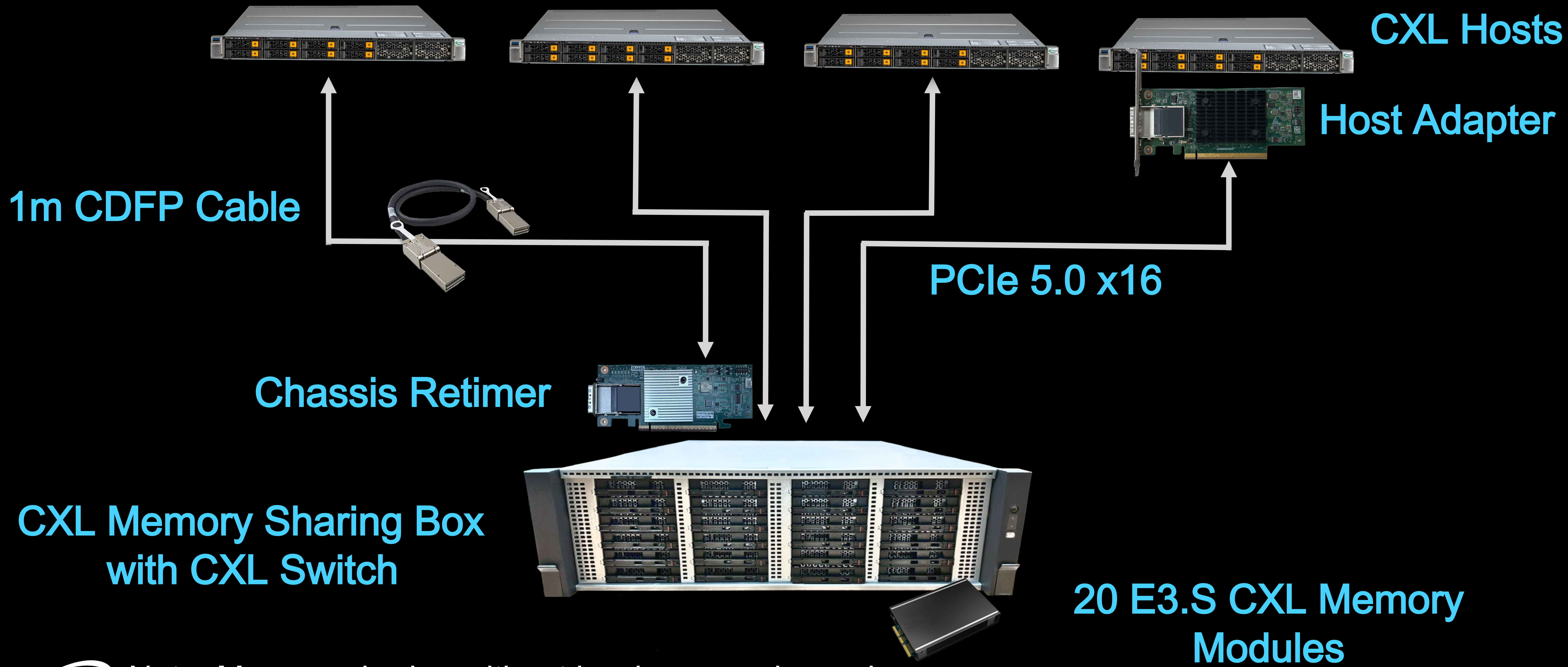
The Solution Enables Memory Sharing up to 5TB



Note: Memory sharing without hardware cache -coherence

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Cluster Configuration

Systems	Configurations
Servers	• Four Intel GNR servers with 512GB DDR5 • One root port is connected to the CXL memory
CXL Memory Appliance	• 4 host -ports are connected to 4 different servers • 5T CXL shared memory (256GB*20)

Configuration Consideration

1. The servers should have exact the same local DDR to avoid confusion.
2. The CXL memory modules are assigned in sequence.

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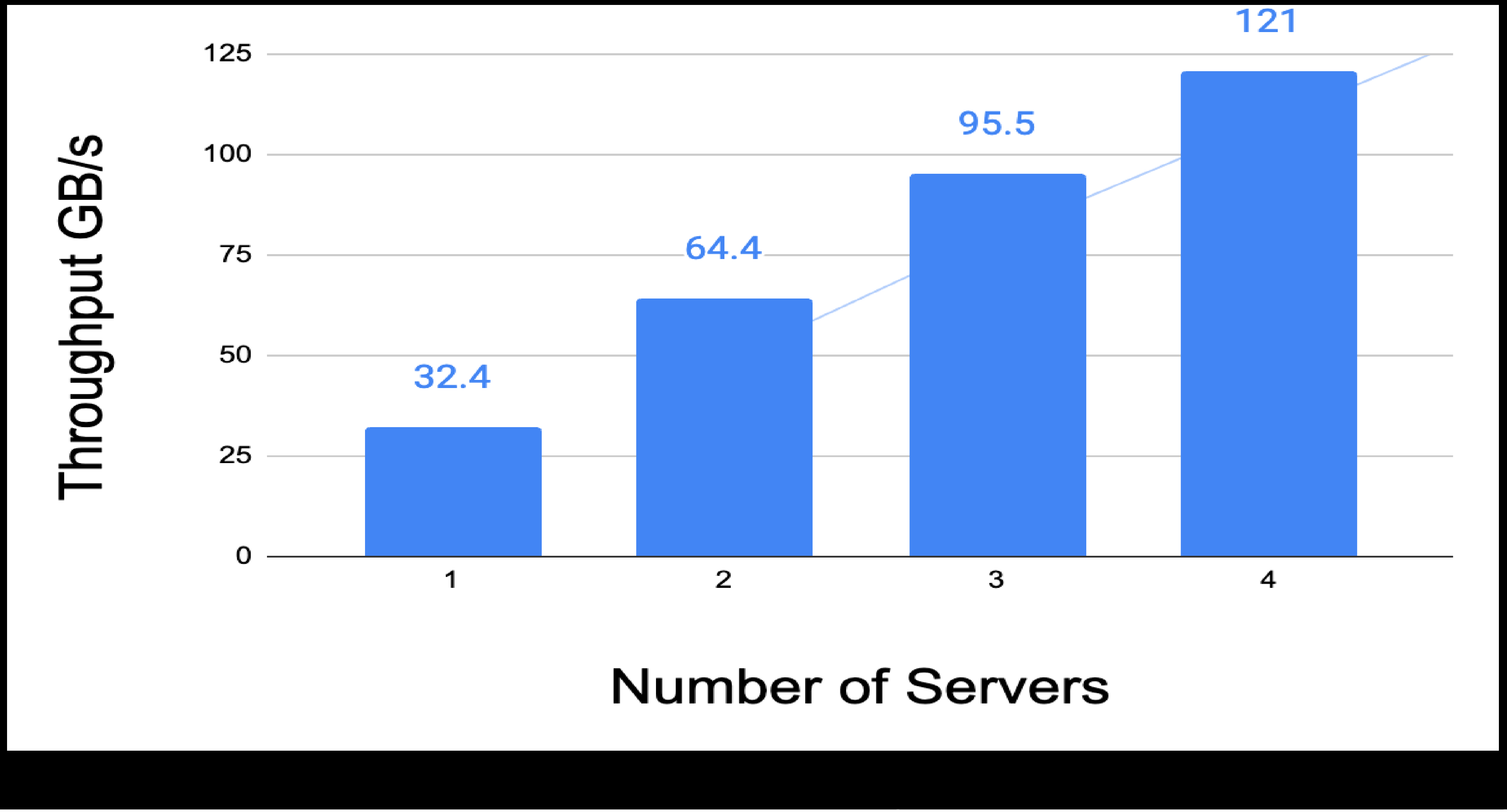
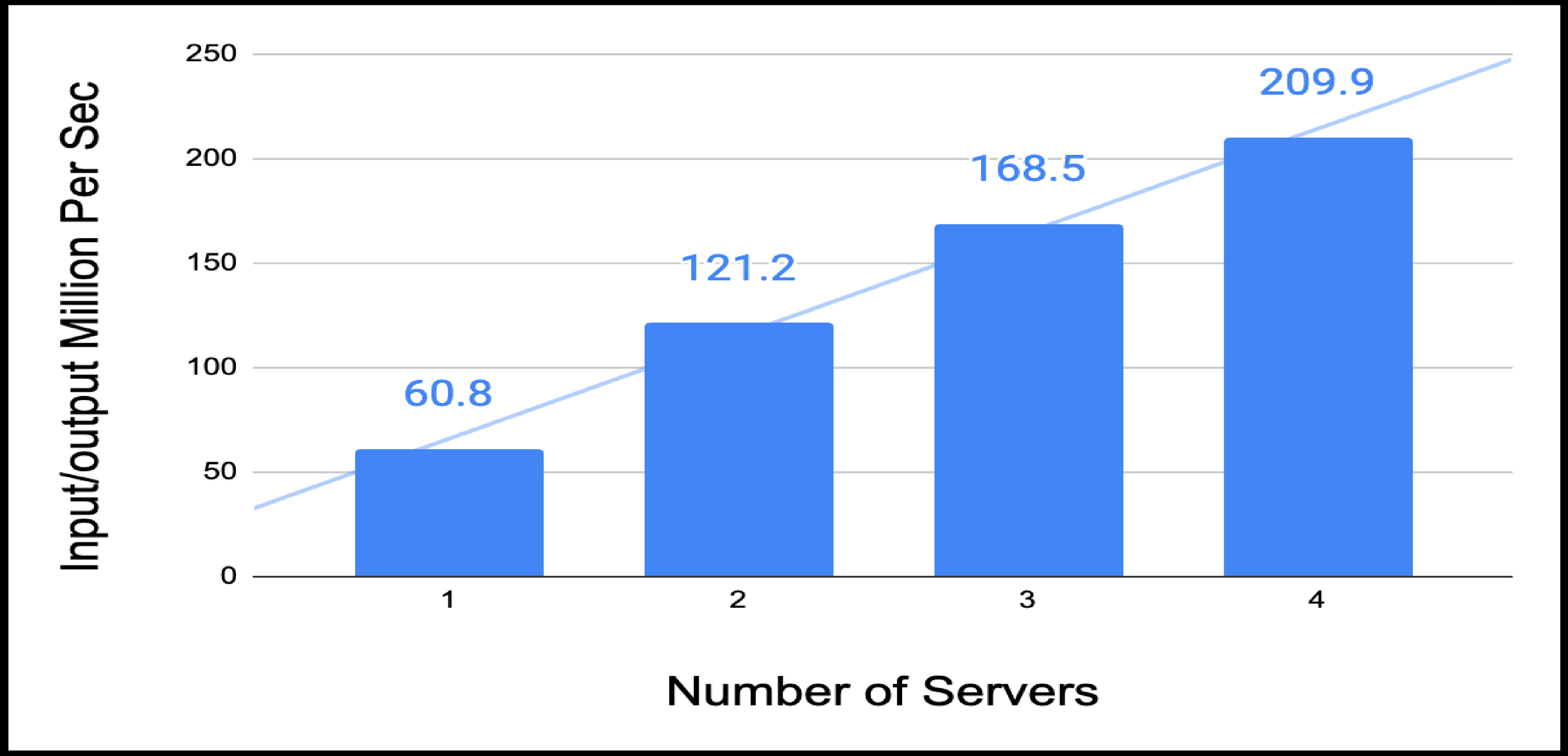
Maximum Bandwidth 121GB/s and IOPS 210M





Random Read	Server 1	Server 2	Server 3	Server 4
Server DDR5#	Intel EMR 32GB x2	Intel GNR 64GB x1	Intel GNR 64GB x1	Intel EMR 16GB x4
4 servers throughput	BW=**32.4GiB/s**	BW=31.1GiB/s	BW=32GiB/s	BW=**25.5GiB/s**
4 servers Input/Output	IOPS=**60.8M**	IOPS=60.4M,	IOPS=47.3M	IOPS=**41.4M**
Poolmap	4x E3.S 256G	4x E3.S 256G	4x E3.S 256G	4x E3.S 256G

FMS *the* Future *of* Memory *and* Storage

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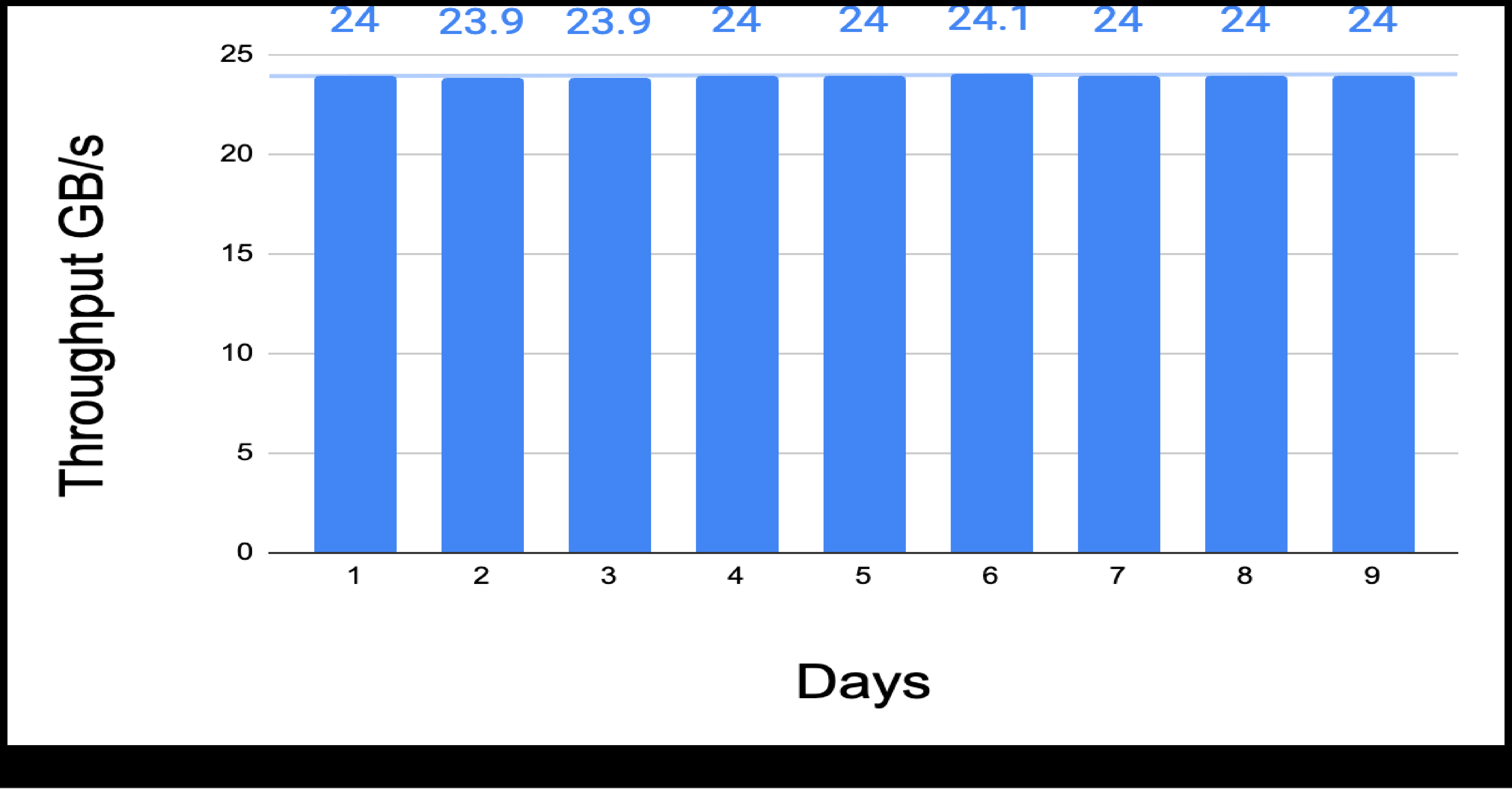
Max perf of One CXL Sharing Memory and One Root Port



1. 4 servers share ONE 256GB CXL memory
2. The throughput is 24GB/s for 9 days
3. Each CPU is with 128 CPU cores and each core gets 2GB memory (total 256GB)
4. Continuous stress to the single CXL memory for 9 days

MLC	Server 1
Server	Intel GNR with 64GB
All Read	BW=**43.3**GiB/s
1:1 Read-writes	BW=**62.1**GiB/s
Poolmap	**20x E3.S 256G(5TB CXL memory)**

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Implementation Challenges

Items	Description
Server Platform	• Intel CXL memory address starts from 2GB • AMD reser 12GB in 1T space
Server BIOS	• CXL enabled settings • CXL memory address configuration
Re-timer	• Common/ SRIS clock setting
CXL Driver	• OS kernel dependency

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Implementation Challenges

Items	Description
Linux kernel	• DAX and NUMA memory in Kernel 6.2 • CXL memory in Kernel 6.3 and beyond
Memory Error Handling	• Error handling and behavior of CXL switch • CXL memory controller capability

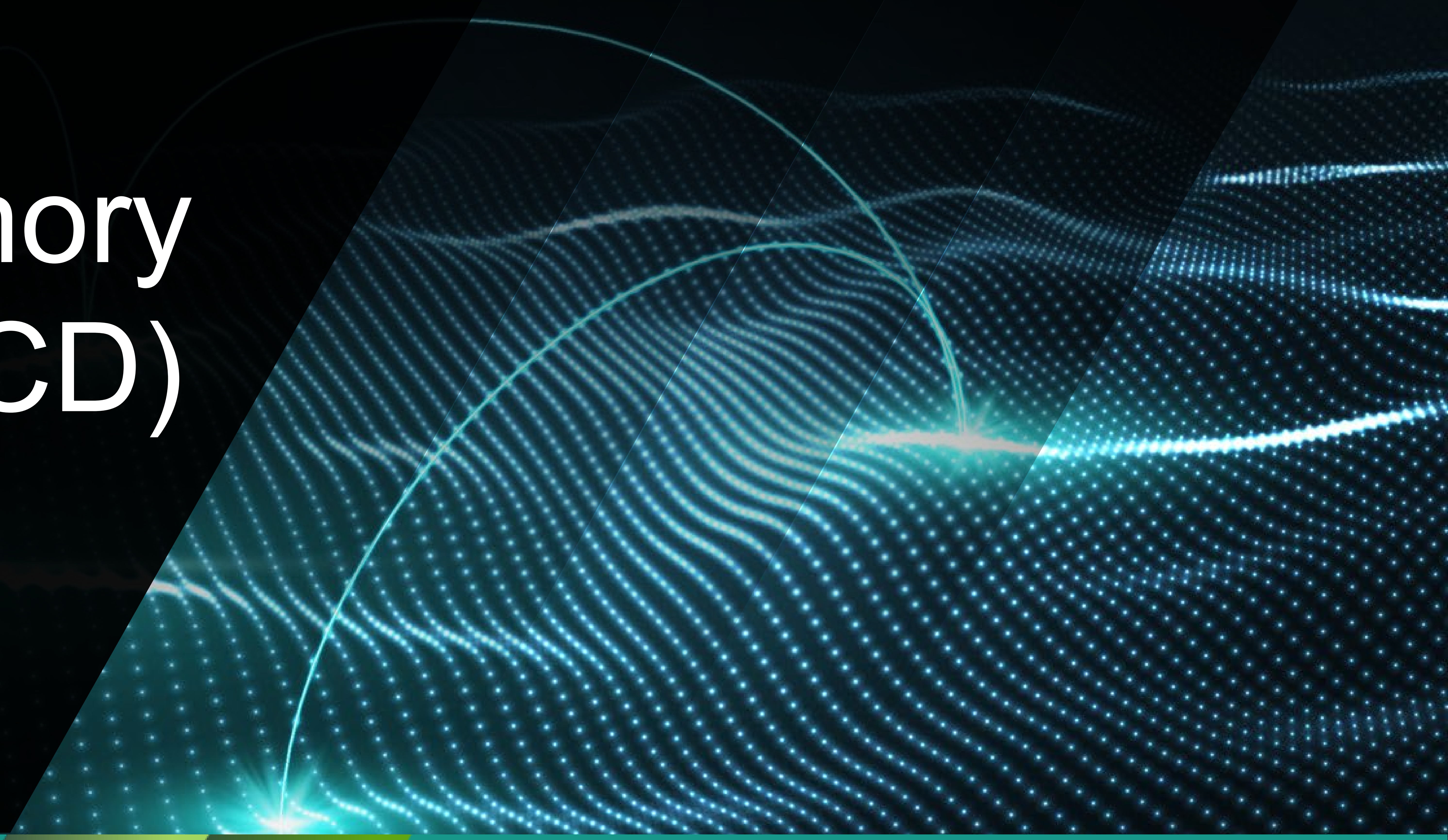
Call to Actions - Usage, Ecosystem, Partners

Usage Cases from users	Deploy the suitable usage cases such as in-memory database, big data processing, HPC, AI, and so on.
Ecosystem colloboration	Seamless integrate across multiple layers including CPU, BIOS, CXL drivers, OS, CXL memory modules work together to deploy the CXL solutions in real usage cases
Software partners	Build the robustic management in the existing IT systems including the memory discovery, orchestration, monitoring and analytics, trouble-shooting

Supporting Dynamic Memory Allocation (DCD)

Joseph Slember

XConn Technologies



CXL Dynamic Memory Allocation

What is Dynamic Memory Allocation?

- Ability to change how much CXL Memory is presented to a server dynamically
  - Host kernel will be able to determine changes made to the memory presented without crashing
  - Utilizes Dynamic Capacity Disk code in modified kernel
    - CXL 3.1 Feature that can be used now
- Uses XConn Technologies Switch to export CXL Memory to a host via 2.0 Endpoint
- The Switch is able to change how much memory and from which CXL cards is presented to the host

CXL Dynamic Memory Allocation

What are the benefits of CXL Dynamic Memory Allocation?

- Multiple hosts can connect to the XConn CXL Switch..
- Ability to change how much CXL memory is presented to hosts on the fly as application needs change
- Ability to present different sources of CXL memory to hosts on the fly
- Enablement of MLD functionality
- Enablement of Memory Sharing and Memory Pooling without host crashing
- CXL Memory can be presented as NUMA memory or as a DAX Device

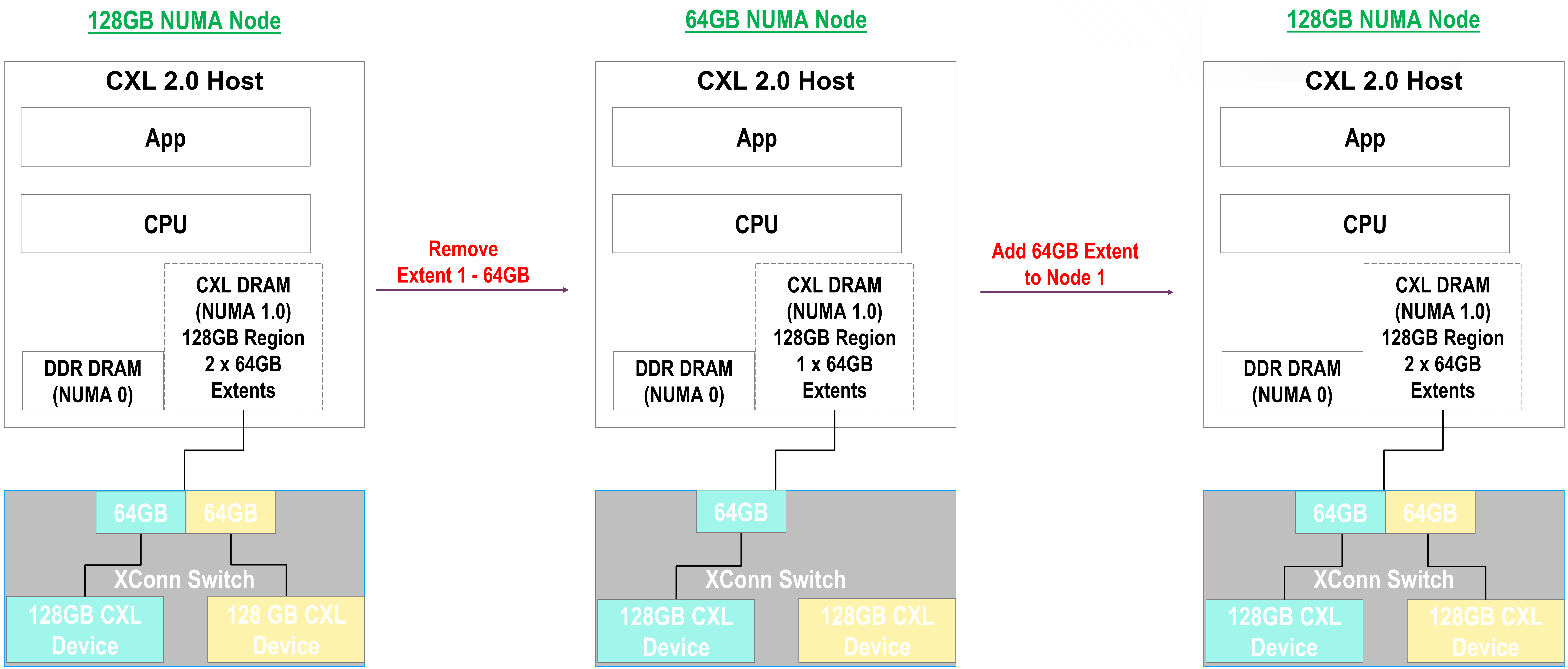
CXL Dynamic Memory Allocation

What are the benefits of Dynamic Memory Allocation?

- Dramatically increase efficiency
- Increase application performance
- Optimize Data Center costs
- Reduce Software Stack Complexity

- Disaggregation of Memory and Accelerators:
- Memory Tiering
- Scalability
- Reduced Latency

CXL Dynamic Memory Allocation Demo



128GB NUMA Node

CXL 2.0 Host

App

CPU

DDR DRAM (NUMA 0)

CXL DRAM (NUMA 1.0) 128GB Region 2 x 64GB Extents

64GB 64GB

XConn Switch

128GB CXL Device

128 GB CXL Device

Remove Extent 1 - 64GB

64GB NUMA Node

CXL 2.0 Host

App

CPU

DDR DRAM (NUMA 0)

CXL DRAM (NUMA 1.0) 128GB Region 1 x 64GB Extents

64GB

XConn Switch

128GB CXL Device

128GB CXL Device

Add 64GB Extent to Node 1

128GB NUMA Node

CXL 2.0 Host

App

CPU

DDR DRAM (NUMA 0)

CXL DRAM (NUMA 1.0) 128GB Region 2 x 64GB Extents

64GB 64GB

XConn Switch

128GB CXL Device

128GB CXL Device

CXL Dynamic Memory Allocation Demo