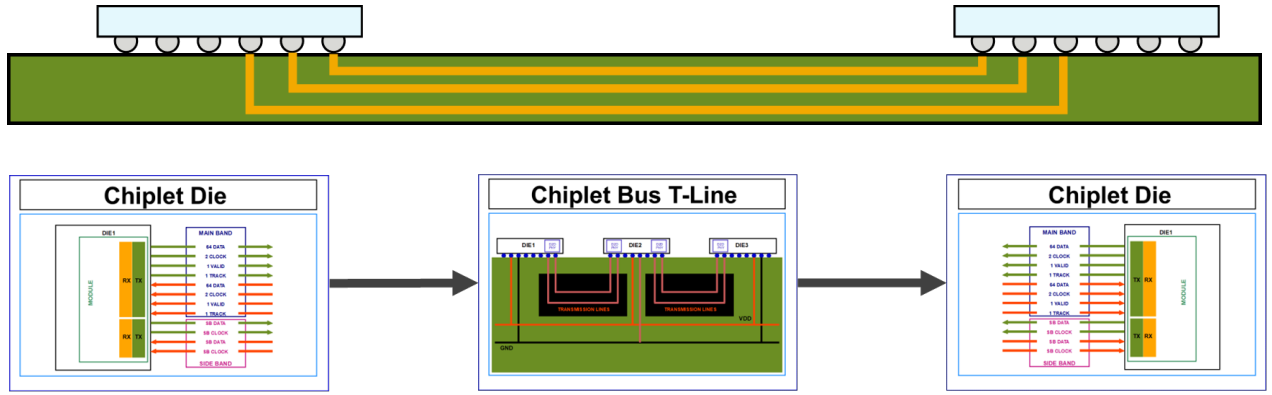
KEYSIGHT FMS

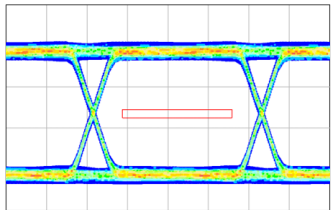
Your Chiplet Design Is Failing the UCIe Spec - Here's Why

Presented by Tim Wang Lee, Ph.D.

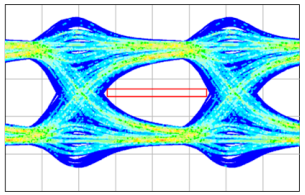
Navigate the EDA Complexities with a Case Study

- Why is the industry shifting to the chiplet design philosophy
- Navigate Electronic Design Automation (EDA) in chiplet designs
- EDA case study on solving chiplet signal integrity issues





Signal Integrity Insights on
- Crosstalk
- Frequency-dependent loss

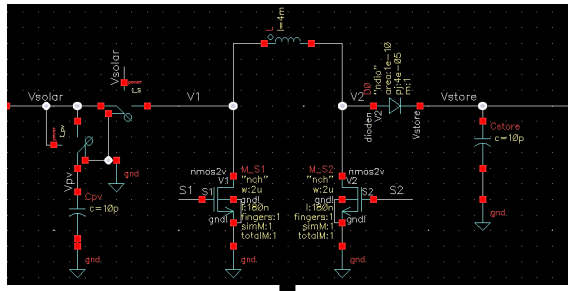


UCIe™ Universal Chiplet Interconnect Express

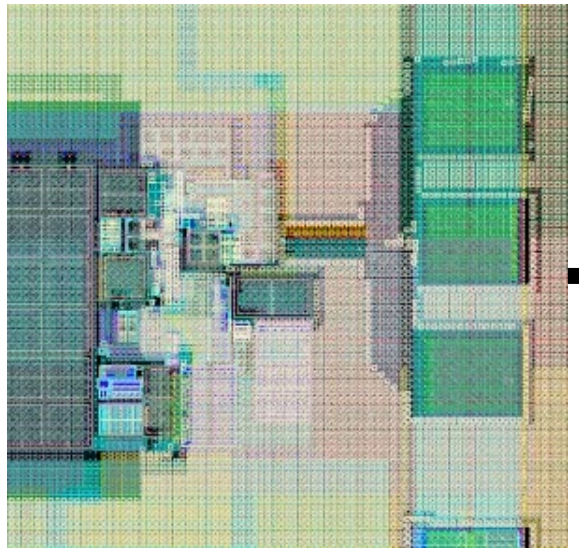
Electrical layer specifications
- Eye mask
- VTF loss
- VTF crosstalk

IC Design from the Schematic, Wafer to the Package

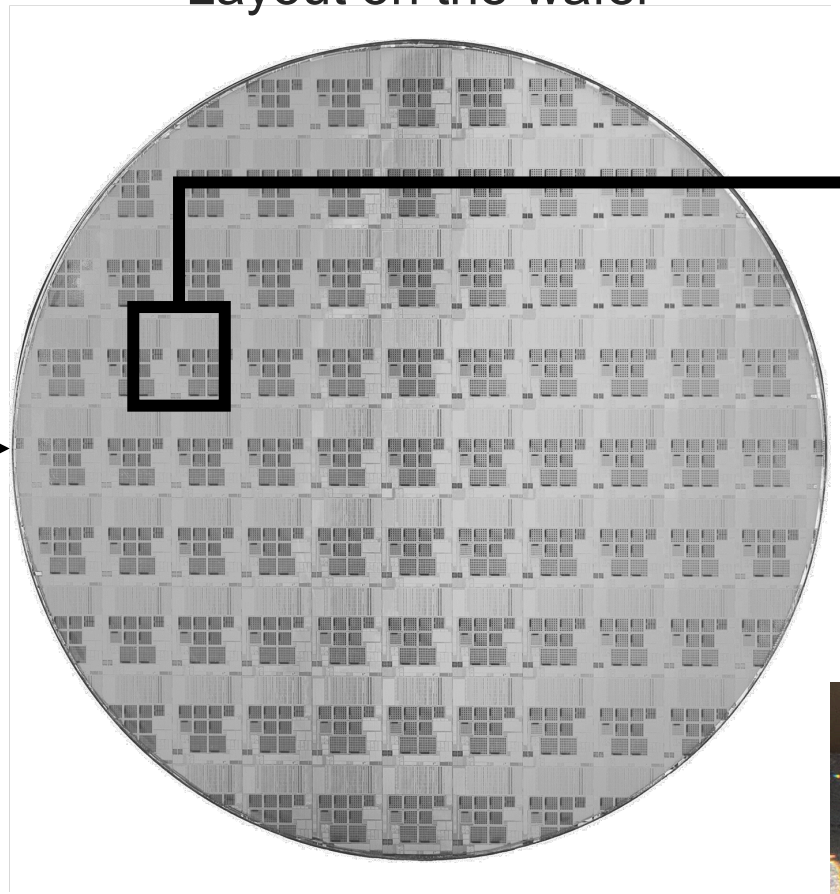
Schematic



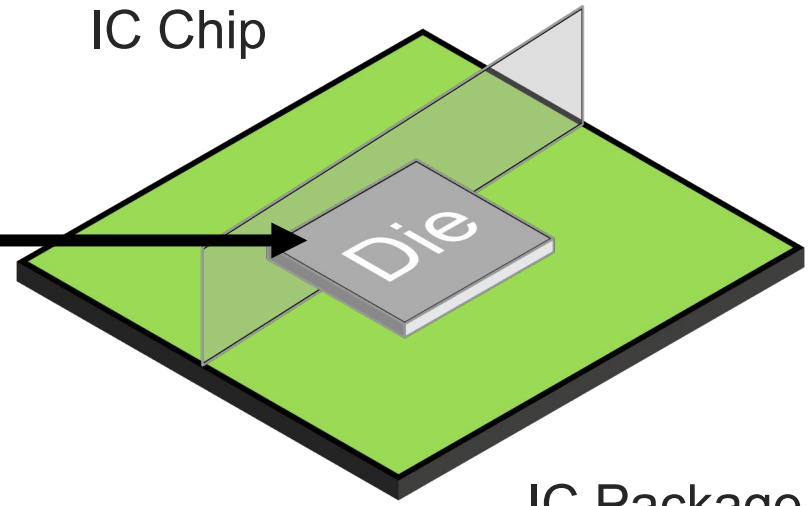
Layout



Layout on the wafer

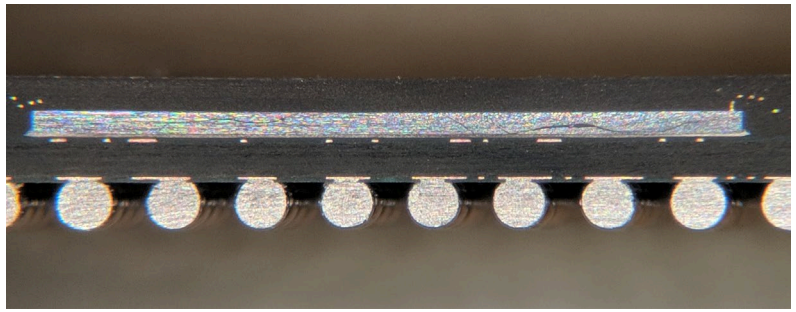


IC Chip



IC Package

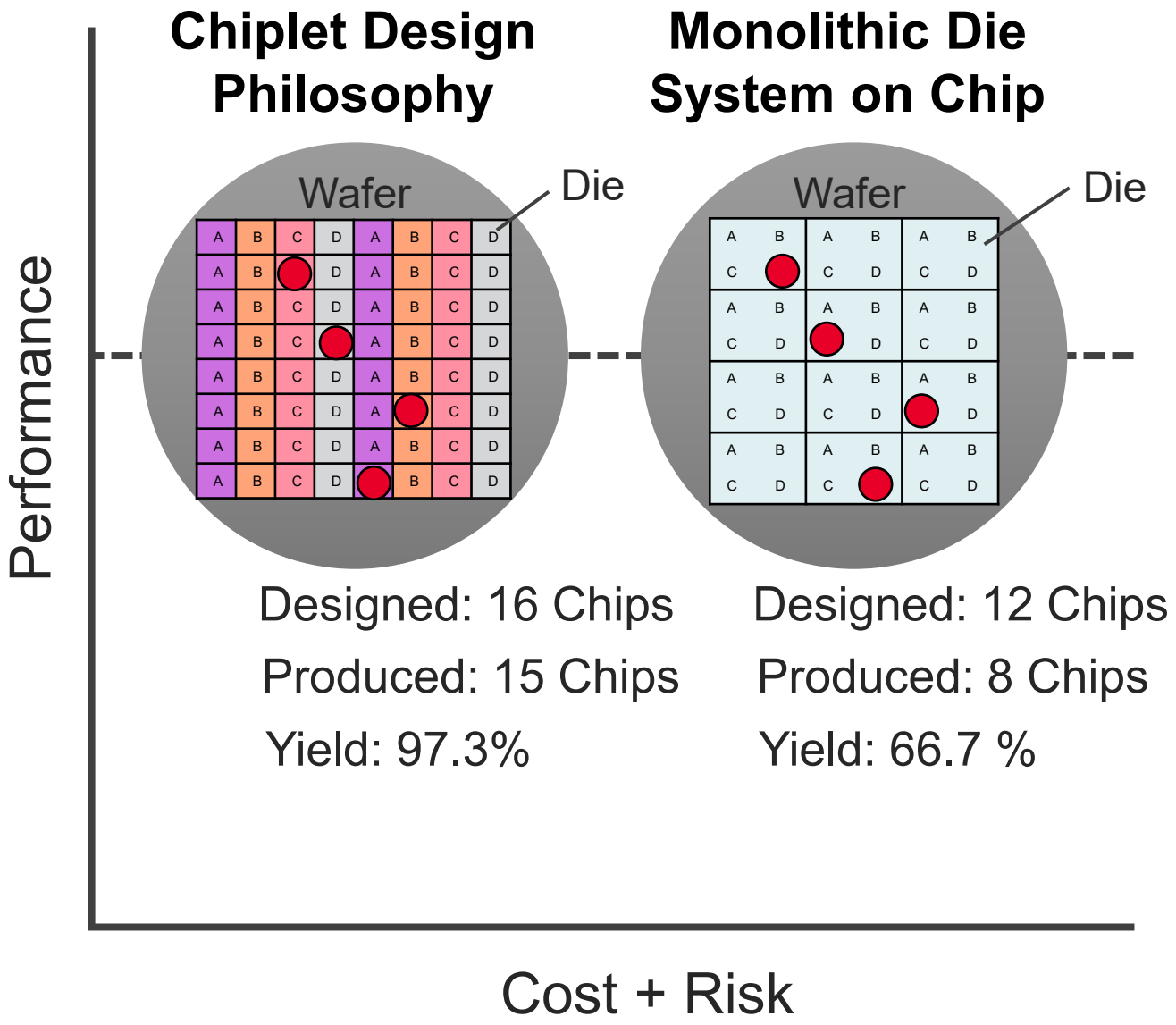
Cross-sectional view



Picture credit: https://miscircuitos.com/design-process-of-chips-asics-flow-from-design-to-tapeout/

Picture credit: https://twitter.com/TubeTimeUS/status/1113567854698225664

Chiplets Improve the Cost vs. Performance of Chip Production



Monolithic approach

4 different functions in one big die

Fn: A (CPU)	Fn: B (Memory)
Fn: C (I/O)	Fn: D (Power)

Chiplet approach

4 different dies for 4 different functions

Die: A	Die: B
Die: C	Die: D

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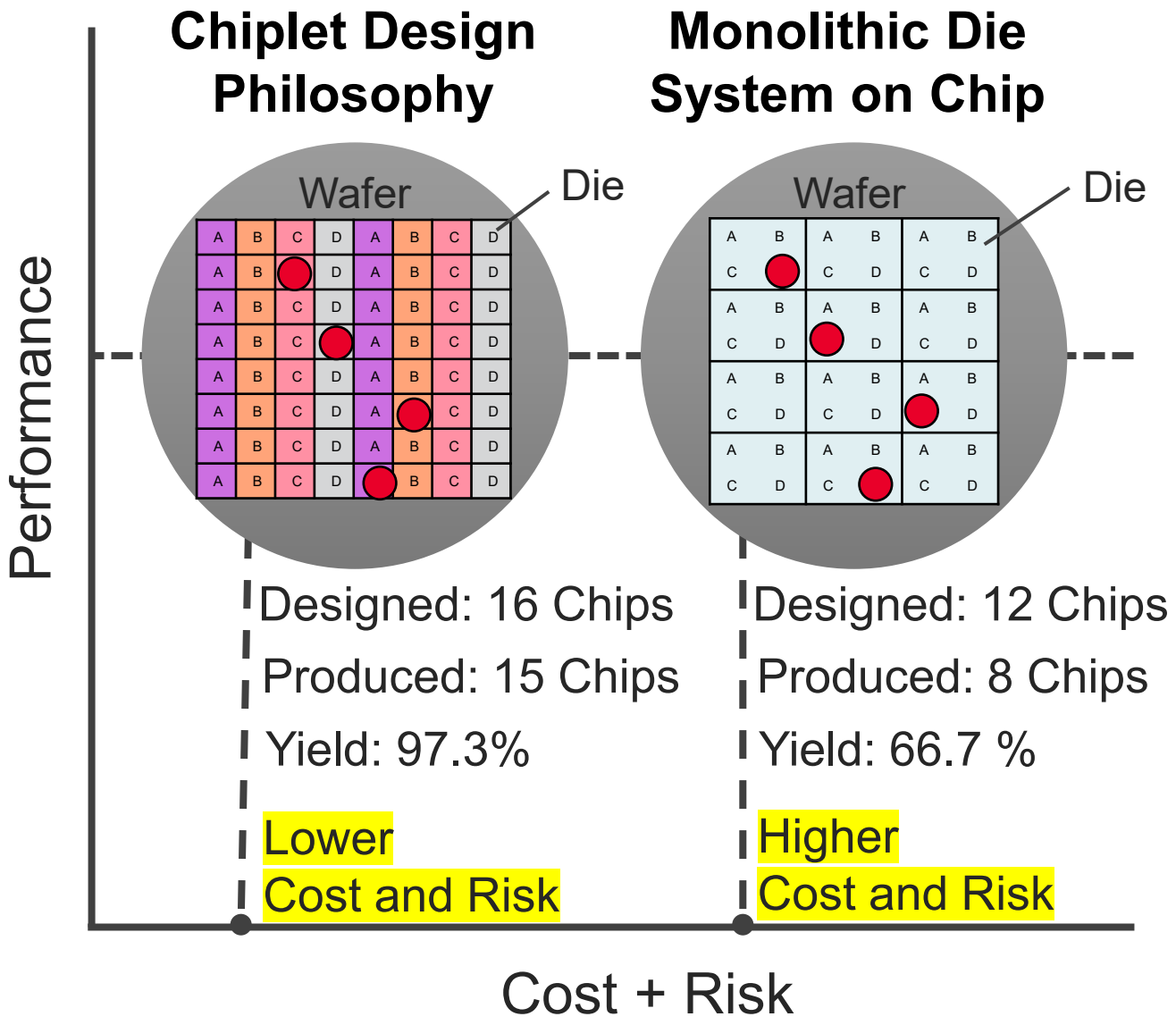
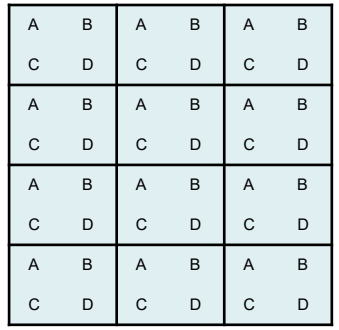
Chiplets Improve the Cost vs. Performance of Chip Production





Monolithic Die SoC

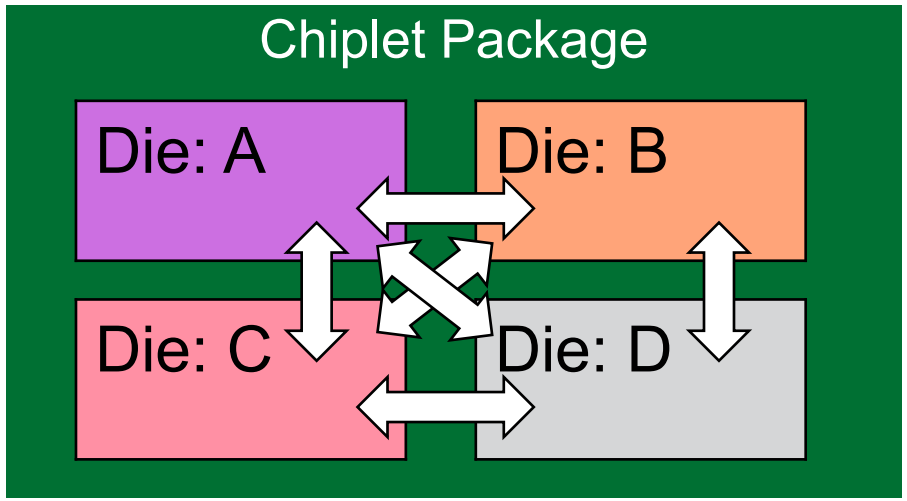
- Requires large mask (reticle) close to fabrication limit
- Has a lower yield
- Higher cost

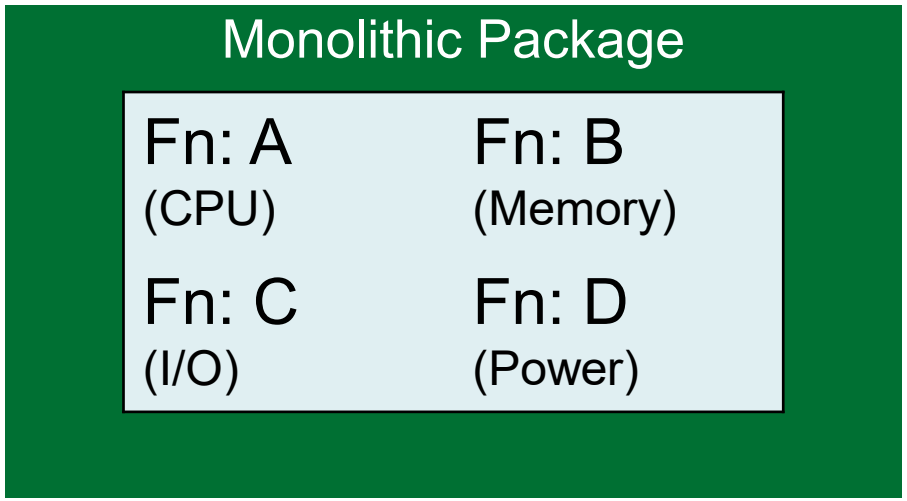
Chiplet Design Philosophy

- Maximizes wafer usage
- Has a higher yield
- Has a lower cost
- Easy to scale!

The chiplet approach reduces cost, risk and improves the scaling ability.

The Catch: Die-to-Die Communication is Important for Chiplets





UCIe™
Universal Chiplet Interconnect Express

Various standards for the die-to-die interface between chiplets

- **UCIe (Universal Chiplet Interconnect express) [2]**
- BoW (Bunch of Wires)
- AIB (Advanced Interface Bus)

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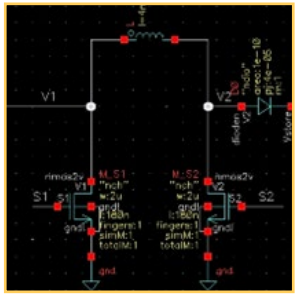
You Need EDA to Save Time and Money

EDA Software and Their Focuses in Chiplet Designs

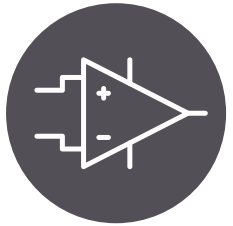
Goal of EDA: Predict and confirm the design's functionality and performance before physical fabrication.

Schematic



Circuit level simulation

- Individual circuit blocks
- Optimize and validate

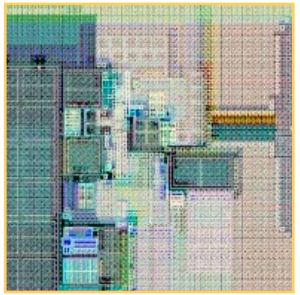


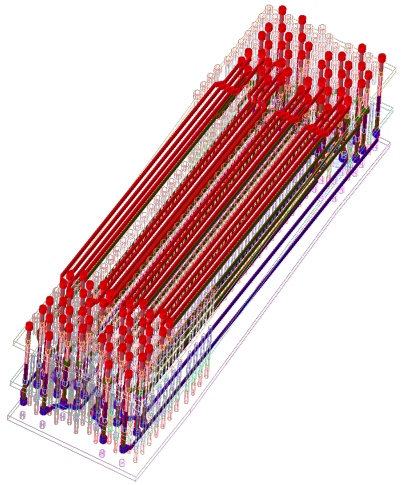
System level simulation

- Behavior between subsystems
- Analyze the signal, and power integrity

Layout vs Schematic (LVS) Verification

Layout





Post-Layout Circuit Simulations

- Signal Integrity (SI)
- Power Integrity (PI)
- Electromagnetic Interference (EMI)

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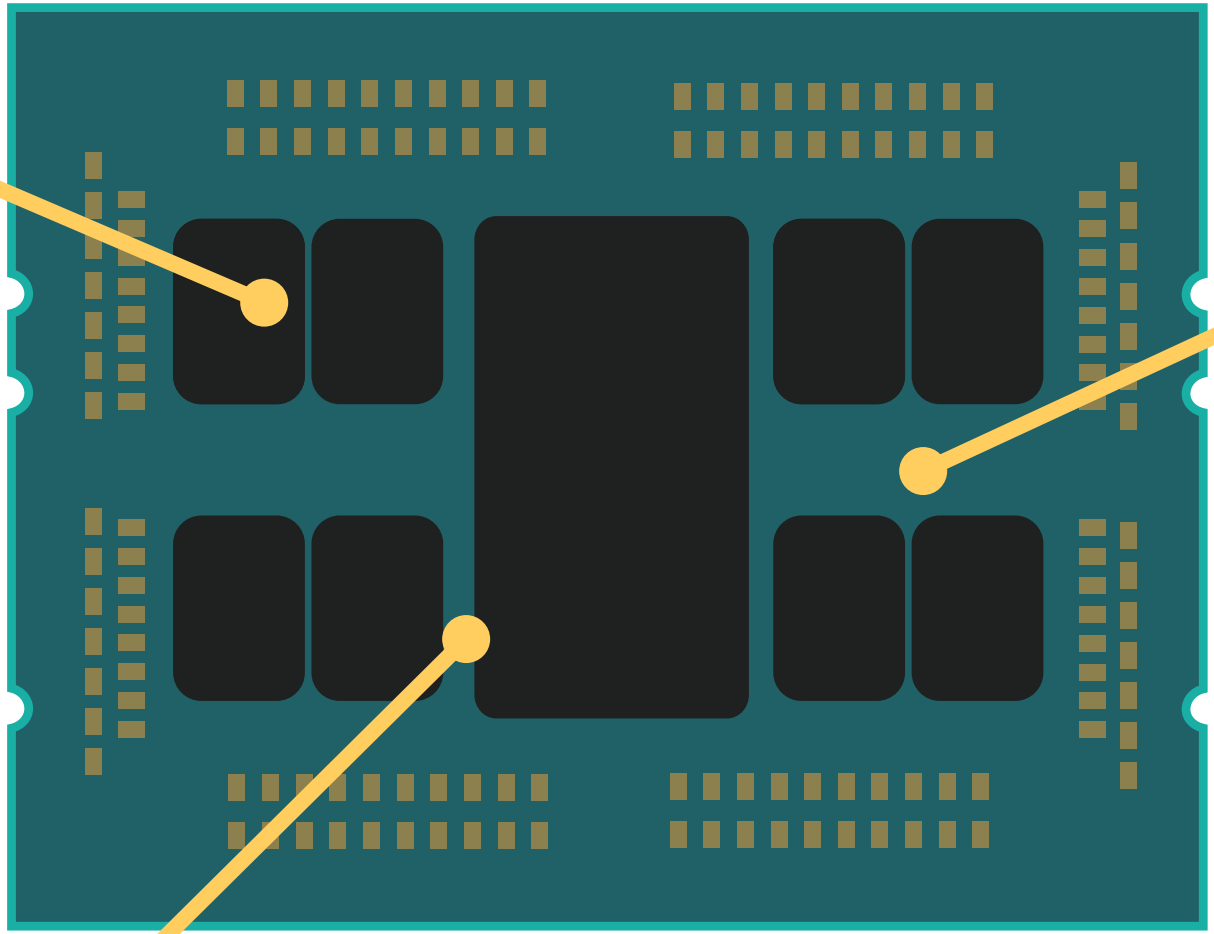
3 Keys to Navigate Chiplet Design Complexities with EDA

Design with chiplet standard compliance in mind

Ensure interoperability and compatibility



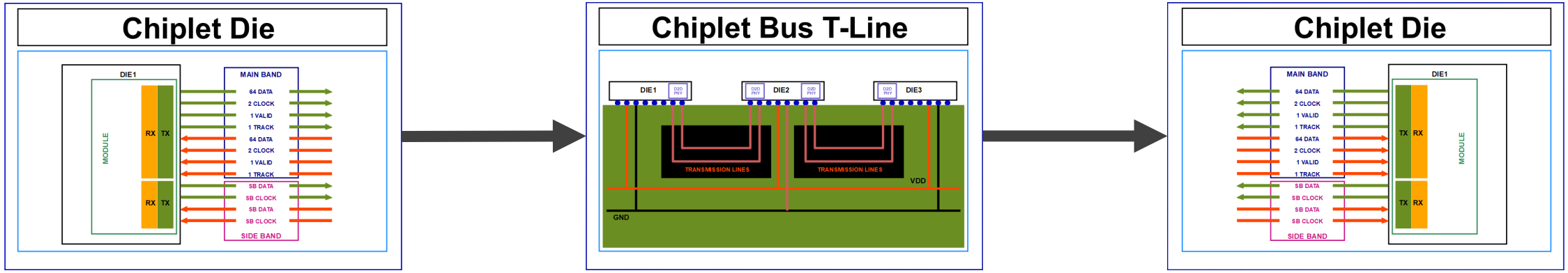
Exercise modular design approach

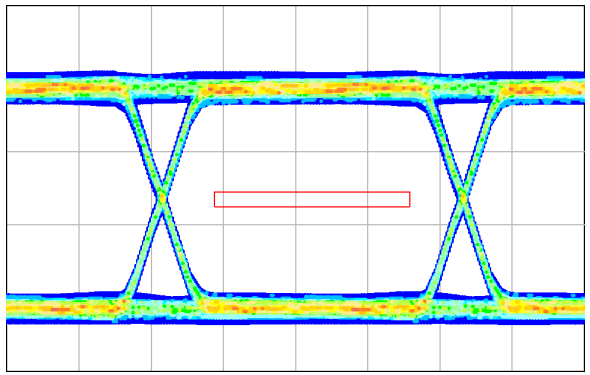
Create robust designs and remove risky dependencies

Perform complete link verification

Predict real-world behaviors and Identify issues early

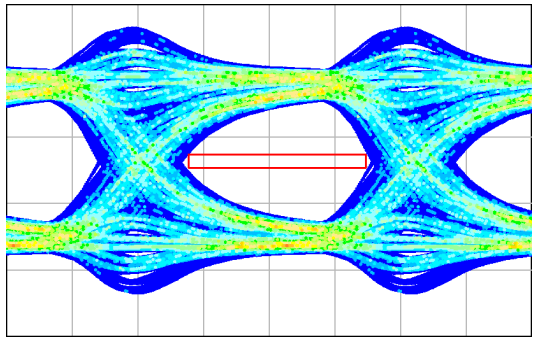
Std Pkg UCIe Link Example with Signal Integrity Insights



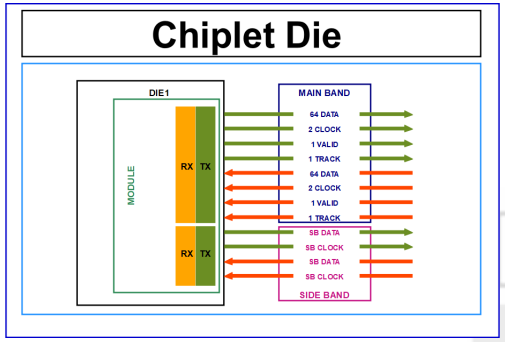


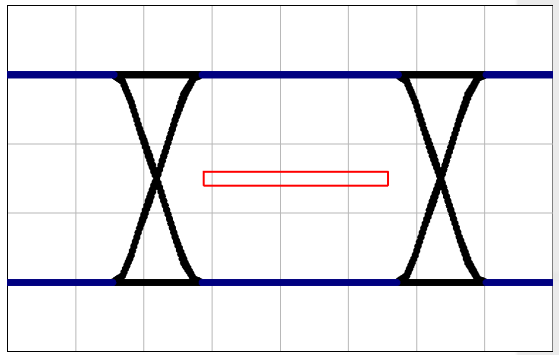
Signal Integrity insights on

- Crosstalk
- Frequency-dependent loss



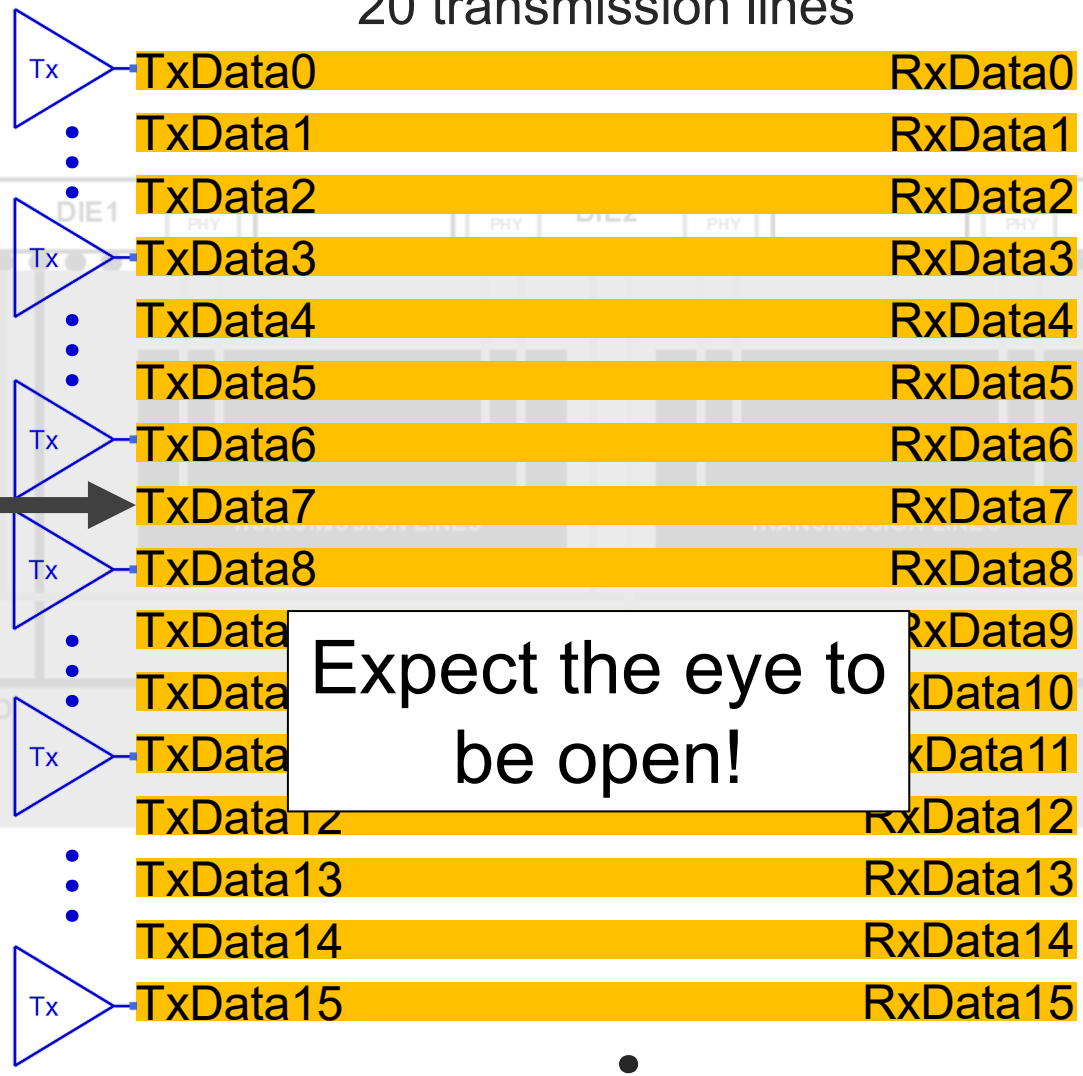
Rule Number 9 : Anticipate Before You Measure or Simulate



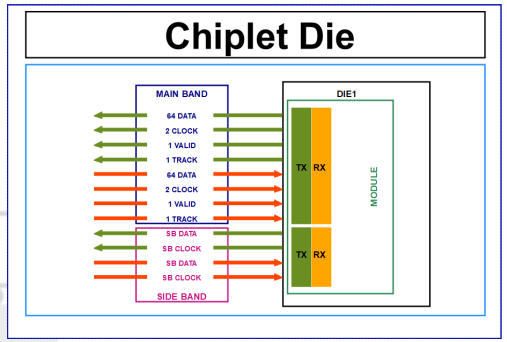


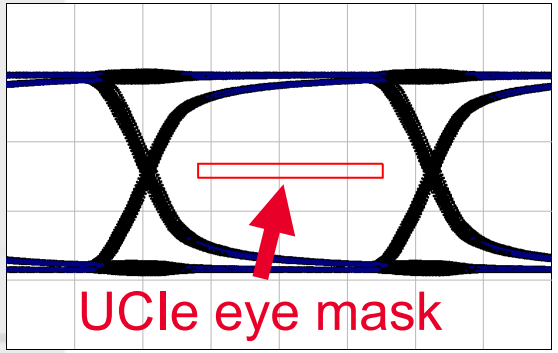
Standard Package
Data rate: 24 GT/s

20 transmission lines



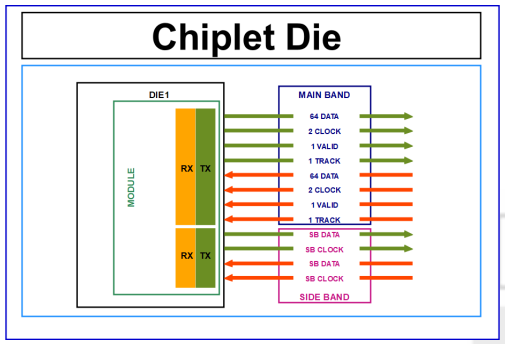
Expect the eye to be open!

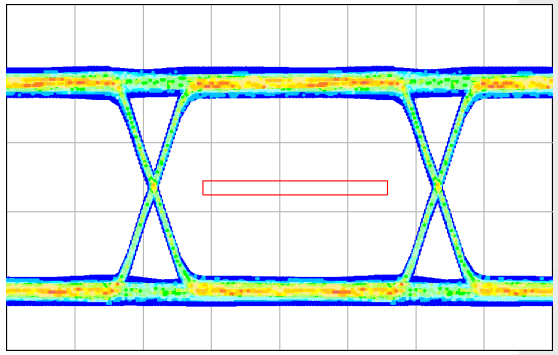




Rx Termination
50 Ω

Simulated Eye Barely Passes the UCIe Eye Mask Test





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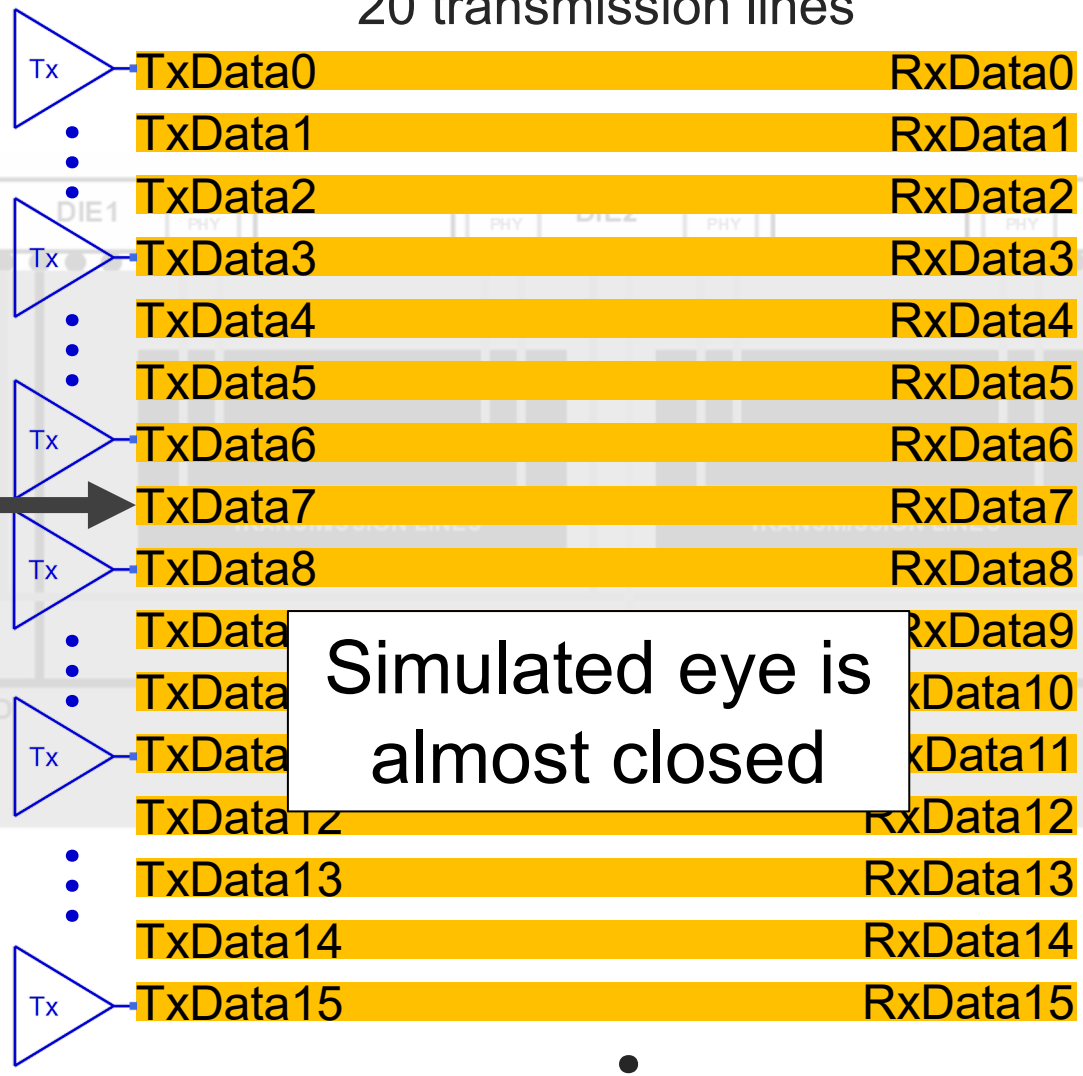
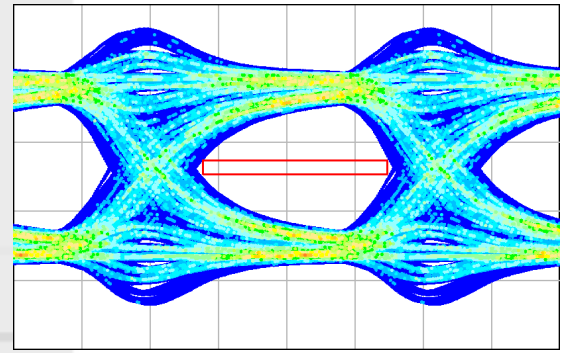


Simulated eye is almost closed



Rx Termination
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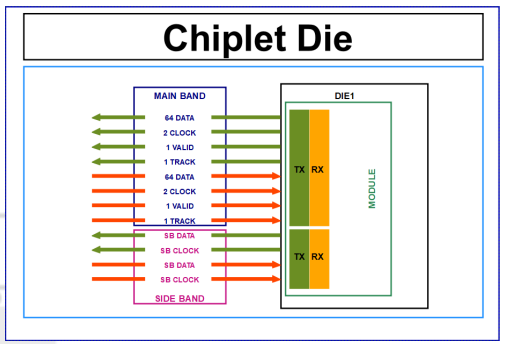
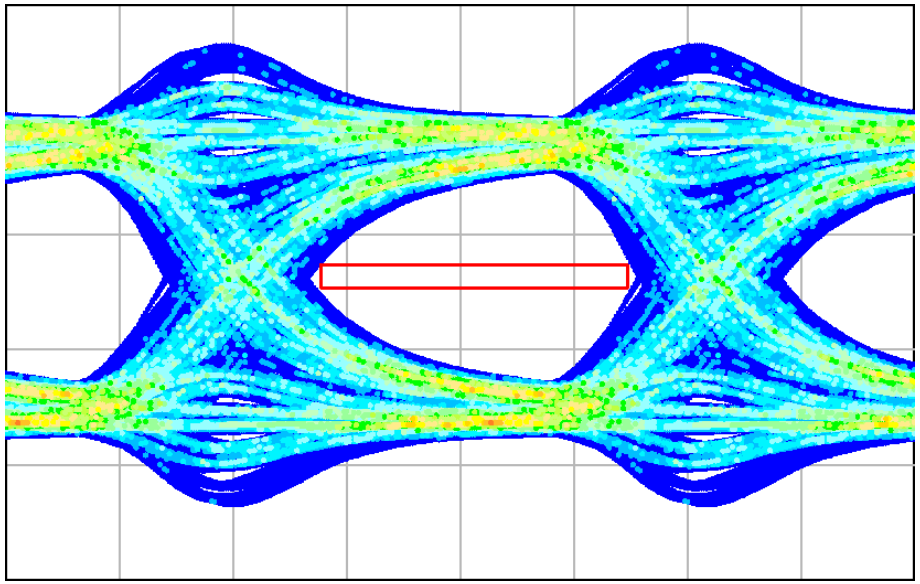
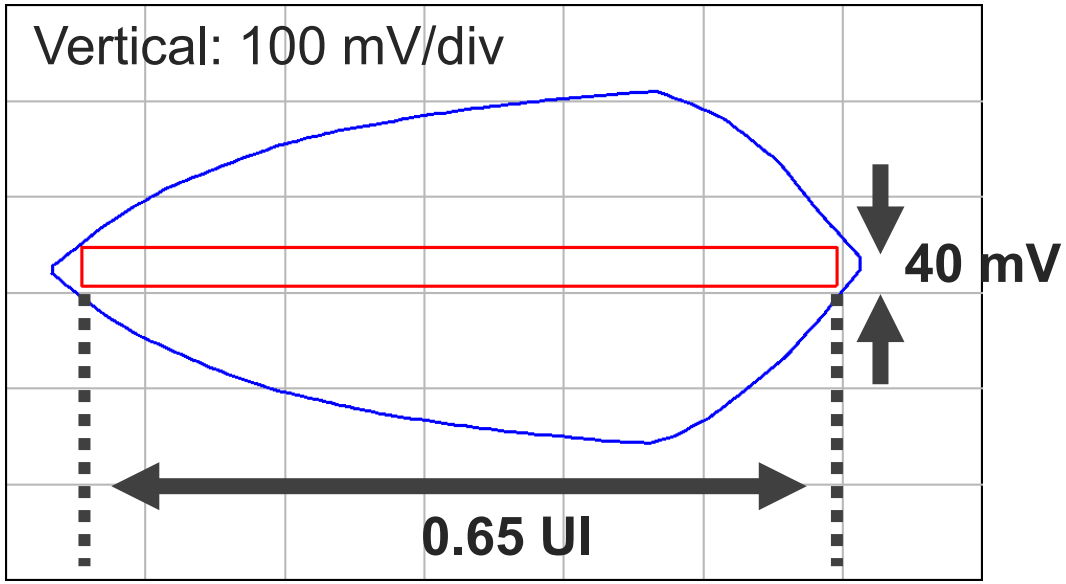


Received Eye, UCIe Eye Mask Definition, 0.2 psec Timing Margin



Standard Package
Data rate: 24 GT/s



Simulation condition: **noiseless** and **jitter-less** behavioral TX and RX models

Data Rate (GT/s)	Eye Height (mV)	Eye Width (UI)
4, 8, 12, 16[1, 3]	40	0.75
24, 32[1,2,3]	40	0.65

The simulated eye is almost closed without noise or jitter. Bad news.

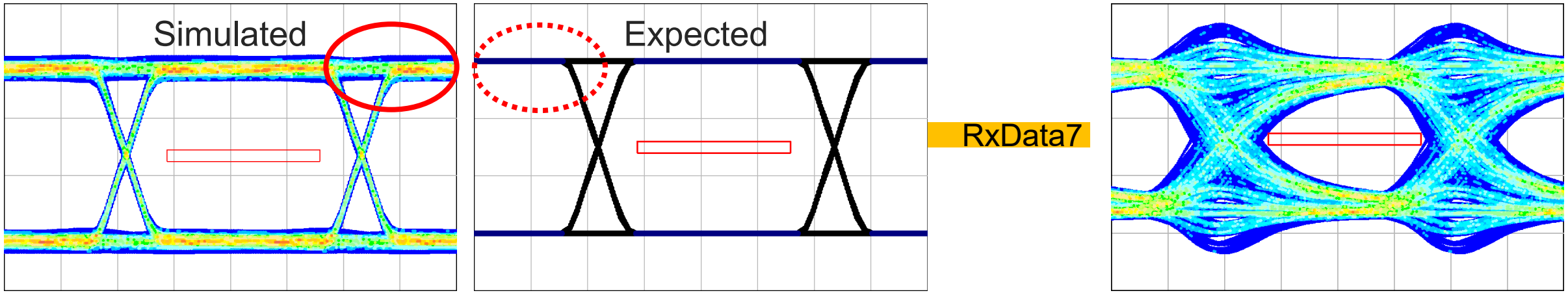
1. Rectangular mask.
2. With equalization enabled.
3. Based on minimum Tx swing specification.

KEYSIGHT

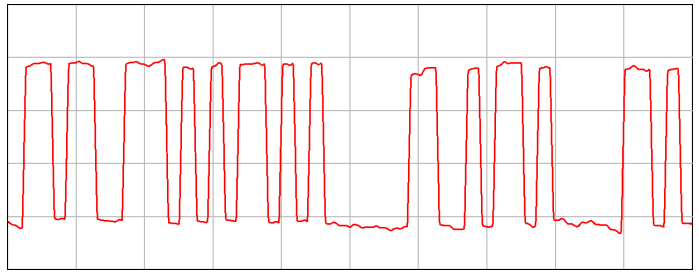
Finding the Root Cause – Reading the Eye Diagram

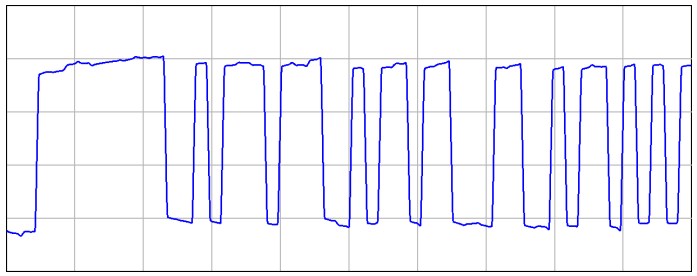
Nearby Channels and the Tx and Rx Eyes

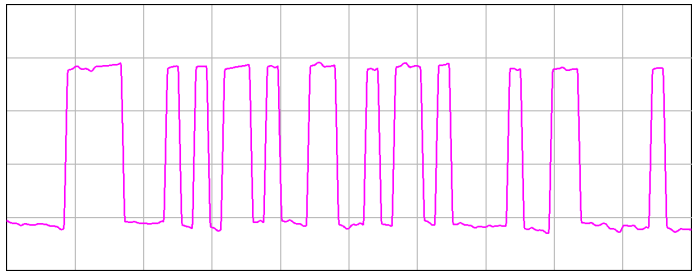
Eye level is thicker than expected



Finding the Root Cause of Unexpected Tx Eye



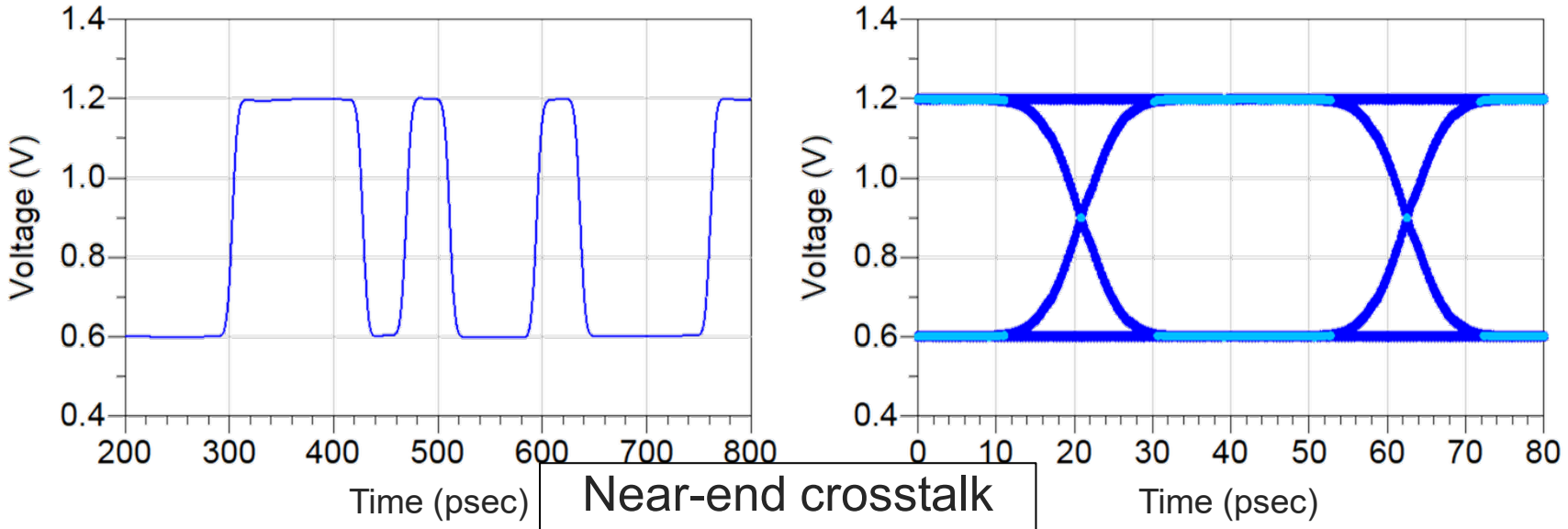




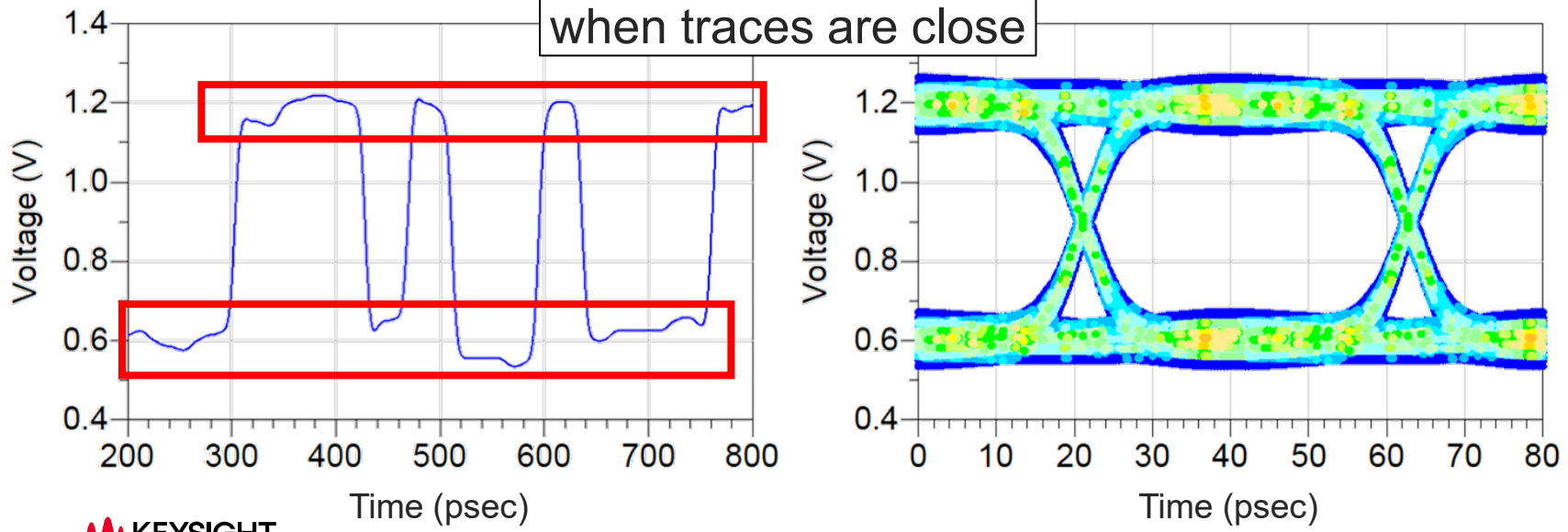
Aggressors coming from both ends

Theory: it is the crosstalk from nearby Tx's that creates the unexpected eye

Confirm Near-end Crosstalk Thickens the Eye Levels



Near-end crosstalk when traces are close



TxData6 RxData6

Spacing = 10x trace width

TxData7 RxData7

Spacing = 10x trace width

TxData8 RxData8

TxData6 RxData6

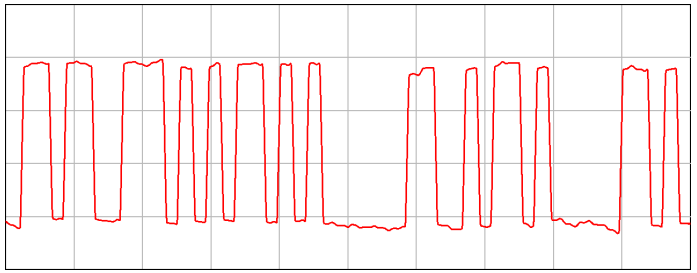
TxData7 RxData7

TxData8 RxData8

Spacing = 1x trace width

KEYSIGHT

Finding the Root Cause of Unexpected Rx Eye



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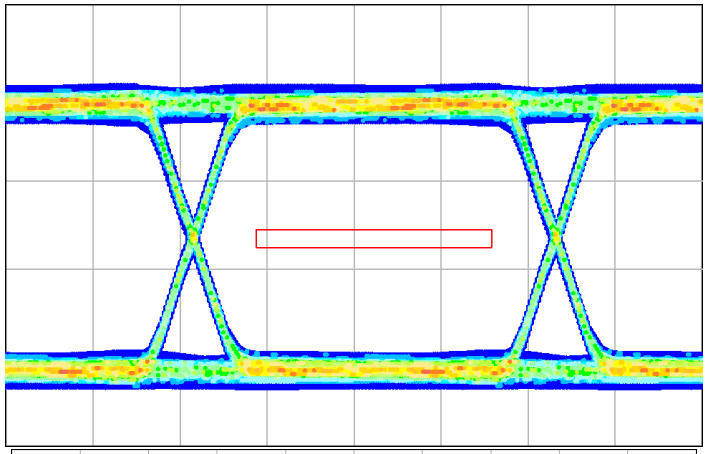
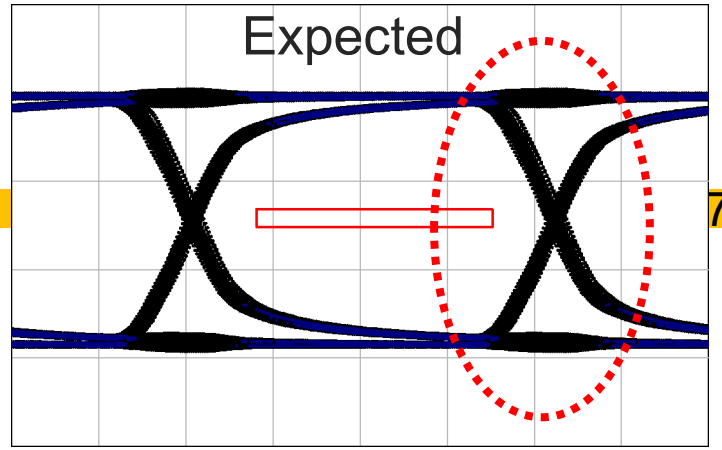
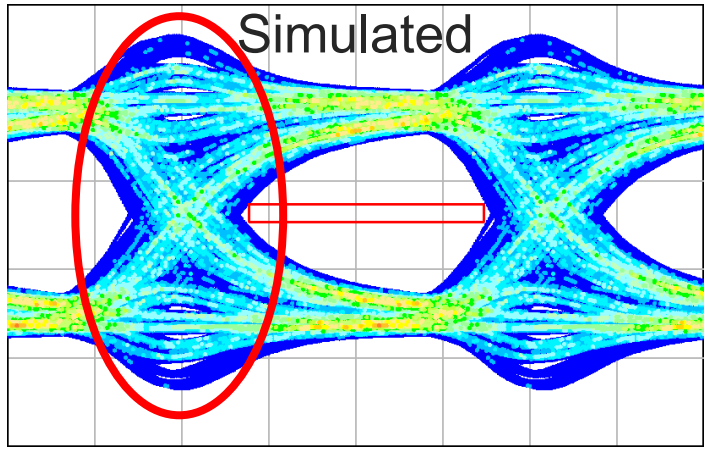
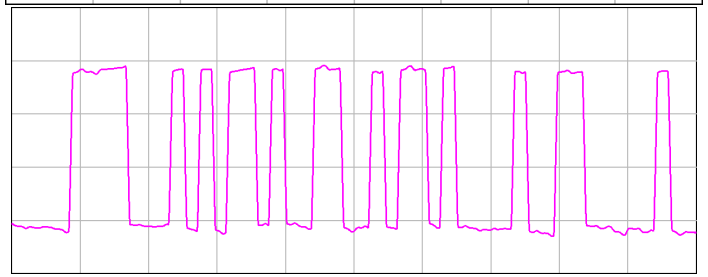


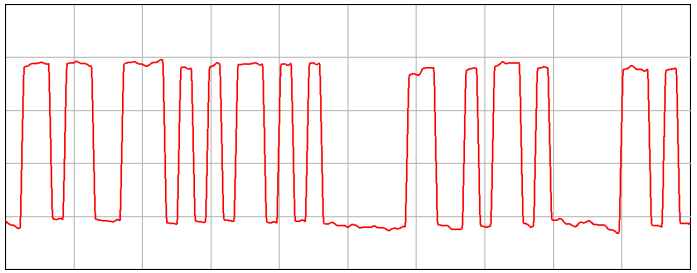


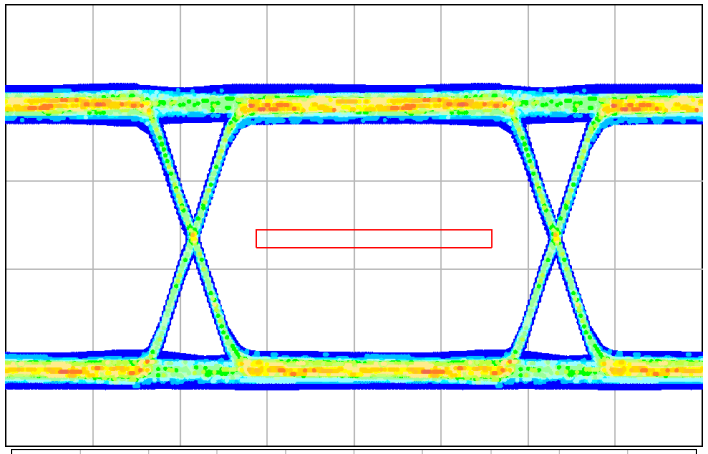


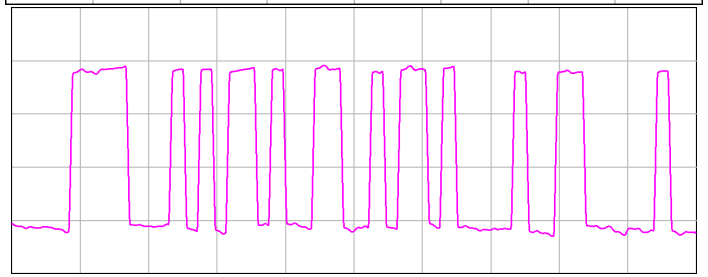
Simulated transition has unexpected peaks



Finding the Root Cause of Unexpected Rx Eye



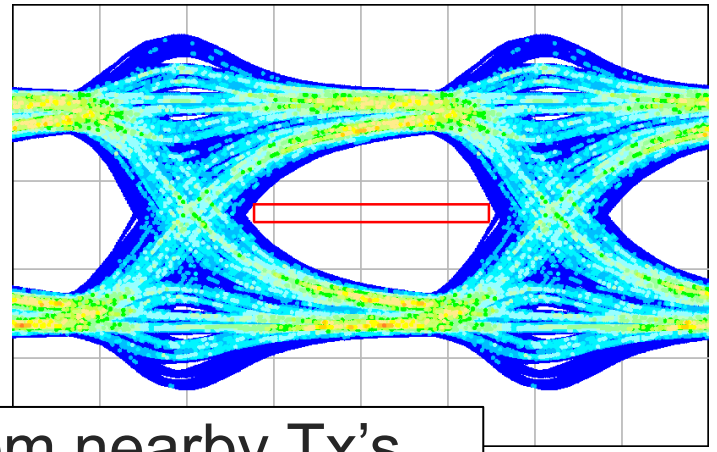




Aggressors coming from both ends

TxData6 RxData6

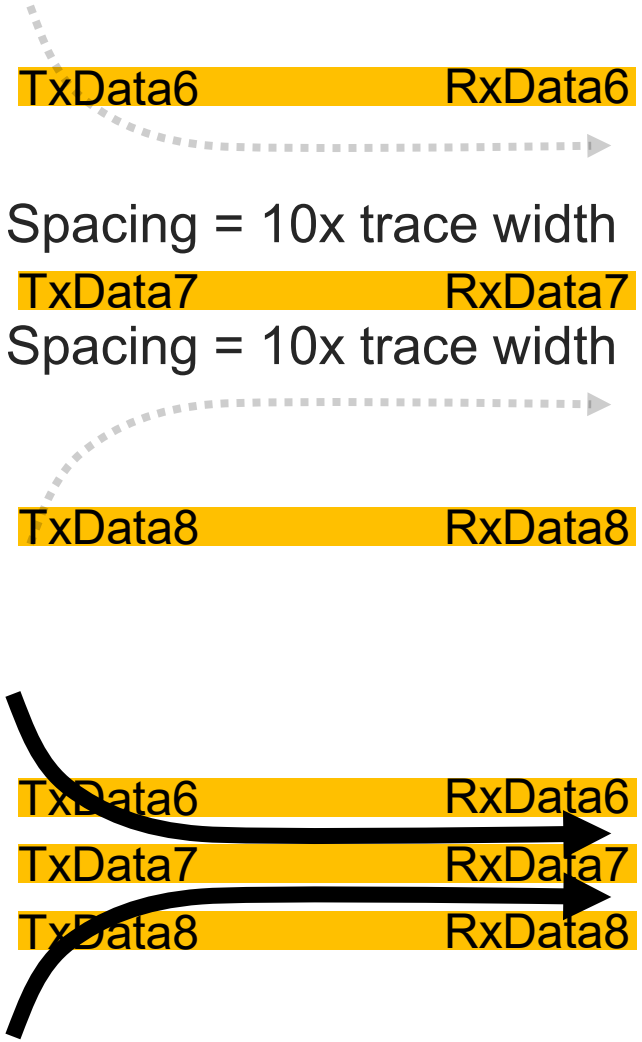
TxData7 RxData7

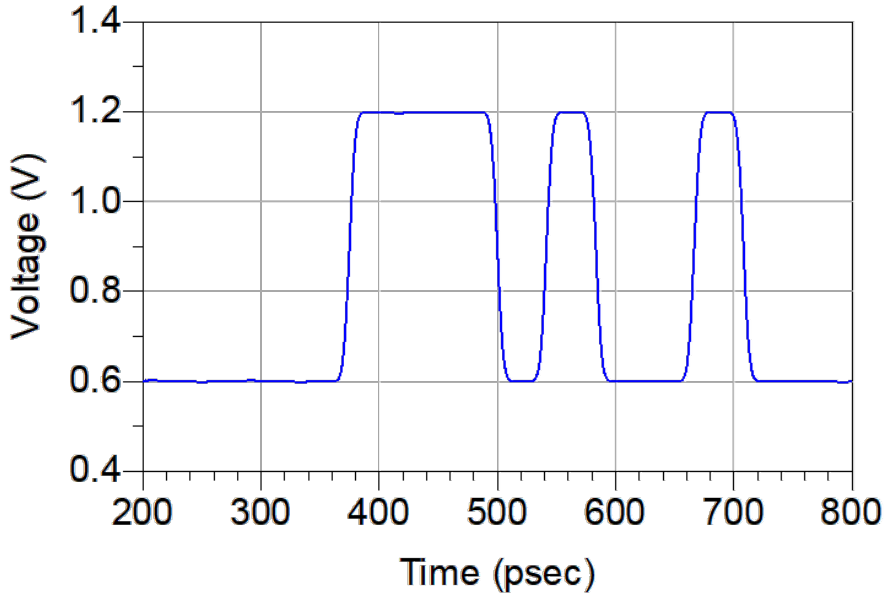


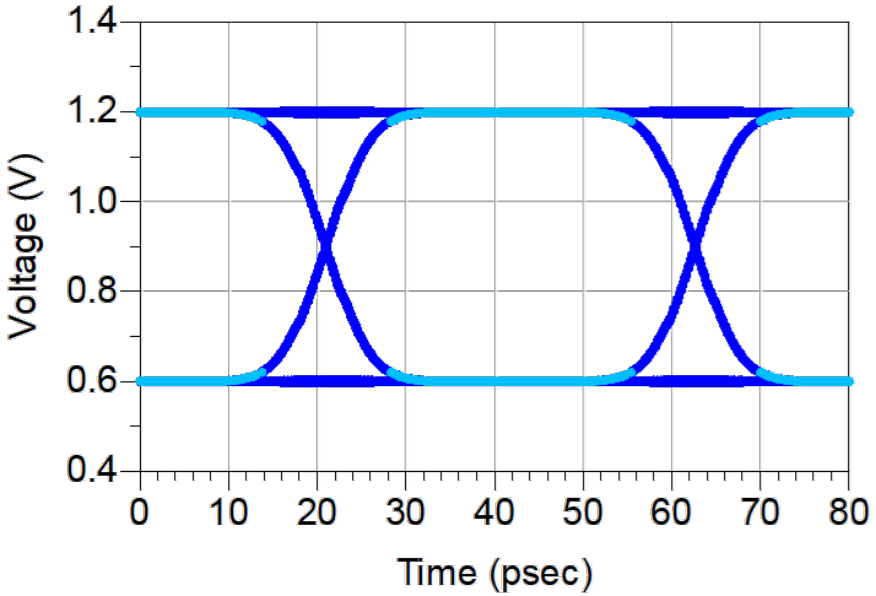
Theory: it is the crosstalk from nearby Tx's that creates the unexpected peaks

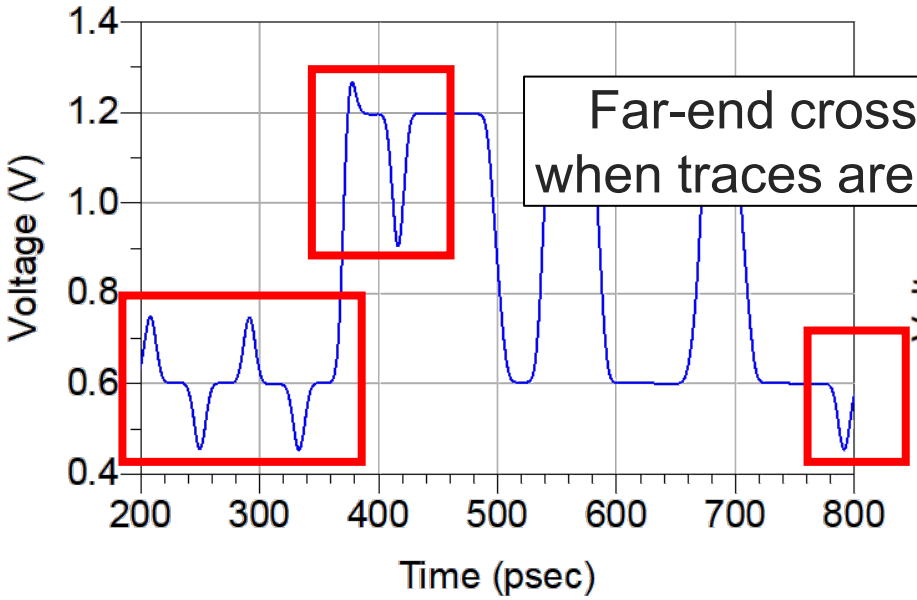
TxData8 RxData8

Confirm Rx Eye Transition Peaks When Traces Are Closer

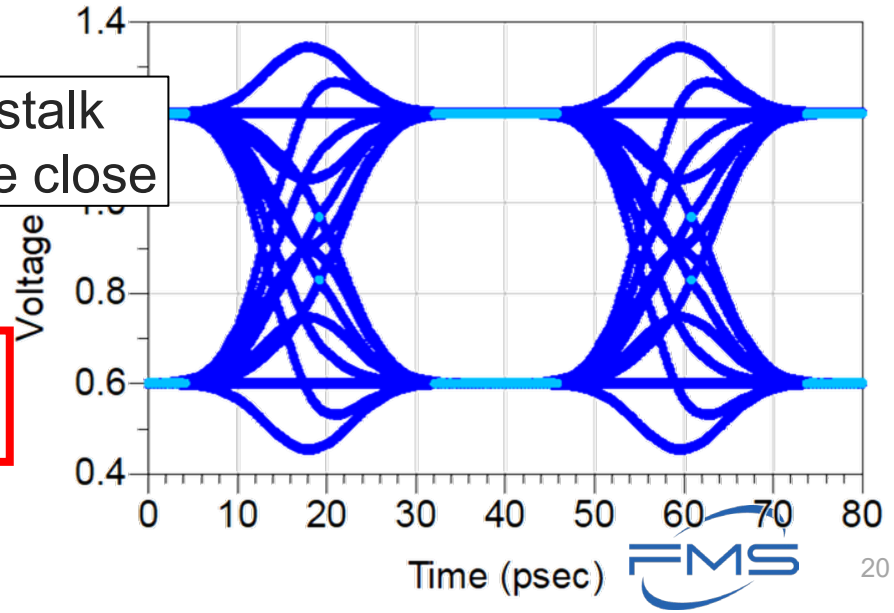








Far-end crosstalk when traces are close

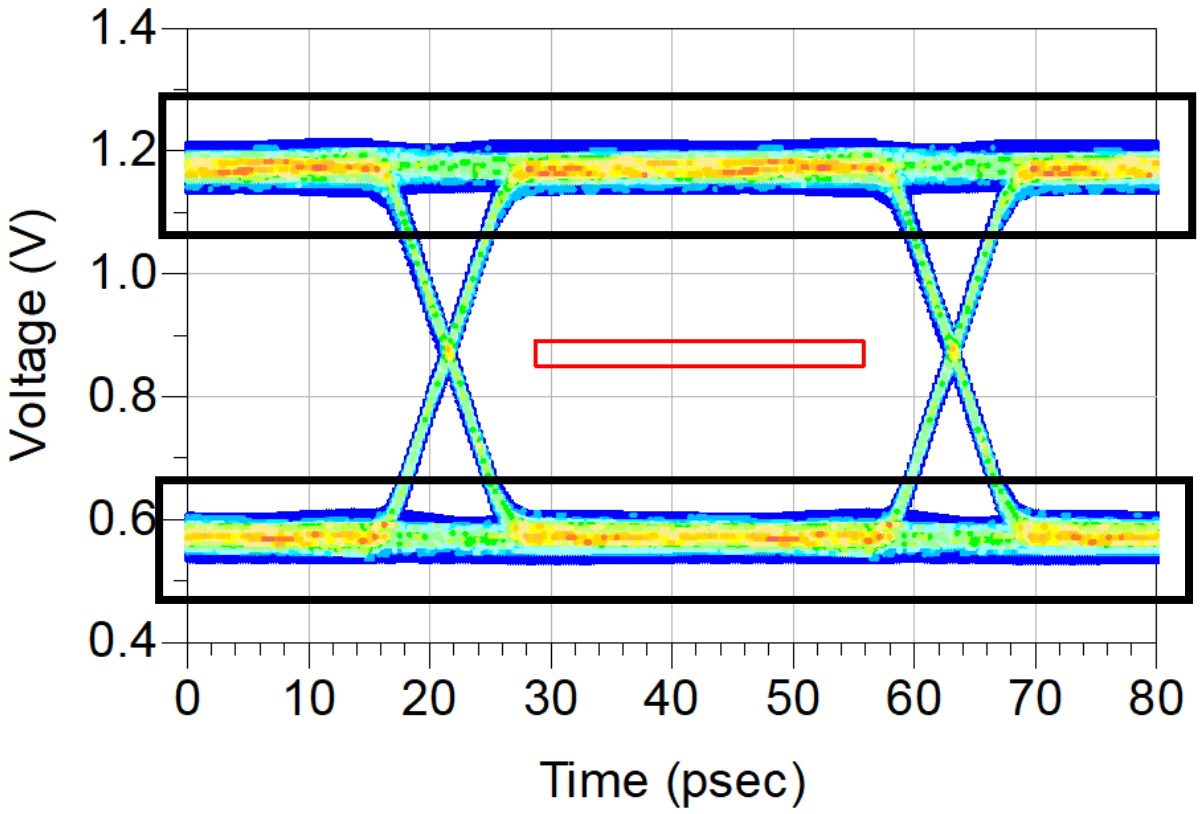


Spacing = 1x trace width

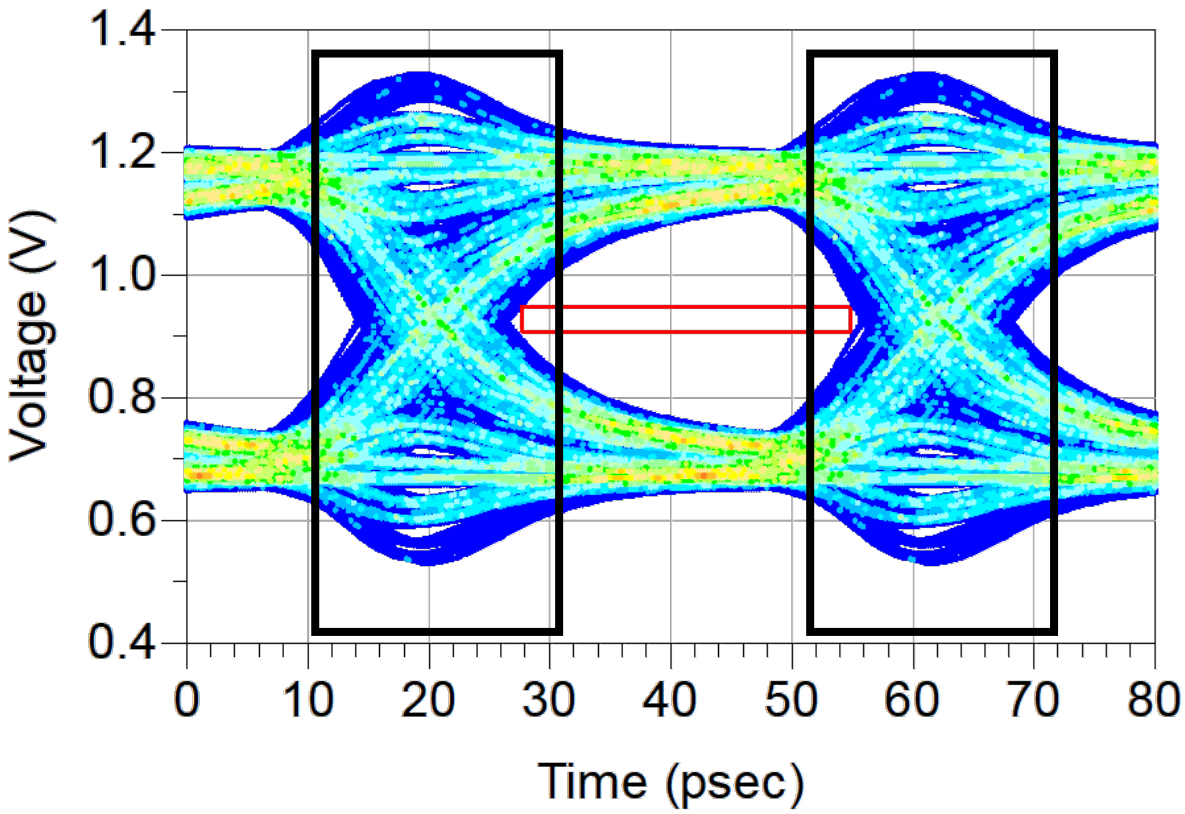
KEYSIGHT

Traces Are Close: Crosstalk Signatures in Tx Eye and Rx Eye

Near-end crosstalk signature



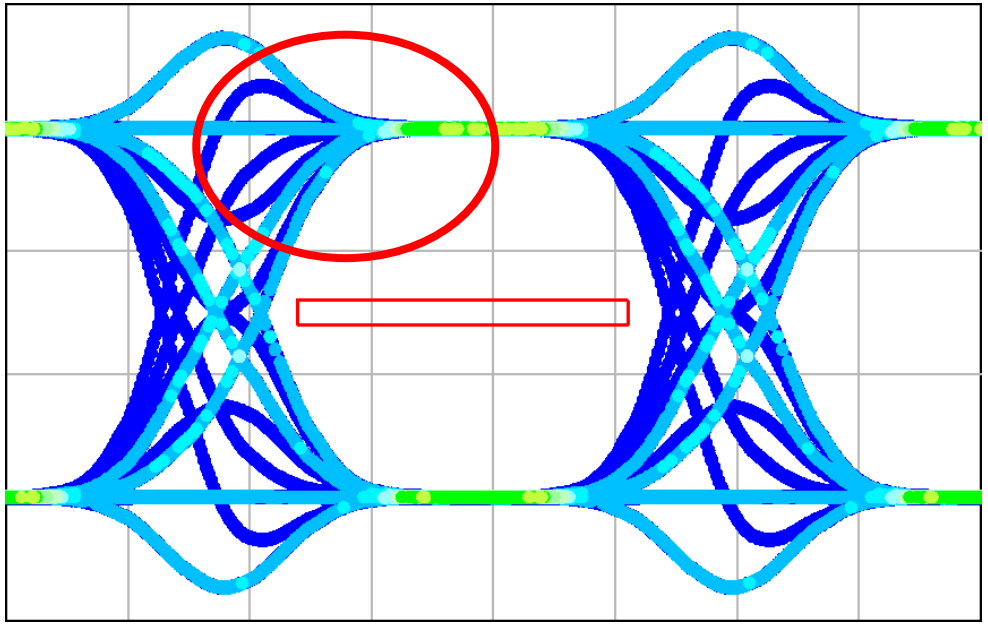
Far-end crosstalk signature



When the eye levels are thick and the far-end eye has peaks in the transitions, traces are likely close enough to induce near-end and far-end cross-talk.

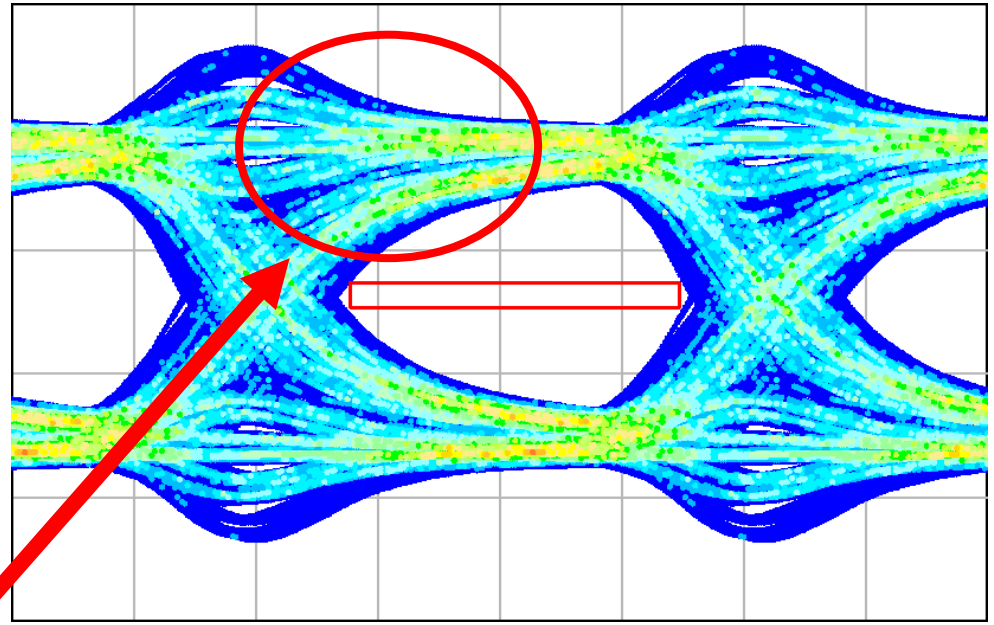
Frequency-dependent Loss Causes Rise Time Degradation

Far-end Crosstalk Example



Simulated with coupled **lossless** line

Simulated Eye



Simulated with coupled **lossy** lines

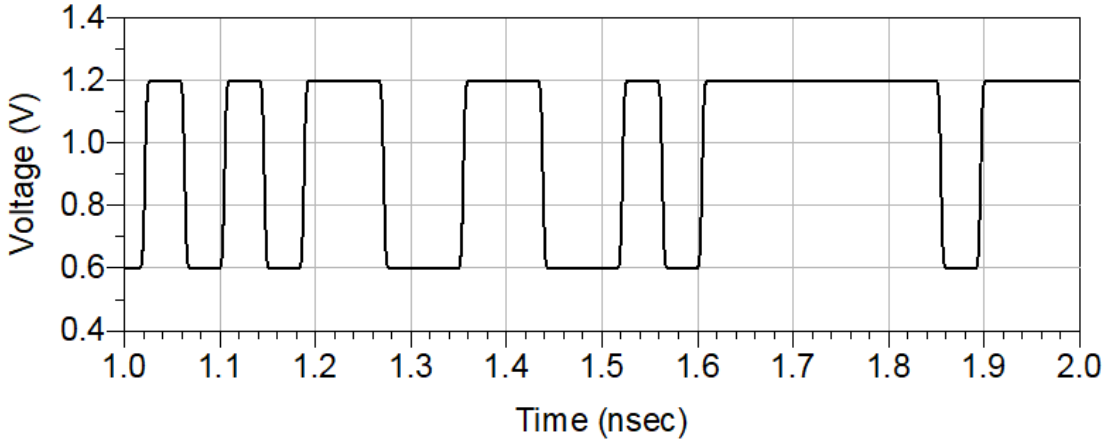
Rise time degradation caused by
frequency-dependent loss

KEYSIGHT

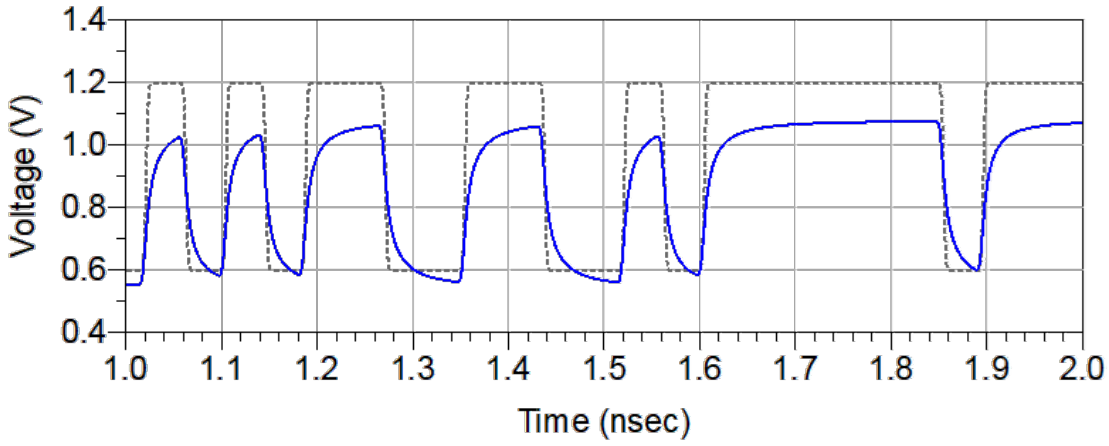
Finding the Root Cause – Frequency-dependent Loss

Interconnects Attenuate High-frequency Components More

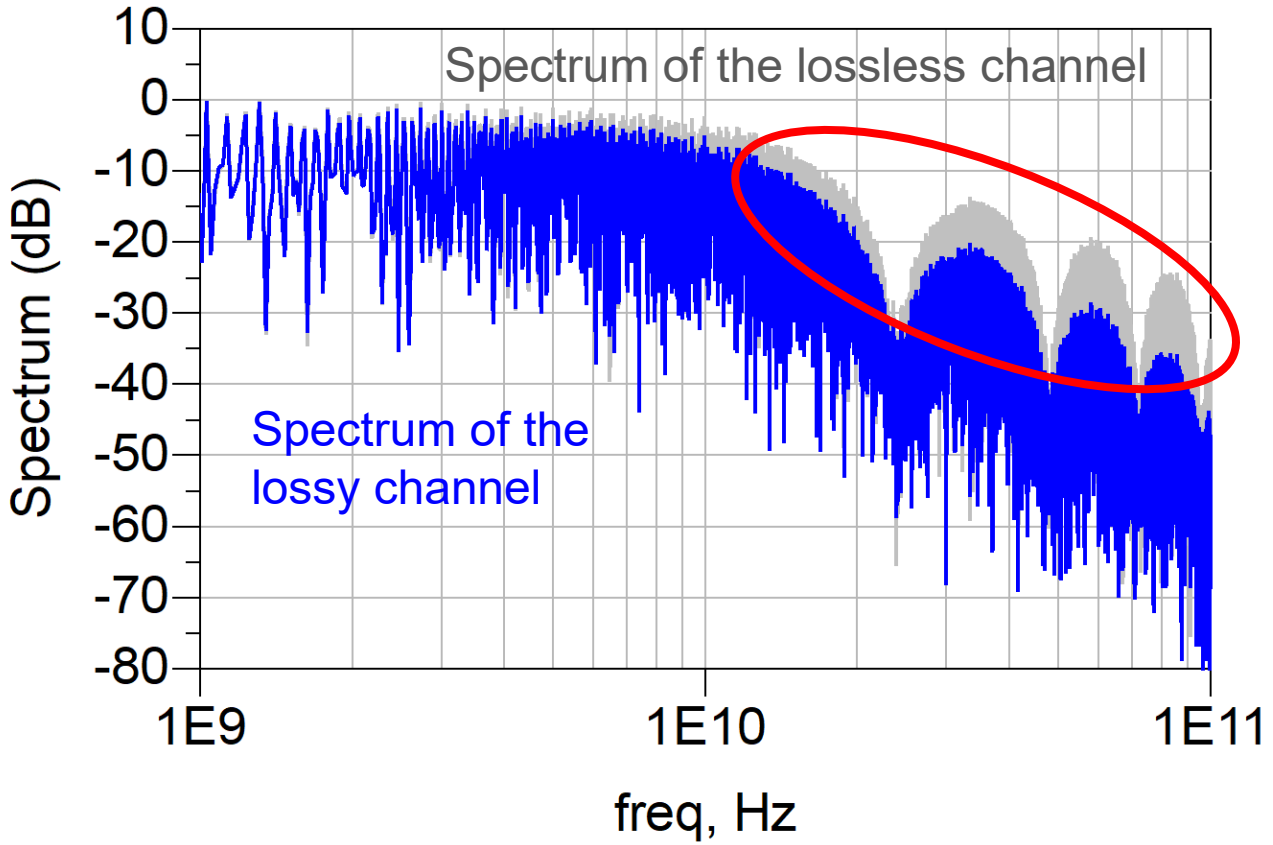
Received waveform after a lossless channel



Received waveform after a lossy channel



The lossy channel acts as a low-pass filter.

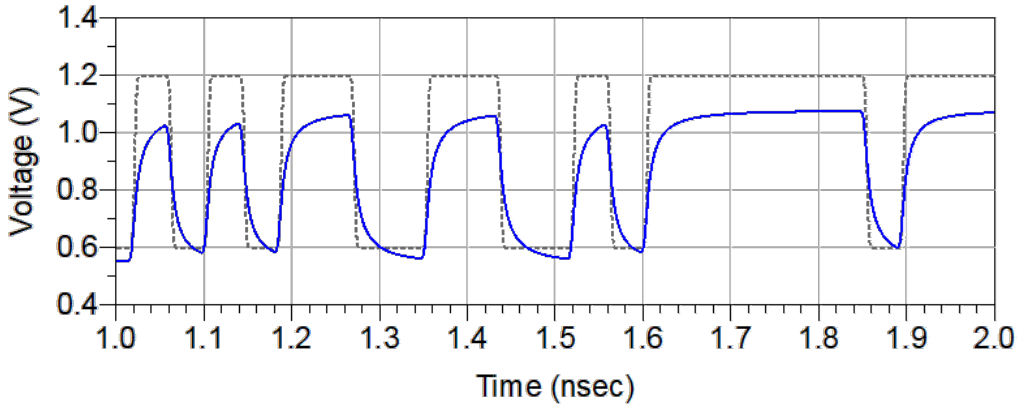


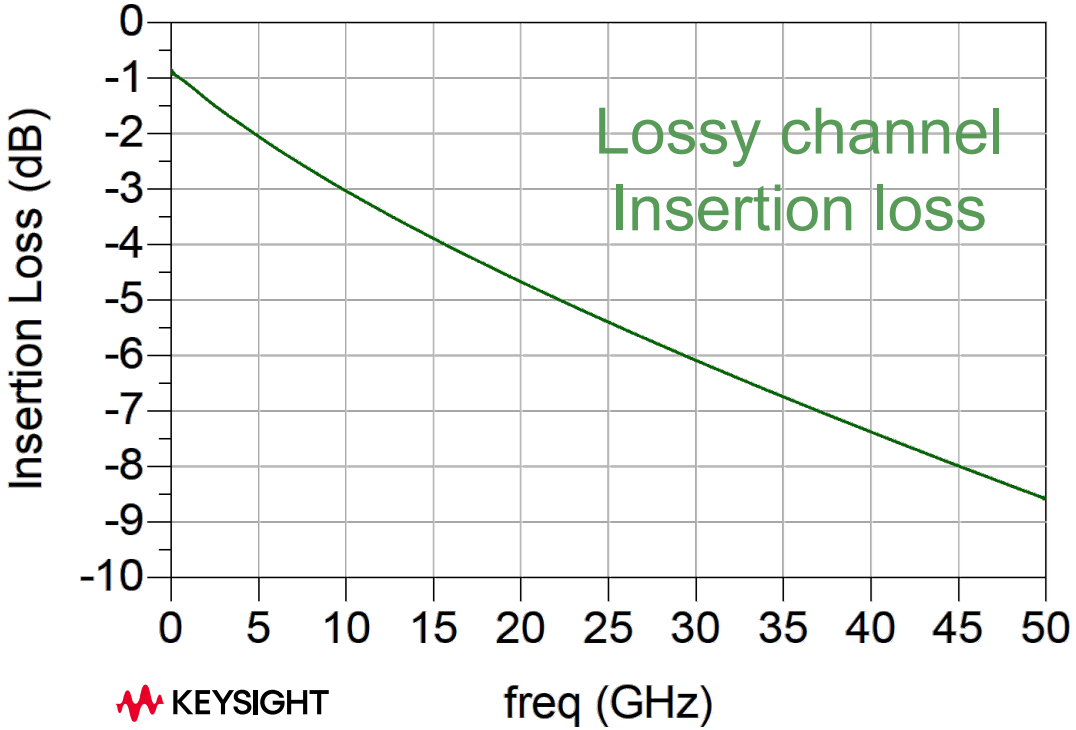
This low-pass filter degrades the fast rise time.

KEYSIGHT

Interconnects Attenuate High-frequency Components More

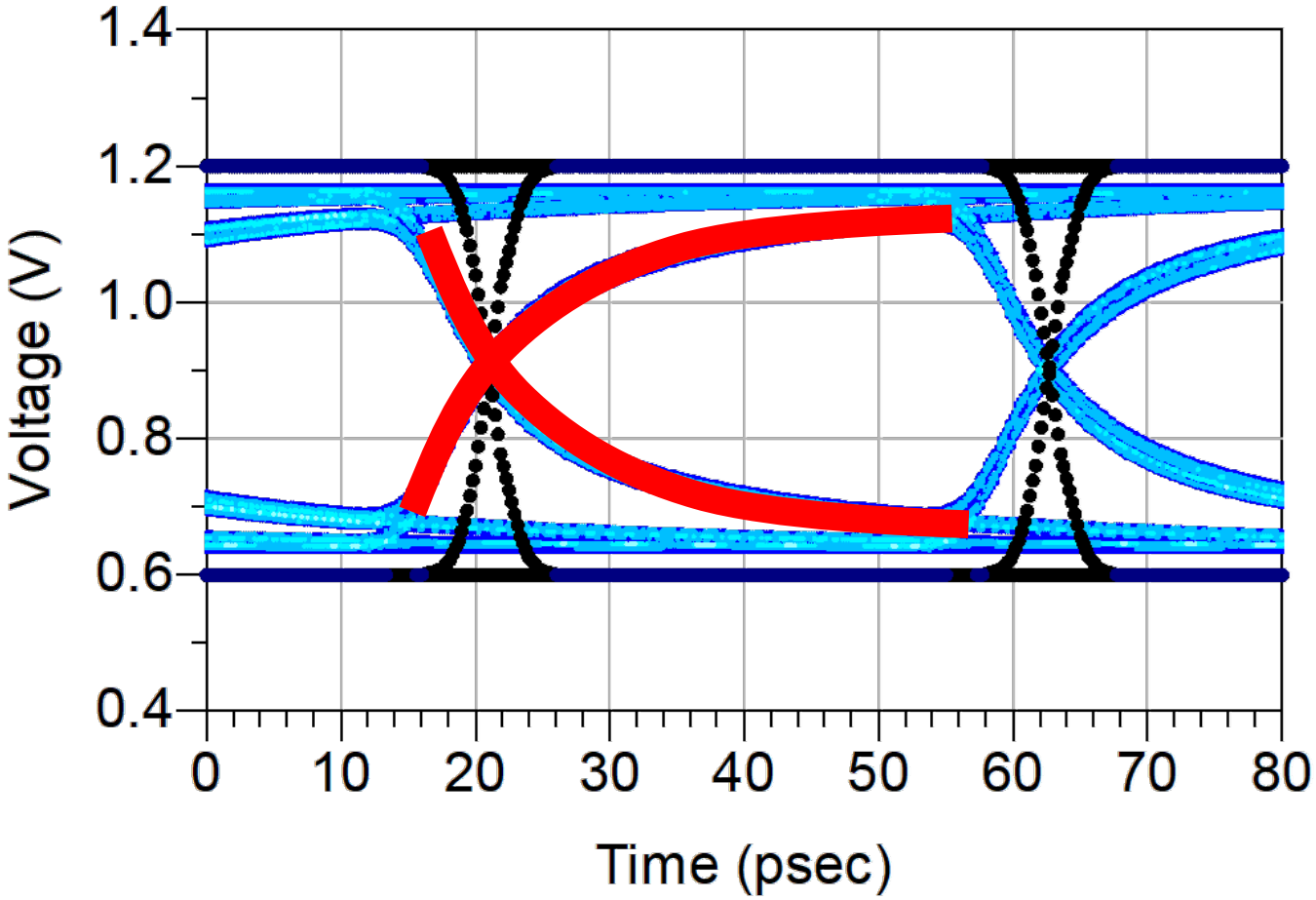
Received waveform after a lossy channel





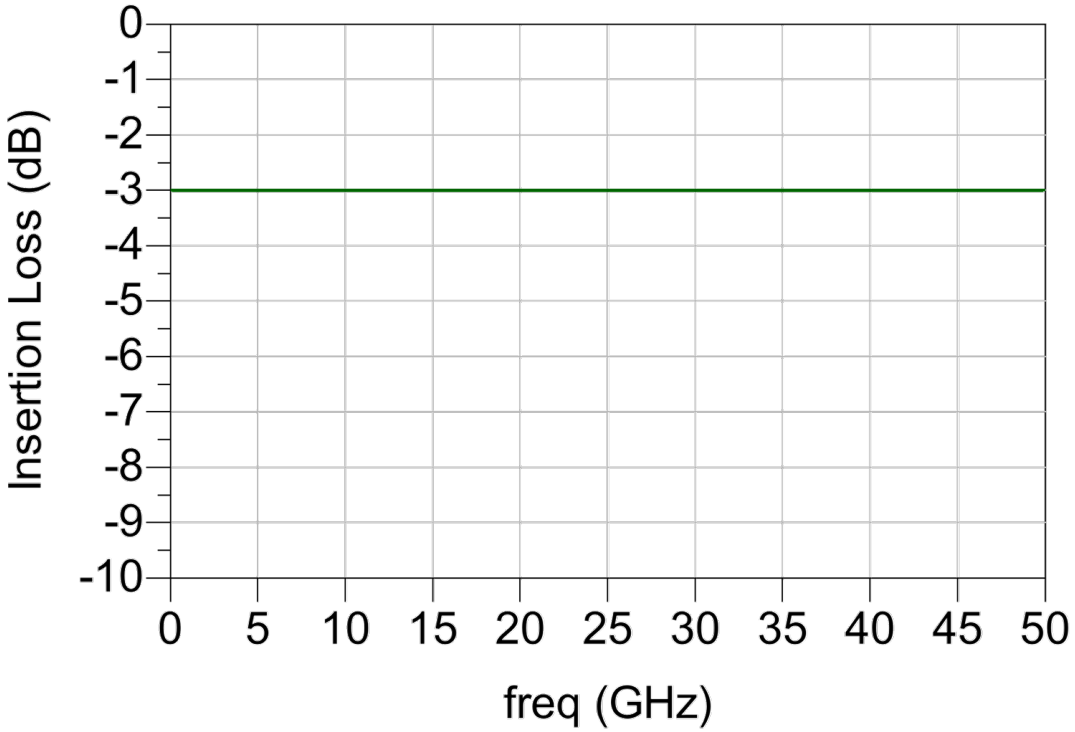
KEYSIGHT

Frequency-dependent loss reduces eye height and width

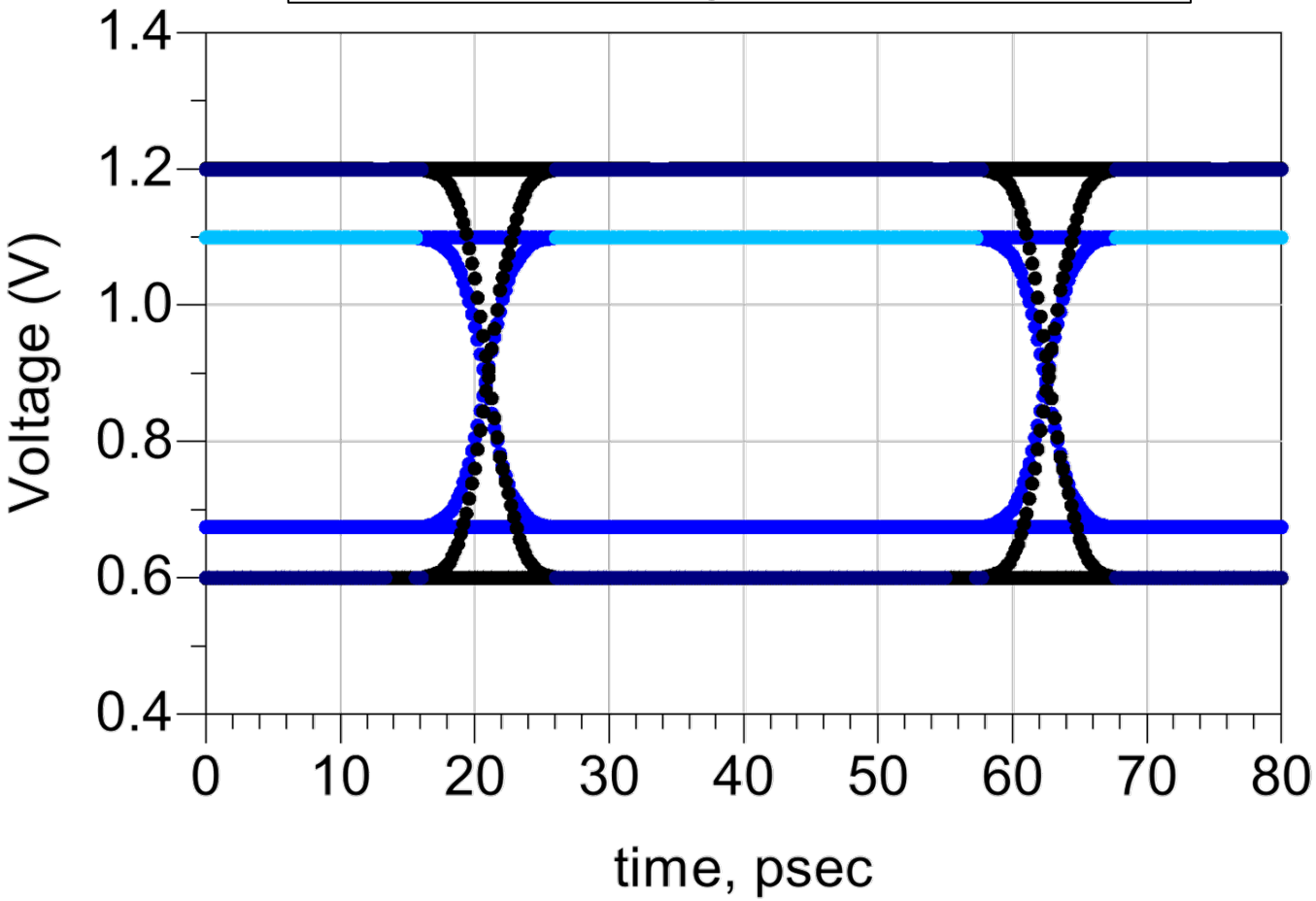


Constant Loss Over Frequency Only Reduces Eye Amplitude

Lossy channel with
constant Insertion loss



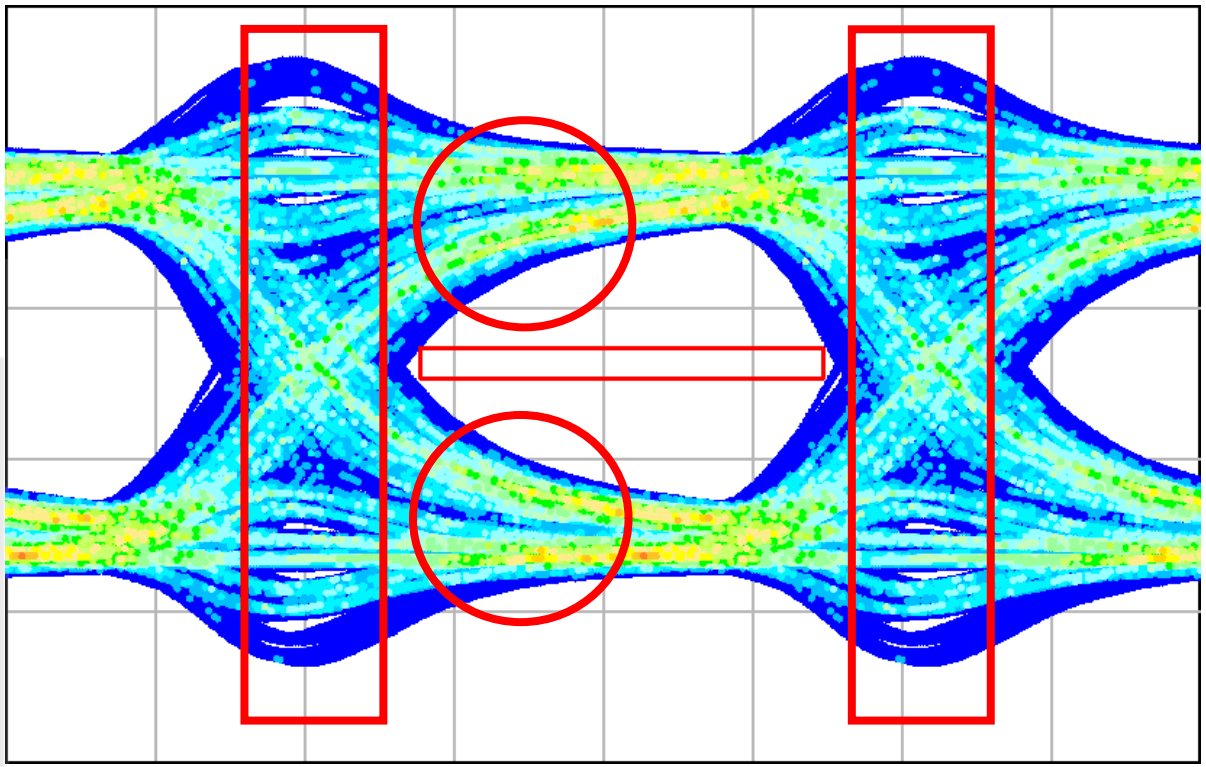
Frequency-independent loss
does not degrade rise time



What We Have Covered So Far

20 transmission lines

TxData0	RxData0
TxData1	RxData1
TxData2	RxData2
TxData3	RxData3
TxData4	RxData4
TxData5	RxData5
TxData6	RxData6
TxData7	RxData7
TxData8	RxData8
TxData9	RxData9
TxData10	RxData10
TxData11	RxData11
TxData12	RxData12
TxData13	RxData13
TxData14	RxData14
TxData15	RxData15

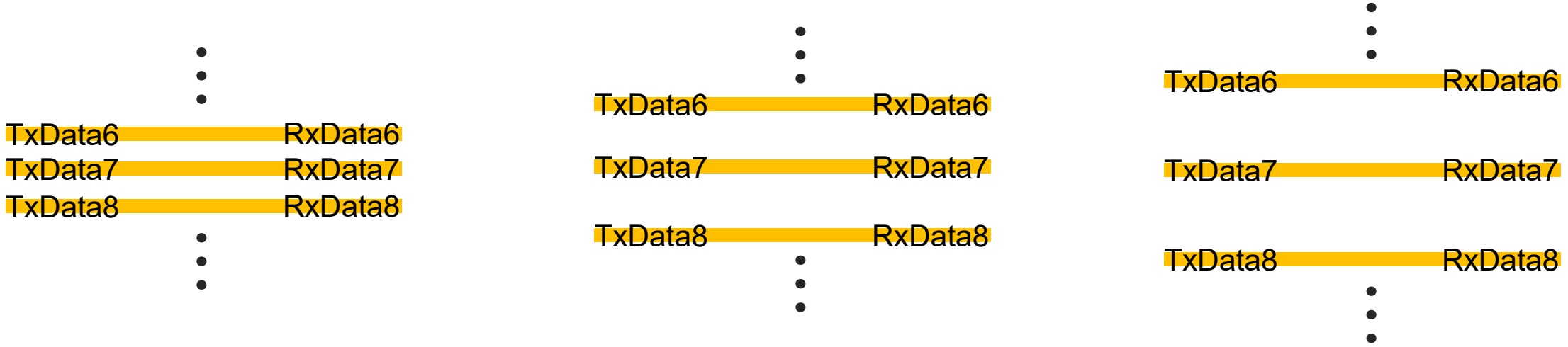


- Eye mask
- Crosstalk signature
- Rise time degradation

KEYSIGHT FMS

Improve the Eye by Eliminating the Root Cause

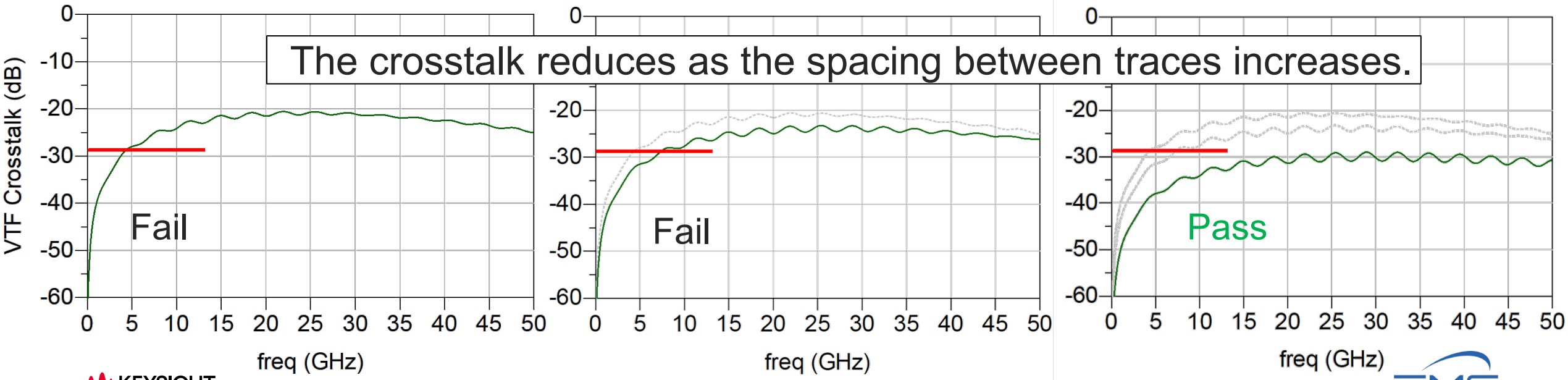
Reduce Crosstalk by Pulling the Traces Farther Apart



Spacing = 2.2x trace width

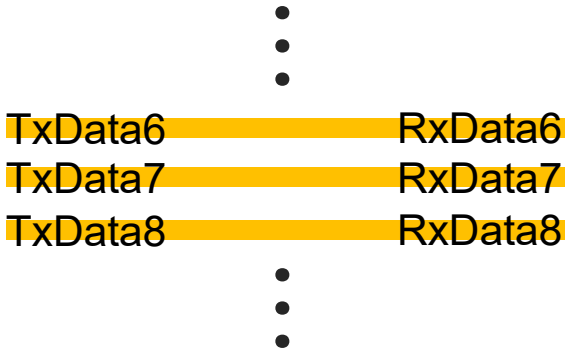
Spacing = 3x trace width

Spacing = 5x trace width

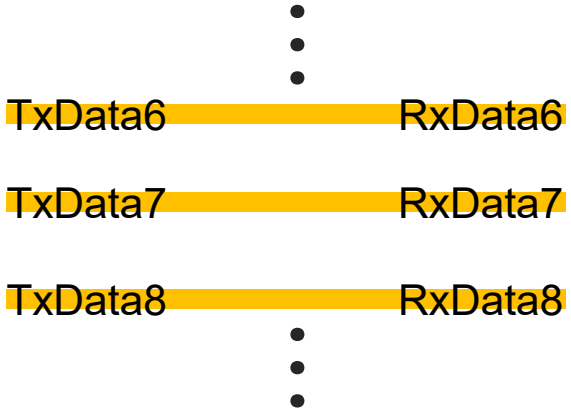


KEYSIGHT

Reduce Crosstalk and Open the Eye by Increasing Spacing

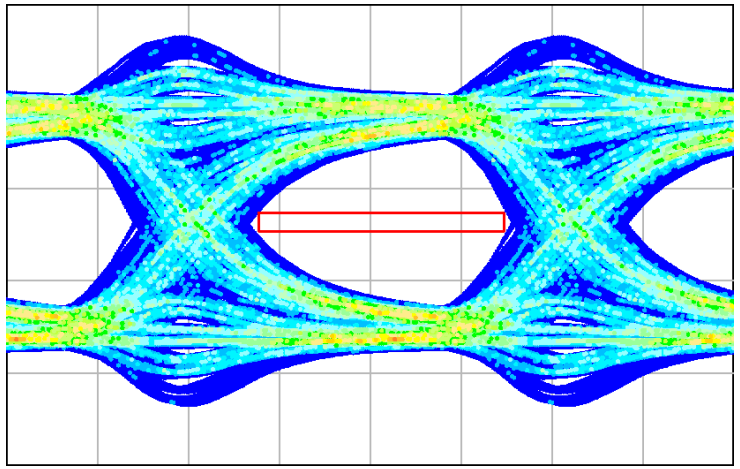


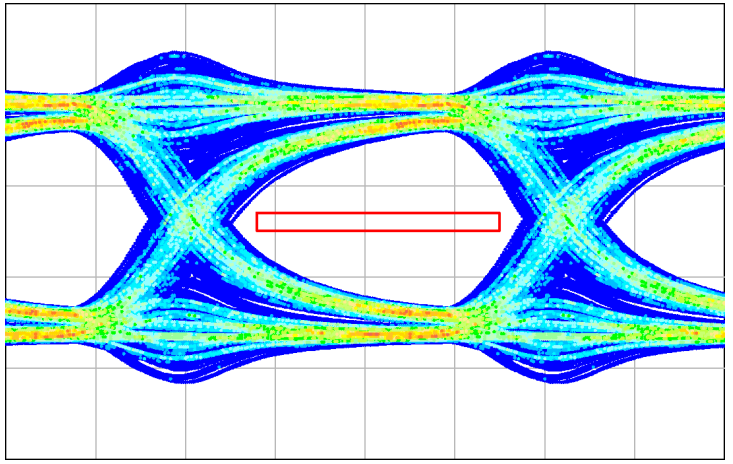
Spacing = 2.2x trace width

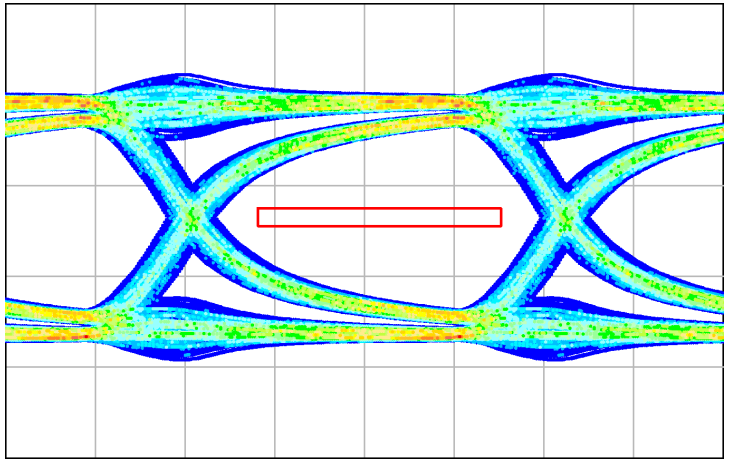


Spacing = 3x trace width

Spacing = 5x trace width

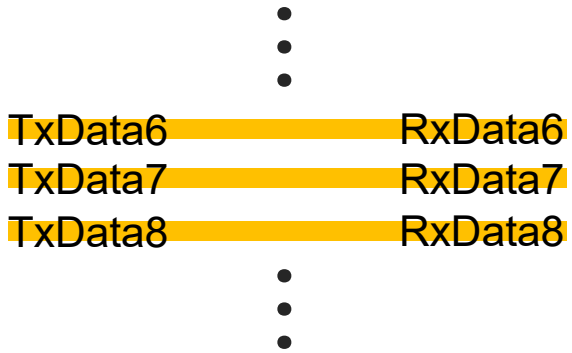




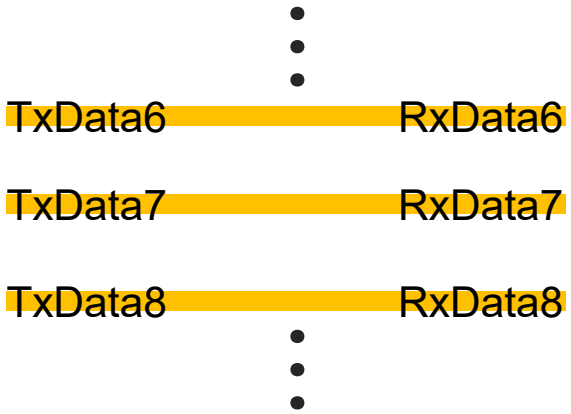


Crosstalk reduces as spacing between traces increases.

Increase Timing Margin by Increasing Spacing

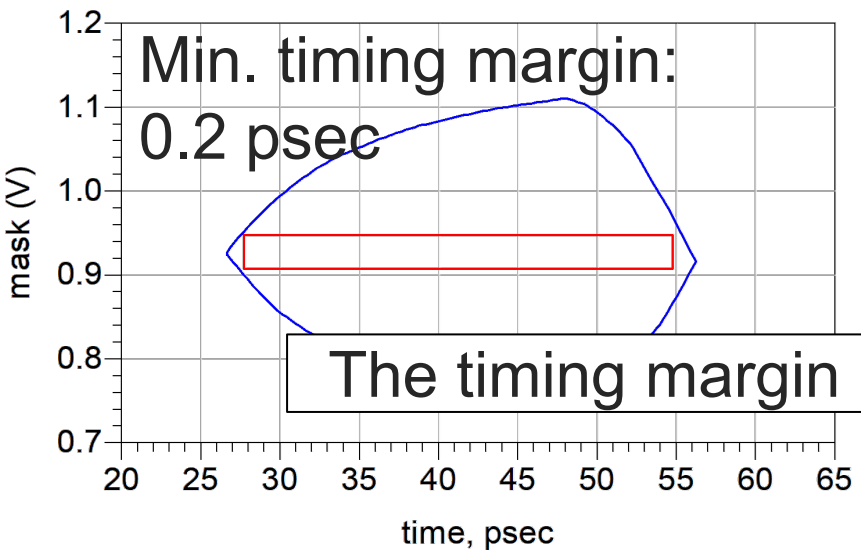


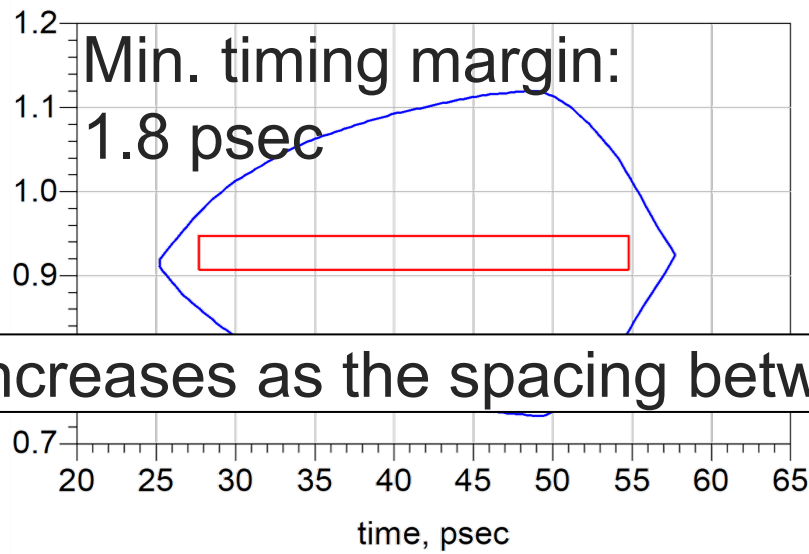
Spacing = 2.2x trace width

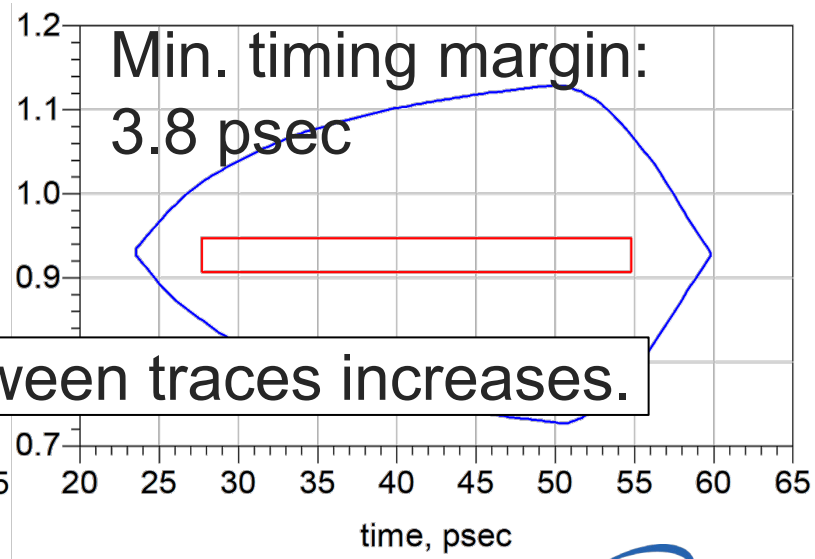


Spacing = 3x trace width

Spacing = 5x trace width



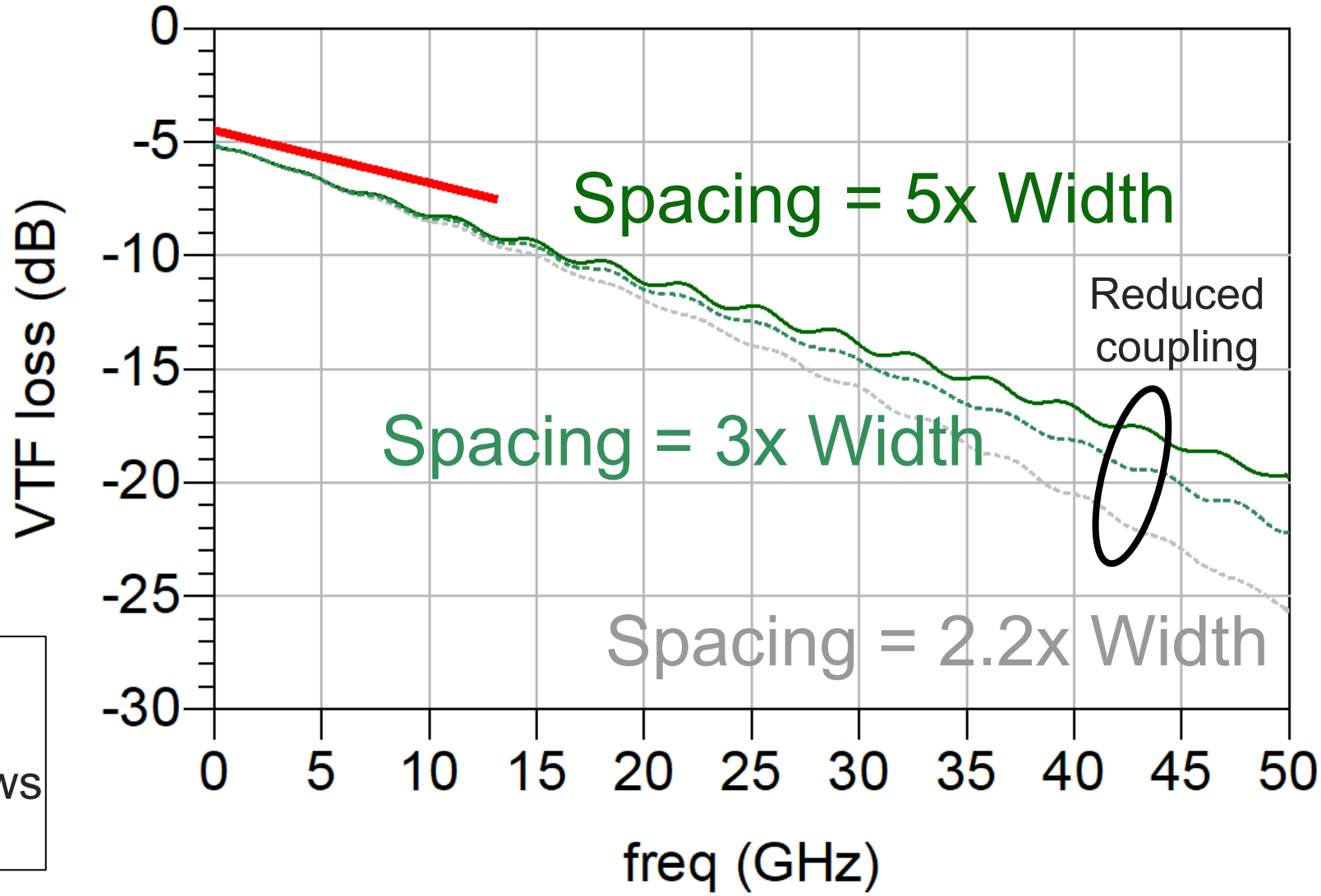




The timing margin increases as the spacing between traces increases.

Expect the Increase of Spacing to Have Little Impact on Loss

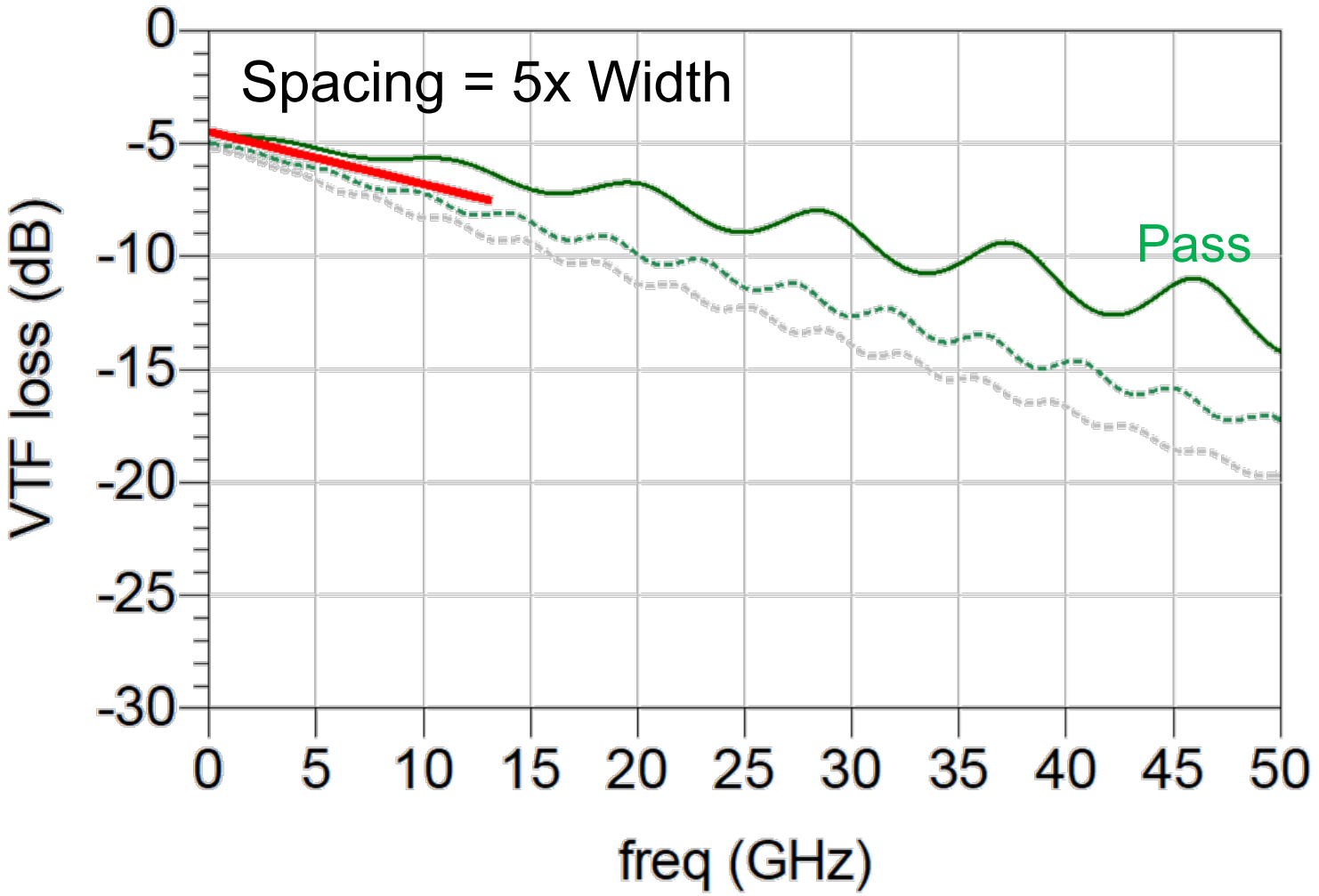
Spacing = 5x trace width



Spacing/coupling does not impact loss in general, but the impact of coupling shows up at higher frequencies.

Shorted the Length to Reduce the Loss and Pass the Line

For the current material configuration, we can only afford a short-reach channel.

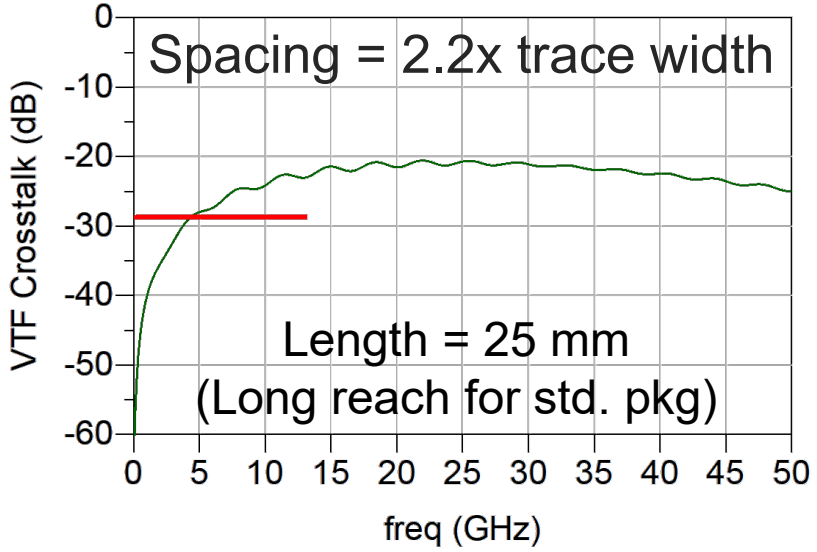


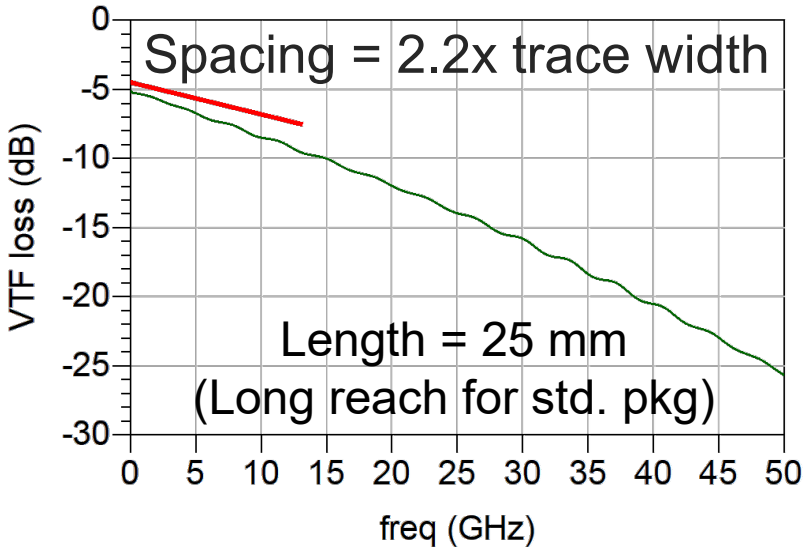
(Short reach for std. pkg)
Length = 10 mm

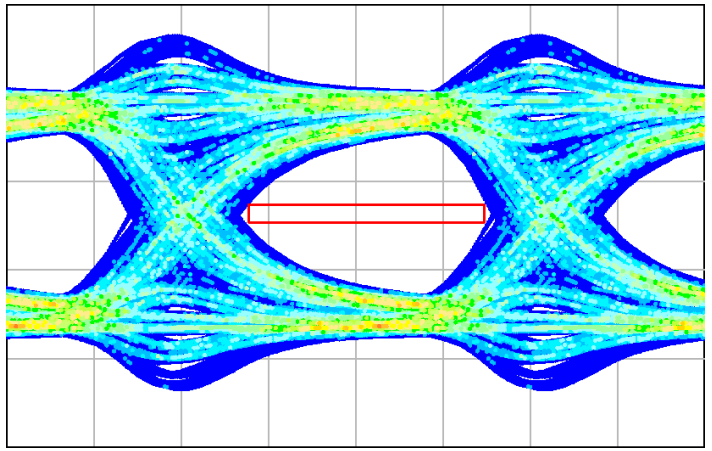
Length = 20 mm

Length = 25 mm
(Long reach for std. pkg)

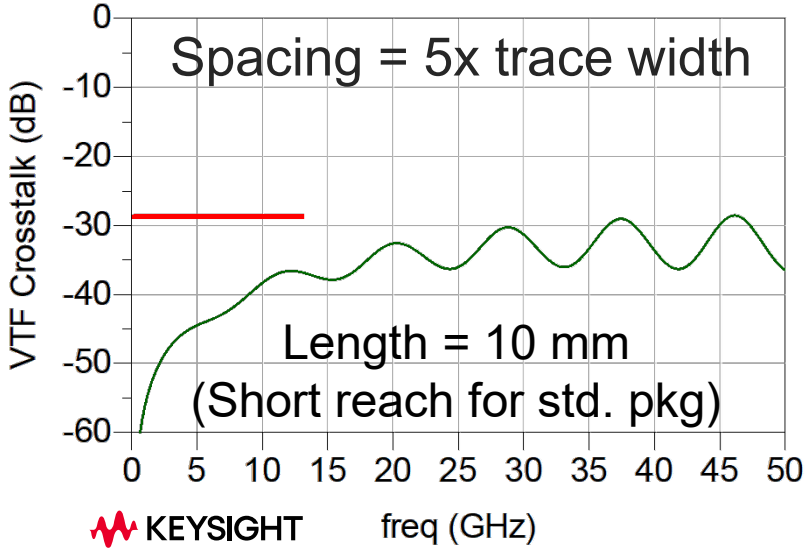
Fixing the Root Cause to Open the Eye

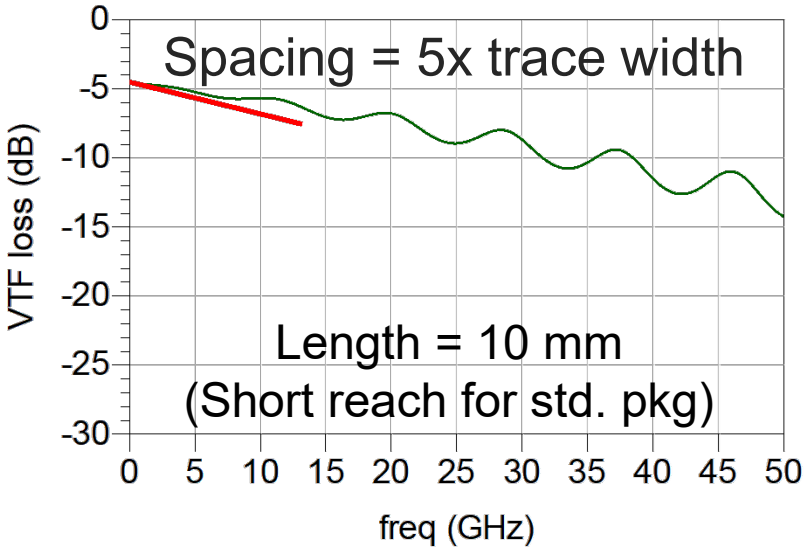


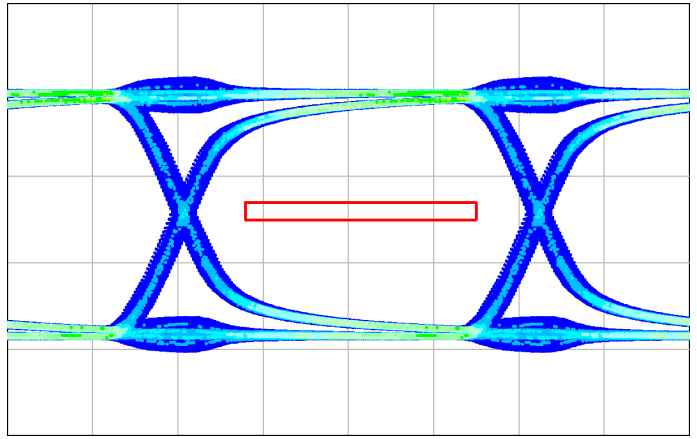




The eye is open after we reduced the root causes, the coupling and loss.





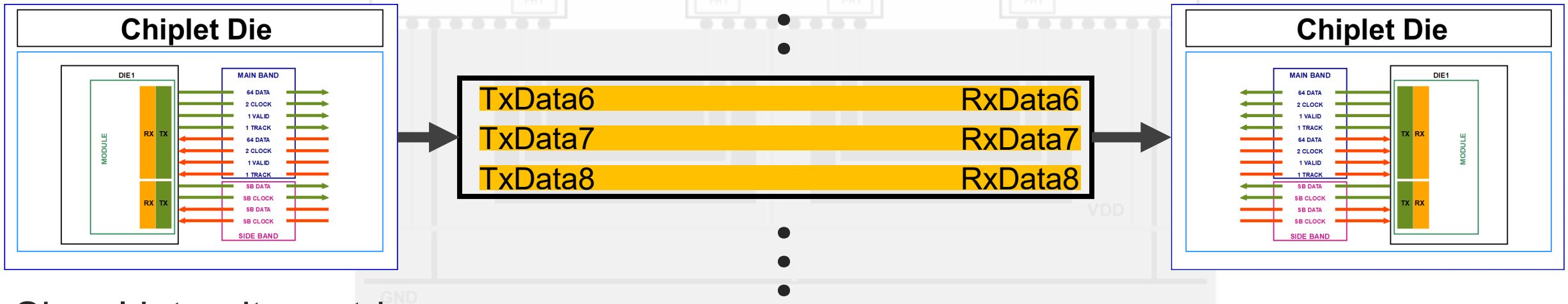


Complete the Signal Integrity Journey

Standard Package
Data rate: 24 GT/s

20 transmission lines

Rx Termination
50 Ω



Signal integrity metrics
- Tx Eye diagrams

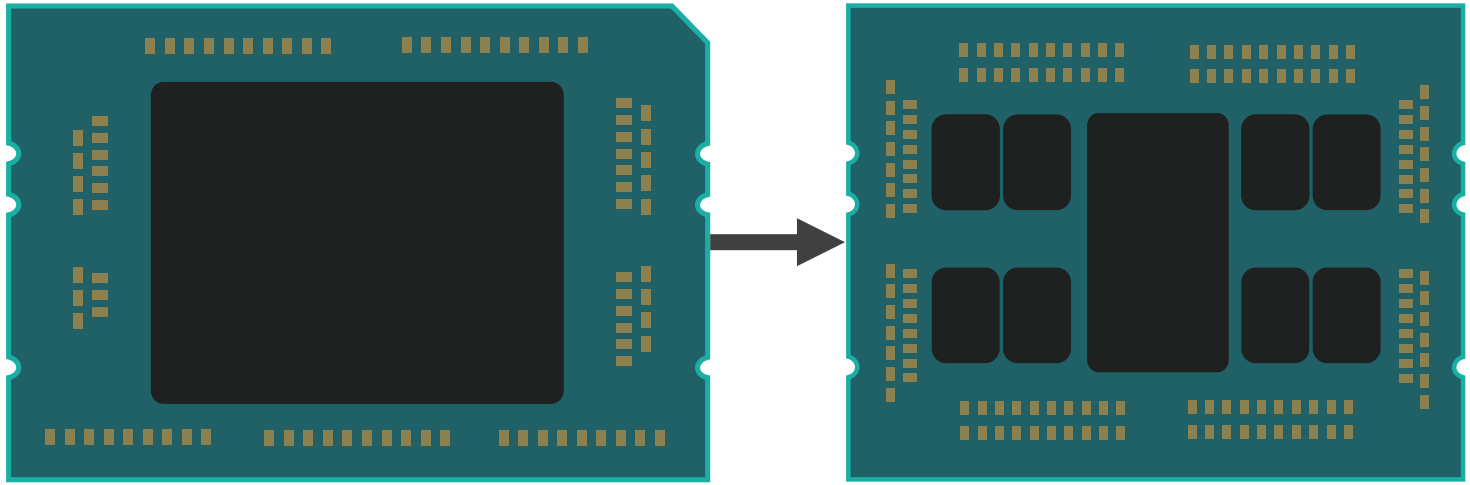
Signal integrity metrics
- VTF loss
- VTF crosstalk

Signal integrity metrics
- Rx Eye diagrams

Chiplet and UCIe Standard Quick Recap

Monolithic Die Designs

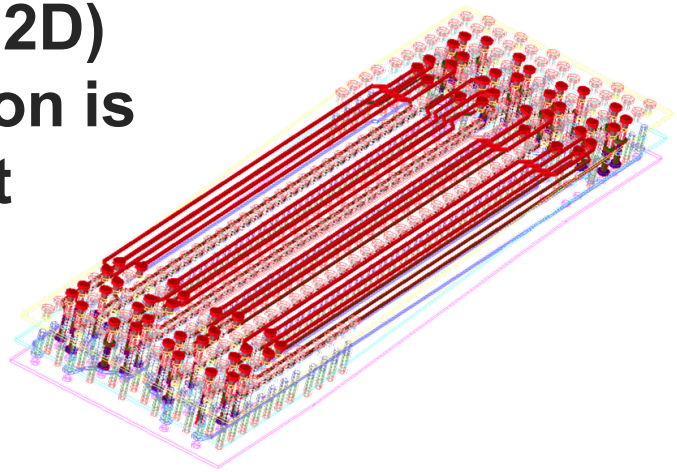
Chiplet Designs



Chiplet Design Philosophy

- Maximizes wafer usage
- Has a higher yield
- Has a lower cost
- Easy to scale!

Die-to-die (D2D) communication is important

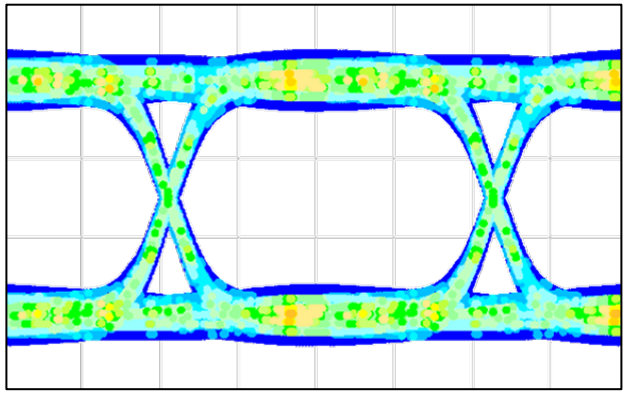


Standards to facilitate the adoption

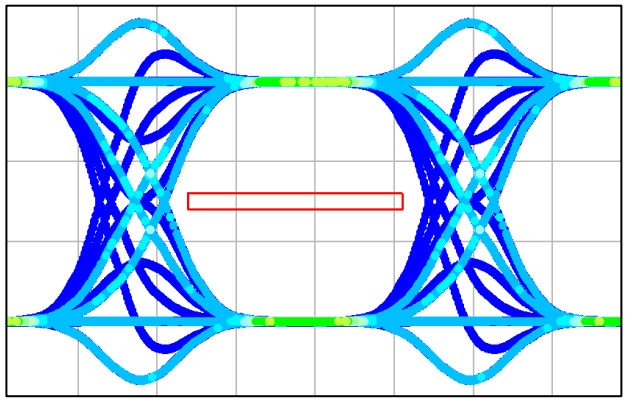
UCIe™
Universal Chiplet Interconnect Express

Signal Integrity Insights Summary

Rule number 9 [3]: Anticipate Before You Measure or Simulate

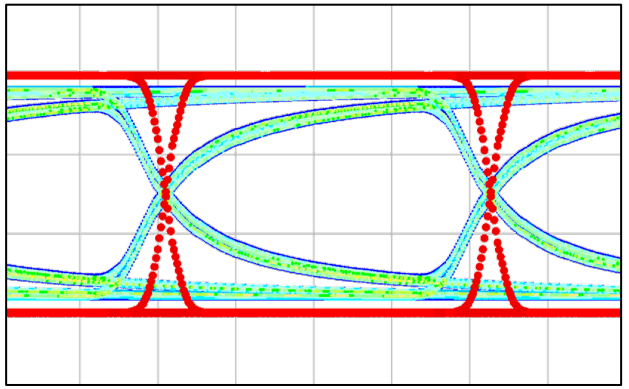


Near-end crosstalk



Far-end crosstalk

Increase spacing to more than 3-5 times of trace width to reduce coupling.



Frequency-dependent loss

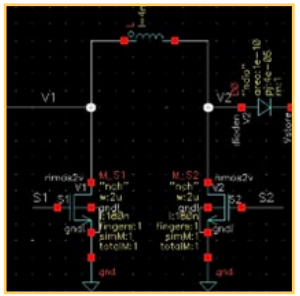
Reduce channel length to reduce loss

It's best to find the root cause to fix the problem!

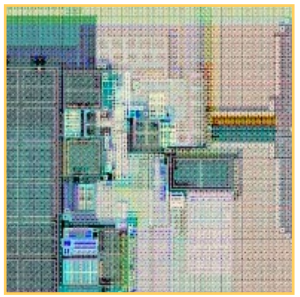
Navigate Chiplet Design Simulation Complexities

EDA is important in the design cycle to help predict the final chiplet performance

Schematic

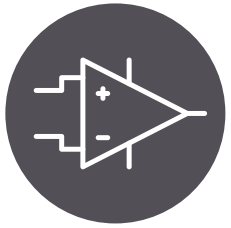


Layout

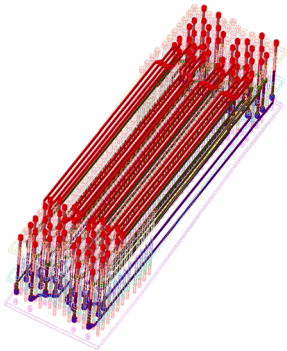


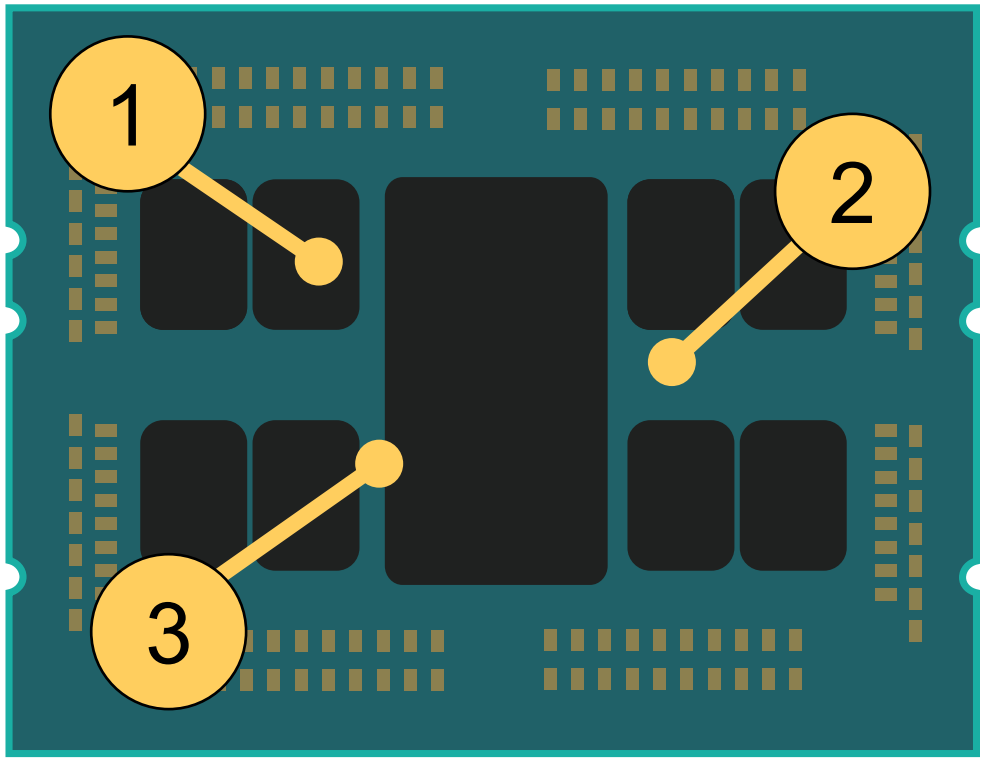
Circuit

System



Layout





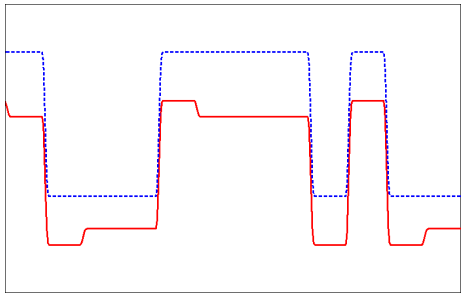
- Design with chiplet standard in mind
- Exercise modular design approach
- Perform complete link verification

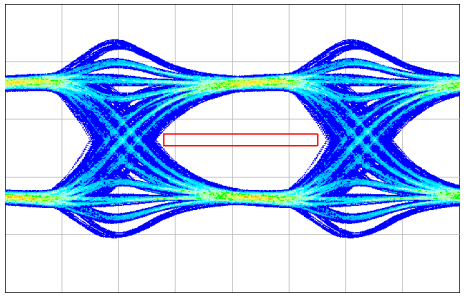
Key Attributes to a Chiplet D2D Comm. SI Analysis Software

UCIe™ Universal Chiplet Interconnect Express

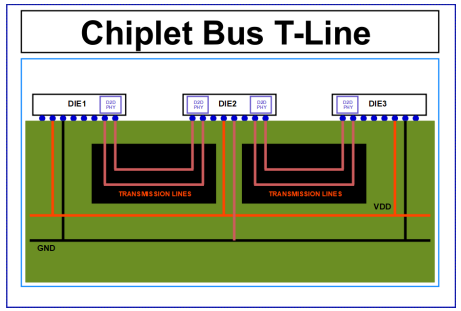
Standard-focused
Let the software work for you

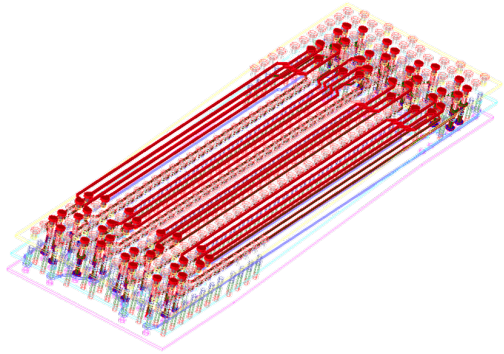
Tx and Rx Termination and Equalization
Explore possible design and solution space



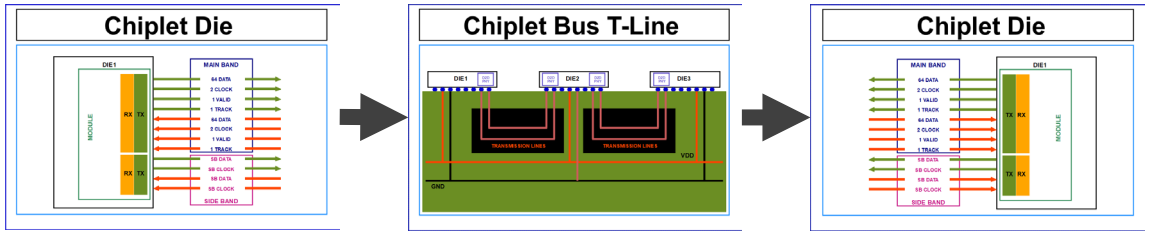


Die-to-Die Interconnect Extraction and Modeling
Understand design space and validate design choices

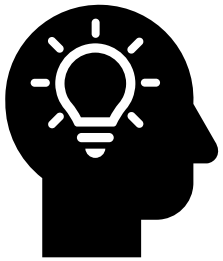




Die-to-Die Channel Link
Identify problem early, reproduce existing problem



Usability and Integration
Don't work for the computer



KEYSIGHT

FMS

KEYSIGHT FMS

Thank you

References

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