UCIe Update

Universal Chiplet Interconnect Express™ (UCIe™)
An Open Standard for Chiplet Development

- UCIe Guiding Principles
  - Open chiplet ecosystem
  - Backward-compatible evolution to ensure investment protection
  - Optimized power, performance, and cost metrics applicable across the entire compute continuum
  - Continuously innovate to meet the needs of the evolving ecosystem

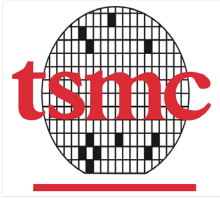
Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.

High-bandwidth, Low-latency, Power-efficient, Cost-effective Interconnects for
AI, HPC, Cloud, Edge, Enterprise, 5G, Automotive, Handhelds

UCIe™
Universal Chiplet Interconnect Express

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive the open chiplet ecosystem.



140+ Member Companies…and growing!

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140+ Member Companies

Achronix Semiconductor Corp

Advanced Micro Devices

Advanced Semiconductor Engineering, Inc.

Advantest America, Inc.

Akrostar Technology Co., Ltd

Alchip Technologies, Ltd. Taiwan Branch

Alibaba Inc.

Alphawave Semi

Amkor Technology, Inc.

Ampere Computing

Analog Devices Incorporated

AP Memory Technology Corporation

Applied Materials, Inc.

Arm Limited

Arteris, Inc.

ASMedia Technology Inc.

Astera Labs

Atron (Chongqing) Technologies, Limited

Ayar Labs

Beijing Henghuizhixun Technology Co., Ltd.

Blue Cheetah Analog Design Inc.

BMW of North America LLC

Broadcom Inc.

Cadence Design Systems Inc.

Ceremorphic, Inc.

ChangXin Memory Technologies, Inc.

Ciena Corporation

CoMira Solutions Inc

Credo Semiconductor, Inc

Deca Technologies, Inc.

DENSO Corporation

d-Matrix

Douyin Vision Co., Ltd

Dream Chip Technologies GmbH

DreamBig Semiconductor Inc.

ECARX Limited

Egis Technology Inc.

e-Infochips Inc (An Arrow Company)

Eliyan Corp.

Ericsson AB

eTopus Technology Inc.

EVAS Intelligence Co., Ltd.

EXTOLL GmbH

ForwardEdge ASIC

FuriosaAi

Futurewei Technologies, Inc.

Global Unichip Corporation (GUC)

GlobalFoundries U.S. Inc.

GM Global Technology Operations LLC

Google

HANA Micron, Inc.

Honda Motor Co., Ltd.

Huixi Technology Co. Ltd (Rhino Auto)

IBM

Imec vzw

Infineon Technologies AG

InfiniLink Inc.

Innosilicon Microelectronics (Wuhan) Co. LTD.

Inpsytech,Inc.

Intel Corporation

JCET Group Co., Ltd.

Kandou Bus SA

Keysight Technologies

Kiwimoore (Shanghai) Semiconductor Co., Ltd_

KNiulink Semiconductor Ltd.

Kyocera-AVX

LG Electronics

Lightmatter

M SQUARE Ltd. Shanghai

M2 Semiconductor Ltd.

Macronix International Co., Ltd

Marvell Asia PTE Ltd

MediaTek Inc.

Mercedes-Benz Research & Development North America, Inc.

Meta Platforms, Inc.

Microchip Technology Inc.

Micron Technology Inc

Microsoft

MIPS Tech LLC

MIRISE Technologies Corporation

Mixel, Inc.

MosChip Technologies

National Institute of Advanced Industrial Science and Technology

nepes Corporation

Neuchips Inc.

Neuron IP Inc

NHanced Semiconductors, Inc.

Nippon Telegraph and Telephone Corporation

Nissan Motor Co., Ltd.

Nokia Solutions and Networks Oy

Nuclei System Technology Co., Ltd

NVIDIA

OPENEDGES Technology. Inc.

Physim Electronics Technology Co., LTD

Powerchip Semiconductor Manufacturing Corp (PSMC)

proteanTecs, LTD.

Qualcomm, Inc.

Qualitas Semiconductor

Rapidus Corporation

Rebellions

Renesas Electronics Corporation

Robert Bosch GmbH

Rohde & Schwarz GmbH & Co. KG

Samsung Electronics Co, Ltd.

Sanechips Technology Co., LTD

Semitronix Corporation

Shanghai UniVista Industrial Software Group Co., Ltd.

Shanghai Zhaoxin Semiconductor Co., Ltd.

Shinko Electric Industries Co., LTD.

Siemens Industry Software Inc.

SiliconAuto B.V.

Siliconware Precision Industries Co. Ltd.

SK Hynix Inc.

SkyeChip

SmartDV Technologies

Socionext Inc.

Synopsys Inc

Taiwan Semiconductor Manufacturing Co., Ltd.

Tektronix Inc

Tenstorrent Inc.

Teradyne, inc.

Texas Institute for Electronics, The University of Texas at Austin

Texas Instruments Incorporated

The MathWorks, Inc.

Thine Electronics, Inc.

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Toyota Motor Corporation

Truechip Solutions PVT LTD

Tsavorite Scalable Intelligence, Inc

Unisoc (Shanghai) Technologies Co., Ltd

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Untether AI

Valens Semiconductor

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VIA NEXT Technologies, Inc.

Volkswagen Aktiengesellschaft

Winbond Electronics Corporation

xFusion Digital Technologies Co., Ltd

Xi'an UniIC Semiconductors Co.,Ltd.

Xpeedic Co., Ltd.

Xsight Labs Ltd.

Zero ASIC Corporation

Zhejiang Zentel Memory Technology Co., Ltd.

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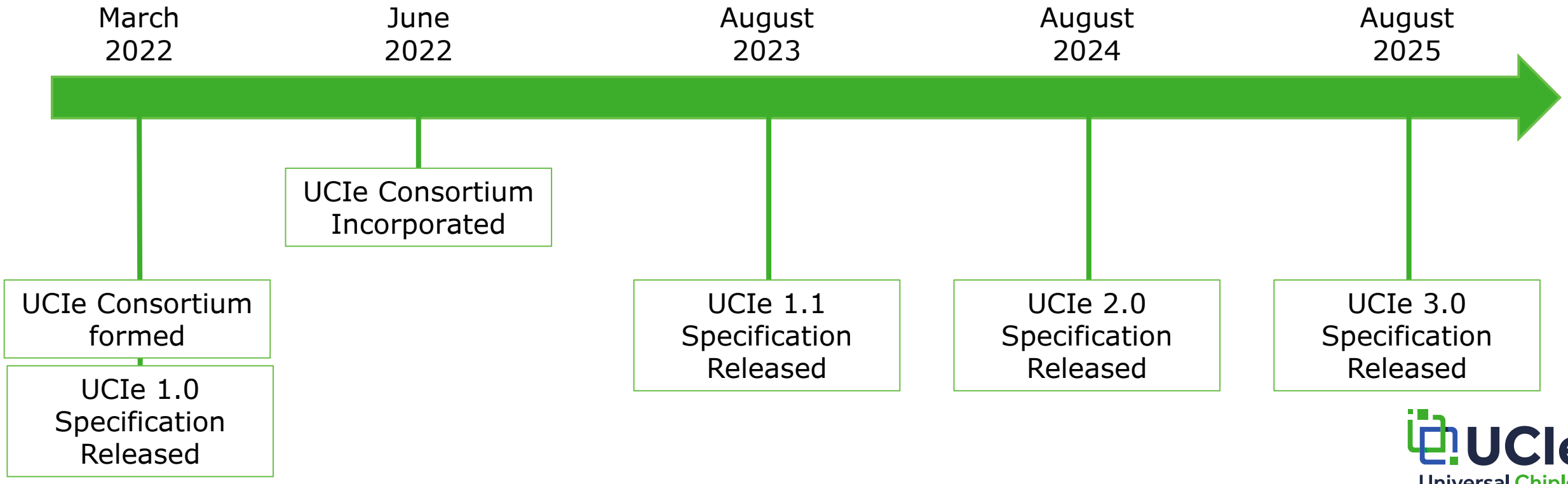
Member-Driven Evolution



UCIe™ Universal Chiplet Interconnect Express

UCIe 3.0 Specification Feature Overview

- **Higher bandwidth density:** 48 GT/s and 64 GT/s for UCIe-S and UCIe-A
  - Doubling the data rate to power next-gen multi-chip systems such as AI and HPC while maintaining low power.
- **New Usages:** Added support for continuous transmission protocols
  - Enables uninterrupted data flow in Raw Mode for new applications such as connectivity between SoC and DSP chiplets.
- **Power Savings:** Runtime recalibration and L2 Optimization
  - Enable power-efficient link tuning during operation by reusing initialization states.
  - Reduces Idle Power on the sideband.
- **Manageability Infrastructure Enhancements:** Future standardization efforts
  - Enhancements for Early Firmware Download, Sideband Priority Packets, Extending Sideband Reach, Open Drain Pin, and Fast Throttle/Shutdown.

UCIe™ Universal Chiplet Interconnect Express

Doubling Data Rates for UCIe-A and UCIe-S

- **Motivation:** Continued demand for higher linear bandwidth density for SoCs used in applications such as AI, HPC, etc., with shore-line constraints
- **Solution:** Increase the data rate from maximum 32 GT/s to 48 and 64 GT/s
- **UCIe's Approach:**
  - Full backwards compatibility – same sideband, valid, track, data, training, etc.
  - Signaling: NRZ Uni-directional
  - Clocking: Quarter rate for 48/64 GT/s; free running
  - BER: 10^{-15} for 48 GT/s and 10^{-12} for 64 GT/s
  - Termination: RX Termination required for both UCIe-S and UCIe-A
  - Enhanced Equalization: 3-tap TX FFE (1-pre + 1-post); 1st order (passive) RX CTLE : can possibly be combined with T-coil network; Optional 1-tap RX DFE
  - B/W Density target: 1.7-2x linear, 1.3-1.6x areal.
  - Power Target: 0.5-0.75pJ/b
    - Breakdown: ~ 40% TX, 40% RX, 20% common circuits
- **Result:** Linear B/W Density increases 1.65x/2x for UCIe-S/UCIe-A with similar power efficiency

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Key Metrics with UCIe 3.0

Characteristics / KPIs	UCIe-S (2D)	UCIe-A (2.5D)	UCIe 3D	Comments
Characteristics				
Data Rate (GT/s)	4, 8, 12, 16, 24, 32, 48, 64		Up to 4	UCIe 3D SoC Logic frequency – power efficiency is critical Added 48G and 64G with UCIe 3.0
Width (each cluster)	16	64	80	UCIe 3D: Options or reduced width to 70, 60…
Bump Pitch (µm)	100 – 130	25 – 55	≤ 10 (optimized) > 10 – 25 (functional)	Must scale so that UCIe fits within the bump area, UCIe-3D must support hybrid bonding
Channel Reach (mm)	≤ 25	≤ 2	3D vertical	UCIe-3D: FtF, FtB, BtB, multi-stack possible
Target for Key Metrics				
BW Shoreline (GB/s/mm)	28 – 224 278, 370	165 – 1317 1975, 2634	N/A (vertical)	For UCIe-S and UCIe-A: First row is for 4-32G. Second Row is for 48G and 64G respectively
BW Density (GB/s/mm^2)	22 – 125 144,192	188 – 1350 1235, 1646	4,000 (9µm) – 300,000 (1µm)	For UCIe-S and UCIe-A: First row is for 4-32G. Second Row is for 48G and 64G respectively
Power Efficiency Target (pJ/b)	0.5 (<=16 G) 0.75 (>= 32 G)	0.25 (<=12G) 0.3 (16G – 32G) 0.5 (>= 48G)	<0.05 at 9µm -> 0.01 at 1 µm	
Low-Power Entry/Exit	0.5nS ≤ 16G, 0.5-1nS ≥ 24G		0nS	No preamble or post-amble
Reliability (FIT)	0 < FIT (Failure in Time) << 1		0 < FIT << 1	
ESD	30V CDM		5V CDM → ≤ 3V	UCIe-3D: 5V CDM at introduction, no ESD for W2W hybrid bonding possible

UCIe continues to deliver compelling power-efficient and cost-effective performance

Optimized Manageability Framework

- **Early Firmware Download**
  - **Function:** Standardize data structures and capabilities for firmware download
  - **Benefit:** Enable chiplet use of firmware without each chiplet in SiP needing its own flash or firmware loading mechanisms
- **Priority Packets Over Sideband**
  - **Function:** Permit low-latency (bounded) transmission of sideband messages for notification events
  - **Benefit:** High-priority events are not blocked by low-priority traffic
- **Extended Reach Sideband (UCIe-S only)**
  - **Function:** Permit 100mm sideband channel to minimize hops/daisy chaining SiP
  - **Benefit:** Enables star topology with sideband – director chiplet connected to each chiplet
- **Open Drain Pins**
  - **Function:** Open Drain Pins enable low latency, bi-directional events
  - **Benefit:** Simultaneous SiP wide broadcast to all chiplets
- **Fast Throttle and Emergency Shutdown**
  - **Function:** Setup open drain IO and map critical notification events as potential broadcast in System-in-Package (SiP)
  - **Benefit:** Provides a standard approach across chiplet vendors to ensure critical function interoperability at the SiP level

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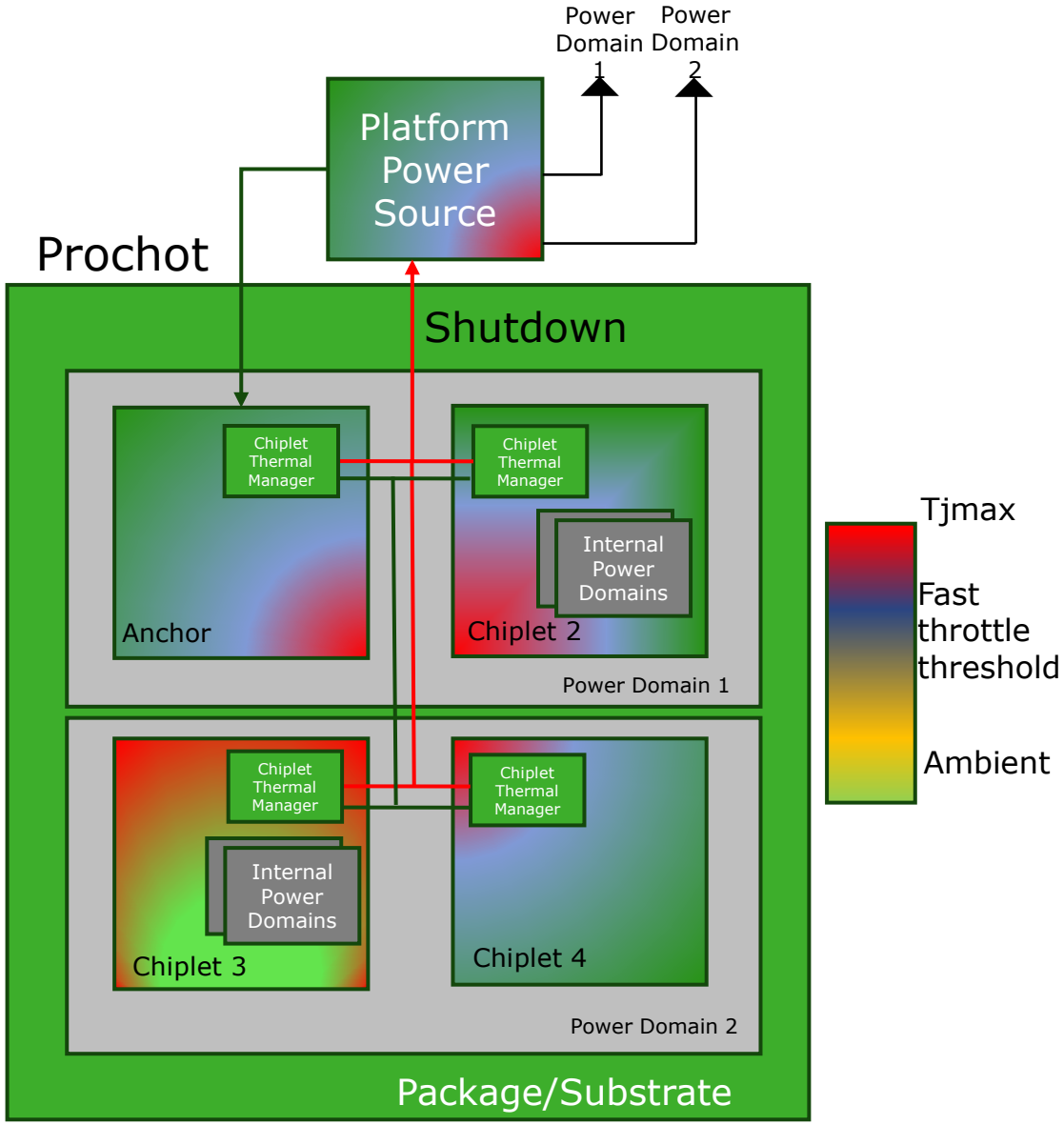
UCIe 3.0 Solution



- Fast throttle
  - Introduce a common dedicated open drain bidirectional pin on the chiplets
  - Wires from all chiplets participating in a thermal zone are tied together, such that any combination of chiplets can pull down the pin
  - Chiplet(s) assert the pin when the respective internal fail-safe temperature limit is hit or if signaled from the external platform running hot.
  - When asserted, all participating chiplets throttle to the pre-negotiated level and at a defined rate
- Emergency Shutdown
  - Introduce a dedicated open drain bidirectional pin on the chiplets and an off-package driver
  - Wires from all chiplets participating in a thermal zone are tied together, such that either one can pull down the pin
  - Chiplet(s) assert the pin when their max temp limit is hit.
  - SiP exposes the shutdown to internal (through the directional nature of this communication) and external power source i.e., off-package driver for shutdown

UCIe™ Universal Chiplet Interconnect Express

Summary

- The UCIe Consortium is committed to establishing an open chiplet ecosystem and a ubiquitous interconnect at the package level.

- The UCIe specification is continuing to evolve, based on end-user feedback, to meet the new usage models.

- **Get involved!** Learn more by visiting www.UCIexpress.org

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Thank You

www.UCIexpress.org