UCIe Chiplet Ecosystem: Interoperable Testbench for Multi-Vendor IP Integration

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Background : Chiplet Ecosystem

❑ Current State of Chiplet Marketplace

- Market for chiplets is growing rapidly
- Increased enthusiasm for creating an “open chiplet economy”
- Open chiplet interconnect standards gaining traction – UCIe, BoW (little less though)
- Broad range of applications for chiplets

❑ Challenges

- No interop labs (i.e., Plug fest) for chiplets

→ High tape-out risk for chiplet designs

Call to Action

❑ What?

- Demonstrate interoperability between two UCIe chiplet implementations from independent vendors using Siemens Avery UCIe Verification IP in a simulation environment
- Leverage Siemens UCIe Compliance Testsuite to demonstrate UCIe 3.0 spec compliance

❑ Why?

- Create a model for collaboration/partnership between chiplet vendors and EDA
- Enable shift left strategy for early detection of design flaws
- Increase vendor confidence in chiplet implementations
- Accelerate adoption of chiplet standards such as UCIe
- Contribute to long-term objective of creating an Open Chiplet Ecosystem

Pilot Project: UCIe Interoperability and Compliance

Alphawave Semi – UCIe-based IO Chiplet
Ayar Labs – UCIe-based Optical Retimer Chiplet
Siemens EDA* – Avery UCIe Verification IP, Testbench development, Compliance Testsuite

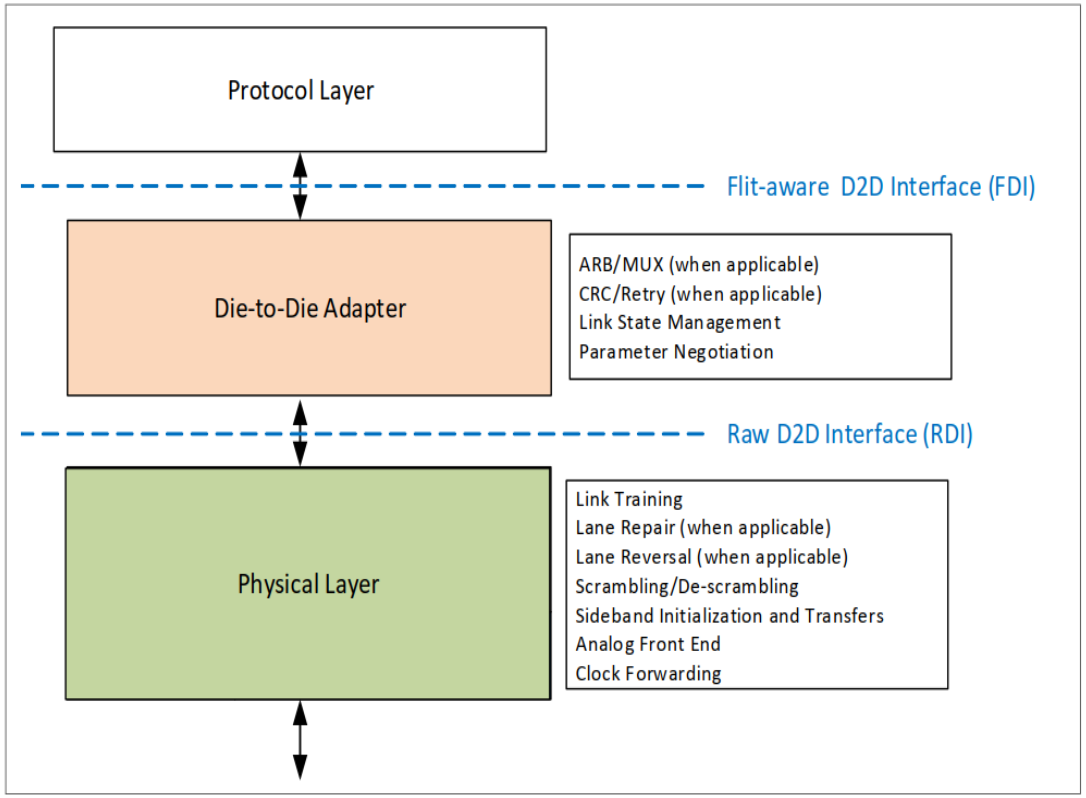
*Siemens as independent 3rd party and owner of the “Golden Reference” testbench

Project Objectives

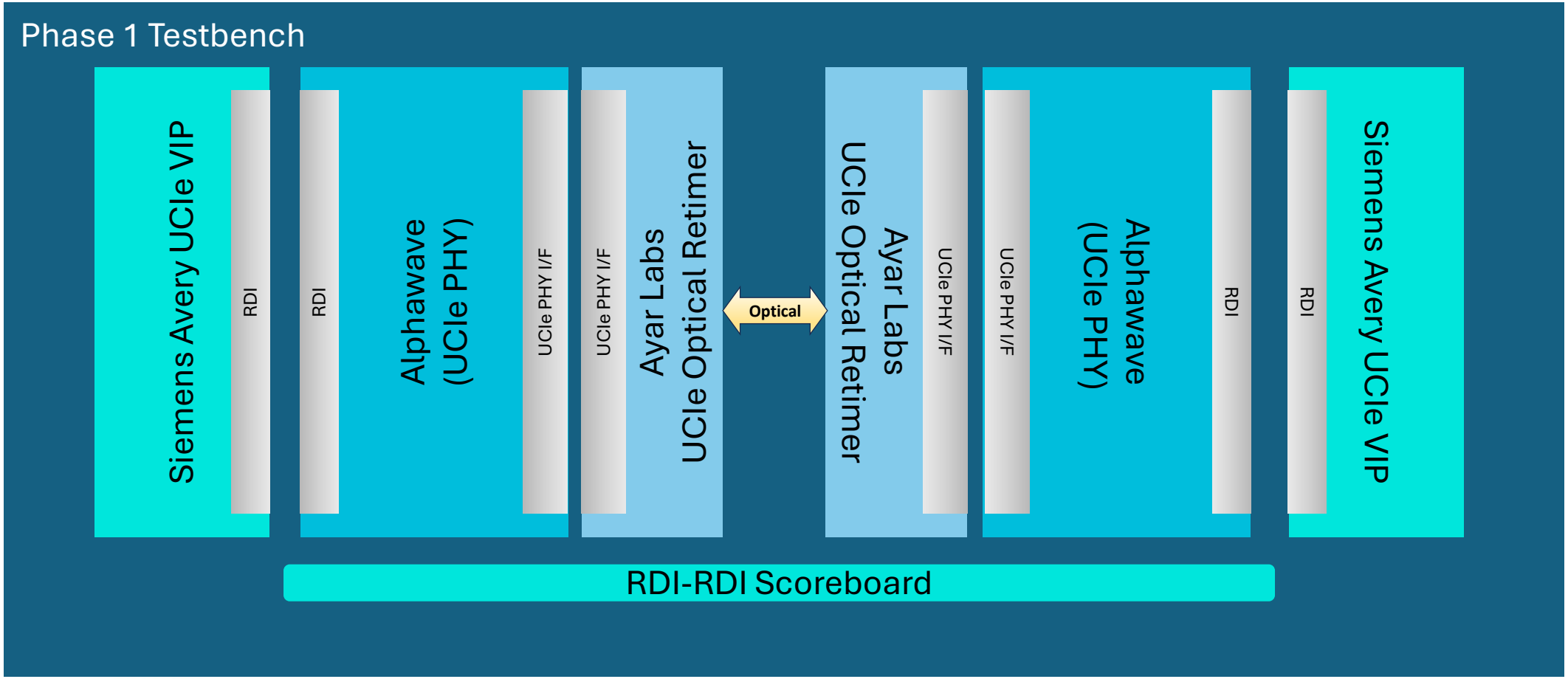
- **Phase 1** – PHY (RDI-to-RDI) compatibility
- **Phase 2** – PHY+D2D (FDI-to-FDI) compatibility

- **Compliance Test Areas**
  - Interface connectivity/compliance
  - End-to-end data path integrity
  - Link Training State Machine (LTSM)
  - Supported protocols/formats
  - UCIe Config/Memory Access
  - Error handling/Retry
  - Latency/Performance monitoring
  - FDI/RDI Interface monitoring and analysis
  - Retimer crediting
  - Functional coverage metrics

Figure - UCIe Layers and Functionalities – *UCIe Consortium*



Simulation Environment



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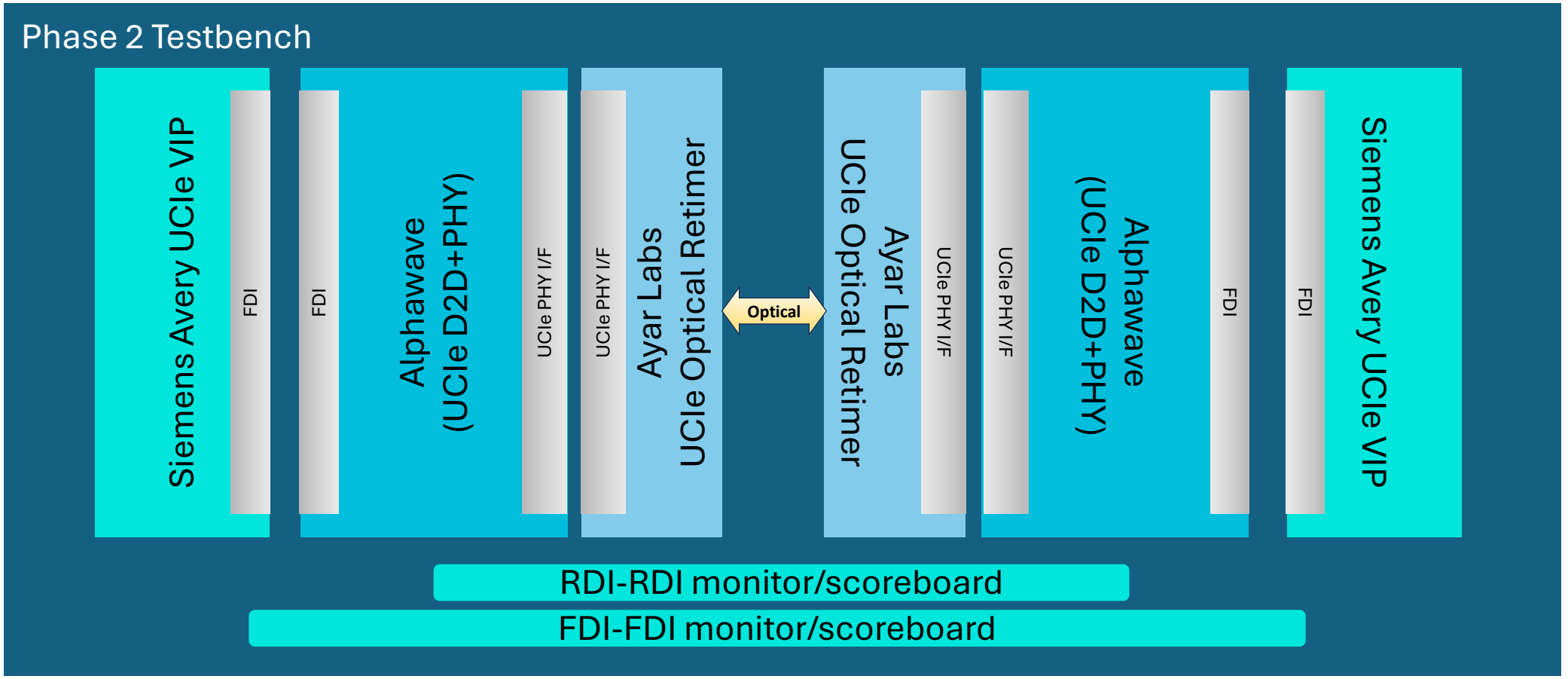

Challenges

❑ Technical

- Resolving differences in spec interpretation
- Developing comprehensive interop/compliance test plan
- RTL/Firmware integration
- Retimer latency modeling

❑ Logistical

- IP readiness
- Protection of IP
- Support model / Issue ownership
- Project scope

Looking Ahead

- Capture lessons learned from this pilot project
- Seek opportunities to reproduce this simulation-based interop model with other chiplet vendors
- Already added the compliance testing for various Manageability features and expanding it further to add UCIe 3.0 features
- Incorporate Avery In-Circuit Simulation for early software modeling
- PCIe/CXL/CXS/AXI/CHI/C2C/JESD compliance testing over UCIe

Conclusion

- Development of an Open Chiplet Ecosystem will necessitate early cooperation between chiplet vendors to ensure robust product interoperability

- Early-stage simulation-based compliance / interoperability testing with the use of 3rd party verification IP can help reduce risk and accelerate the development of spec compliant chiplet designs

Thank You !

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