Perspectives on 3D AND-type Resistive-Gate RAM Development with QLC Capability

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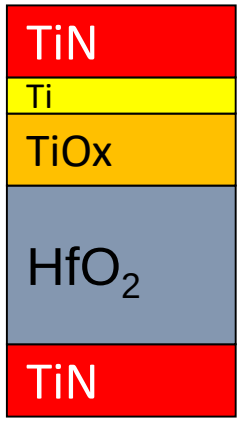
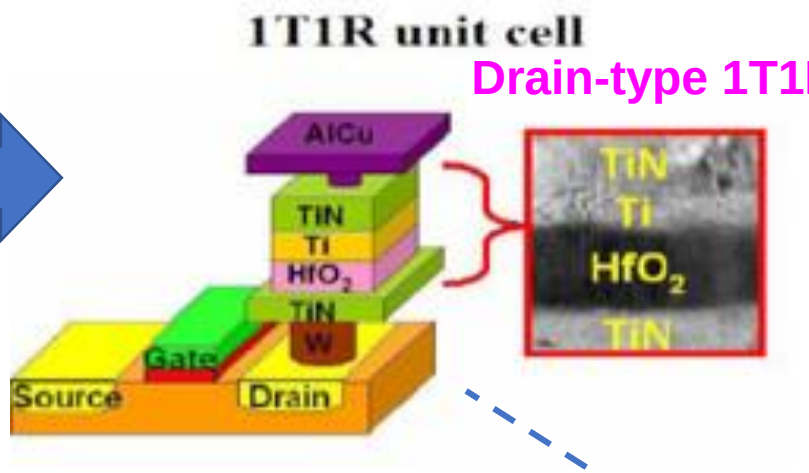
Early stage - Evolution of Resistance Memory Structures



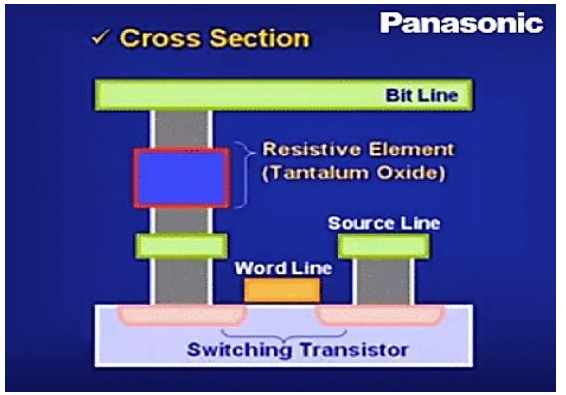
H. Y. Lee et al., IEDM, 2008

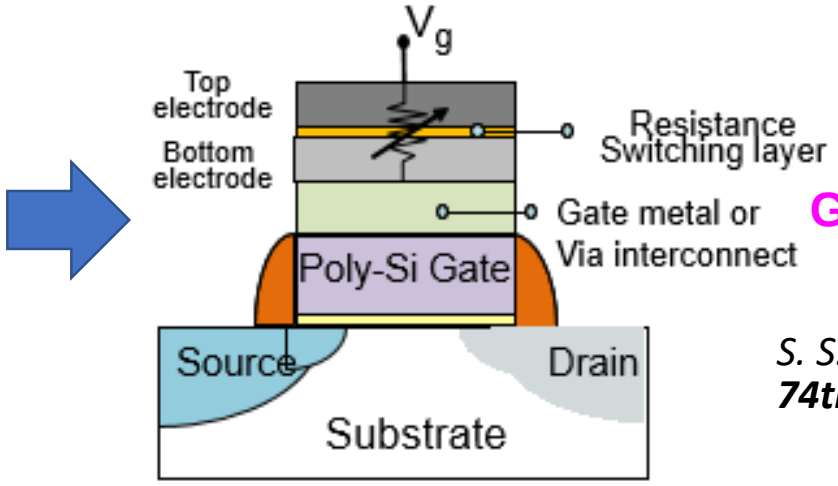


S. S. Sheu et al., VLSI, 2010

RRAM Embedded 8-bit MCU

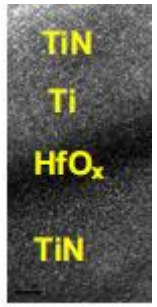
Panasonic, 2013

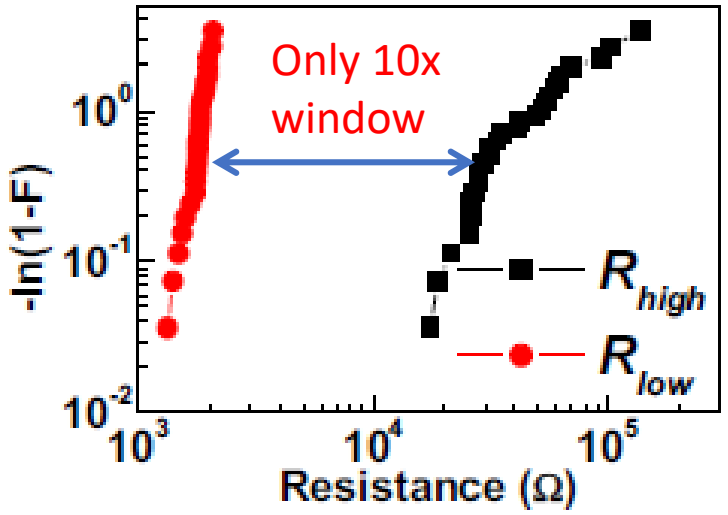




Gate-type 1T1R

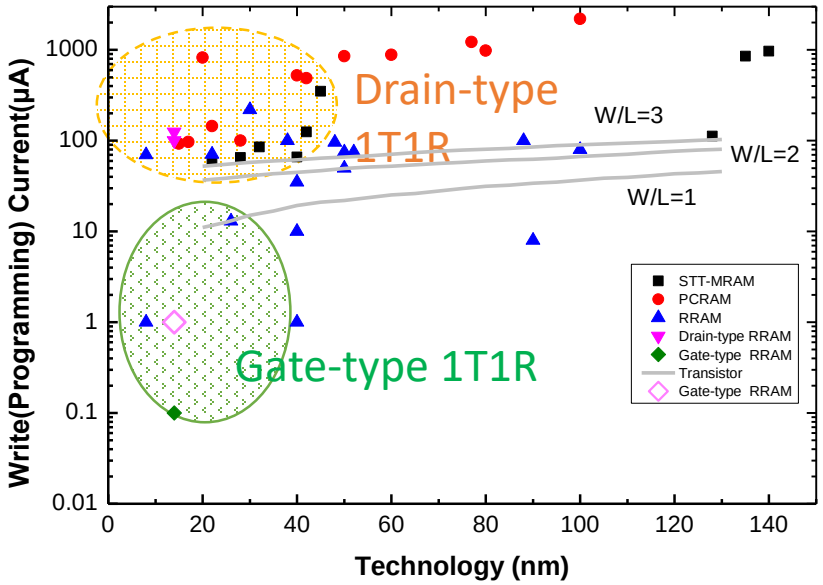
*S. S. Chung et al., **74th DRC**, 2016.*





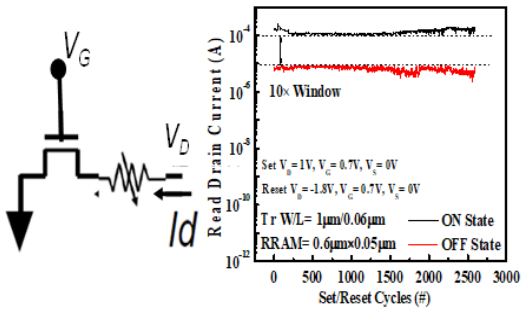
Motivation- 1T1R(gate-type) is more promising

- Conventional 1T1R (drain-type) has
  - ✓limited window (10x or larger)
  - ✓Multi-level operation becomes un-realistic,
- Major advantage of gate-type 1T1R
  - ✓Huge window
  - ✓Very low write current
  - ✓High density for both NOR/NAND

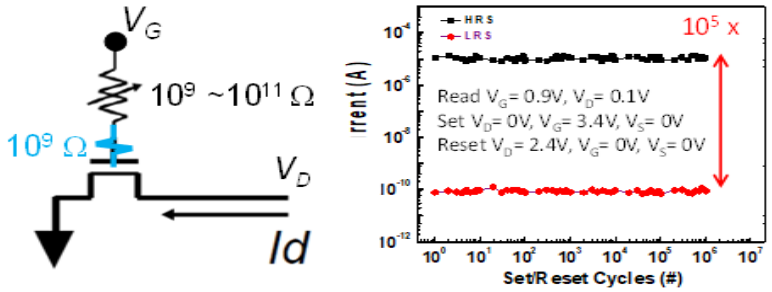


Modified from S. Yu, IEEE Solid-State Circuits Mag., 2016.

Drain-type 1T1R

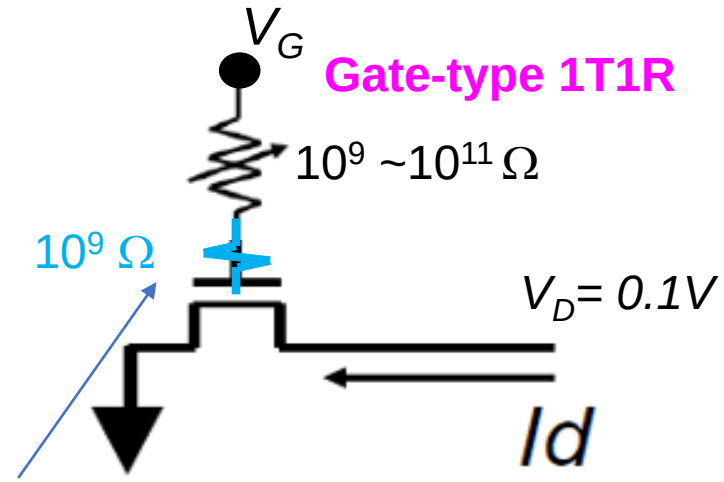


Gate-type 1T1R



Resistive-gate RAM: The Concept

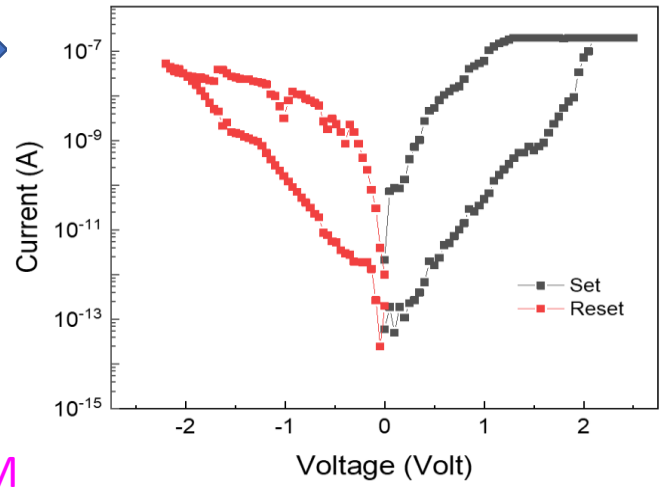
MIM resistance comparable to the FET's gate resistance is the key which enables the resistive switching.

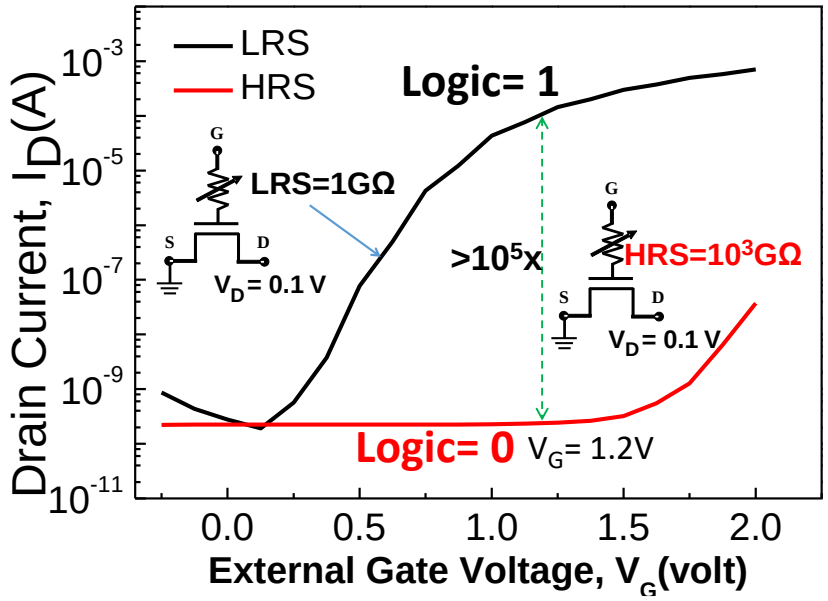


Gate internal resistance for 40nm and beyond

*Ref: S. S. Chung et al., **74th DRC**, pp. 251-252, June 19-22, 2016.*

Low current



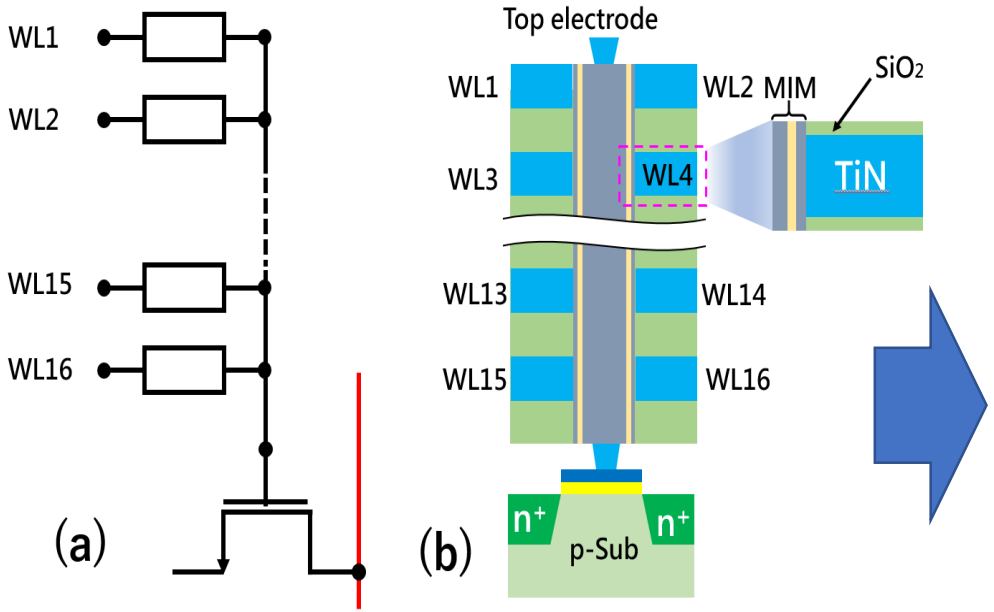


MIM

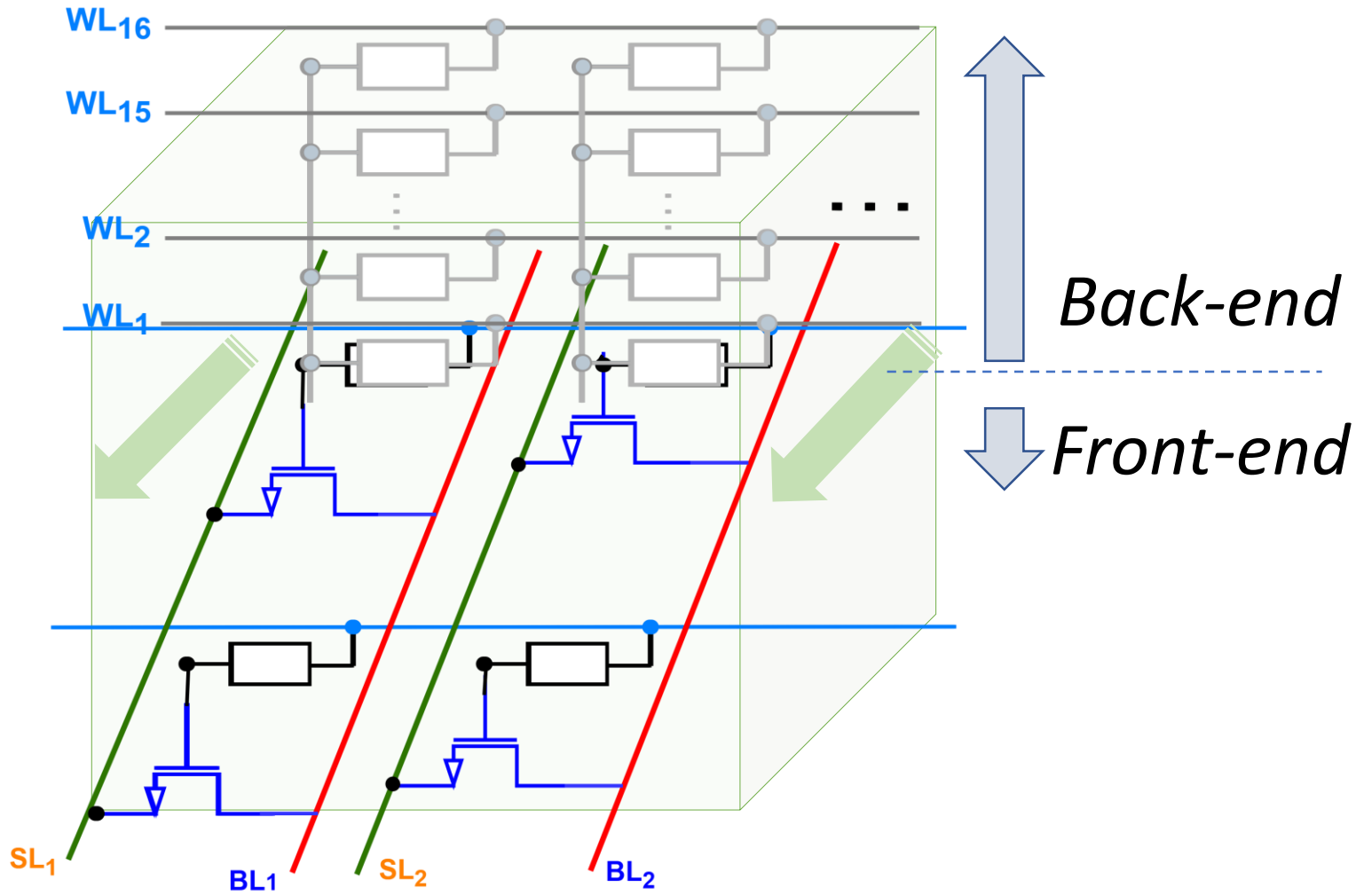
Forming Voltage	Forming-free
SET Voltage	2 V
RESET Voltage	-1.8 V
HRS	3×10^{11} Ω
LRS	2×10^9 Ω
ON/OFF Ratio	>800
Speed(SET/RESET)	10 ns / 4 ns

Resistive-gate RAM: 3D Architecture

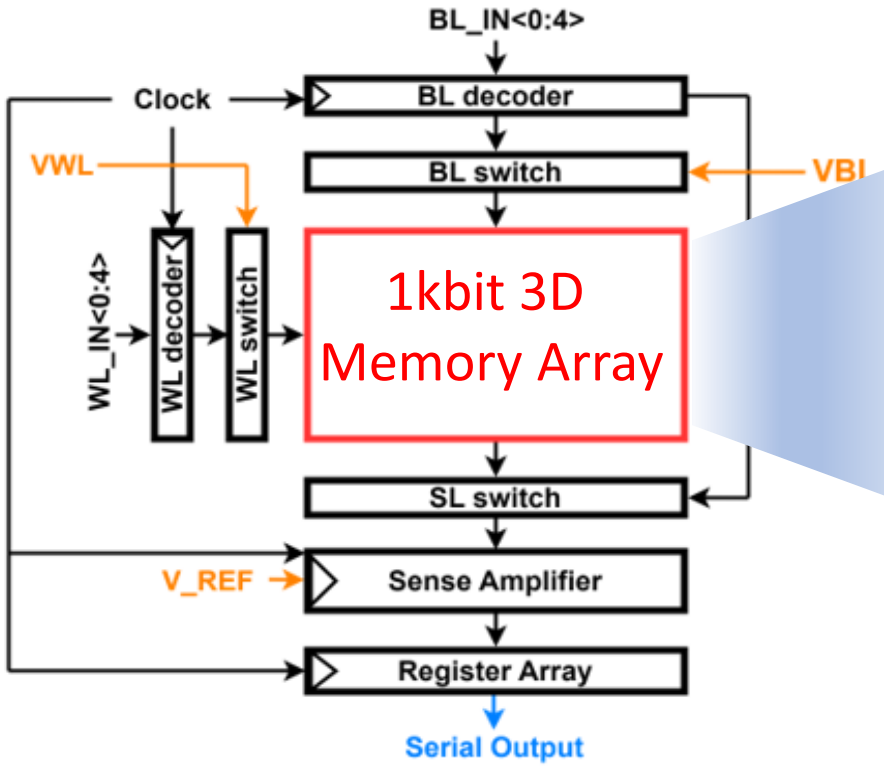
Stage 1: 1T1R extended to 1T16R(2D)



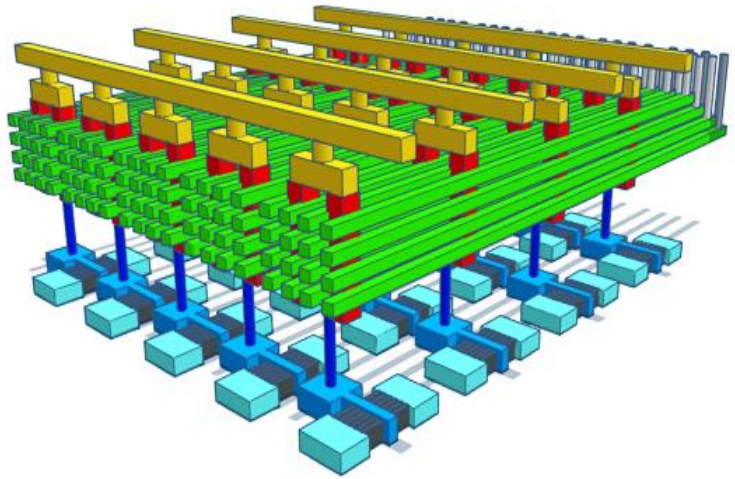
Stage 2: 1T16R into 3D (AND-architecture)



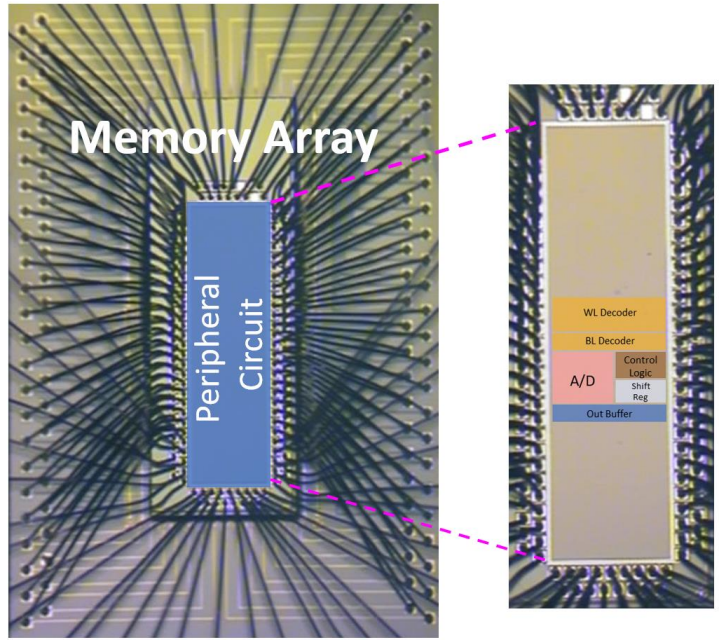
Design of Macro: 3D Memory Array



Functional block of Macro design

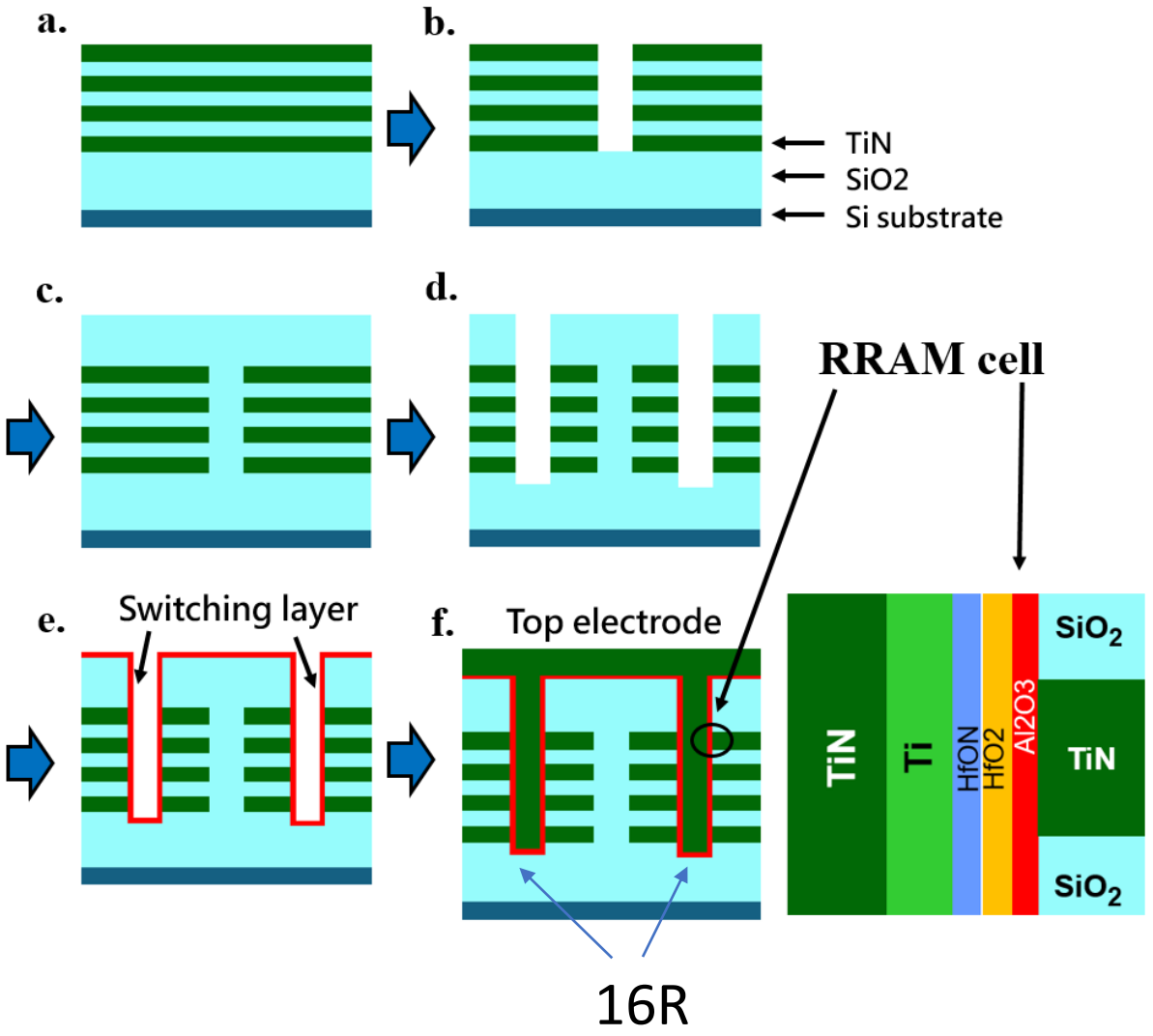


A 3D array built on tsmc 28nm Logic platform



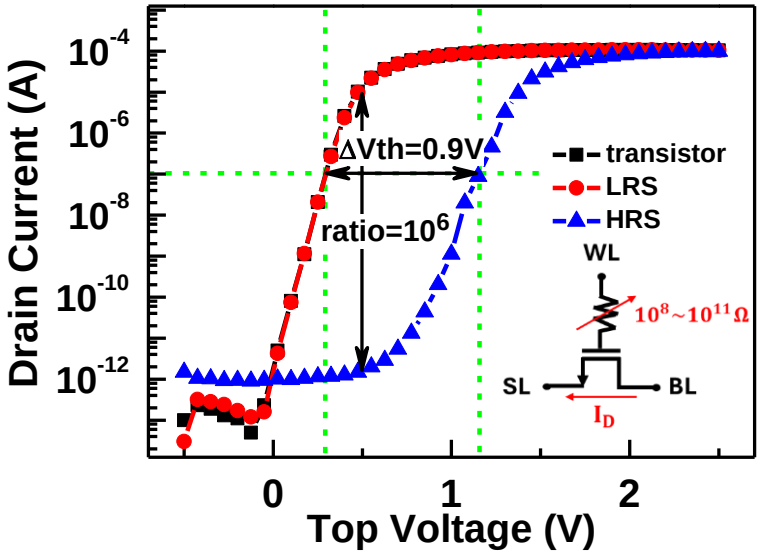
Integration of memory array and peripheral

The schematic of four-layer 3D vertical RRAM and fabrication flow

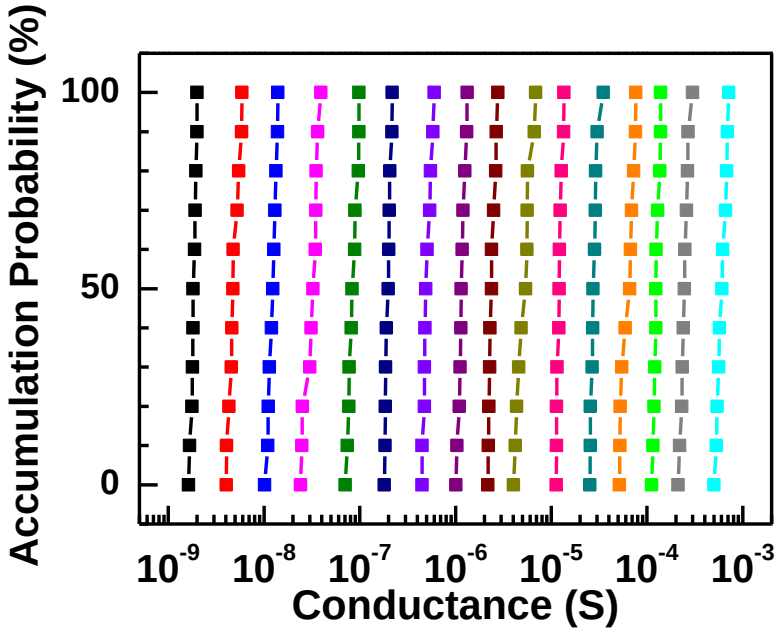


- SiO_2/TiN stacks deposition
- Spacer etch
- SiO_2 spacer deposition
- Plug etch
- ALD Al_2O_3 12Å
- RTA 350℃ 100sec
- ALD HfO_2 10Å
- ALD HfON 30Å
- PVD Ti 10nm
- PVD TiN top electrode
- RTA 300℃ 210sec

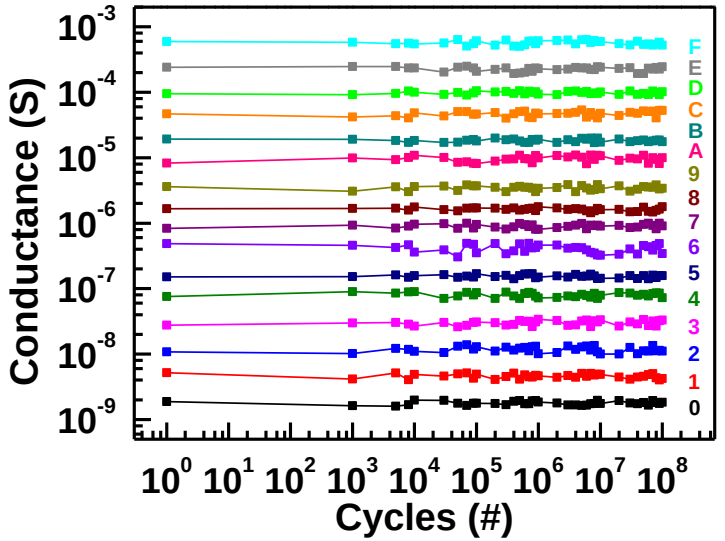
QLC: Realization of 4-bit-per-cell RG-RAM



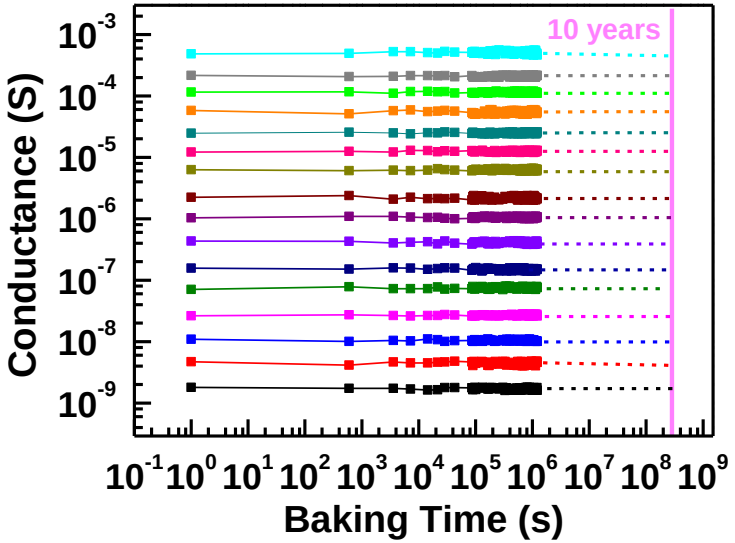
- A larger memory window up to 10^6x can be achieved.



- QLC operation



Endurance > 10^8 cycles



Retention > 10 years

The Comparison with the Floating-gate Memory

	This Work	[1]	[2]	[3]	[4]
Architecture	AND-type RG-RAM	NAND Flash	NAND Flash	NAND Flash	FE-NAND
Memory Window	ΔV_{th}=0.9 V $I_{max}/I_{min}=10^5$	N/A	9.8 V	N/A	1V
Program Time	Set : 30 ns Reset : 30 ns	8 us	1 s	2 ms	1 us
Program Voltage	3 V	24 V	15 V	N/A	3.5 V
Multi-Level	4 bits	3 bits	2 bits	4 bits	2 bits

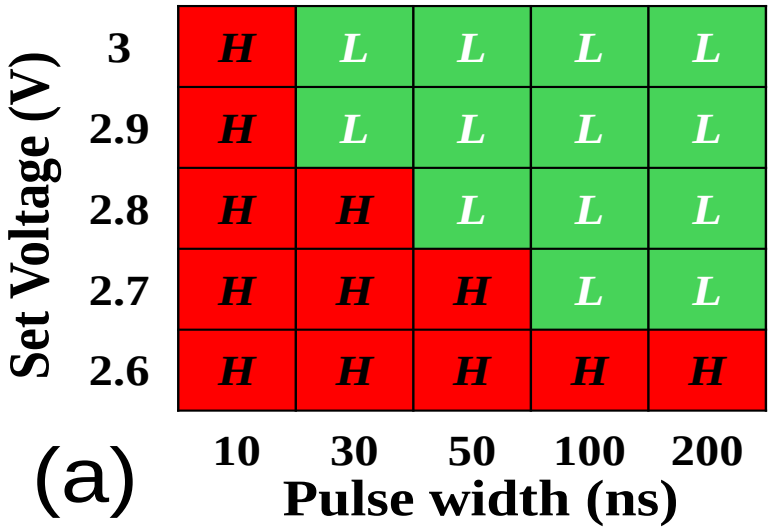
[1] D. Kang et al., ***IEEE ISSCC***, pp. 130-131, 2016. [2] J. Ko et al., ***IEEE ISCAS***, Montreal, Canada, pp. 1022-1025, 2016. [3] S. -H. Kuk et al., ***IEEE IMW***, Monterey, CA, pp. 1-4, 2023. [4] K. Banerjee et al., ***IEEE IMW***, Dresden, Germany, pp. 1-4, 2021.

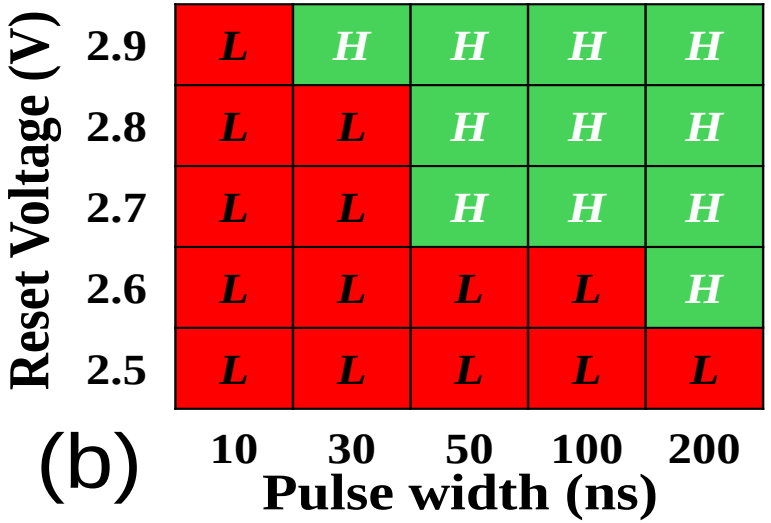
Summary and Conclusions

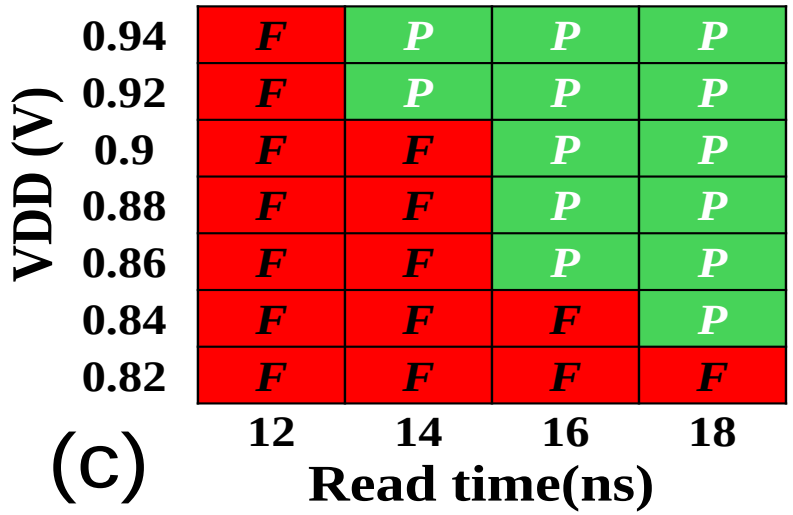
- Resistive-gate Memory (A good solution):
  - The innovation has the chance to replace Floating-gate flash.
  - Macro chip- demonstrating low power, TLC, QLC operations
  - No sneak path, wide window, disturb-free, excellent endurance/retention
- Applications
  - CPU, MCU, GPU for embedded flash; CIM etc.
- Perspectives
  - for embedded and stand-alone either in 2D or 3D architectures,
  - extendable down to FinFET (3nm), nanosheet generations (1nm).

Back-up

Shmoo plot of (a) SET, (b) RESET, and (c) READ operations







1kb RG-RAM chip	
Process	28nm HKMG
Memory Window	10^6x
PGM voltage	2.9V
PGM speed	30ns
Read voltage	0.92V
Endurance	10^8
Retention	>10^6sec@125℃

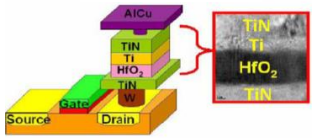
The READ operation can be completed at 0.92V within 14ns.

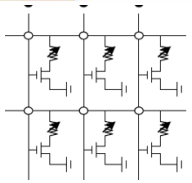
The SET/RESET operation can be completed at 2.9V within 30ns.

RRAM- Technology Advances

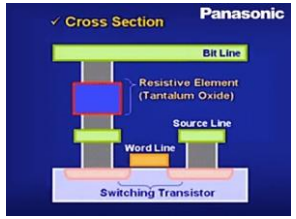
2010 — 2013 — 2015 — 2017 — 2021 — 2023 — 2025

Drain-type 1T1R

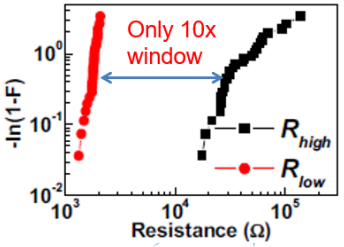




S-S. Sheu VLSI 2010

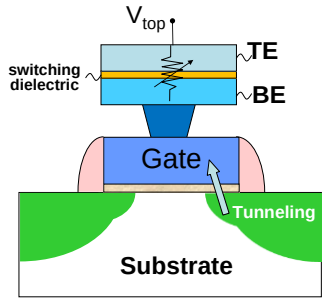


RRAM Embedded 8-bit MCUs (Panasonic)



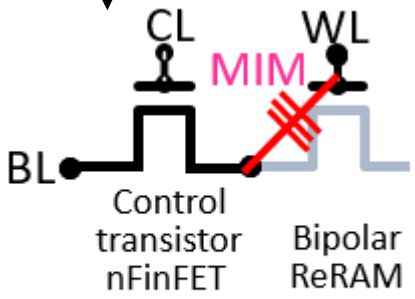
40nm CMOS

Gate-type 1T1R

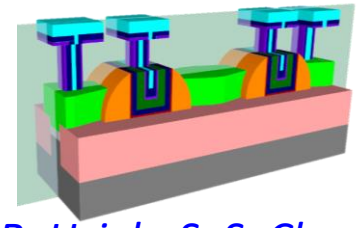


1T RG-Flash S. S. Chung, 2015DRC

16nm FinFET

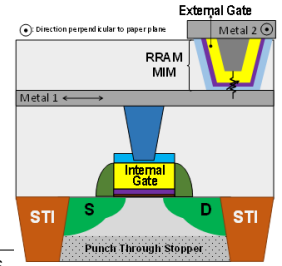


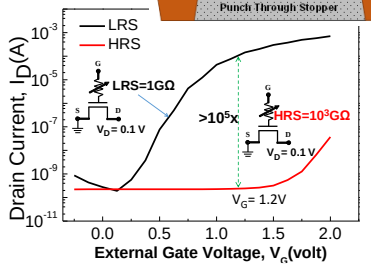
1T1R(drain-type)



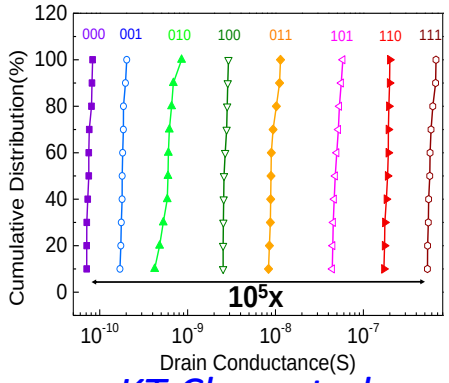
E. R. Hsieh, S. S. Chung et al., Symp. VLSI, 2017

TLC (2021irps)



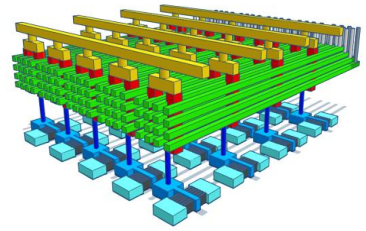


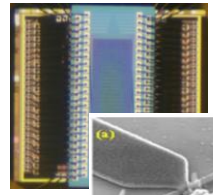
Window > 10^5x

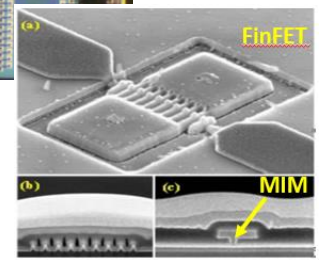


KT Chen et al., IRPS, 2021

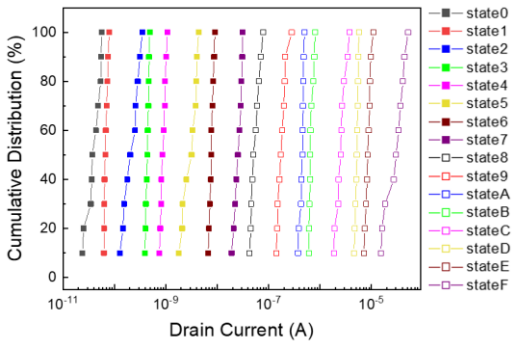
QLC 14nm FinFET (2023irps)







3D



M. Y. Li et al., IRPS, 2023

FMS the Future of Memory and Storage