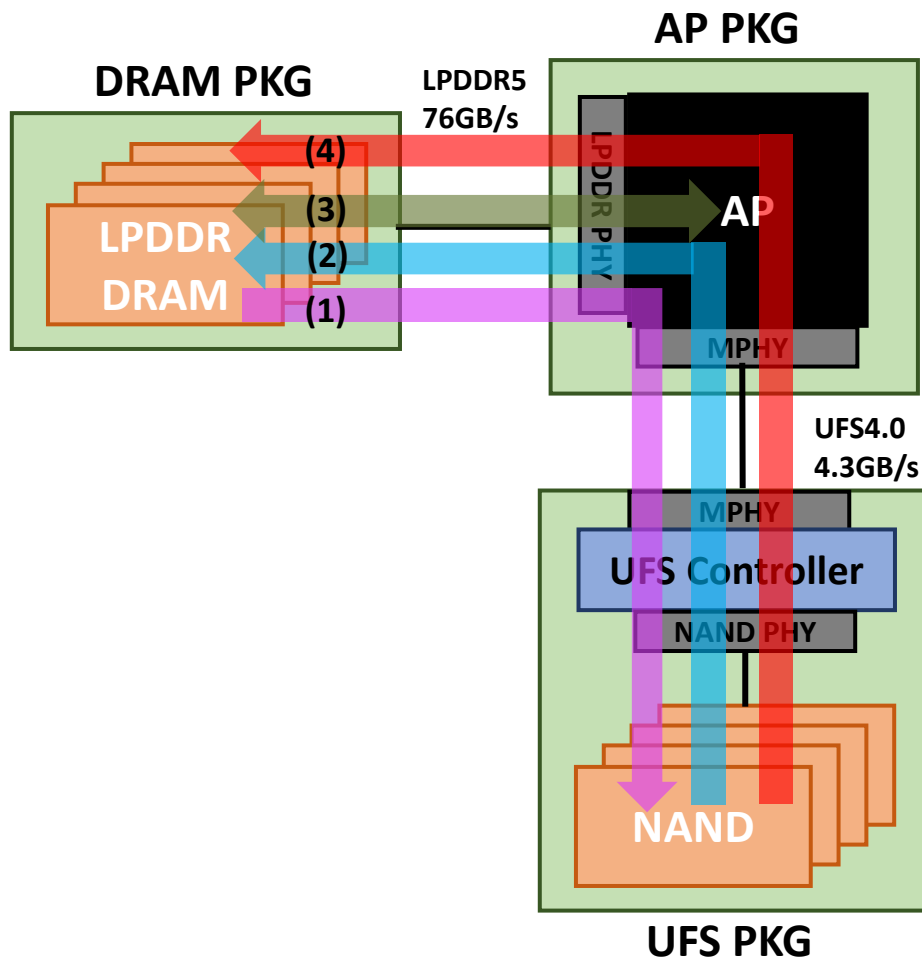


# Start New Game: HBS (High Bandwidth Storage/Solution)

PRESENTER  
**Soojin Kim**



# On-device AI Operations



## (1) Memory allocation

- Move some applications from DRAM to NAND

## (2) LLM loading

- Move LLM application and data from NAND to DRAM

## (3) AI operations

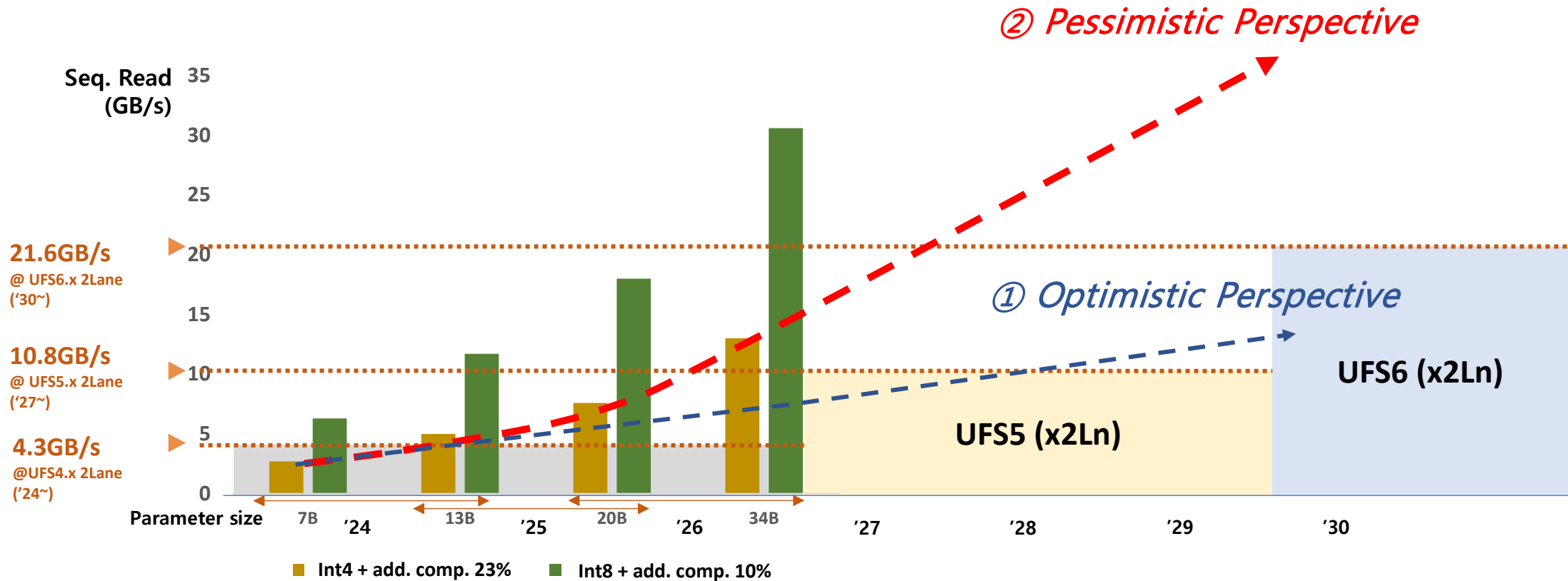
- AP reads LLM data from DRAM and performs AI operations

## (4) Back to previous status

- Move the applications and data from NAND to DRAM

➔ **Data transfer from NAND to DRAM must be completed within 1 second for better user experience**

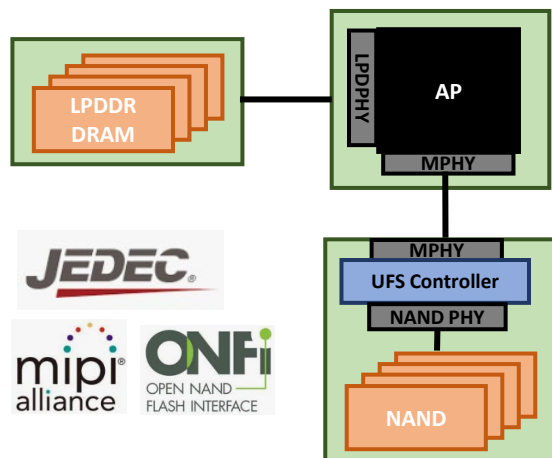
# UFS Bandwidth



- Optimistic Perspective: UFS BW will be sufficient due to the reduction of model size
- Pessimistic Perspective: UFS BW will be insufficient to satisfy the requirements for flagship smartphone

# HBS (High Bandwidth Storage/Solution)

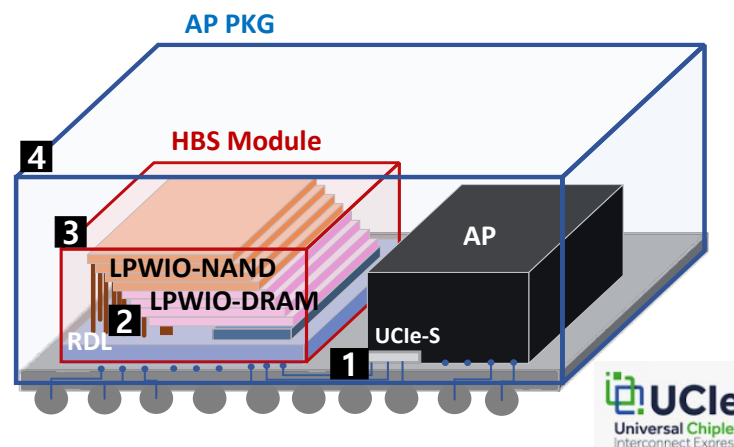
- Novel architecture to increase bandwidth for on-device AI without power increment



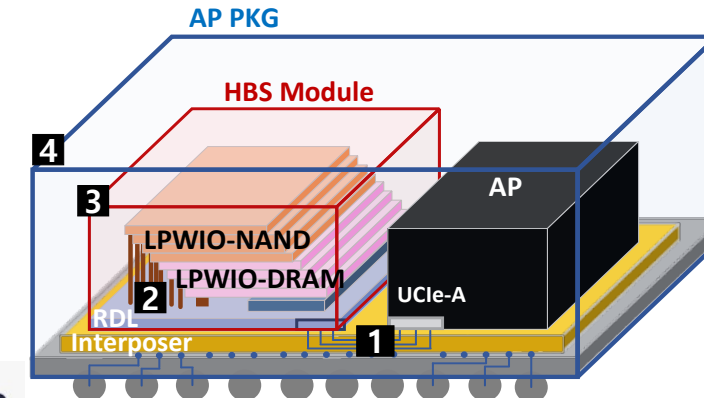
- DRAM I/F: LPDDR (JEDEC)
- UFS Host I/F: UFS/UniPro/MPHY (JEDEC, MIPI)
- NAND I/F: ONFI (JEDEC)
- PKG: Wire Bonding

Proposed  
Architecture

< AP-HBS PKG w/UCIe-STD >



< AP-HBS PKG w/UCIe-ADV >

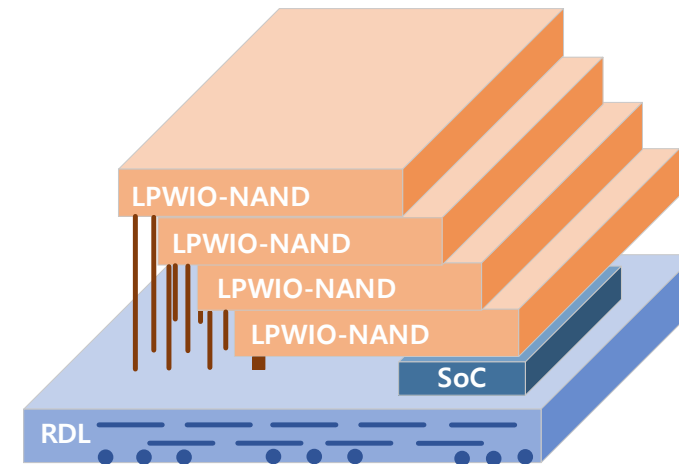
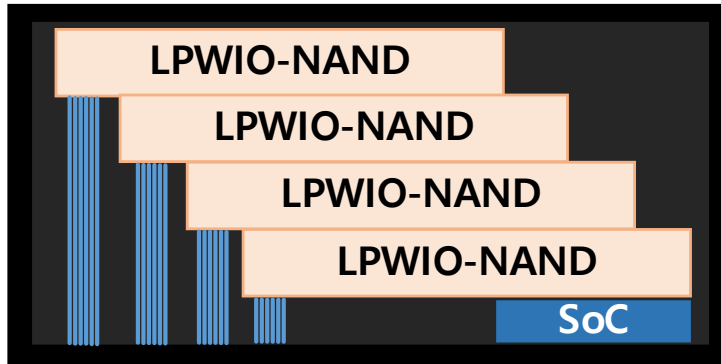


- All: Chiplet D2D I/F (UCIe, etc)
- PKG: Vertical wire Fan Out (VFO)

- 1 AP ↔ storage/memory interface: UFS/LPDDR → UCIe
- 2 Controller ↔ media Interface: wide-IO & D2D interface
- 3 Controller-DRAM-NAND: VFO package
- 4 AP-storage-memory: 1-PKG integration

# LPWIO-NAND (Low Power Wide-IO NAND)

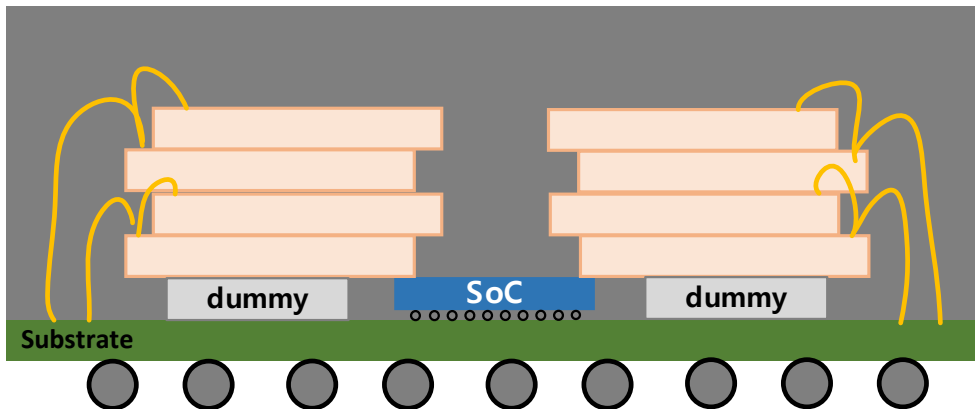
- Increasing # of channels, DQs, planes, and page size for higher bandwidth
- D2D interface for lower pJ/bit
- VFO package technology for wide-IO connections



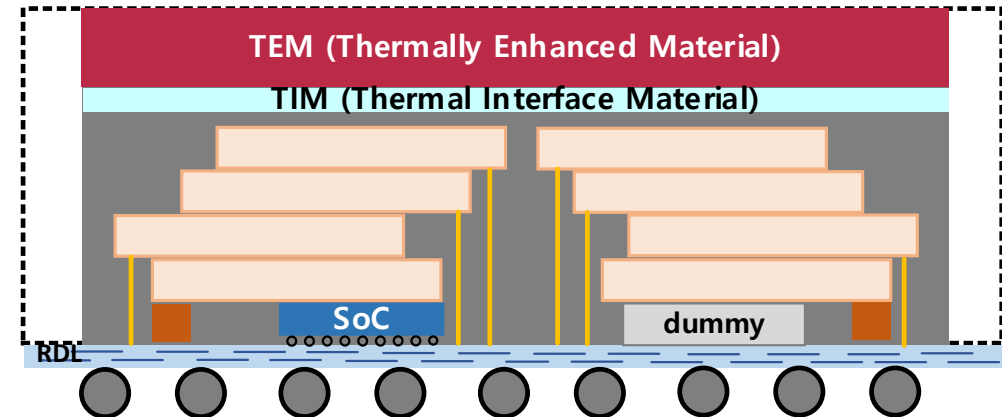
# VFO (Vertical wire Fan Out) Package

- VFO package is an integration technology of vertical wire and FOWLP
- VFO shows a remarkable 27% reduction in z-height<sup>1)</sup>
  - Redundant space in WB package can be removed
  - Thermal resistance can be improved by TEM/TIM

\* FOWLP (Fan-Out Wafer Level Package)  
\* RDL (Re-Distribution Layer)



< Wire-Bonding PKG >

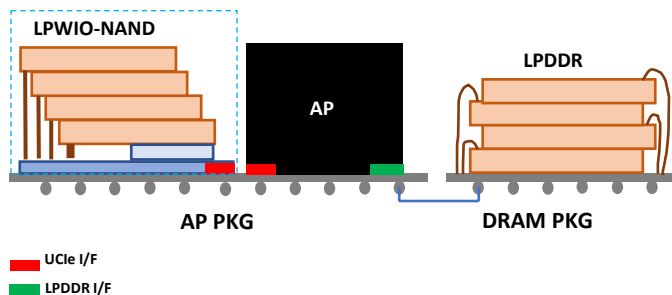


< VFO PKG with TEM/TIM >

# HBS (High Bandwidth Storage/Solution) Options

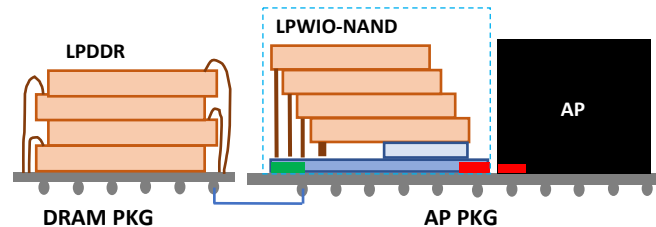
Option#1

Storage BW x4 (Chiplet)



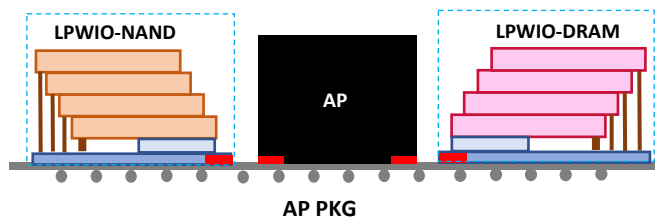
Option#2

+ DRAM BW x2



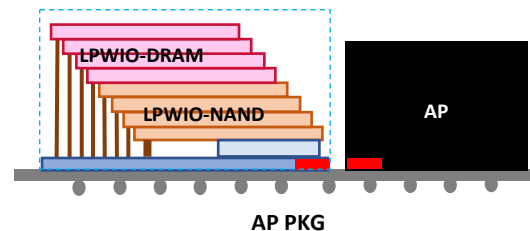
Option#3

+ DRAM BW x4 (Chiplet)



Option#4

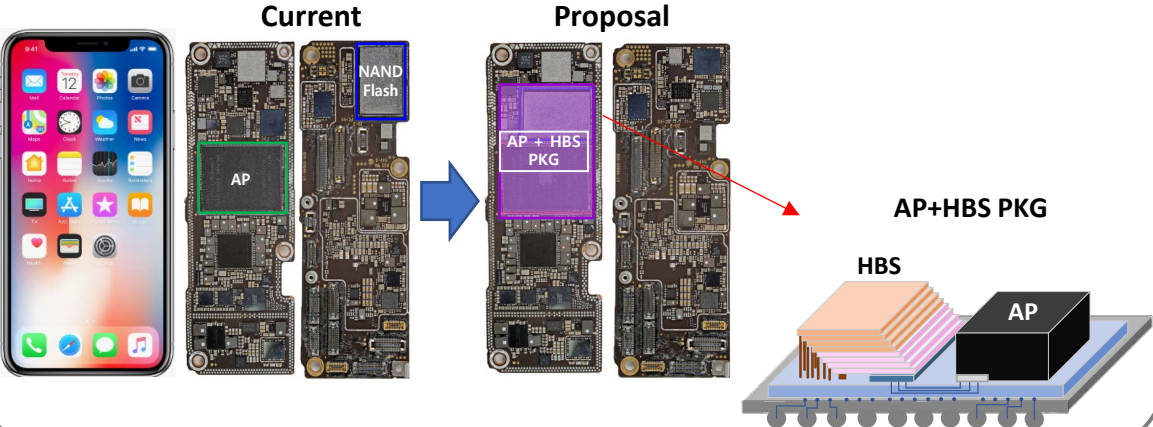
All-in-One Solution (SCM)



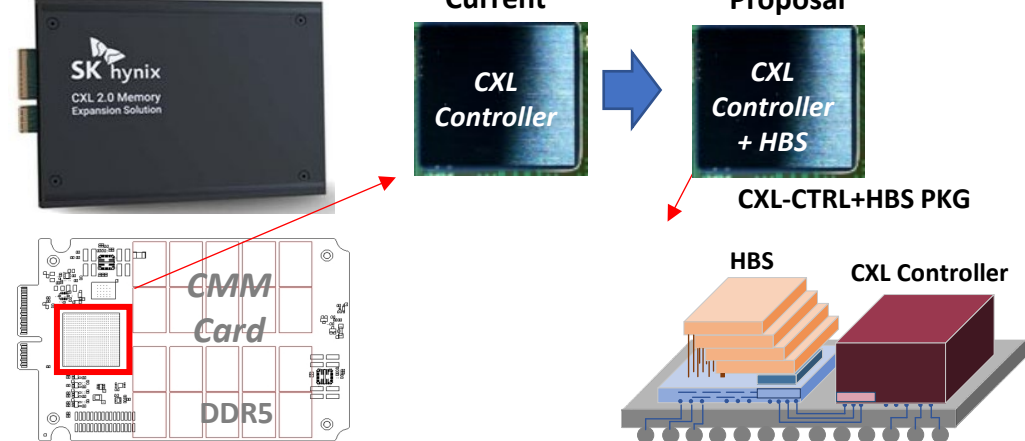
# Example of HBS Applications



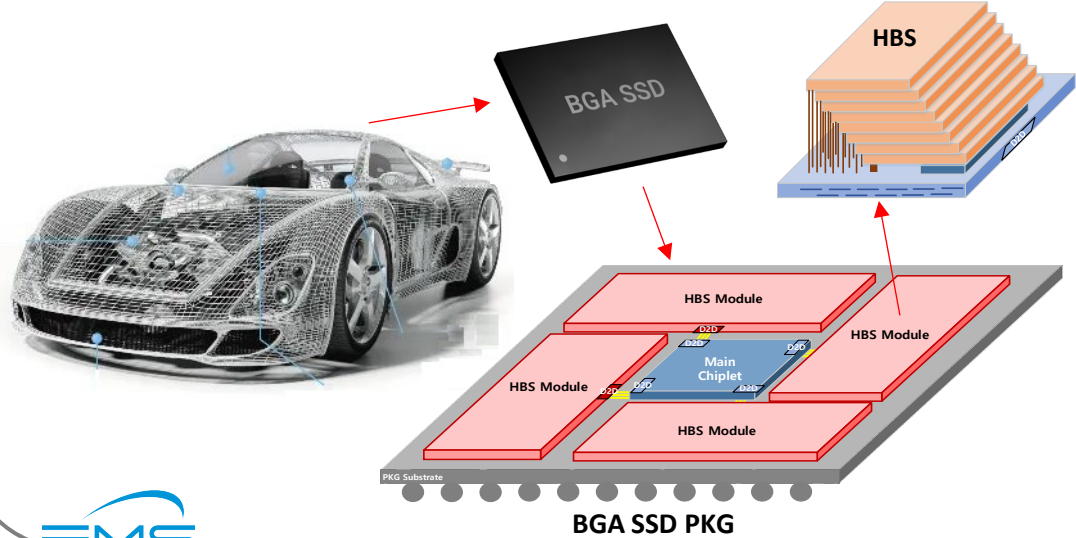
## < Smartphone >



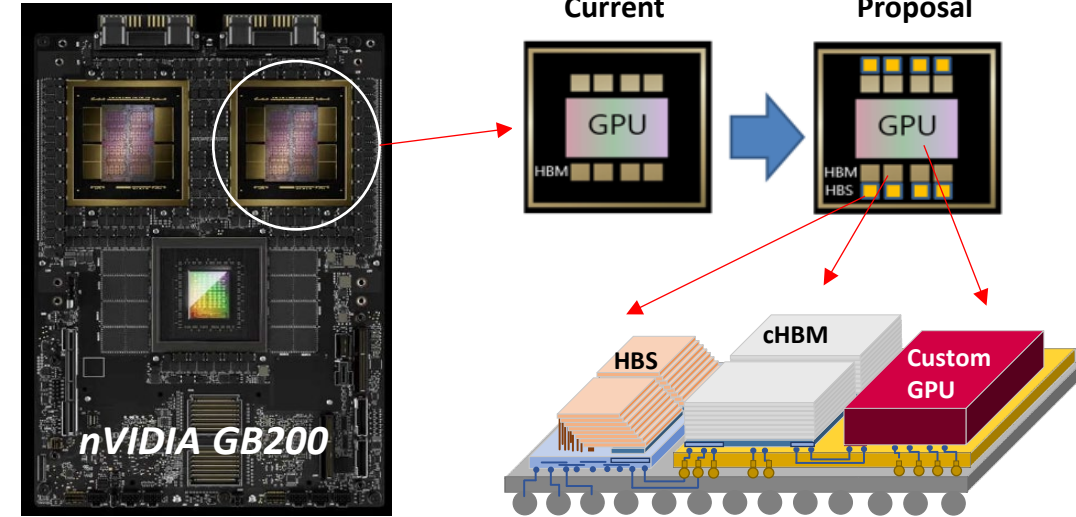
## < CXL-hybrid Memory >



## < Automotive >

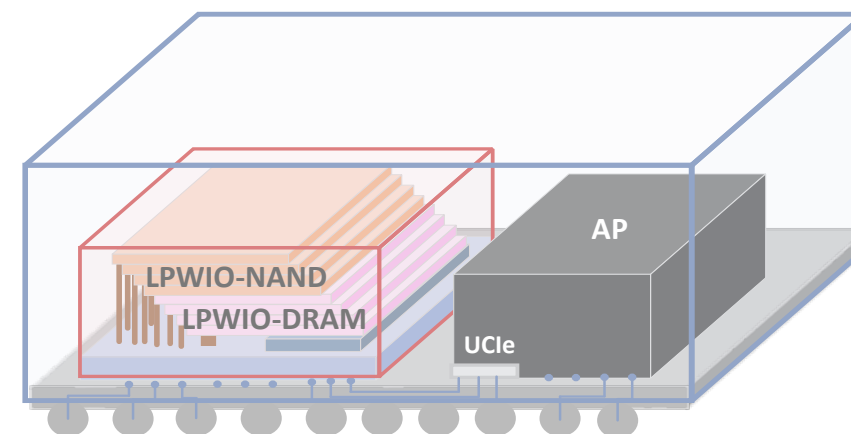


## < GPU >





- Novel HBS (High Bandwidth Storage/Solution) architecture is proposed to address the limitation of storage bandwidth and power optimization challenges
  - Expand DQ pins of NAND flash memory → LPWIO-NAND
  - Apply D2D interface between LPWIO-NAND/LPWIO-DRAM and the controller
  - Use VFO package technology for wide-IO connections
  - Apply UCle interface between host and HBS module
  
- Further study is required
  - D2D LPW-media interface specification and protocol
  - Storage stack framework, etc



# Thank You

# Booth #207

Meet the future of memory.  
Just steps from the entrance.

Innovation starts here,  
Literally.

SK hynix

