New Era of Memory Scalability: MOSAIC Chiplet Architecture for High-Capacity CXL Memory

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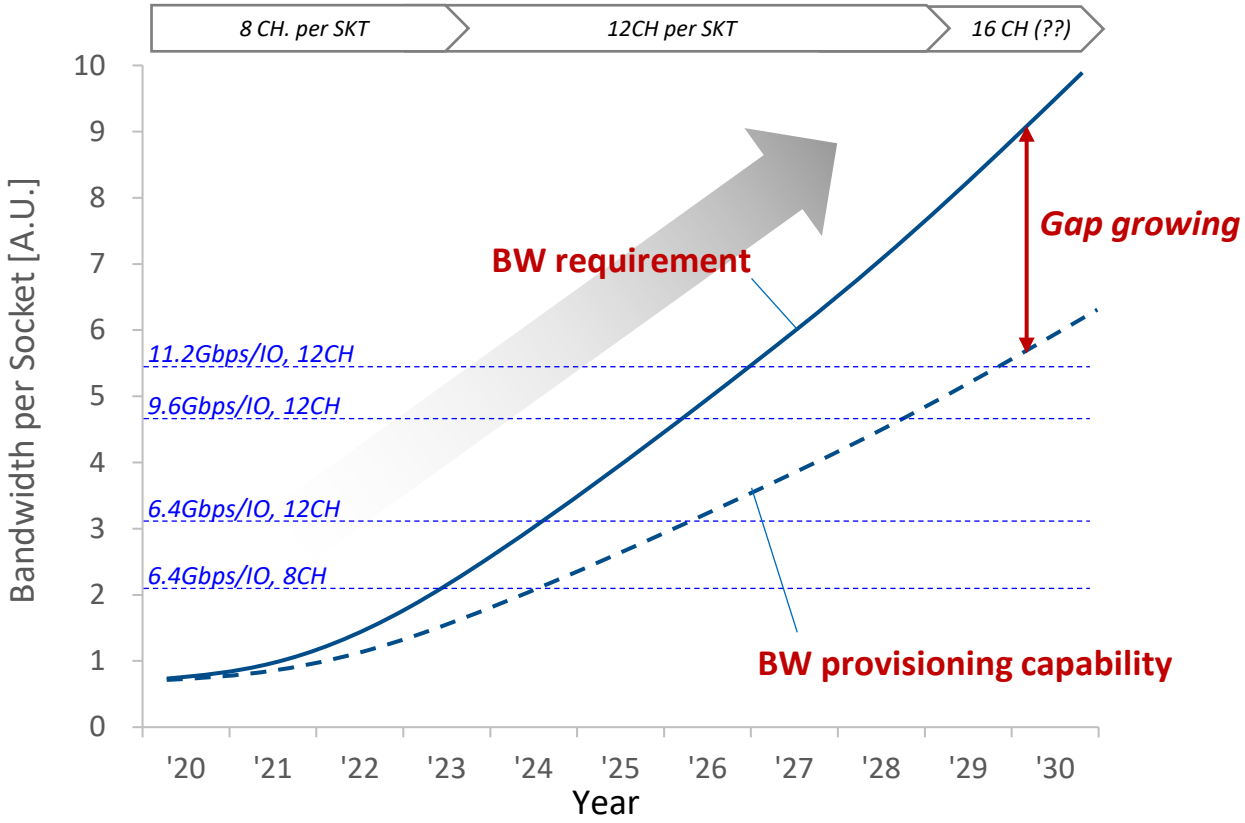
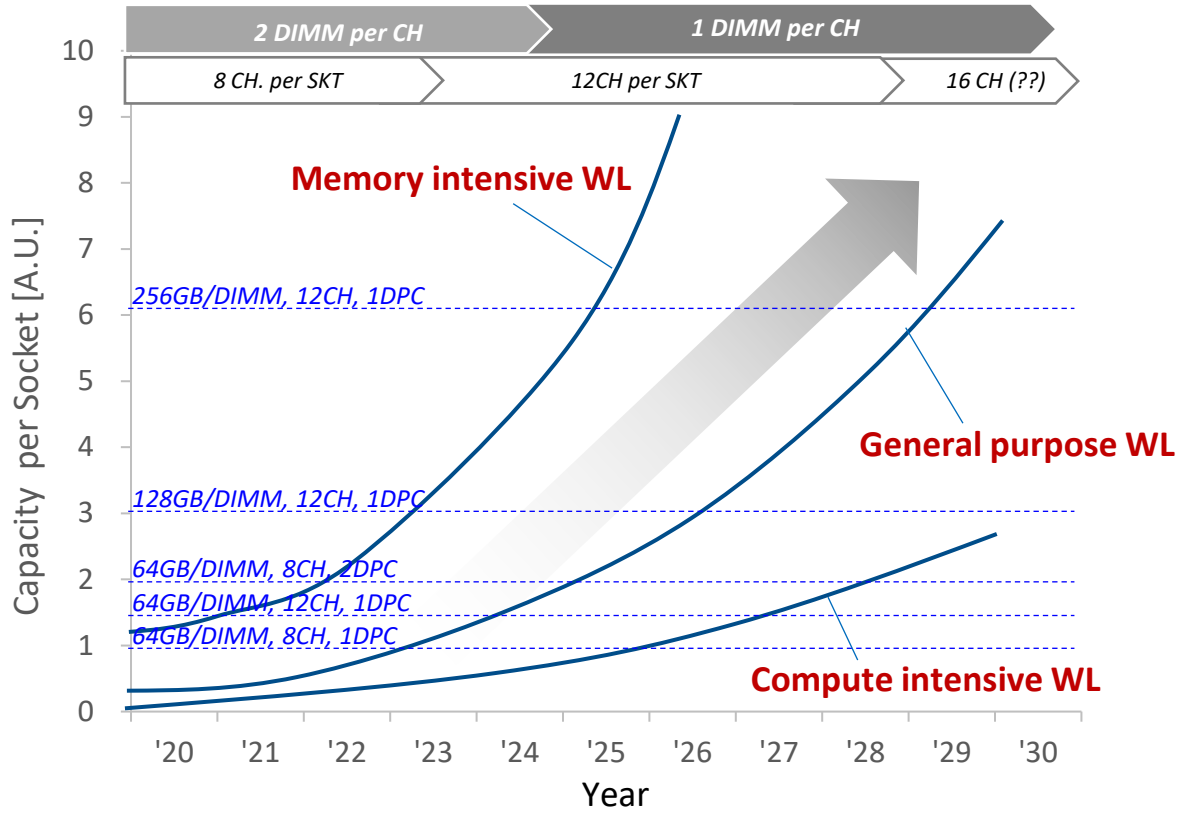
SK hynix

Challenges: Growing Memory Bandwidth and Capacity Gap

✓ Big Memory Era is coming ➔ **More memory bandwidth and capacity**



Memory Bandwidth Requirement

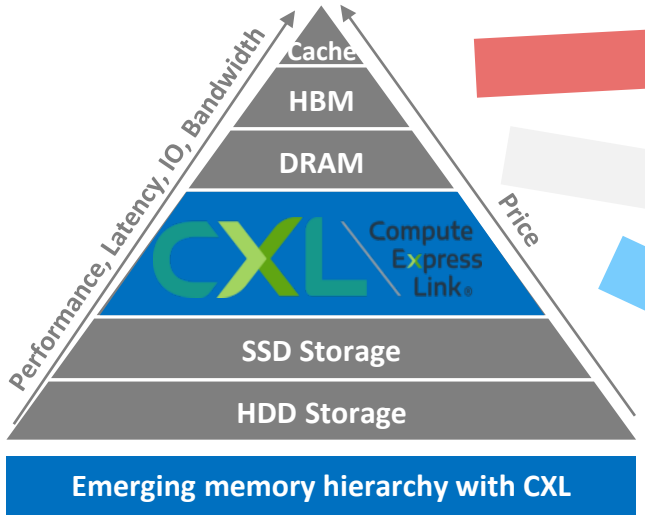


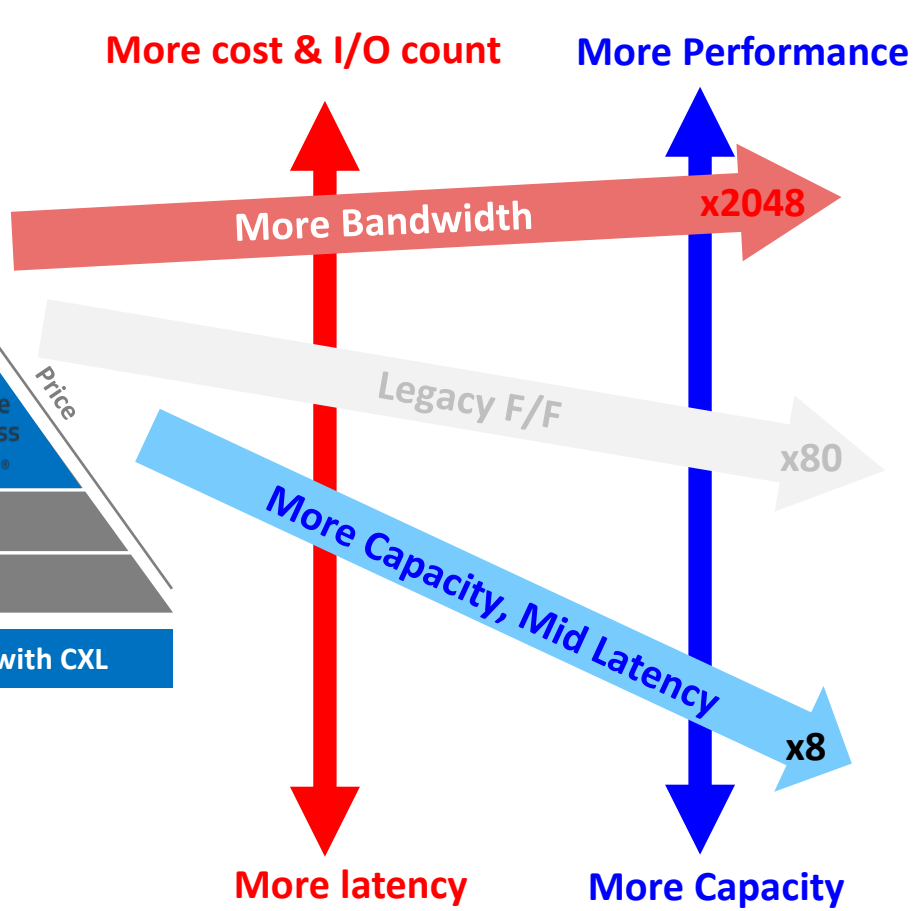
Memory Capacity Requirement

SK hynix, "Adding New Value to Memory Subsystems through CXL", Flash Memory Summit Conference. Aug. 5, 2022

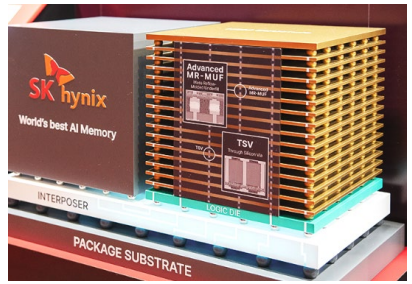
New memory at the Big Memory Era

- ✓ Memory hierarchy is changed in terms of performance, latency, Bandwidth, and cost.
- ✓ New memory (ex. HBM and CXL Memory) have been appeared beyond traditional DIMM type DRAM.





HBM



2TB/s (HBM4)
Up to 36 ~ 48GB

DIMM

~40GB/s (DDR5)
Up to 128 ~ 256GB

CMM (CXL® Memory Module)

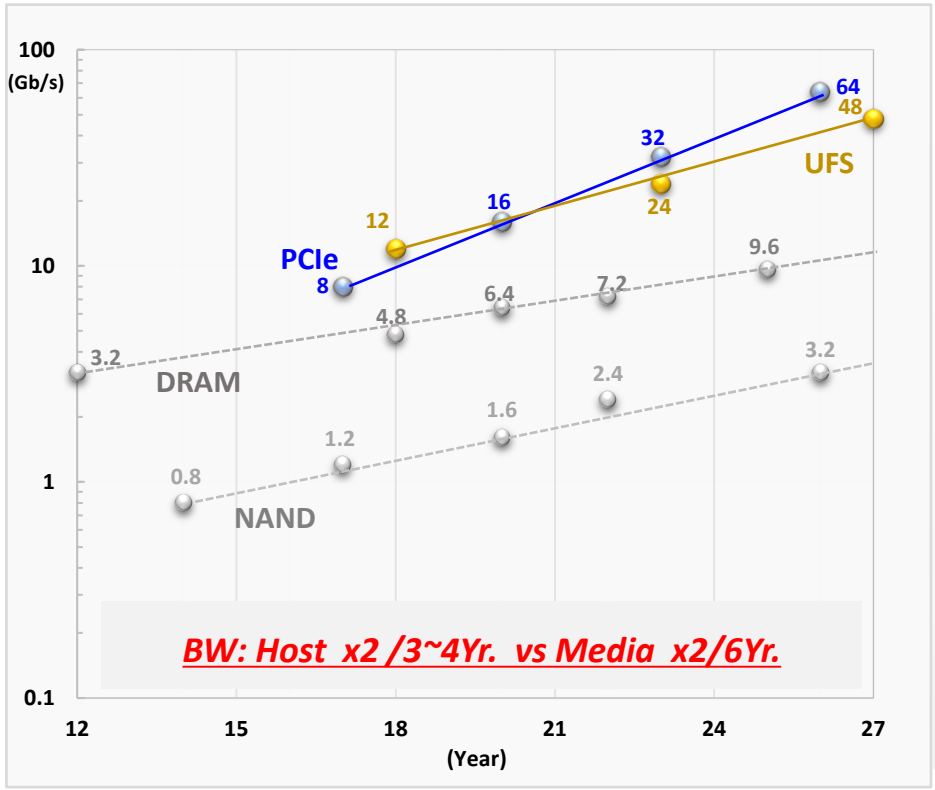
~70GB/s (CXL3.0x8LN)
Up to 512GB ~ 1TB

FMS the Future of Memory and Storage

Challenges: Growing Host & Memory Bandwidth Gap

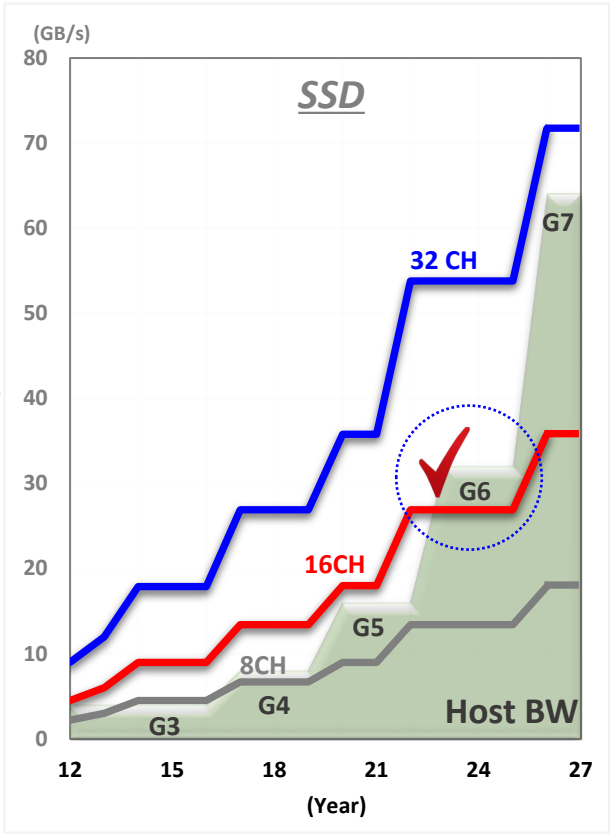
- ✓ Bandwidth of Host increase faster than one of Media ➔ **Higher data rate & more channels in media**
- ✓ Chiplet based scalable architecture can overcome the bottlenecks of media design.

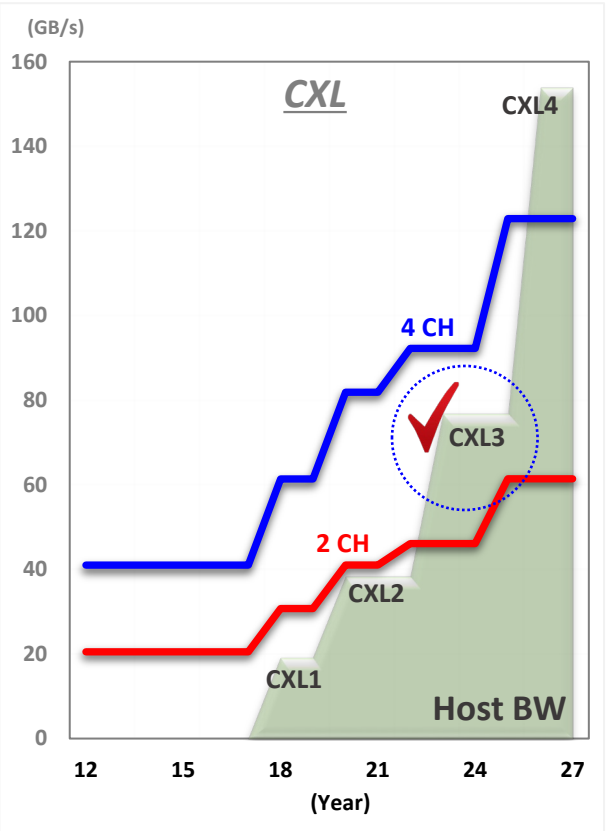
【 I/F Speed Trend 】



More Channel

【 Gen6 Host vs. Media BW 】





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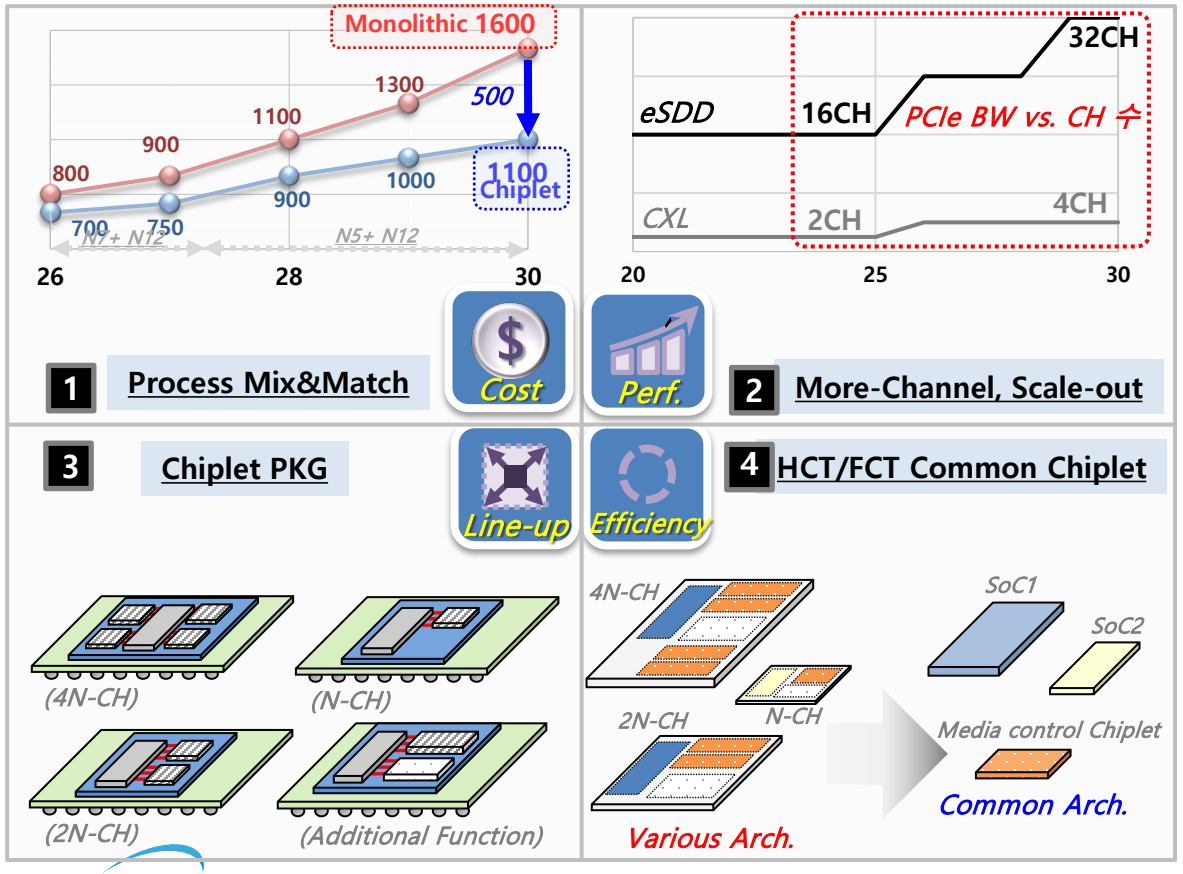
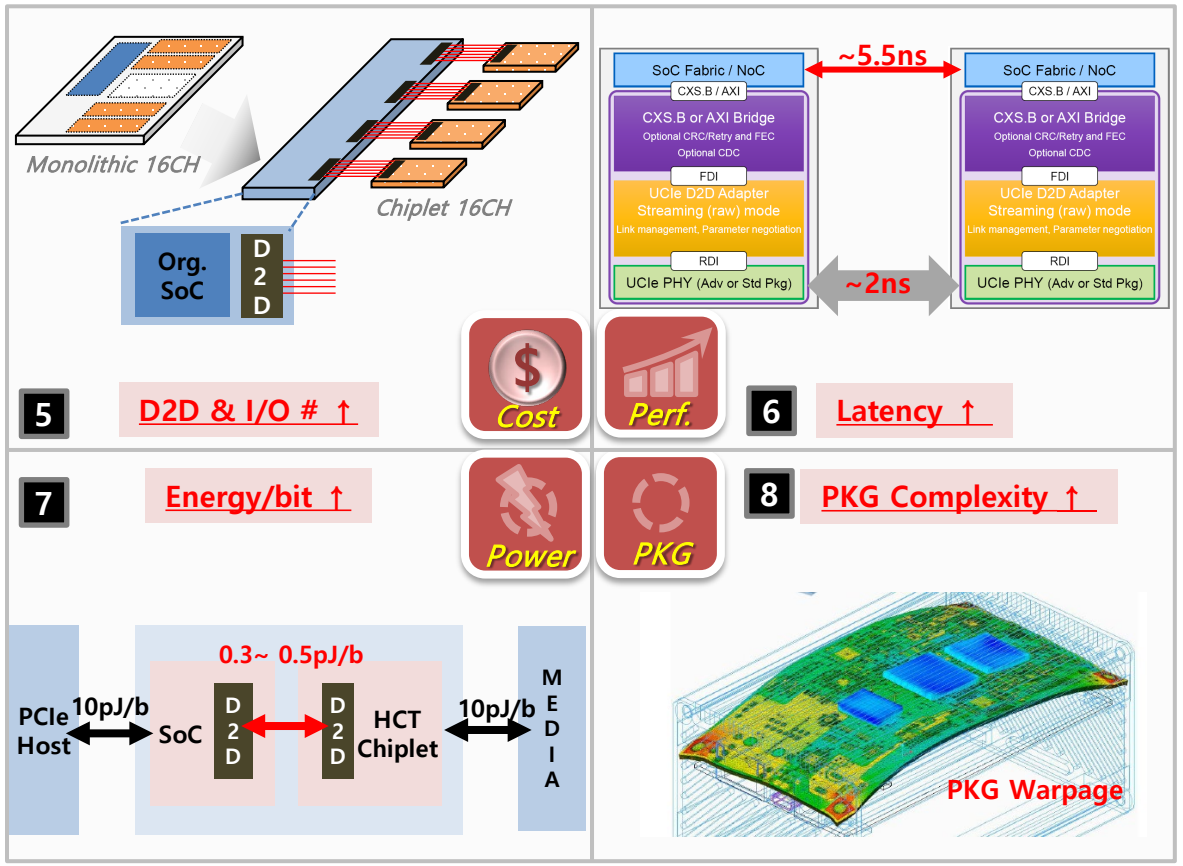
Chiplet Pros & Cons for memory applications

- ✓ Pros: Low-cost (Mix&Match), each CH and Line-up expansion, more efficient.
- ✓ Cons: Increase IO counts, latency, power and PKG complexity.

【 Pros 】



【 Cons 】



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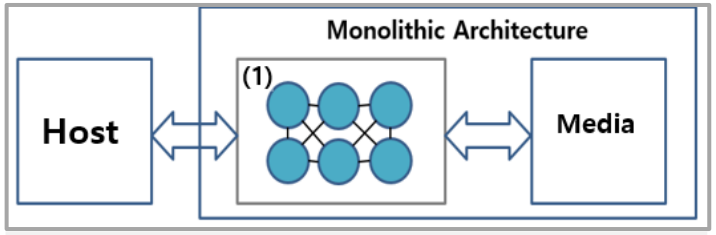
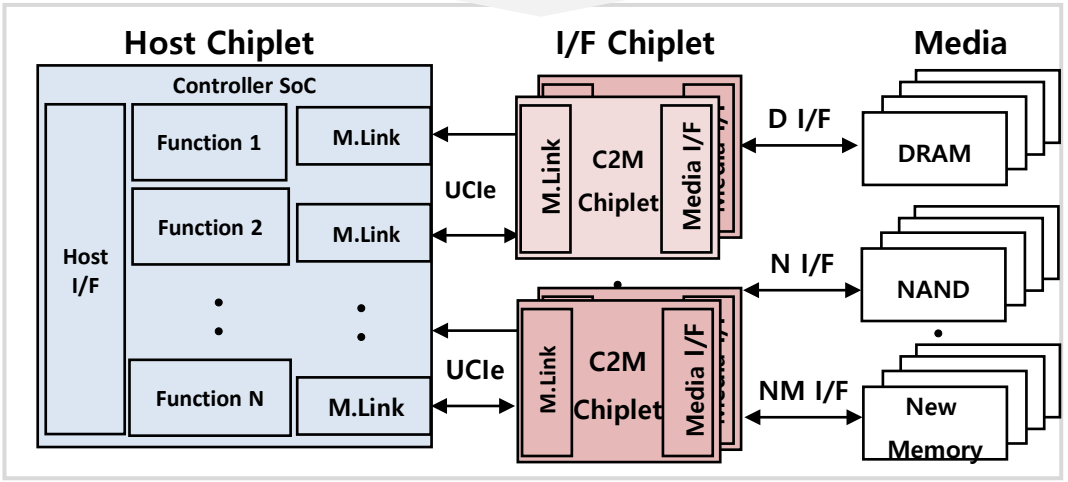
MOSAIC: Chiplet Architecture of SK hynix

- ✓ Monolithic (All-in-one, Single Skeleton) ➔ Optimized in single SoC, Poor diversity and flexibility
- ✓ Chiplet (Separated, Loosely Coupled) ➔ Mix&Match, better for functional expansion & change



MOSAIC



Modular: smaller & Independent in function & fabrication process

Object-oriented: Individually optimized & Re-usable for various application

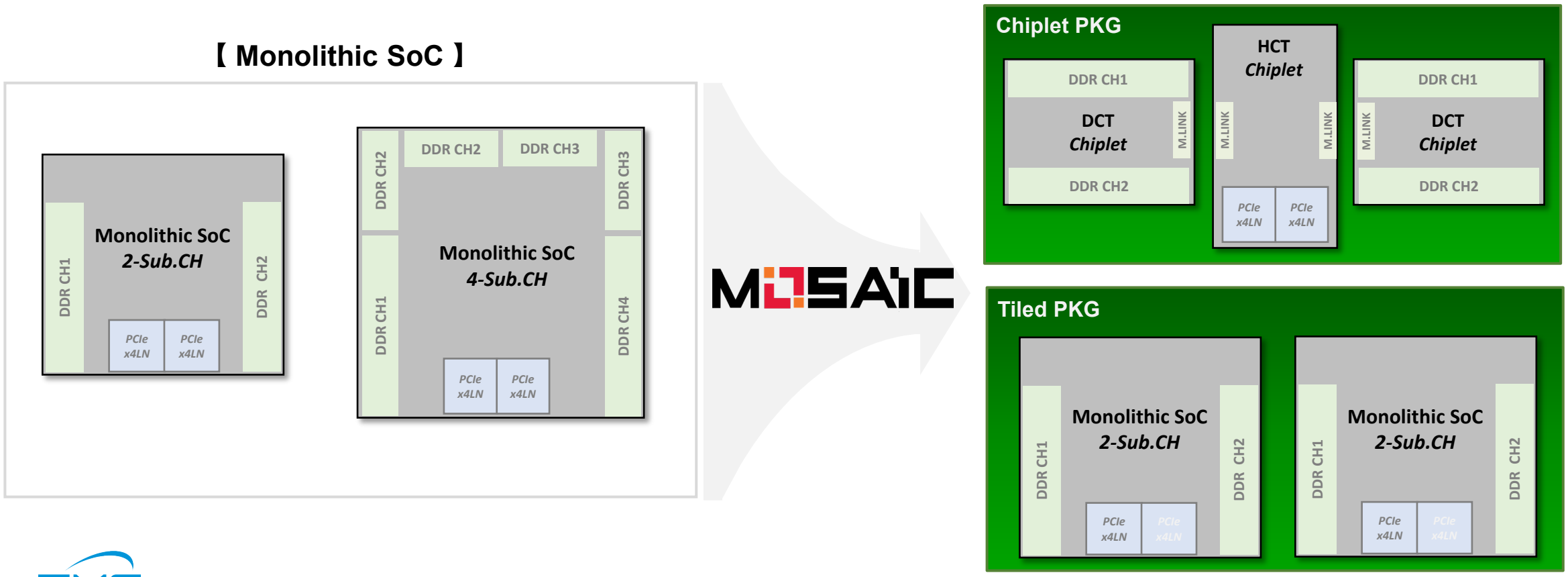
Scalable: Resembled to create a system

Architecture: Architecture on package

Incremental-Change: Easy expansion in Media/Compute/Hybrid w/ Mix&Match

MOSAIC: Tiled & Chiplet Architecture

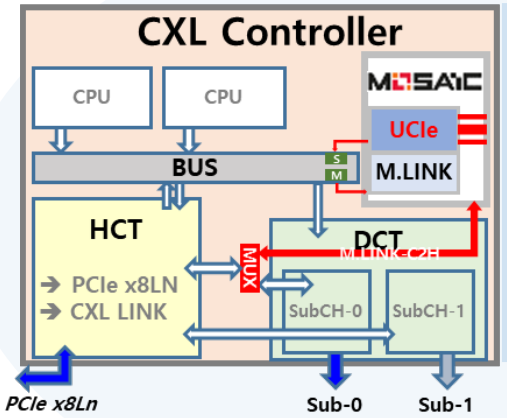
- ✓ There two approach for channel expansion of CXL Memory (Tiled &r Chiplet Architecture)
- ✓ Chiplet architecture is more cost-effective solution.



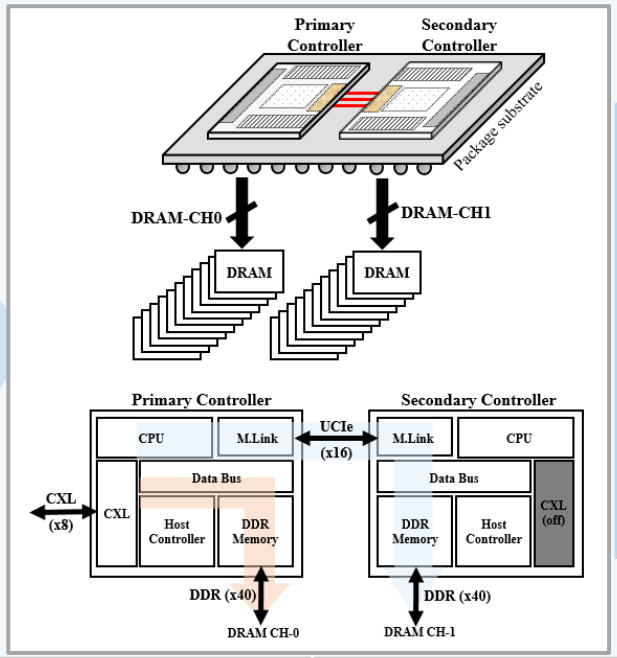
MOSAIC : Chip, PKG & CXL Memory Module

- ✓ x2 Bandwidth & Capacity in CMM using a Chiplet PKG w/ 2-tiled controllers.
- ✓ Reduce yielded cost up to 50~60% due to better yield & proper placement for a smaller chip

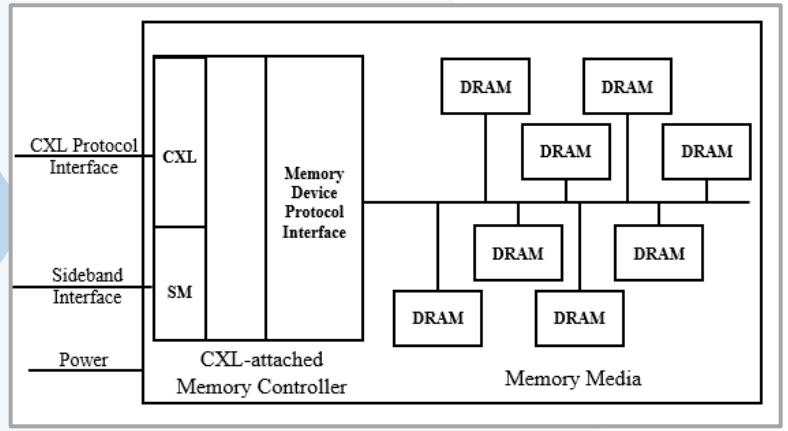
【 Chip 】

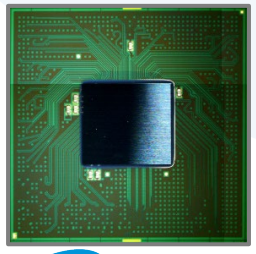


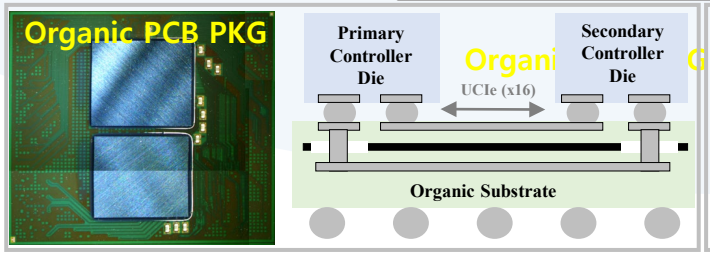
【 Package 】

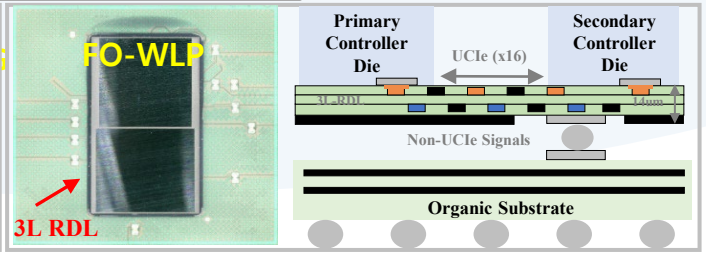


【 CMM-Module 】









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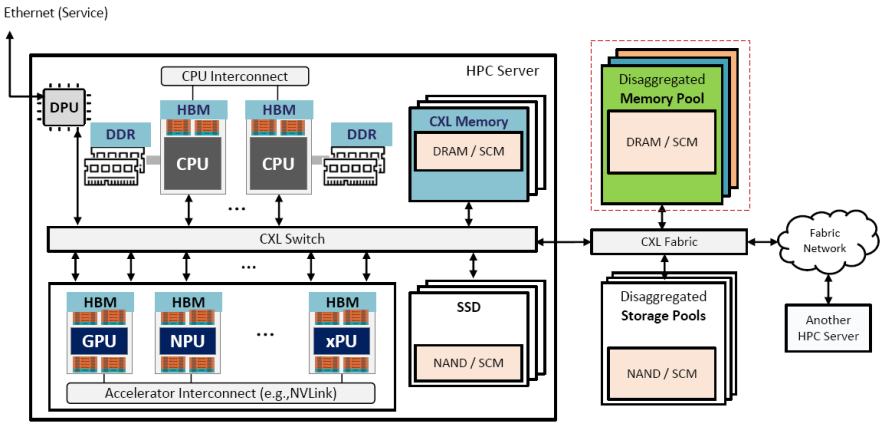
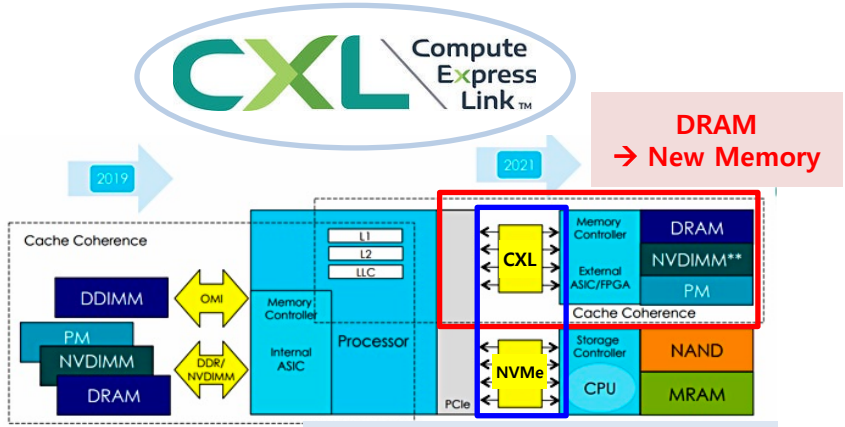
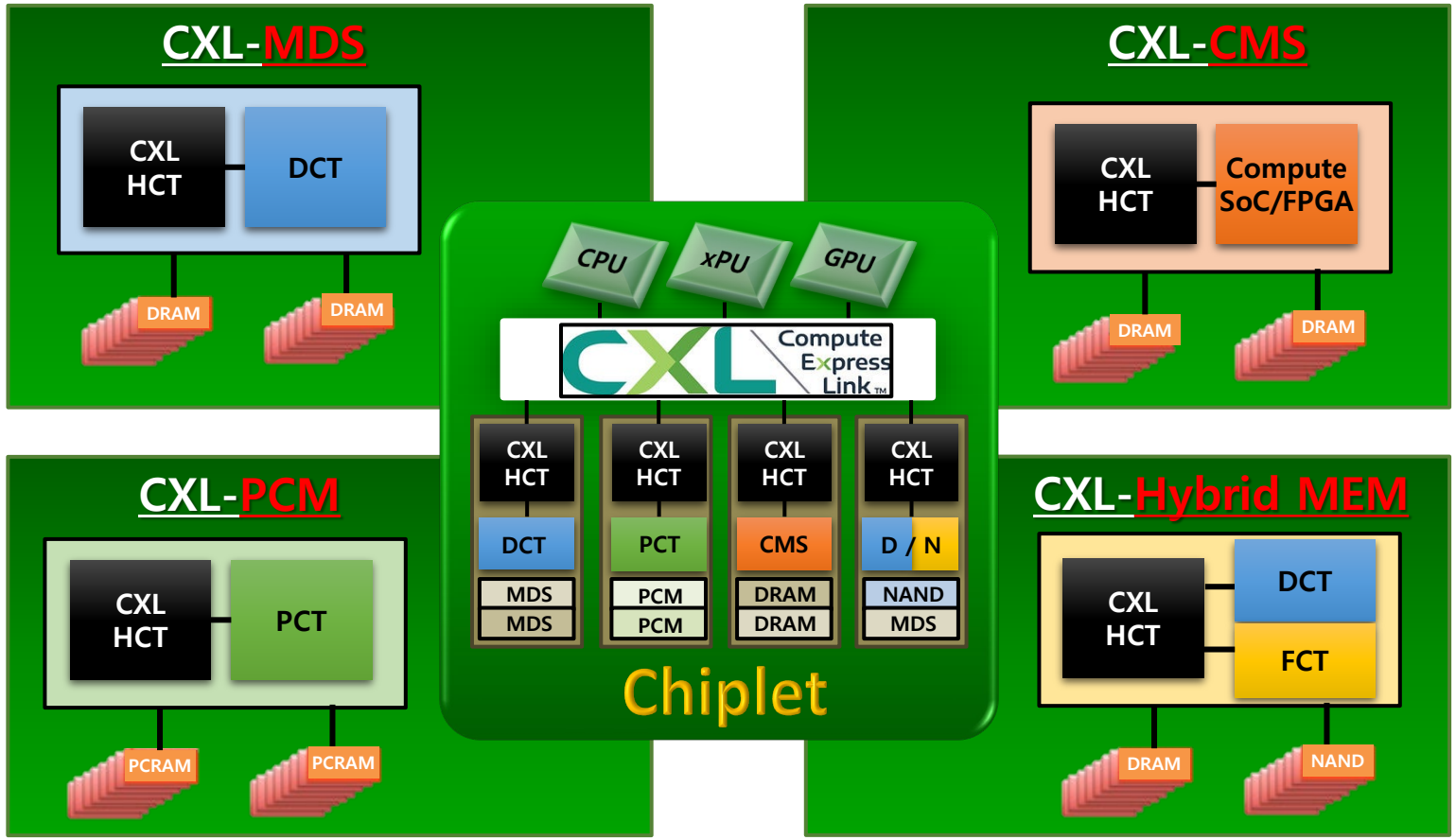
Next chiplet architecture for memory applications

- ✓ CXL can enable memory pool with different types of memory media (ex. HBM, SSD, CXL, PCM..)
- ✓ CXL common chiplet can be solutions to support various media and companion chips.







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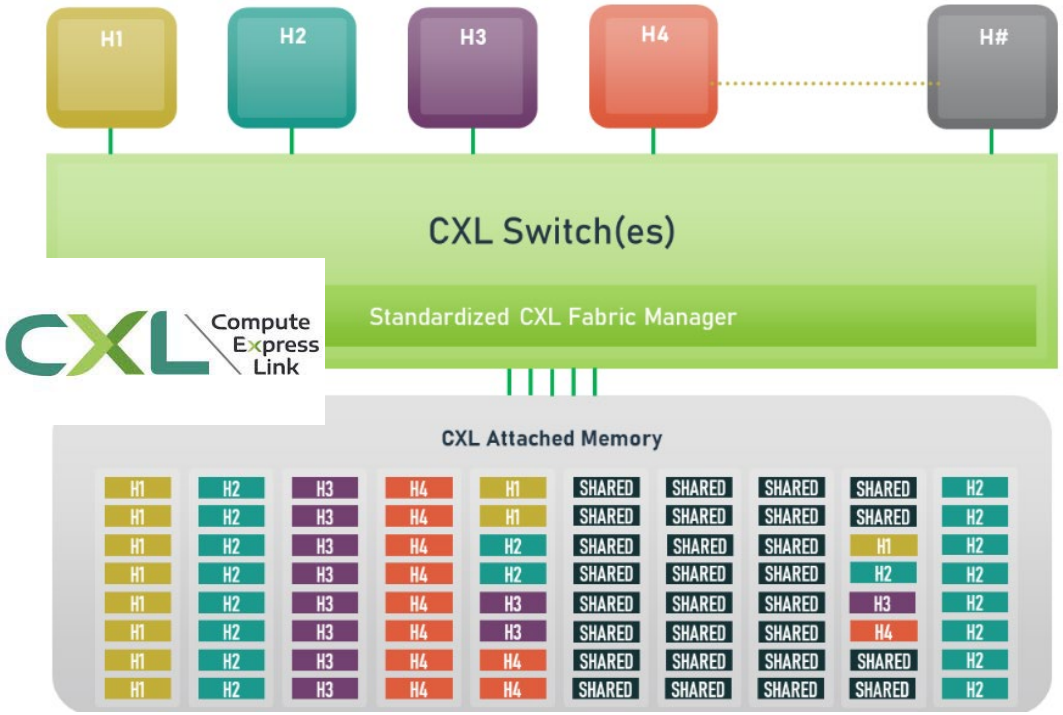
Memory Expansion w/ CXL Memory

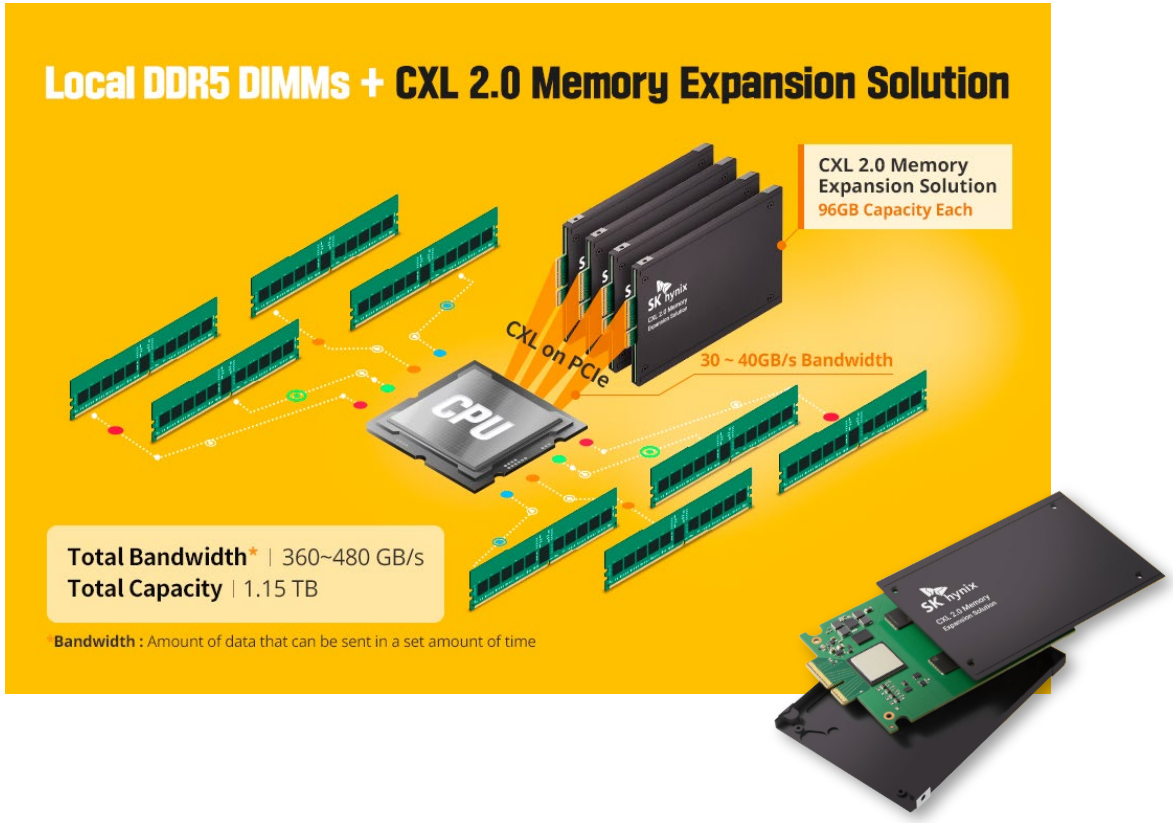
- ✓ Memory Pooling and Sharing is available with CXL-memory.
- ✓ SK hynix has owned memory expansion solutions with DDR5 DIMMs & CXL Module.

【 CXL-Memory Pooling and Sharing 】



https://computeexpresslink.org/blog/explaining-cxl-memory-pooling-and-sharing-1049/

【 SK hynix memory expansion w/ CXL + DIMM 】



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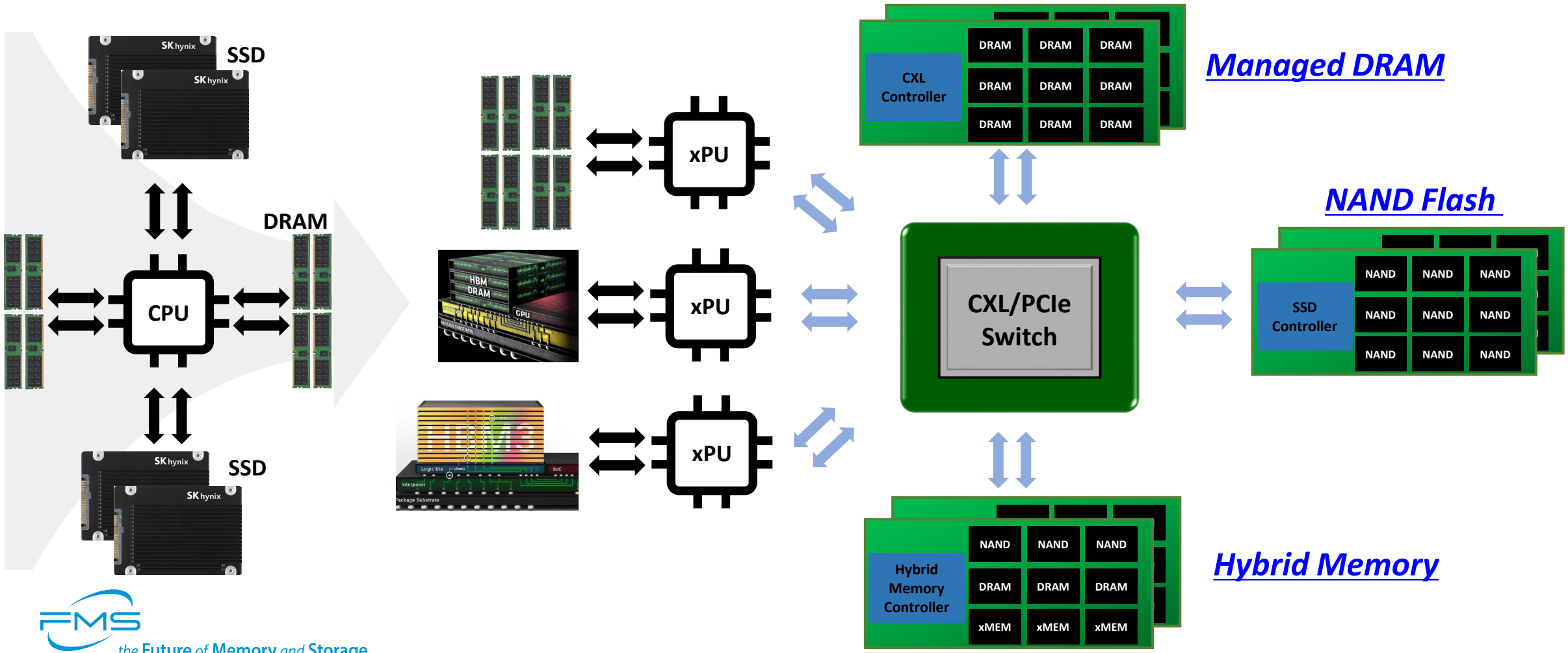
Expansion of Memory Eco-system

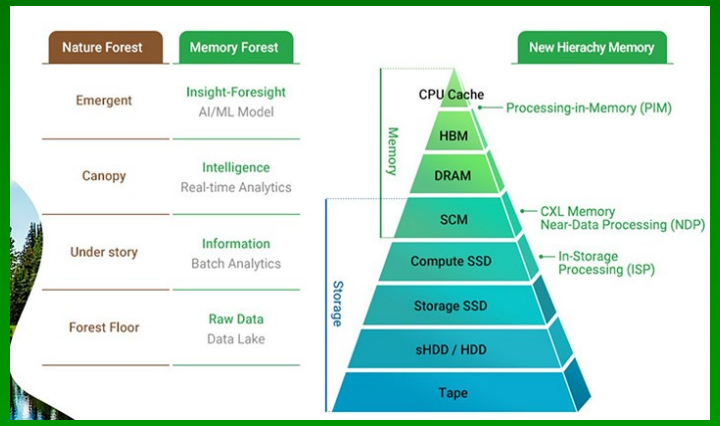
- ✓ Simple traditional computing system and memory hierarchy has been expanded based on CXL/PCIe/NVMe using various memories.



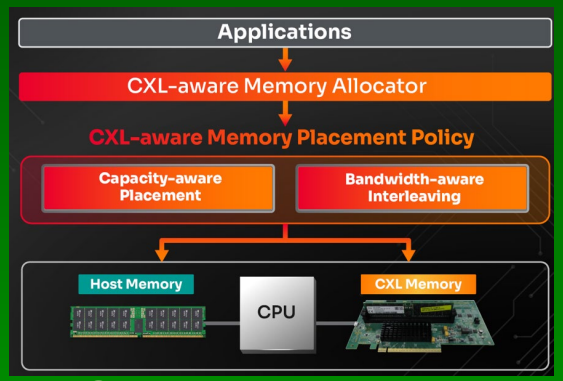
Memory Eco-systems of SK hynix

- ✓ On preparing for Chiplet architecture (MOSAIC), S/W (HMSDK), H/W (CXL Module, TSV/VFO PKG)

MEMORY FOREST

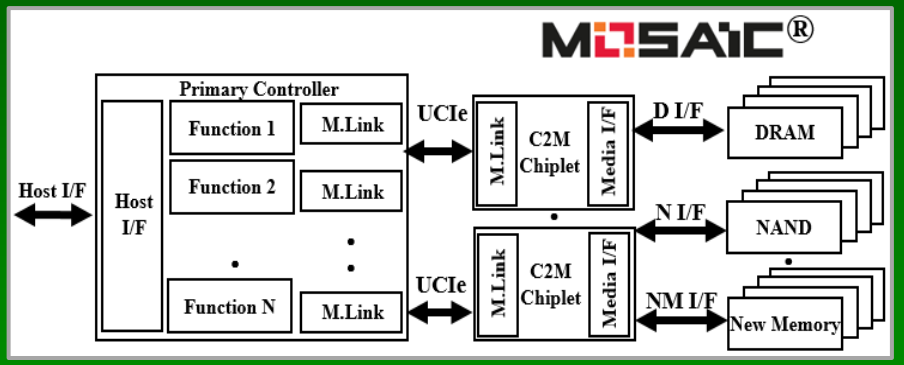


S/W

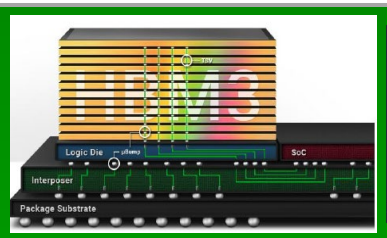


HMSDK

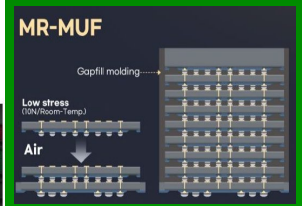
Chiplet Architecture



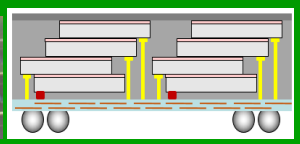
PKG



TSV



VFO*

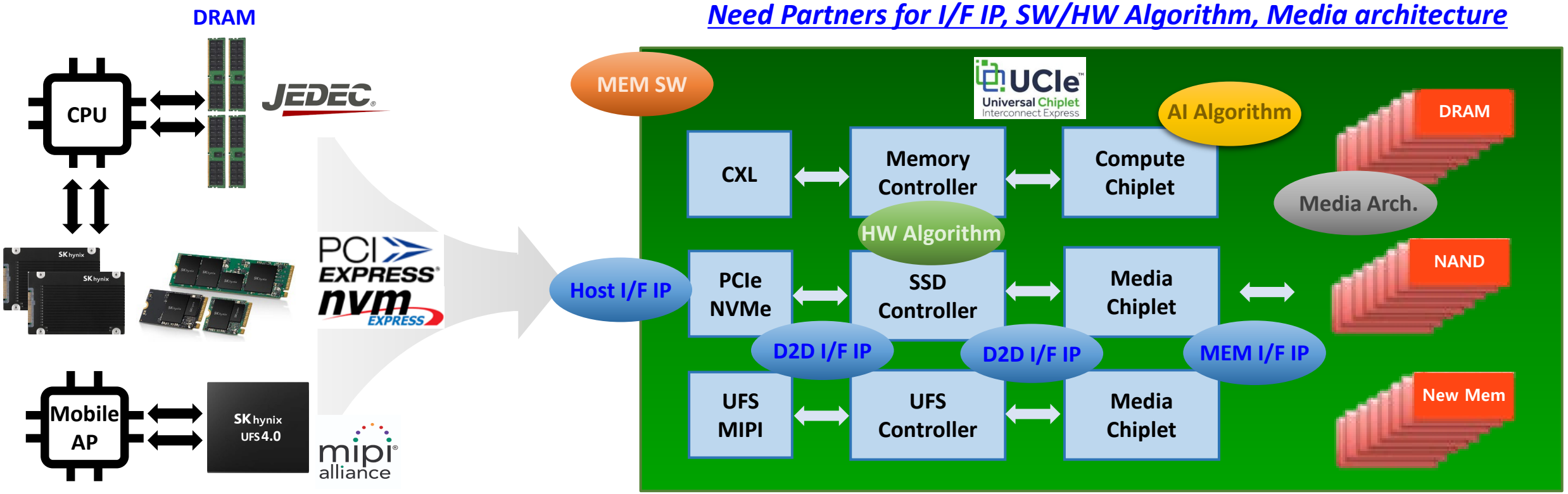


CXL Module

* 2024 IEEE 74th Electronic Components and Technology Conference, "Vertical Fan-Out(VFO) package with enhanced form factor and performances for mobile" applications

Memory Eco-system with Industry Partners

- ✓ Close collaboration with all CXL eco-system partners across the entire system hierarchy is essential for successful launch of future CXL products



For Technical discussion or partnership with SK hynix,
email to Dongsop Lee (dongsop.lee@sk.com) or Minsoon Hwang (minsoon.hwang@sk.com)

FMS the Future of Memory and Storage

Thank You

Booth #207

Meet the future of memory.
Just steps from the entrance.

Innovation starts here,
Literally.

SK hynix