

# SSD Controller for Space Applications

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# Electronic devices in outer space

## 1. Radiation-Hardened (Rad-Hard) hardware

- Materials, insulating substrates
- Redundant circuit
- Memory ECC

## 2. Physical shielding

## 3. Fault Tolerance

- Redundant module, data integrity (data path parity).
- Watchdog timers, self-checking logic.

## 4. Software Mitigation

- Detect anomalies
- Reroute HW resources

**Total Ionizing Dose (TID)**  
Cumulative damage  
Entire device

**Single Event Effects (SEE)**  
Transient damage  
Circuits / registers

# Challenges of SSD controller in outer space

## Controller

- 1. Control path fault tolerance**
  - SEU in control logic (especially state machine)
  - FW hanging
- 2. Data path fault tolerance**
  - Bit flips during transfer / register
  - Encryption / Scrambler / Encoder
- 3. NAND management**
  - FTL / metadata protection
  - Wear out / Retention
  - Power fail

Single event upset  
(SEU)  
Single event transient  
(SET)  
Single event latch-up  
(SEL)  
SEFI  
SEB  
SEGR

## NAND

TID  
Thermal range

**Relatively immune to SEE.**

- Passive storage mechanism.
- High threshold to change the amount of charge
- LDPC

# Soft error

- Mainly caused by cosmic ray.
- x2.2 for every 1000m.

Electronic devices  
in outer space

An election in a Belgium town, 2008

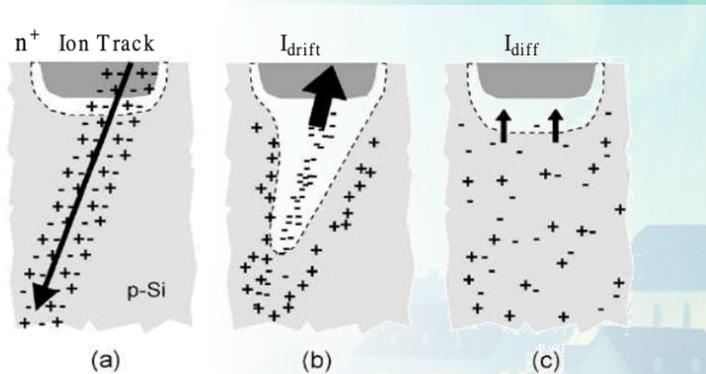
Self driving automotive

1km

10km

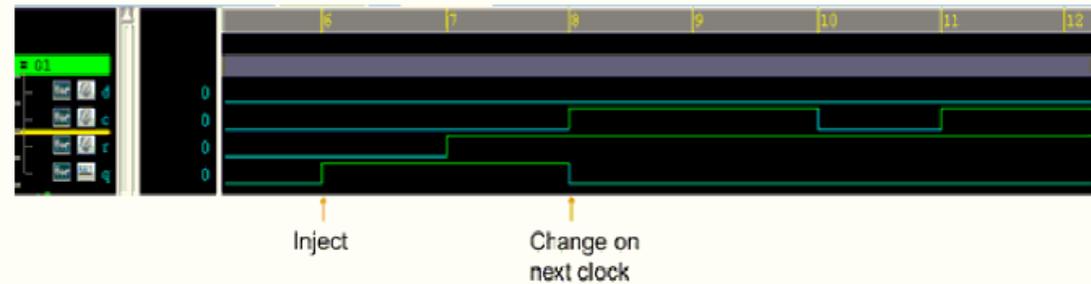
# Soft error types

- Single event upset (SEU)
  - Memory or flip-flops
  - Bit flip
- Single event transient (SET)
  - Combinational circuits
  - A voltage spike in circuits



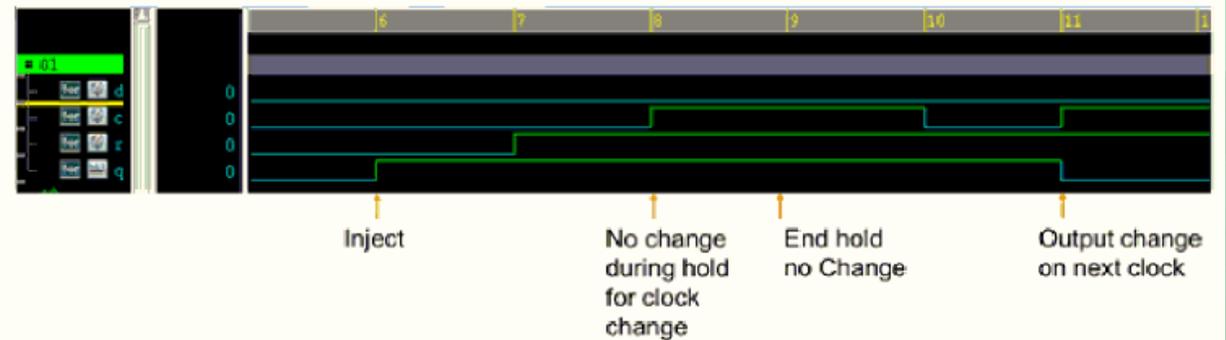
## Transient SEU

Example:  $NA \sim (6) \{PORT "test.d1.q"\}$



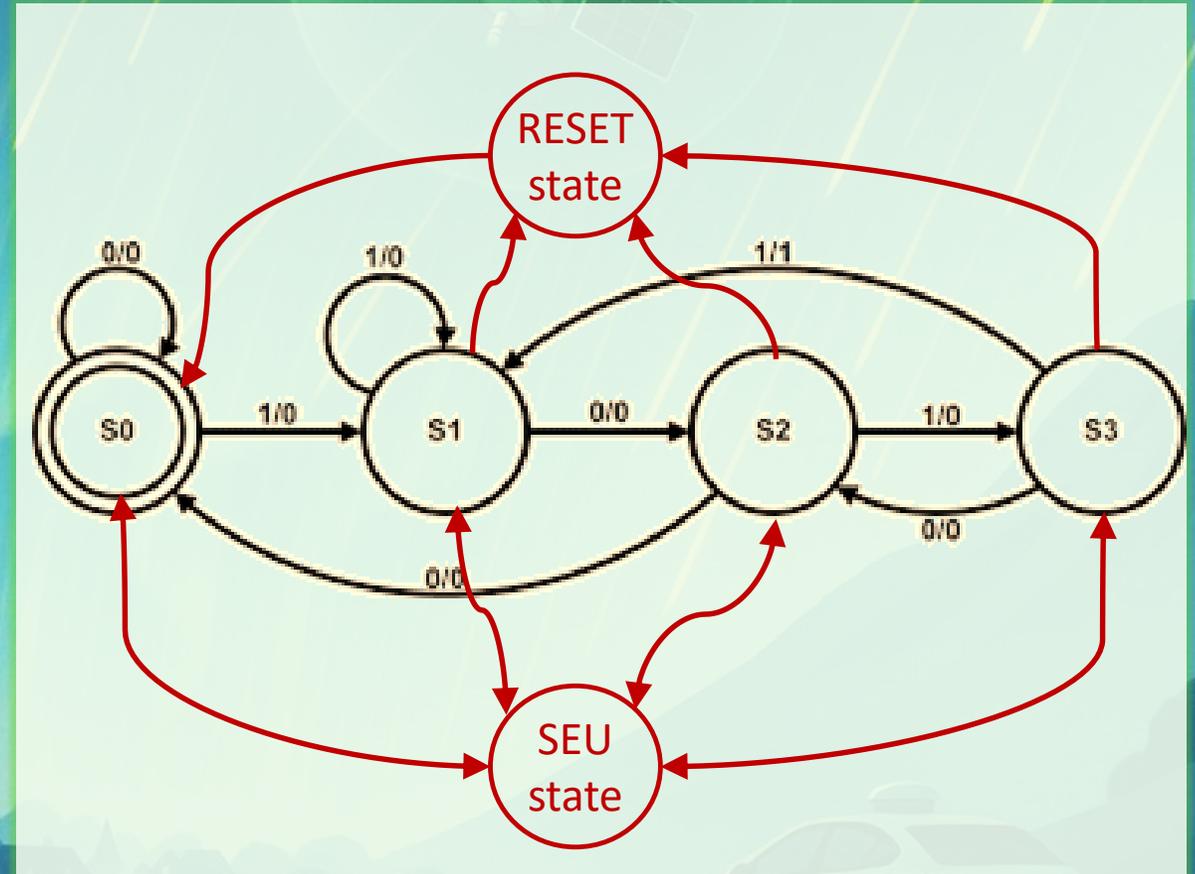
## Transient Hold

Example:  $NA \sim ([6^9]) \{PORT "test.d1.q"\}$



# Control path soft error

- State registers against SEU
  - ECC for state registers
    - Ex. One-hot states + Hamming code
    - Validate state registers
    - Detection and recovery
    - Correction to original state
- State transition signals against SET
  - Validate state transition signals
    - Time and space redundancy.
    - Hand shake.
    - Use levels instead of pulses.
- Design with atomicity principle

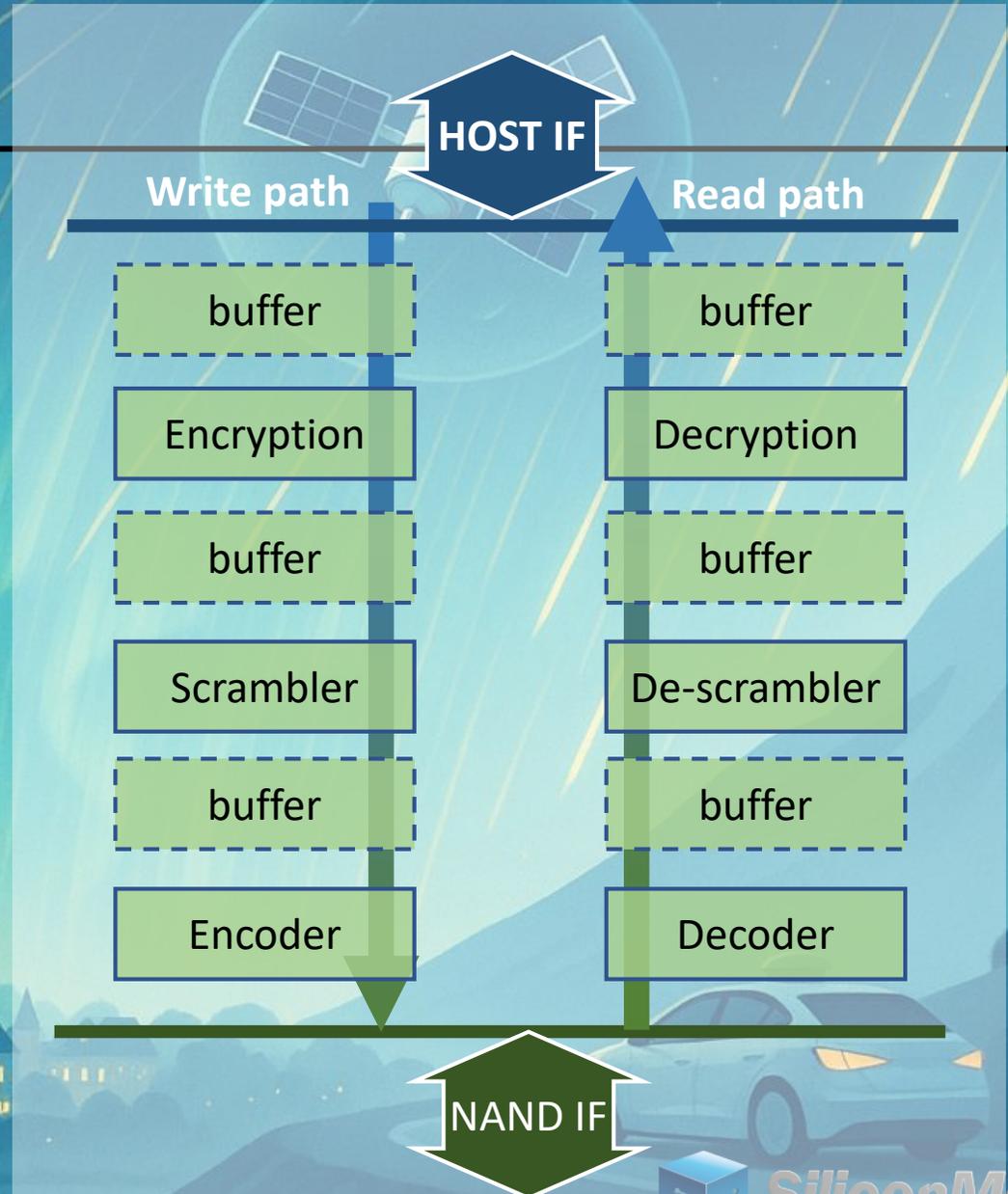


# Data path soft error

- Host E2E / data parity
  - Check the entire path
- Memory scrubbing
  - Protect buffers

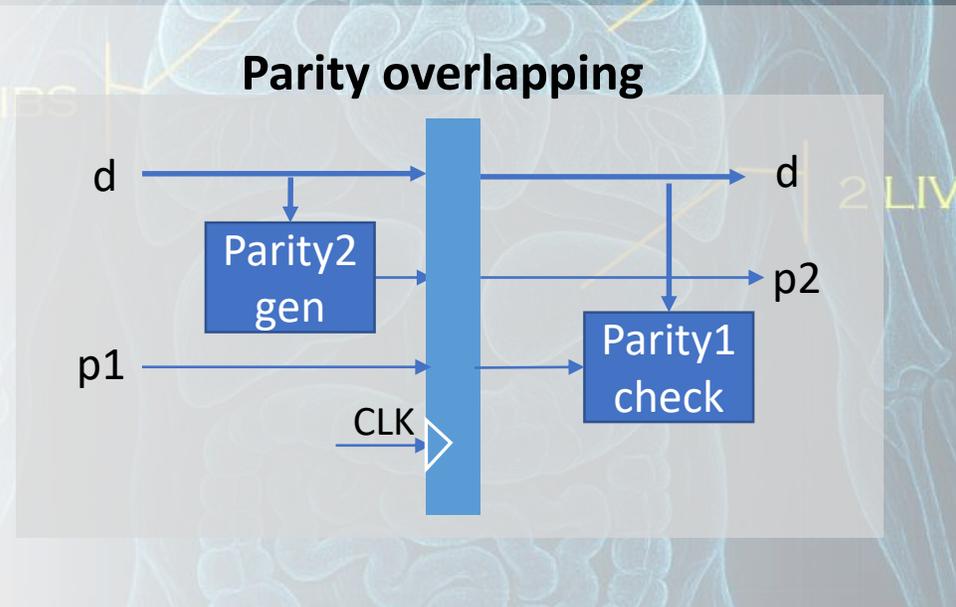
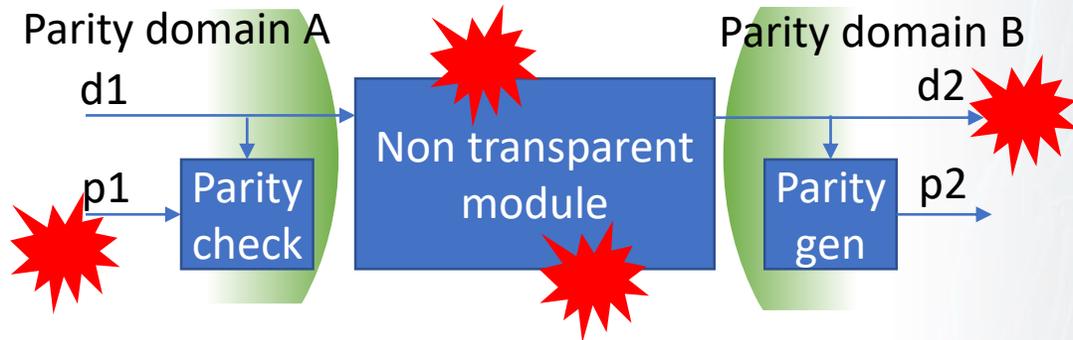
- Encryption /decryption
- Scrambler
- LDPC

Difficult!  
Especially for the write path

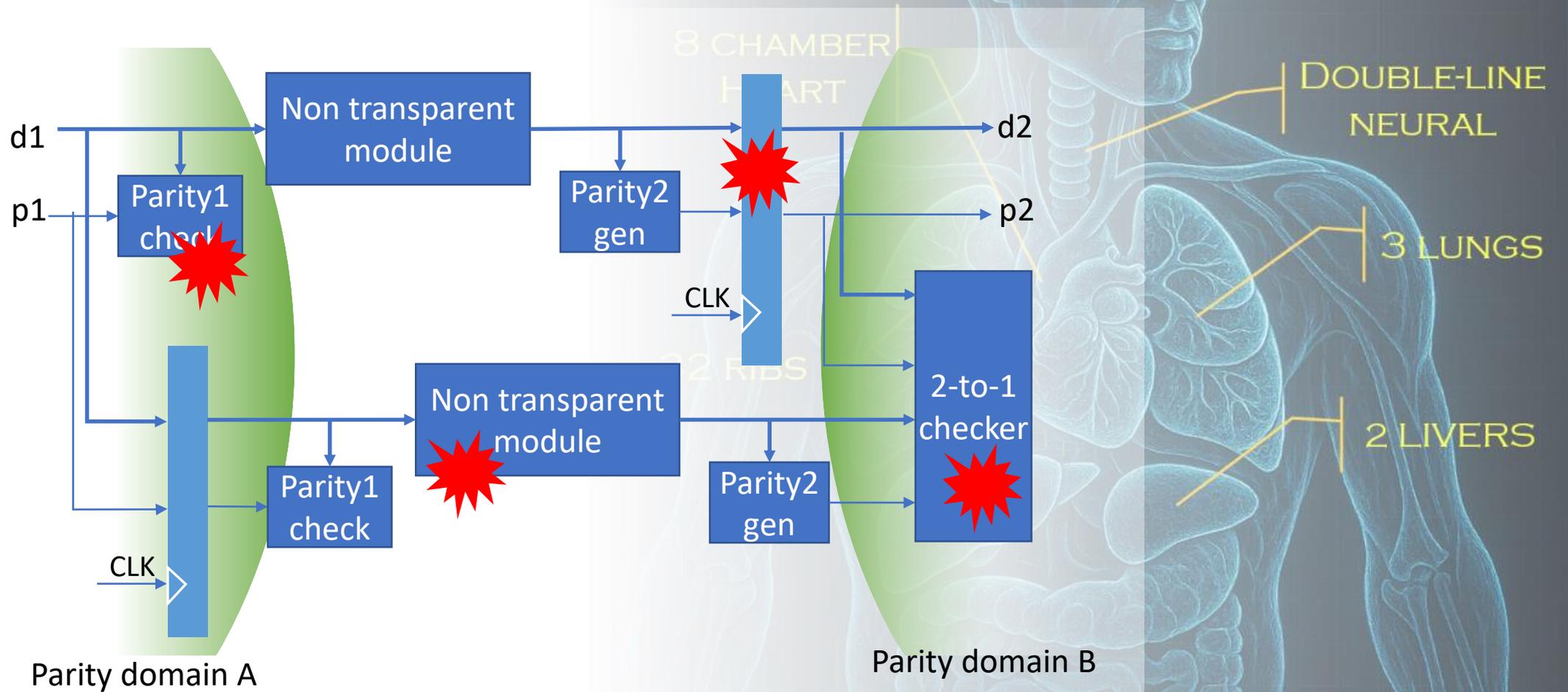


# Non-transparent modules

- Encryption, Compression, Scrambler, Encoding ... etc
- Invalidate existing parity or ECC
  - Data is modified intentionally.
- Isolate parity domain

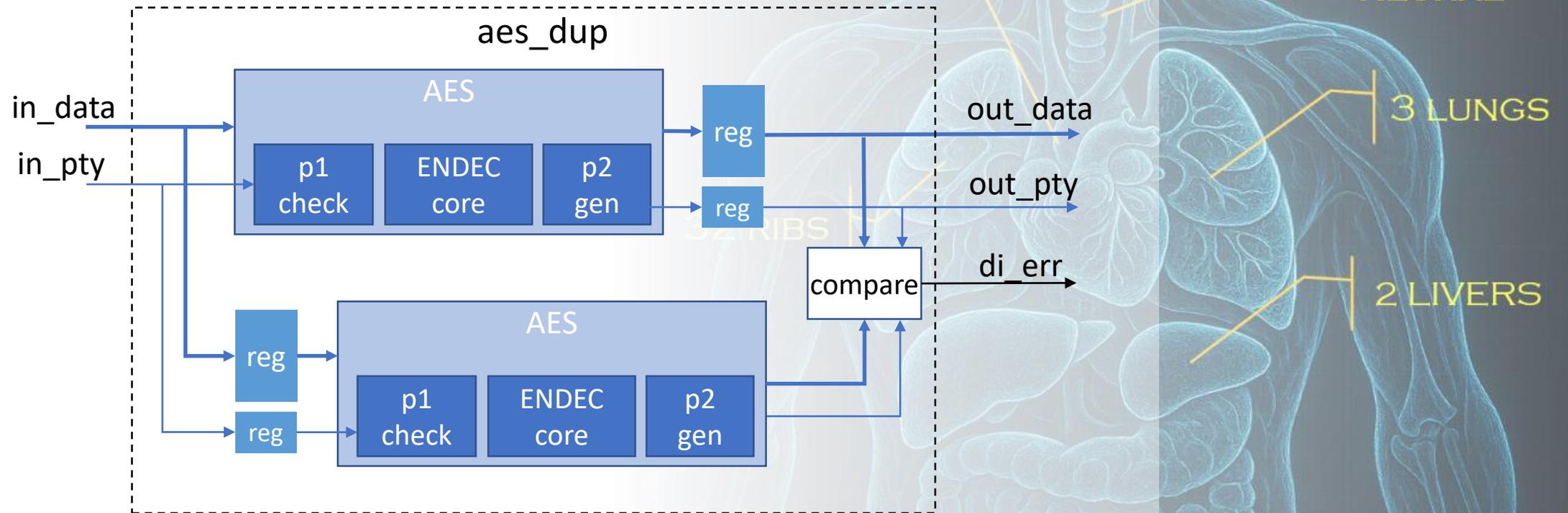


# Non-transparent modules

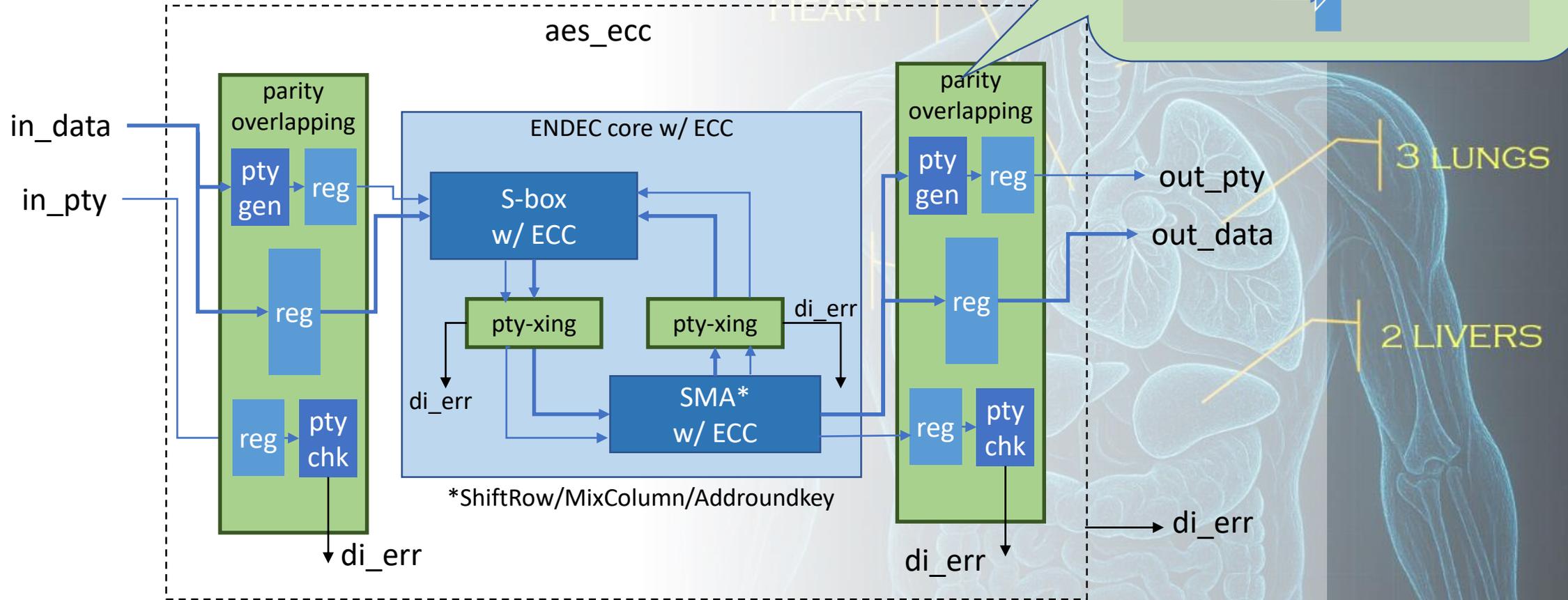


# Duplicated modules

- How about huge module like AES?



# Protected modules



# Comparison

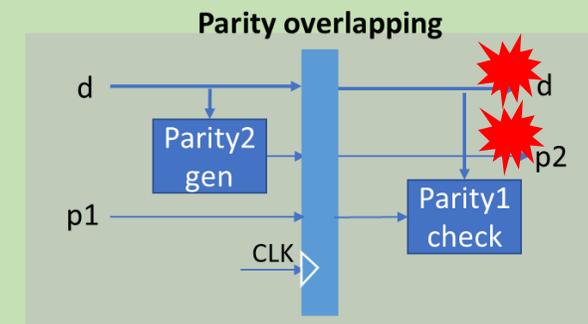
## HW results

AES endec	area	Average power	Peak power
Duplication	149k	16.5	21.1
ECC Protection	120k	12.1	15.2
	80.53%	73.3%	72.04%

## Fault simulation

AES endec	Total injected fault	Non detection rate
Duplication	39489252	0.48%
ECC Protection		0.89%

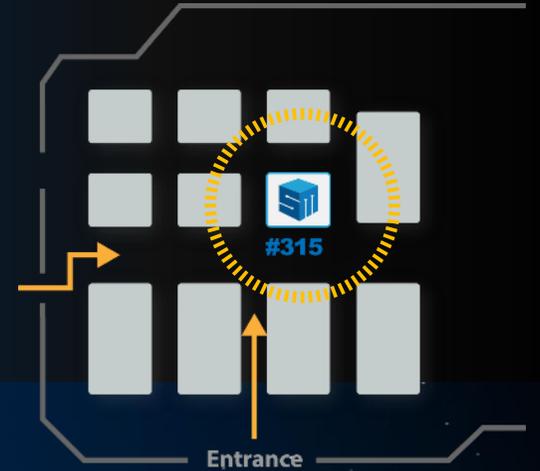
Fault at output interface, will be detected at the next stage.



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