A Distributed Controller for Flexible Applications in the AI Era

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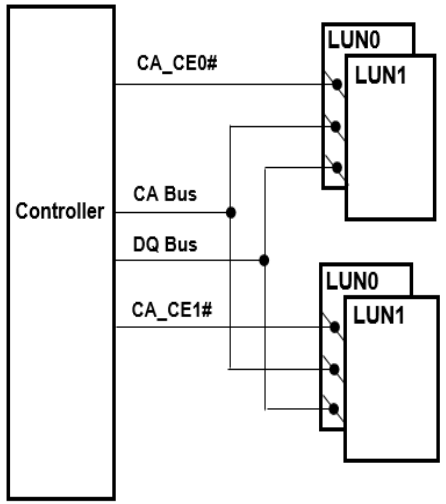
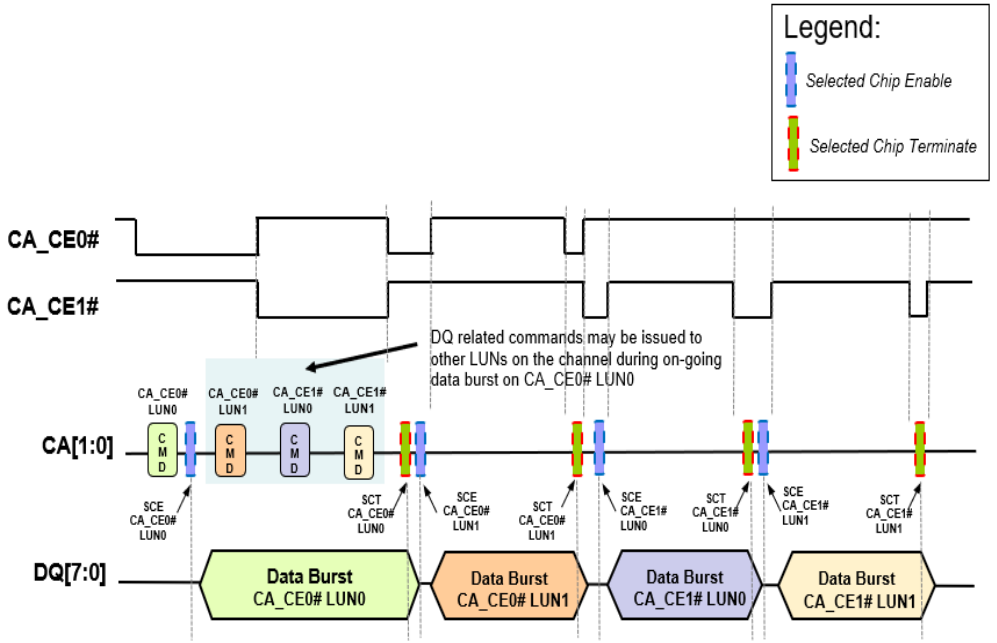
Agenda

- Latest NAND Technology
- The AI Challenge
- Controller Innovation: Meeting New Demands
- Looking Ahead: The Future of NAND in the AI Era

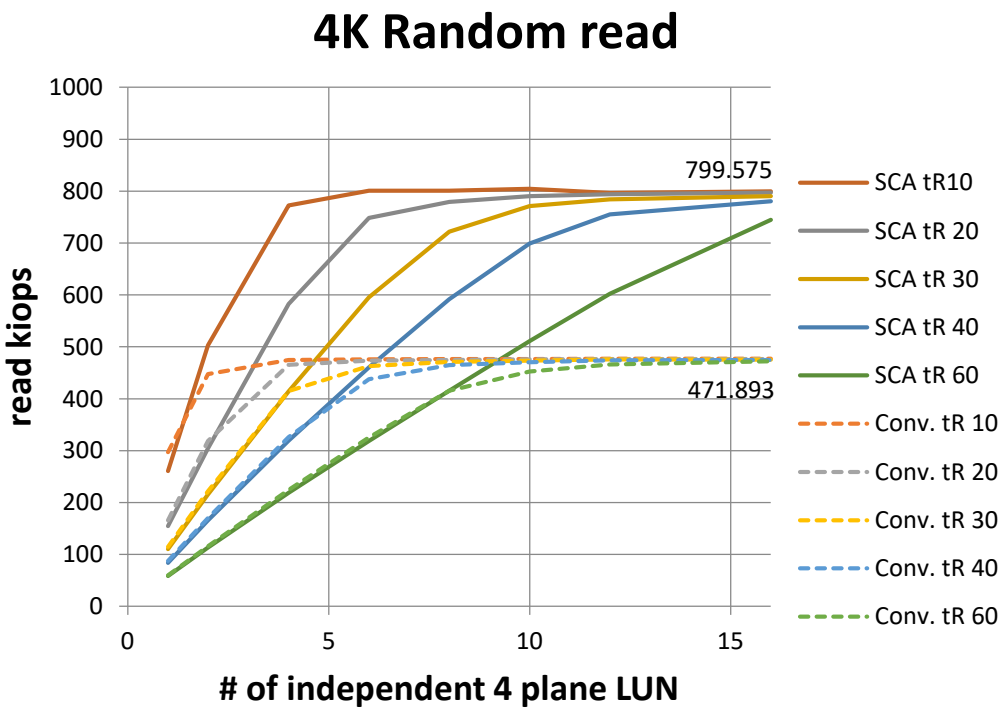
Overview

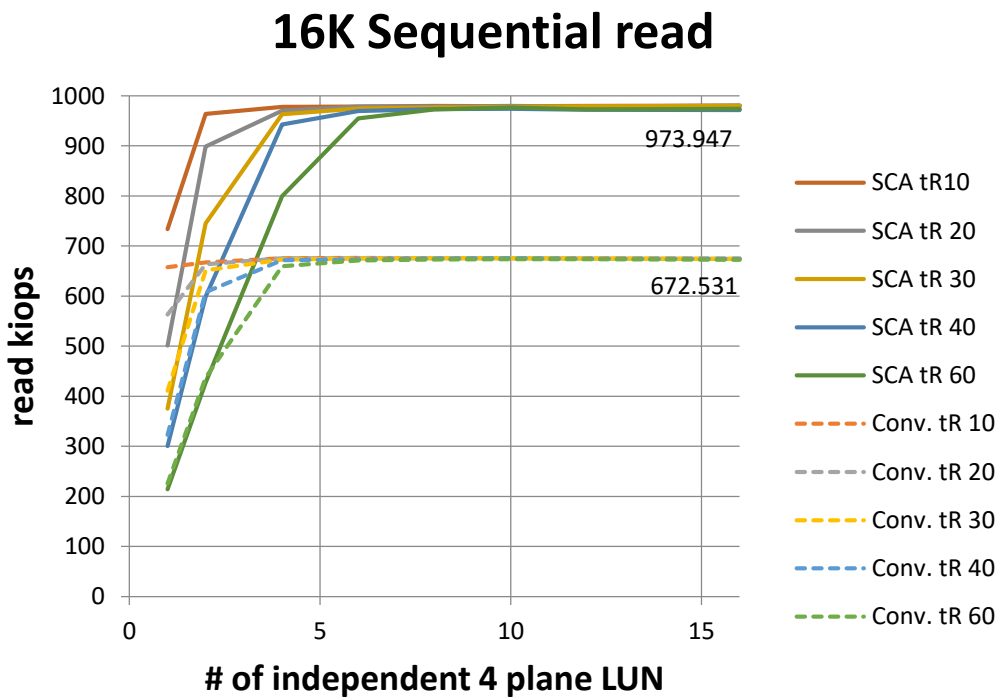
- NAND flash memory is a core component in modern storage systems.
- NAND interface speeds are rapidly evolving.
- ONFI 5.1 update and its key innovation—the Separate Command Address (SCA) protocol





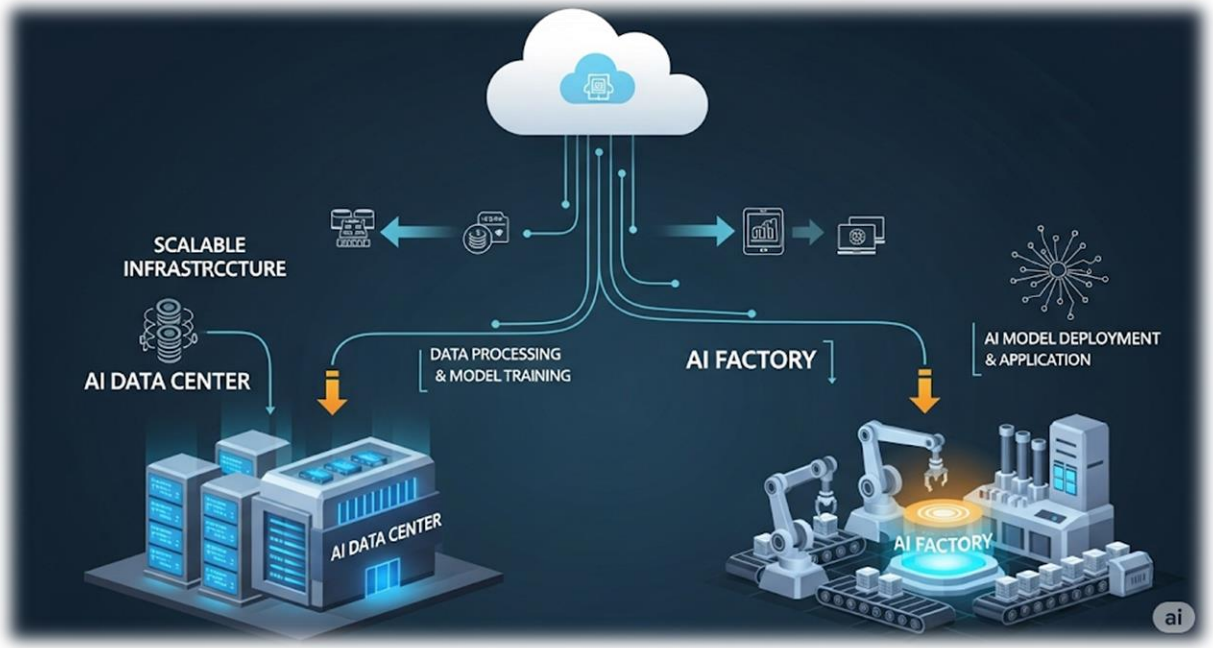
Comparison SCA and Conv. at DDR4800





Current Challenges in the NAND Industry

- **AI workloads demand more flexible and high-performance storage solutions**
  - Massive Data Throughput
  - Parallel Access & Scalability
  - High-Capacity & Tiered Storage
  - Inference Optimization

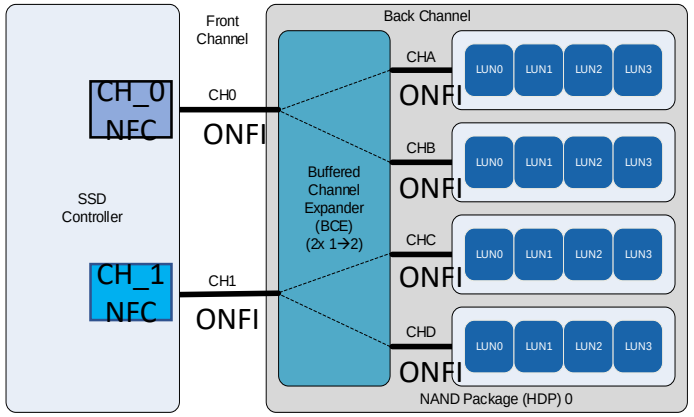


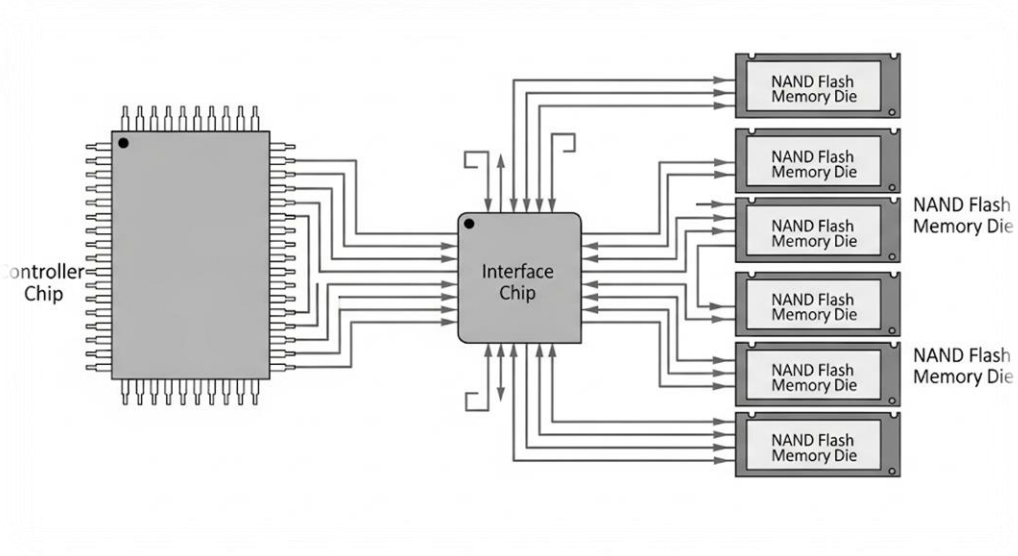
Current Challenges in the NAND Industry

- **Critical Pain Points in NAND Technology**
  - Performance Bottlenecks
  - Signal quality
  - Energy consumption

Current Challenges in the NAND Industry

- Increased Performance and Scalability
- Enhanced Signal Integrity



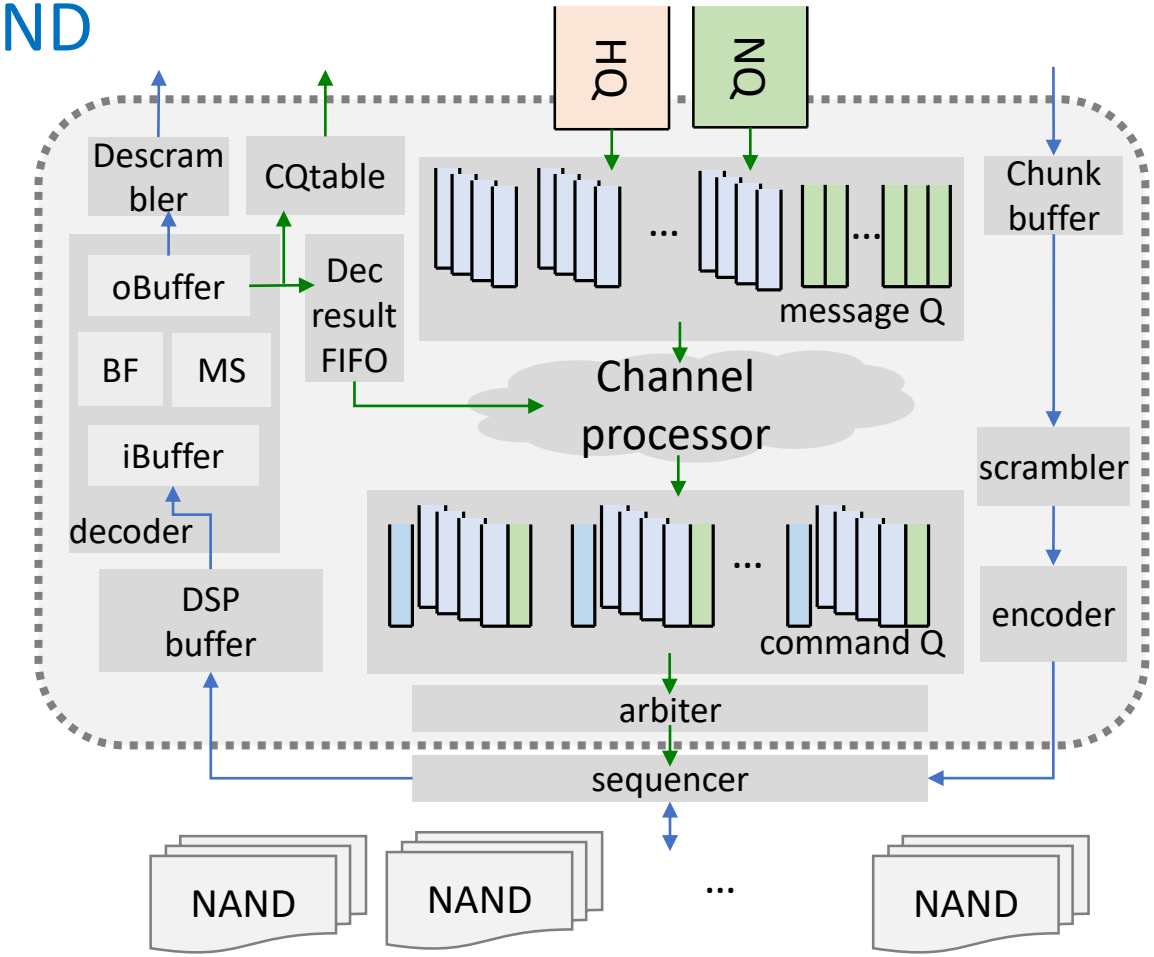


Controller Innovation: Meeting New Demands

- Parallelism and Channel Scaling
- Intelligence
- QoS & Latency Management
- Compute-in-Storage (CIS) / Computational Storage

A simple architecture of FPU

- Take care all dirty works of NAND
  - Error retry
  - Media healthiness
- Transparent and error free access
  - Physical address access
  - Low latency



Distributed Controller

DPU

NVMe, FTL, GC, Near data process

Example
- SerDes / PCIe switch
- Compression/deduplication
- AI inference accelerator

…etc

FPU

Transparent Error-free NAND access

Example
- Enterprise FPU
- Specialized sequential read FPU
- FPU w/ 512B for GPU IO

…etc

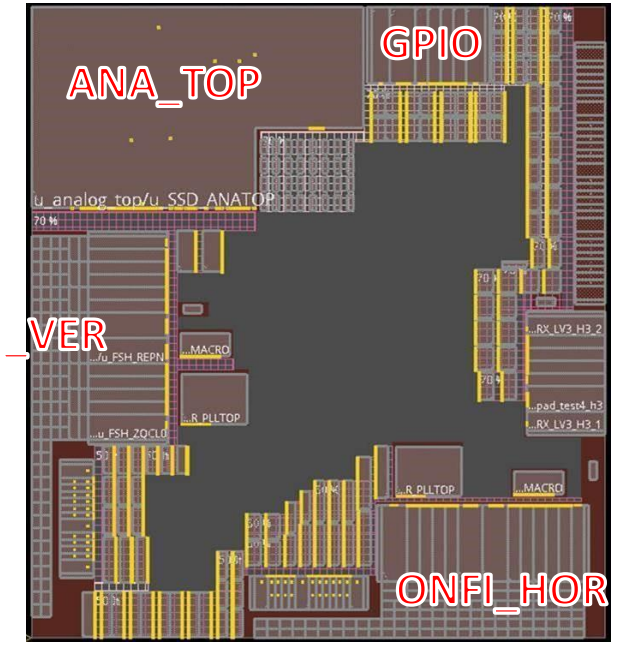
- Flexibility
  - 4CH mainstream => DPU + 4CH FPU
  - 8CH performance => DPU + 4CH FPU x 2
- Efficient data transfer, power saving
  - coded data on ONFI (w/ LDPC parity) => data (w/o LDPC parity) on SerDes.
- Better thermal distribution
- Fault tolerant (e.g. DPU 12nm, FPU 6nm), Zig-Zag update.
- Highly customizable: DPU x FPU

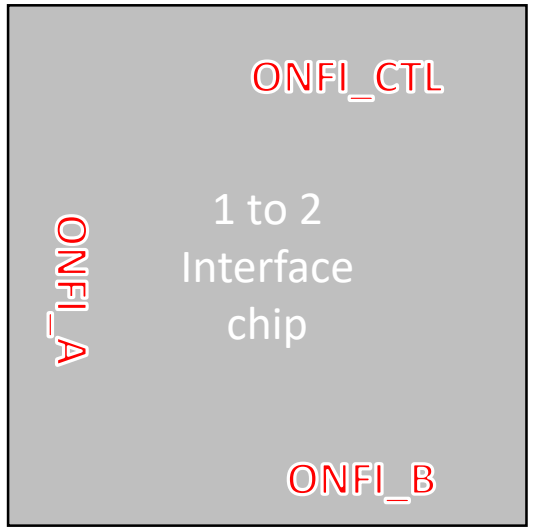
Buffer chip V.S. FPU

Feature	Analog Switch	Re-driver	Re-timer	FPU direct sub-channels
Function	Routes/selects analog signals	Amplifies and equalizes degraded analog signals	Fully regenerates digital signals (data + clock)	Integrates signal conditioning & protocol handling in controller.
Signal Type	Analog	Analog (with equalization for digital signals)	Mixed-signal (analog front-end, digital regeneration)	Mixed-signal (analog PHYs, digital logic for protocol/timing)
Protocol Aware	No	No	Yes	Full Protocol Awareness
Jitter Handle	no active compensation	Compensates for deterministic jitter (ISI).	Compensates for both ISI and random jitter, resets jitter budget.	Optimal Jitter Control
Noise Impact	Can introduce minimal noise/attenuation	Amplifies existing noise, can add its own noise	Removes noise, retransmits a clean signal	Minimized by design
Complexity & Cost	Low	Medium	High	No extra chip, higher design cost
Timing Delay	Minimal added delay	Some propagation delay	Large delay due to regeneration pipeline	internal pipeline delays
Use Case	NA	Conventional protocol	Conventional + SCA	Conventional + SCA w/o additional latency

FPU Test Chip

- SMI FPU chip with two ONFI interface can double data bandwidth with NAND die use TSMC shuttle to make a silicon prove at end of 2025





Why not utilize it better?

Looking Ahead: The Future of NAND in the AI Era

- **Trends and Vision:**
  Continued evolution of chiplet technology
- **AI Everywhere**:
  From cloud to edge, AI is driving new storage demands.
- **Intelligent Storage**:
  Controllers will evolve to become smarter and more autonomous.
- **Collaboration**:
  Stronger partnerships between NAND vendors and AI platform providers.
- **Next Steps**:
  Expand support for emerging NAND technologies.
  Deep integration with AI frameworks and hardware.

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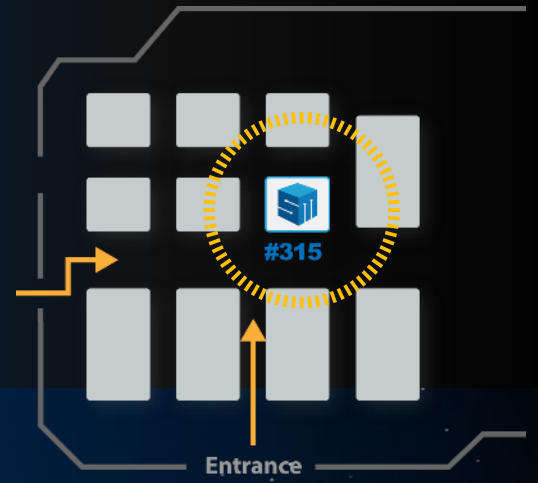

Smart Storage in Motion: From Silicon Innovation to AI Transformation Across all Spectrums!