PCIe® Technology in AI/ML: Maintaining High-Speed Connectivity

FMS 2025 Panel

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About Our Moderator

Al Yanes

PCI-SIG® President

Al Yanes has served as president of the PCI-SIG since 2003 and chairman since 2006 and is a Senior Technical Staff Member at IBM in the IBM FlashSystems Solutions group. He has 40 years of experience working with ASIC /FPGA designs in the I/O industry. Yanes holds 40+ patents for PCI™ and other I/O technologies. Yanes holds a B.S. in computer engineering from Rensselaer Polytechnic Institute.

PCI-SIG® Snapshot

- Organization that **defines the PCI Express® (PCIe®) I/O bus specifications and related form factors like the CopprLink™ Internal and External Cables**
- PCI-SIG was established in 1992
- The PCIe specification was first released in 2003
- Reached **1,000** member companies in Nov. 2024
- Creating specifications and mechanisms to **support compliance** and **interoperability**

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PCI Express® 7.0 Specification Now Available

PCIe® 7.0 Specification released to PCI-SIG Members on June 11, 2025

PCIe 7.0 Specification Key Features and Enhancements:

- Delivers 128.0 GT/s raw bit rate and up to 512 GB/s bi-directionally via x16 configuration
- Utilizes PAM4 (Pulse Amplitude Modulation with 4 levels) signaling and Flit-based encoding
- Provides improved power efficiency
- Maintains backwards compatibility with previous generations of PCIe technology

PCIe® 8.0 Specification Development Underway

The PCIe 8.0 specification is targeted for 2028

PCIe 8.0 Specification Target Features:

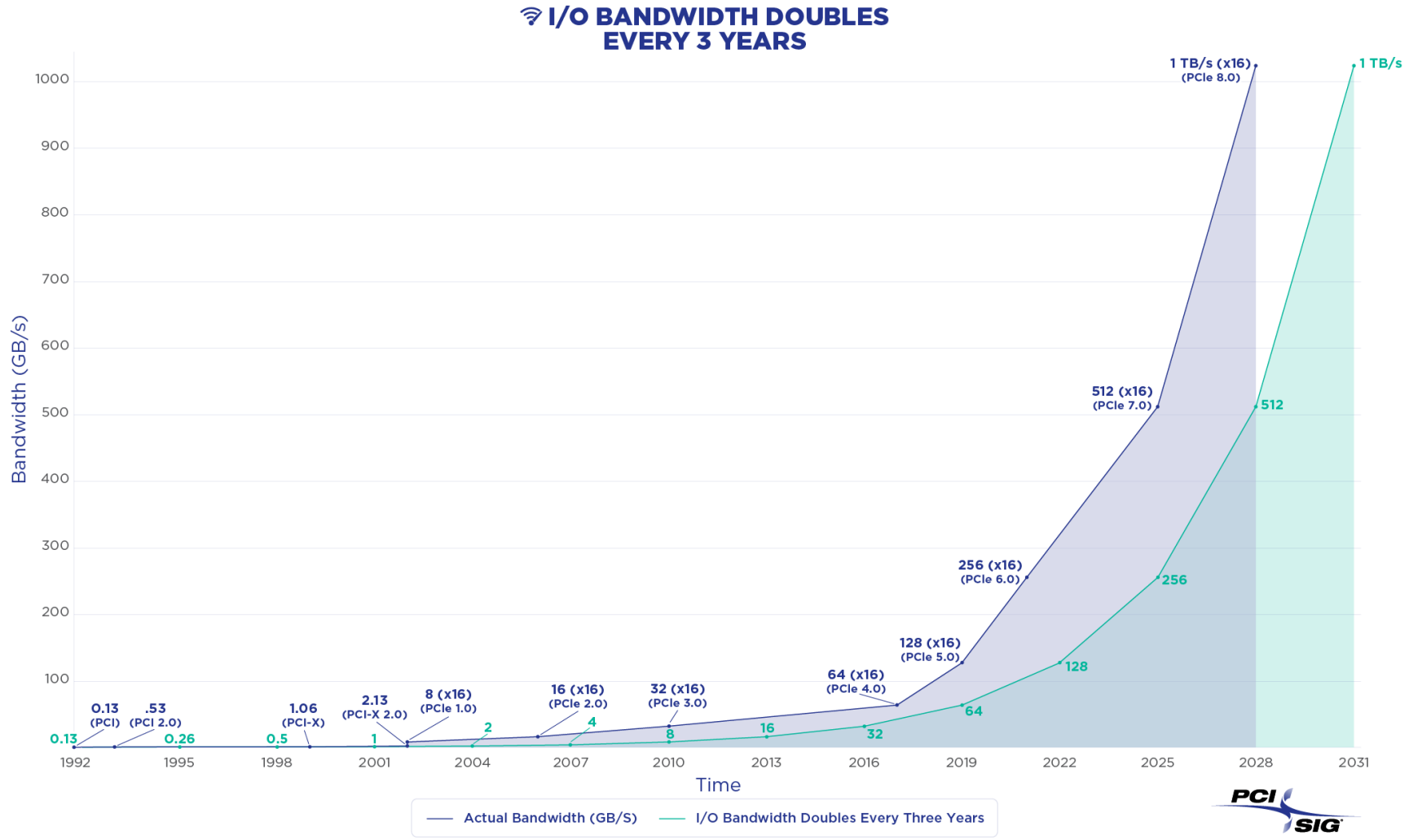
- Deliver 256.0 GT/s raw bit rate and up to 1 TB/s bi-directionally via x16 configuration
- Utilize PAM4 (Pulse Amplitude Modulation with 4 levels) signaling and Flit-based encoding
- Double frequency of PCIe 7.0 specification
- Maintain backwards compatibility with previous generations of PCIe technology
- Protocol enhancements

Revision**	Max Data Rate	Encoding	Signaling
PCIe 8.0 (2028)	256.0 GTs	1b/1b (Flit Mode*)	PAM4
PCIe 7.0 (2025)	128.0 GT/s	1b/1b (Flit Mode*)	PAM4
PCIe 6.0 (2022)	64.0 GT/s	1b/1b (Flit Mode*)	PAM4
PCIe 5.0 (2019)	32.0 GT/s	128b/130b	NRZ
PCIe 4.0 (2017)	16.0 GT/s	128b/130b	NRZ
PCIe 3.0 (2010)	8.0 GT/s	128b/130b	NRZ
PCIe 2.0 (2007)	5.0 GT/s	8b/10b	NRZ
PCIe 1.0 (2003)	2.5 GT/s	8b/10b	NRZ

(*Flit Mode also enabled in other Data Rate with their respective encoding).

**The PCIe specifications are living documents and have multiple versions and Engineering Change Requests (ECNs).Refer to the PCI-SIG website for the most recent version.

PCI-SIG® Roadmap



PCIe® Speeds/Feeds - Pick Your Bandwidth

- **Flexible to meet needs from handheld/client to server/HPC**
- **~Max Total Bandwidth = Max RX bandwidth + Max TX bandwidth**
- **35 Permutations yielding 11 unique bandwidth profiles**
- **Encoding overhead and header efficiency not included**

Specifications	Lanes				
	x1	x2	x4	x8	x16
2.5 GT/s (PCIe 1.x +)	500 MB/S	1 GB/S	2 GB/S	4 GB/S	8 GB/S
5.0 GT/s (PCIe 2.x +)	1 GB/S	2 GB/S	4 GB/S	8 GB/S	16 GB/S
8.0 GT/s (PCIe 3.x +)	2 GB/S	4 GB/S	8 GB/S	16 GB/S	32 GB/S
16.0 GT/s (PCIe 4.x +)	4 GB/S	8 GB/S	16 GB/S	32 GB/S	64 GB/S
32.0 GT/s (PCIe 5.x +)	8 GB/S	16 GB/S	32 GB/S	64 GB/S	128 GB/S
64.0 GT/s (PCIe 6.x +)	16 GB/S	32 GB/S	64 GB/S	128 GB/S	256 GB/S
128.0 GT/s (PCIe 7.x +)	32 GB/S	64 GB/S	128 GB/S	256 GB/S	512 GB/S
256.0 GT/s (PCIe 8.x +)	64 GB/S	128 GB/S	256 GB/S	512 GB/S	1 TB/S

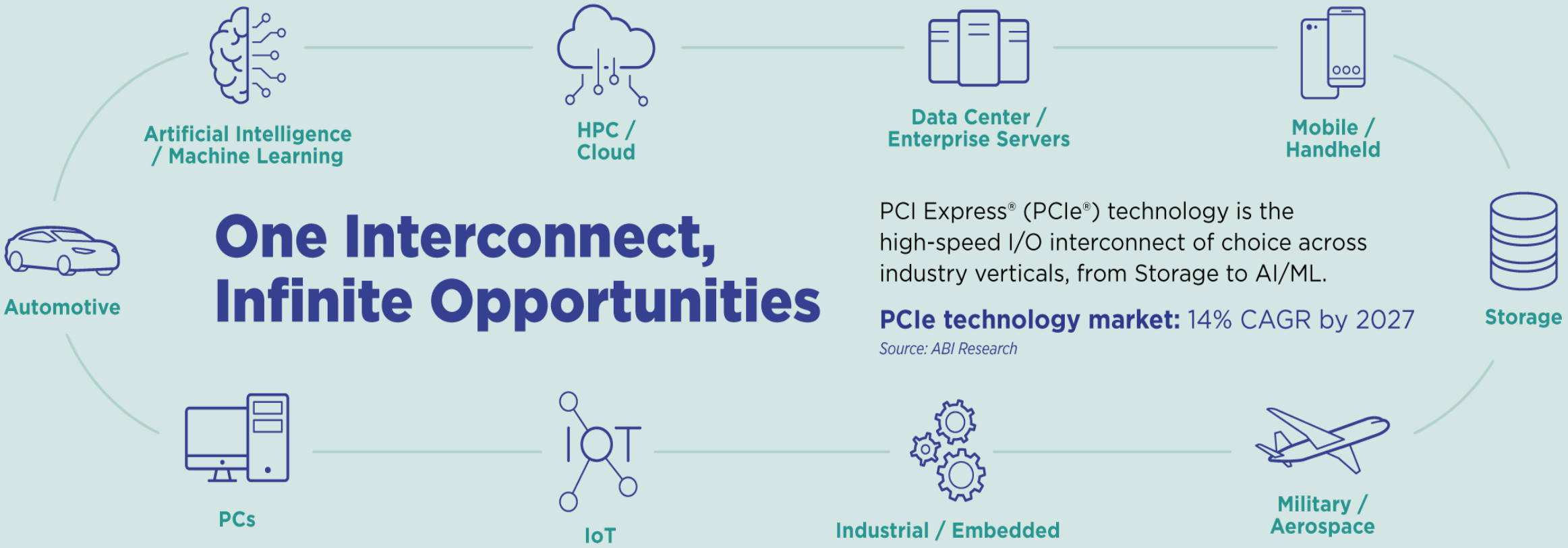
+ = data rate supported by this and subsequent spec revisions.

Optical Aware Retimer Specification

PCI-SIG® released the industry's first standard-based optical PCIe® solution to members on June 11, 2025

- **Why did PCI-SIG develop an Optical Aware Retimer?**
  - The objective of the Optical Work group has been to standardize optical PCIe architecture in a way that is easily transferred to existing PCIe 6.0 designs and devices and is included in the new PCIe 7.0 specification; experts from Logic, Protocol, Optical, and Electrical supported the creation of this solution
- **Optical Aware Retimer ECN**
  - Seamlessly enables various optical technologies for optical interconnection between existing PCIe 6.4 and 7.0 specification-compliant Switch, Root-Complex and Endpoint silicon designs
  - Grants extended reach across racks and pods
  - Allows multiplexing and data mapping across electrical and optical domains
  - Enables more compact implementations than electrical copper solutions
- **Target Market Segments:**

PCIe® Architecture in Industry Verticals



Panel Members

Meet the Speakers

Sam Kocsis

Amphenol

Director of Standards and Technology

&

PCI-SIG Cabling Workgroup Chair

Ron Lowman

Synopsys

PCIe/CXL Product Management

Casey Morrison

Astera Labs

Chief Product Officer