Emerging Trends in Automotive Fabrics and Data Security

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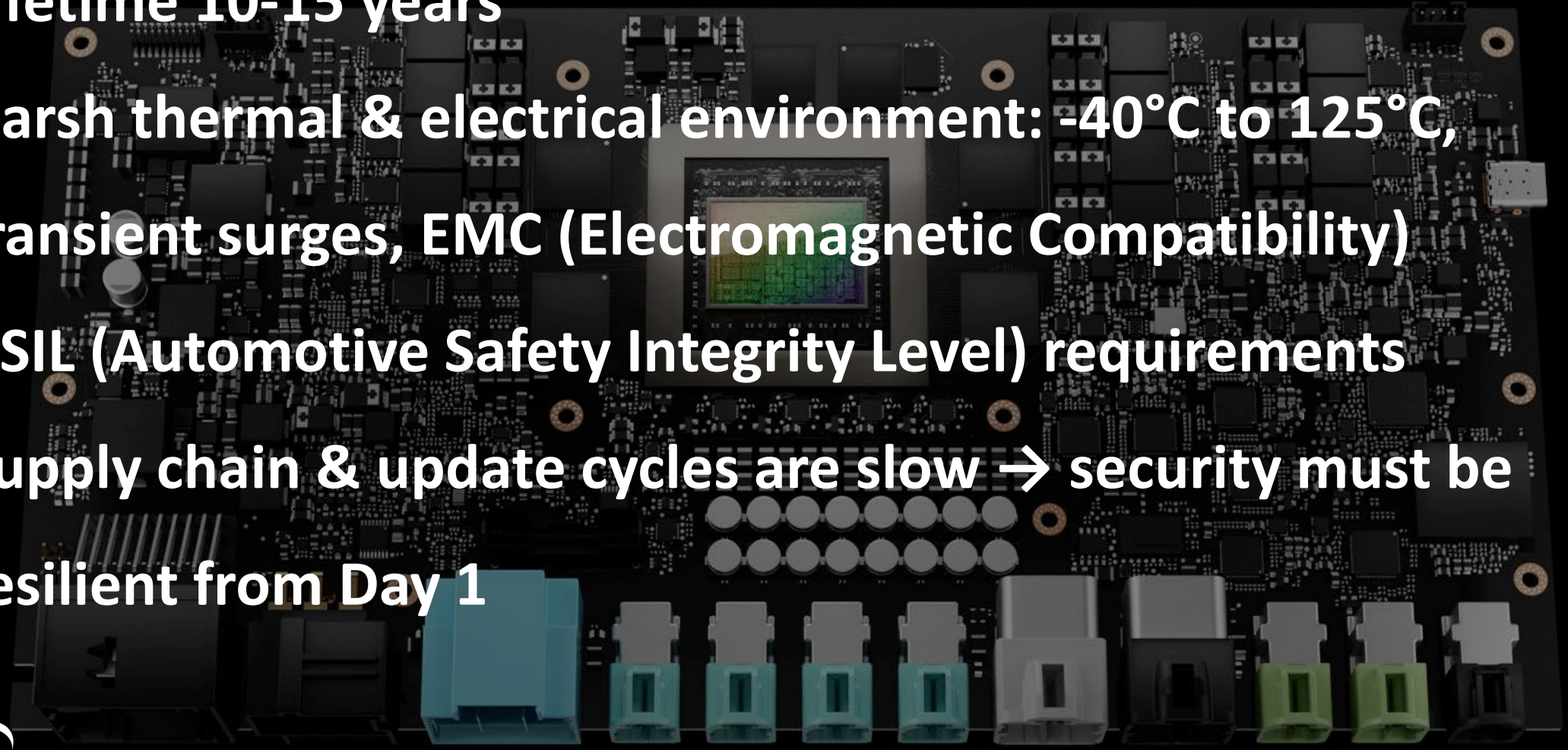
the Future of Memory and Storage

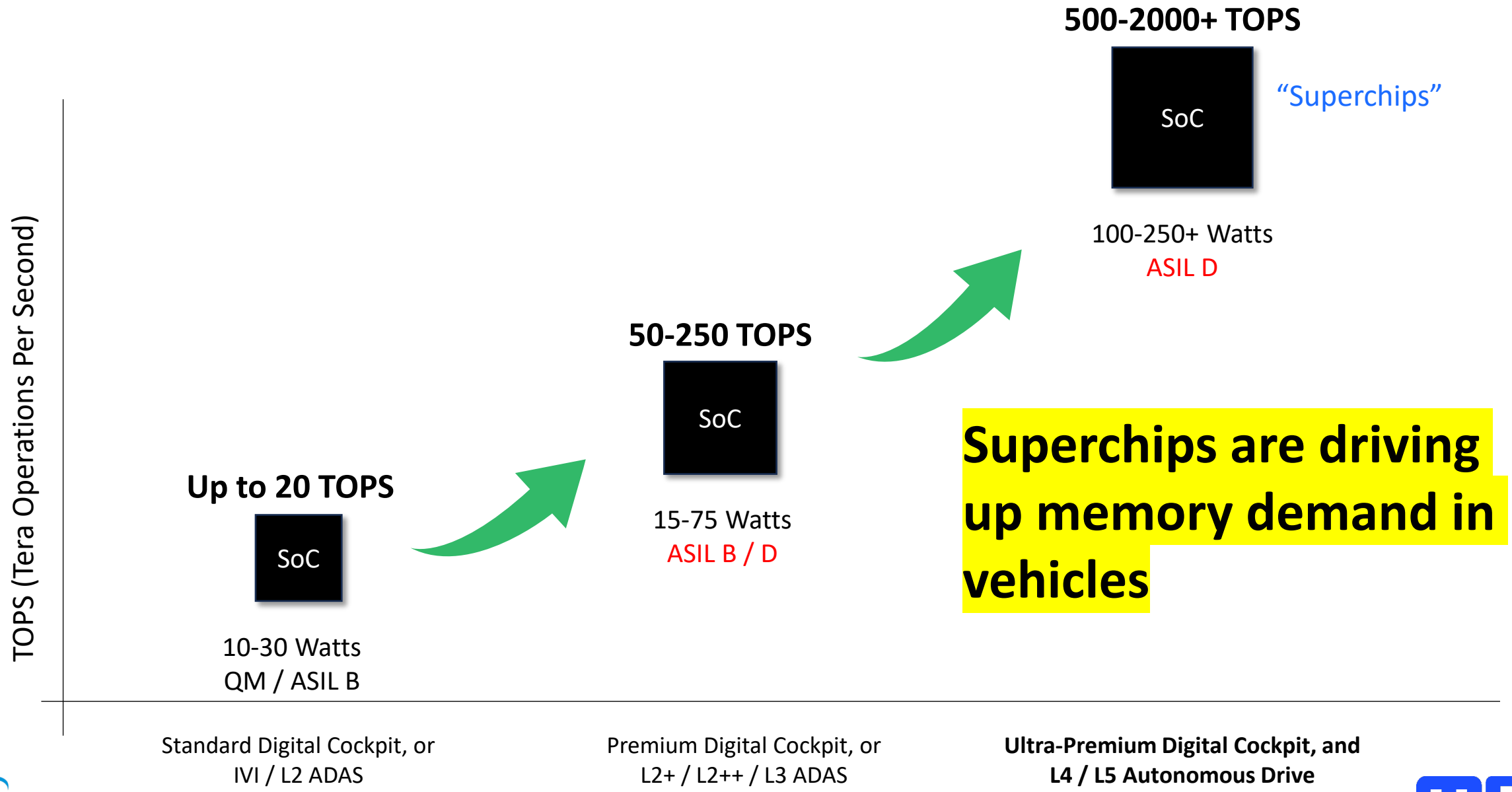
What's Different When Memory Goes Into Cars?

- Lifetime 10-15 years
- Harsh thermal & electrical environment: -40°C to 125°C, transient surges, EMC (Electromagnetic Compatibility)
- ASIL (Automotive Safety Integrity Level) requirements
- Supply chain & update cycles are slow → security must be resilient from Day 1



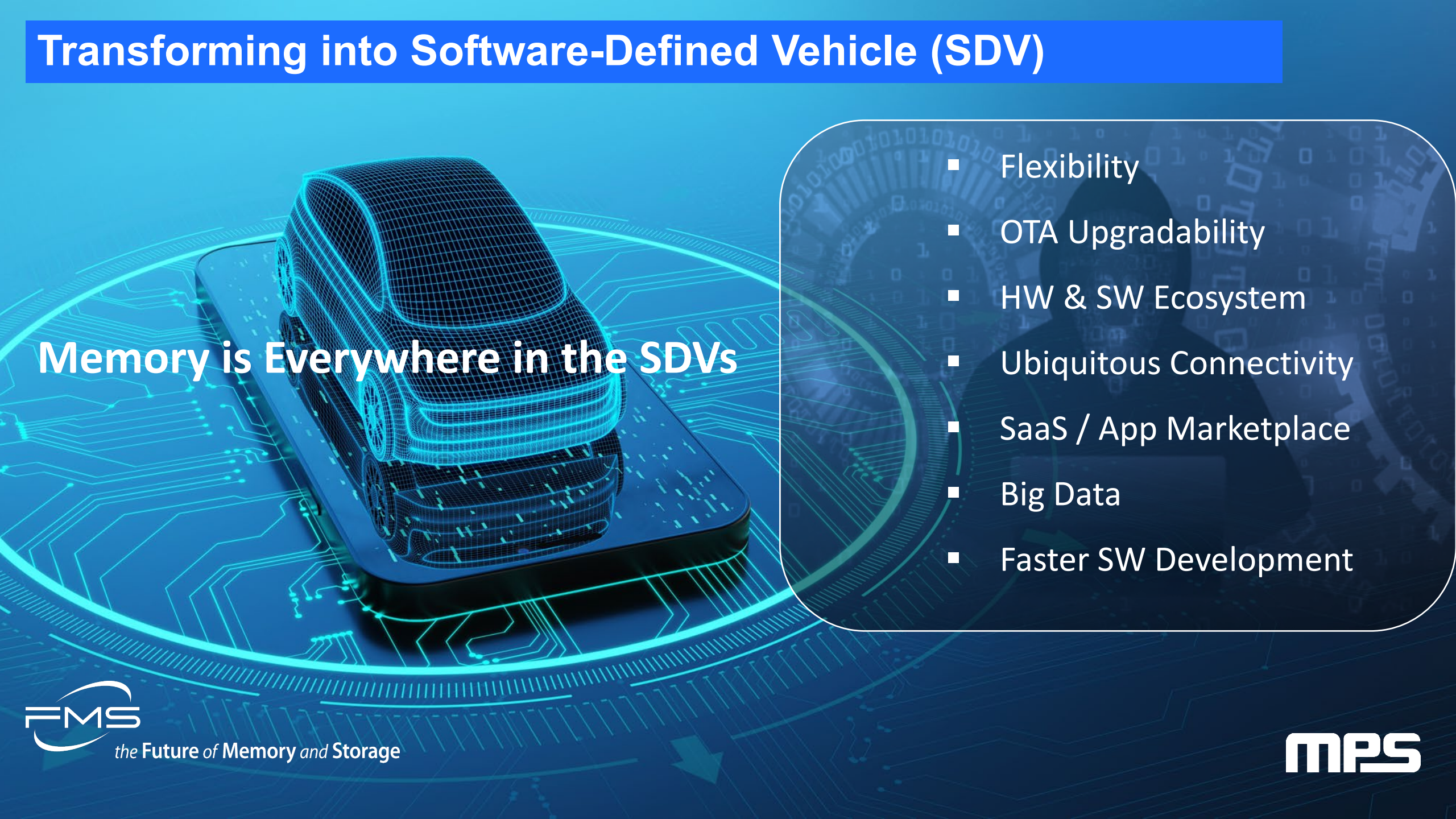
NVIDIA DRIVE Thor – publicly announced late 2022

High Performance Computing Puts Memory at the Heart of the Car



Superchips are driving up memory demand in vehicles

Transforming into Software-Defined Vehicle (SDV)



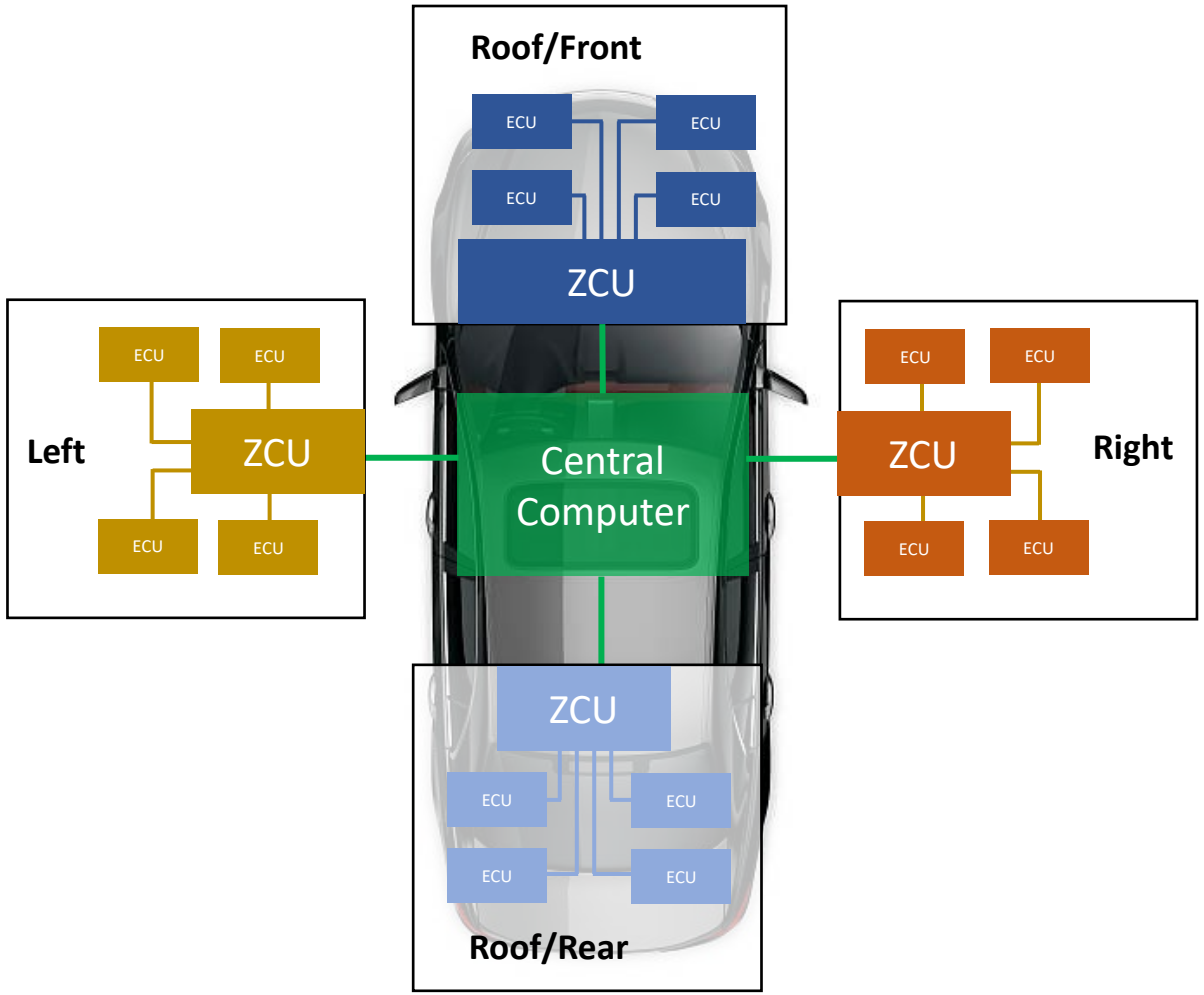
Memory is Everywhere in the SDVs

- Flexibility
- OTA Upgradability
- HW & SW Ecosystem
- Ubiquitous Connectivity
- SaaS / App Marketplace
- Big Data
- Faster SW Development

FMS the Future of Memory and Storage

MPS

The Emerging Attack Surface in SDVs

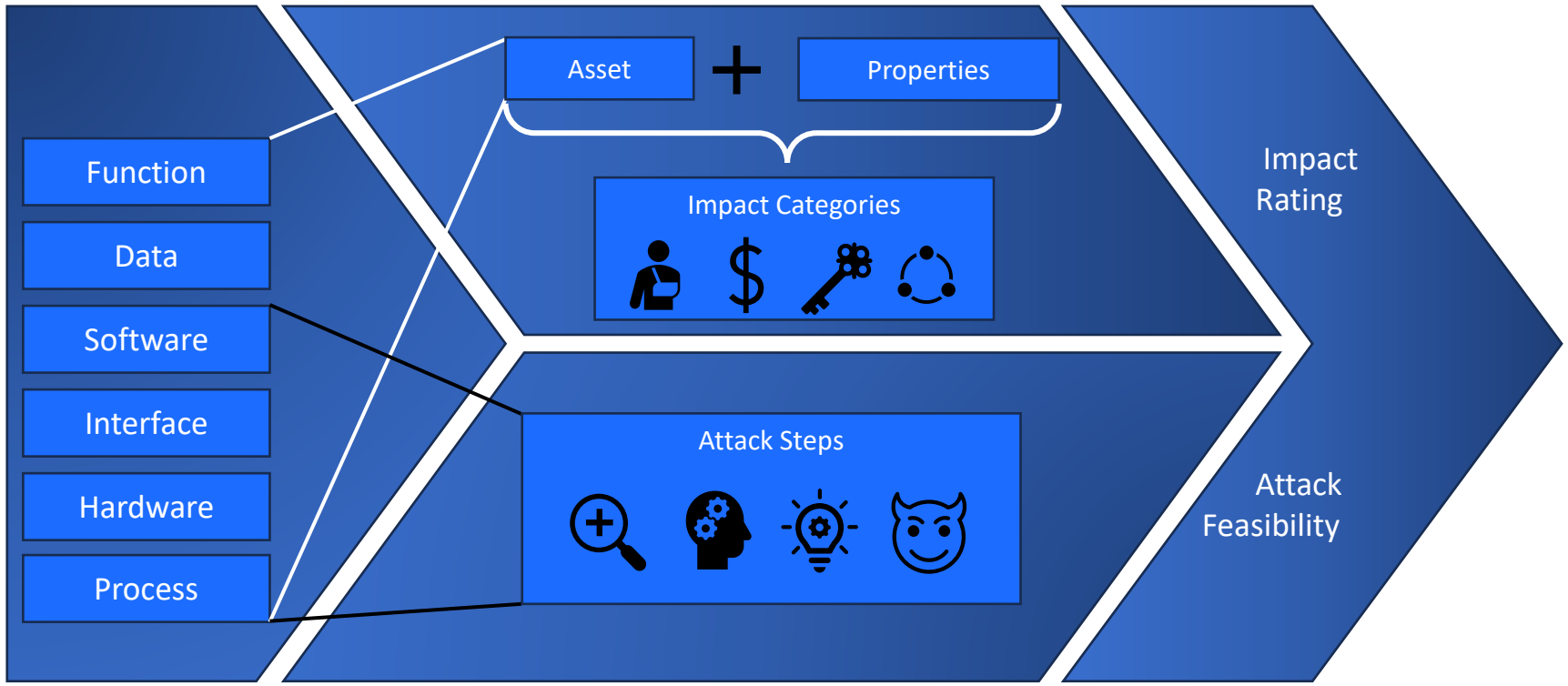


Zonal architecture

- Zonal architecture and Centralizes compute, making memory central to vehicle operation
- More memory usage → more potential attack surfaces
- SDVs mean OTA updates, frequent reconfigurations → DDR must maintain security long-term

Memory Security Gaps

- Spoofing
- Row hammer
- Unauthorized access
- Man-in-the-middle



SPDM: A Good Start, but Not Sufficient

- SPDM = Platform Security Protocol (used for auth & secure messaging)
- Works well in servers, but still spoofable in some cases (e.g., cloned serials)
- Requires frequent updates → **requalification headache in automotive**

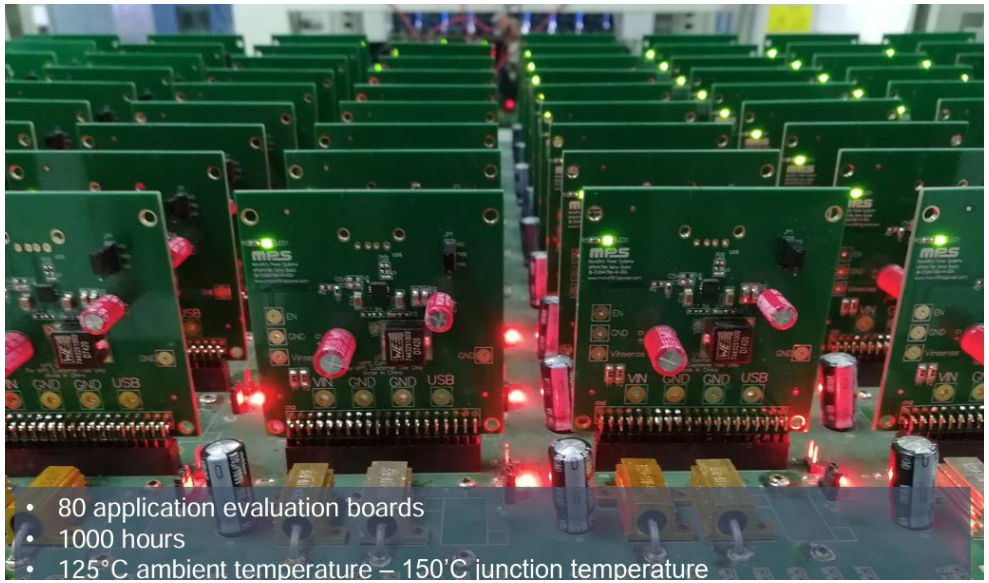
Table 2 Test #	A2	A3	A4	A5	A6	B1	B2	B3	C1	C2	C3	C4	C5	C6	D1	D2	D3	D4	D5	E2	E3	E4	E5	E7	E9	E10	E11	E12	G1-	G5	G6	G7	G8
Test Abbreviation	THB	AC	TC	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	PD	SBS	LI	EM	TDDB	HCI	NBTI	SM	HBM	CDM	LU	ED	CHAR	EMC	SC	SER	LF	MECH	DROP	LT	DS	IWV
DESIGN																																	
Active Element Design		●	●	M		●	●	DJ							D	D	D	D	D	●	●	●	●	●	●	●	●			F			
Circuit Rerouting			A	M																●	●	●	●	●	●	●							
Wafer Dimension / Thickness			E	M		●	●		E	E								●		E	E	E	●										
WAFER FAB																																	
Lithography	●		●	M		●	G		●	●								●					●										
Die Shrink	●	●		M		●	●	DJ							●	●	●	●	●	●	●	●	●	●	●	●	●						
Diffusion/Doping				M		●	G											●		●	●	●	●	●										
Polysilicon			●	M		●		DJ										●		●	●	●	●	●										
Metallization / Vias / Contacts	●	●	●	M		●			●	●					●				●				●	●		●								
Passivation / Oxide / Interlevel Dielectric	K	K	●	M		●	GN	DJ	K	●						●	●	●	●	●	●	●	●	●										
Backside Operation			●	M		●														M	M	●		●					H			H	
FAB Site Transfer	●	●	●	M		●	●	J	●	●					●	●	●	●	●	●	●	●							H			H	
ASSEMBLY																												●					H
Die Overcoat / Underfill	●	●	●	M	●	●																						L				H	
Leadframe Plating	●	●	●	M	●					C	●			●																			
Bump Material / Metal System	●	●	●	M	●	●						●	●													●		L						
Leadframe Material		●	●	M	●					●	●	●		●												●		L	H			H	
Leadframe Dimension		●	●	M							●	●		●												●		L	H				
Wire Bonding	●	●	●	Q	●				●	●													M			●			H				
Die Scribe/Separate	●	●	●	M																													
Die Preparation / Clean	●	●		M		●			●	●																						H	
Package Marking											B																						
Die Attach	●	●	●	M		●																	●			●		L	H			H	H
Molding Compound	●	●	●	M	●	●	●				●	●		●													●	L					
Molding Process	●	●	●	M	●	●					●	●		●														L					
Hermetic Sealing		H	H		H							H		H															H		H		H
New Package	●	●	●	M	●	●	●		●	●	●	●	T	●						●	●		●			●		L	H			H	H
Substrate / Interposer	●	●	●	M	●	●			●	●			T															L	H			H	H
Assembly Site Transfer	●	●	●	M		●	●		●	●	●	●	T	●									●					L	H			H	H

- • Highly Recommended

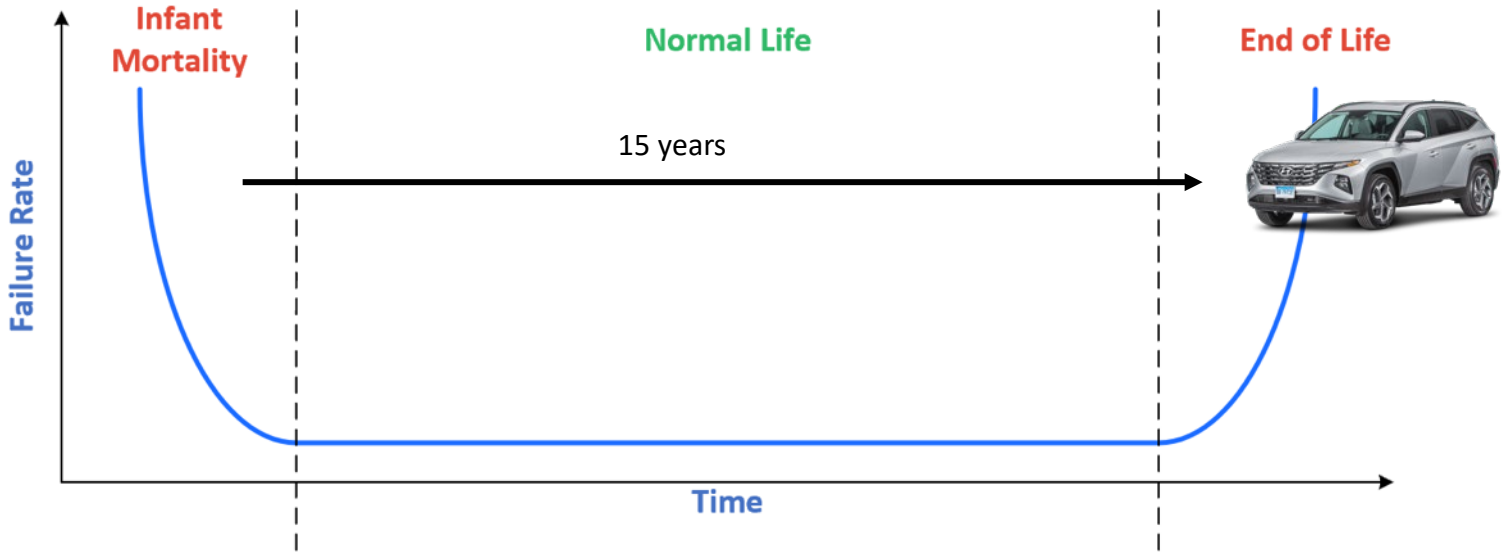
A Only for peripheral routing
B For symbol rework, new cure time, temp
C If bond to leadfinger
D Design rule change
E Thickness only

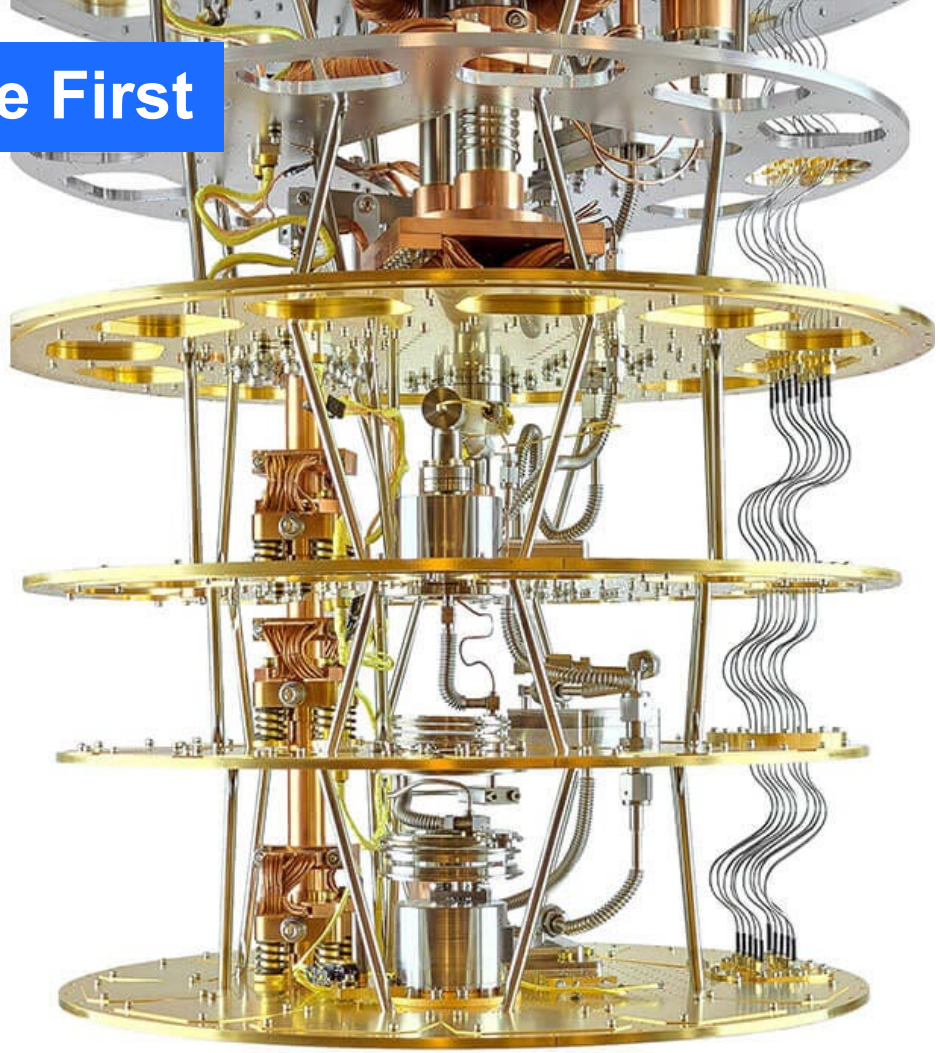
F MEMS element only
G Only from non-100% burned-in parts
H Hermetic only
J EPROM or E^2PROM
K Passivation only

L For Pb-free devices only
M For devices requiring PTC
N Passivation and gate oxide
Q Wire diameter decrease
T For Solder Ball SMD only



Post-Quantum Threats: Why Automotive Might Be First





- Cars shipping in 2025 may still be on the road in 2040
- PQC-ready hardware for memory encryption and secure boot will likely appear in robotaxi first
- Memory vendors need to consider future-proofing hardware-level encryption/latency tradeoffs

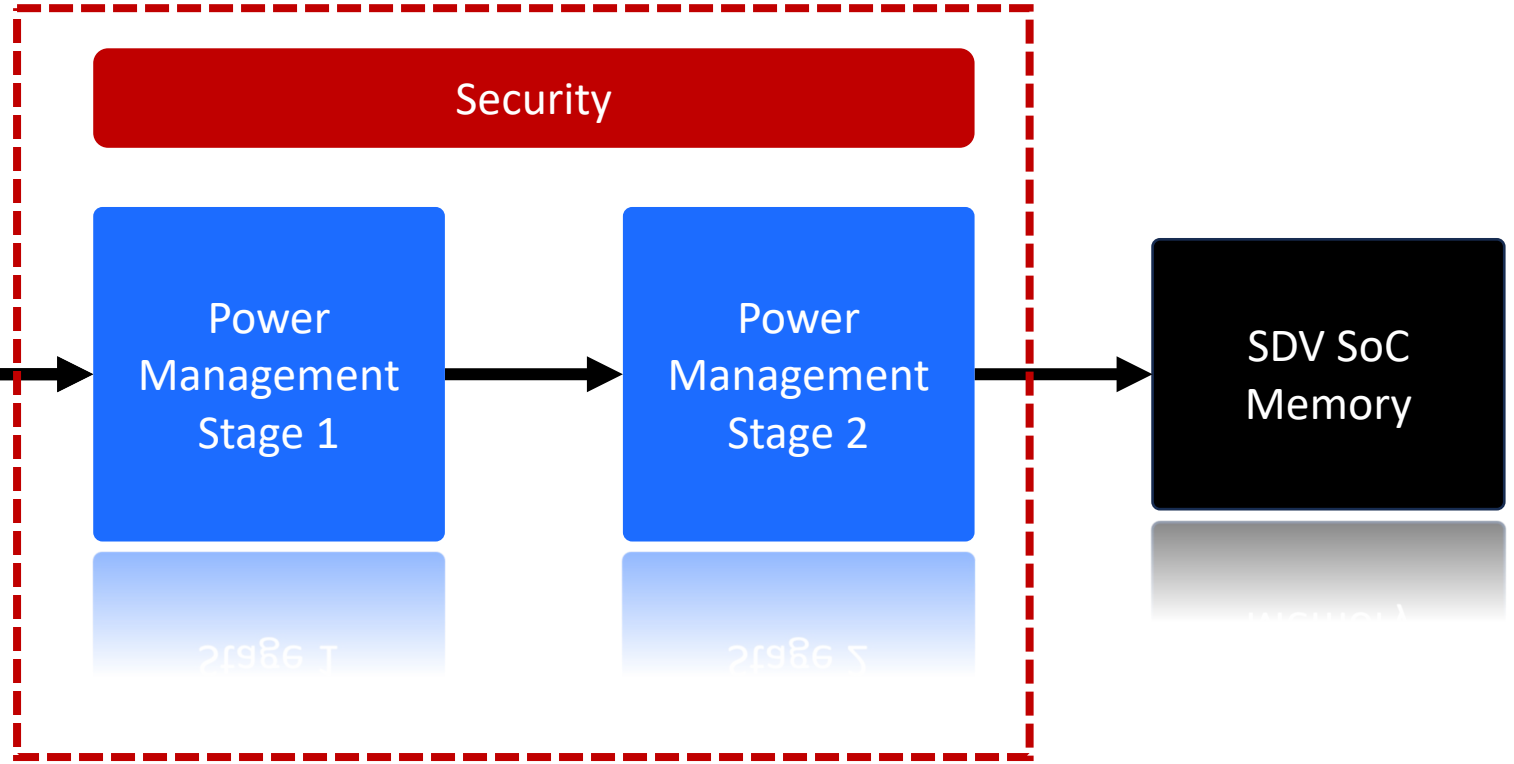
The Missing Link Between SoC and Memory

- Today, Memory has no strong identity verification at boot
- If compromised, SoC can’t distinguish genuine vs. spoofed memory
- Need a new trust anchor—closer to the physical connection

Power, Once an Afterthought, Can Make Data Security

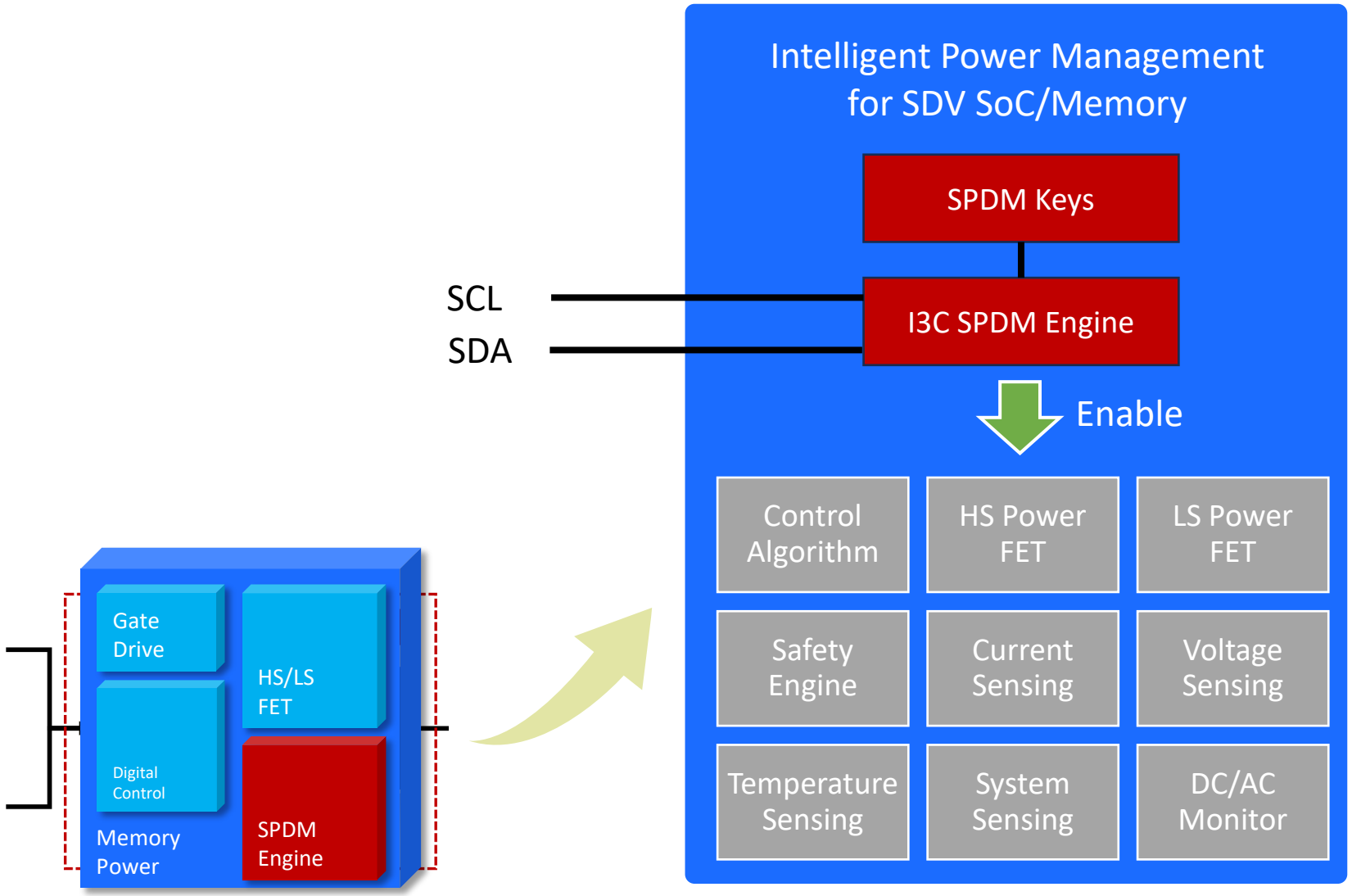
12V/48V Battery

EV Battery

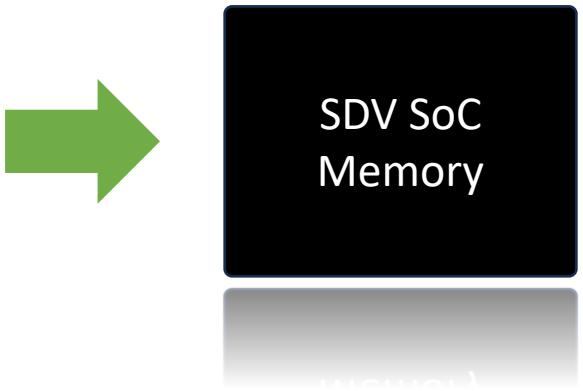


- PMICs already sequence memory power, control I3C
- Natural location to enforce security policies before memory is accessible
- Low-level access = strong control point

PMIC with Embedded SPDM + PQC



- PMIC performs SPDM handshake with host and memory
- Can store certified hash keys, implement PQC algorithms
- Allows memory access **only after authentication passes**



Benefits for Memory Vendors

- Offloads SPDM/PQC complexity from memory module
- No need to requalify DIMMs or SSDs every security cycle
- Security can be upgraded via PMIC firmware, not hardware redesign
- Enables modular design for automotive and edge

Shield from malicious breach **cyberattacks**

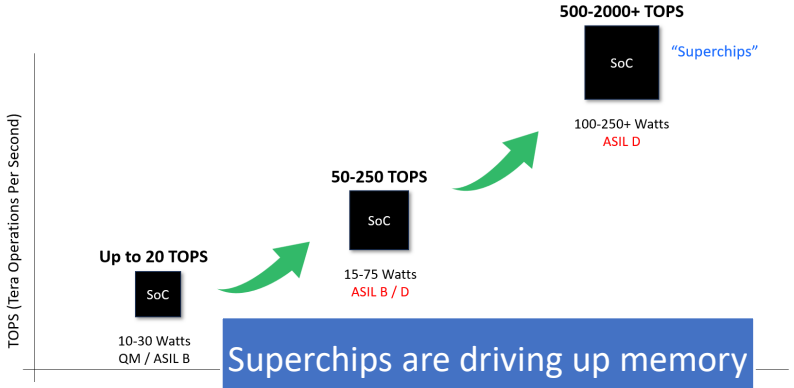
Where This Applies First

SSDs for automotive: high requalification cost → prime market

DDR5/LPDDR for SDV SoCs: high-speed + security need

The Security Landscape Is Not Yet Developed

Recap



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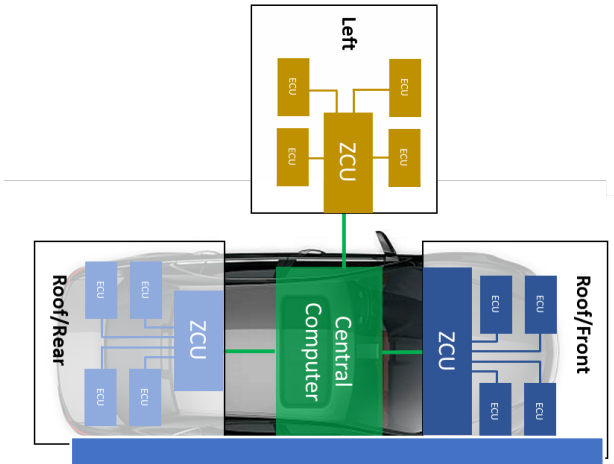
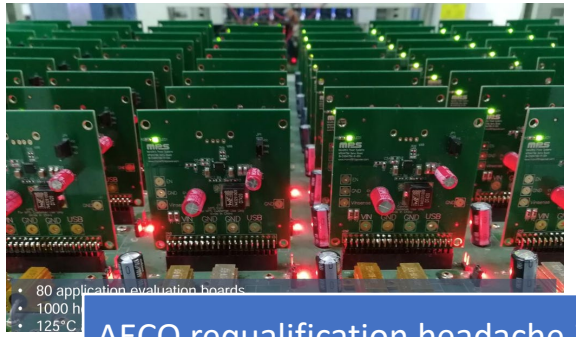
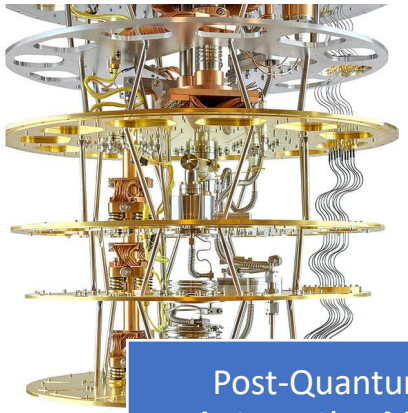


More memory usage in SDV → more potential attack surfaces



AECQ requalification headache in automotive



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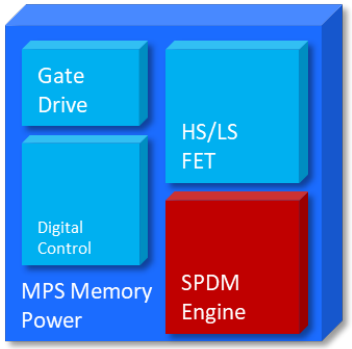

PMIC with Embedded SPDM + PQC

Collaboration for a future-ready, secure memory for automotive

Thank You – Let's Connect

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Webinars & Videos

App Notes / White Papers

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