Testing CXL: Lessons learned from PCIe and NVMe

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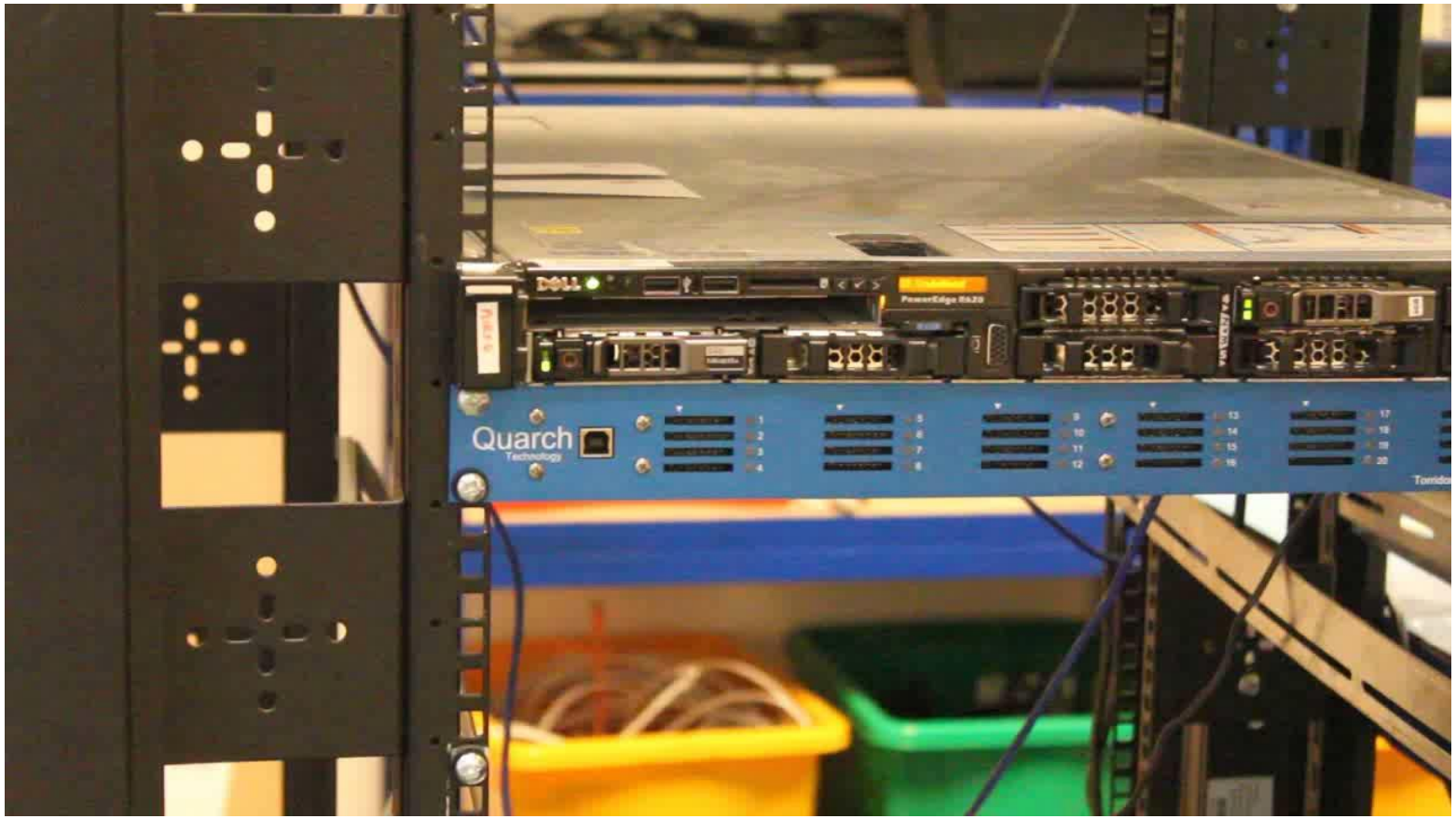
the Future of Memory and Storage

Who are Quarch?

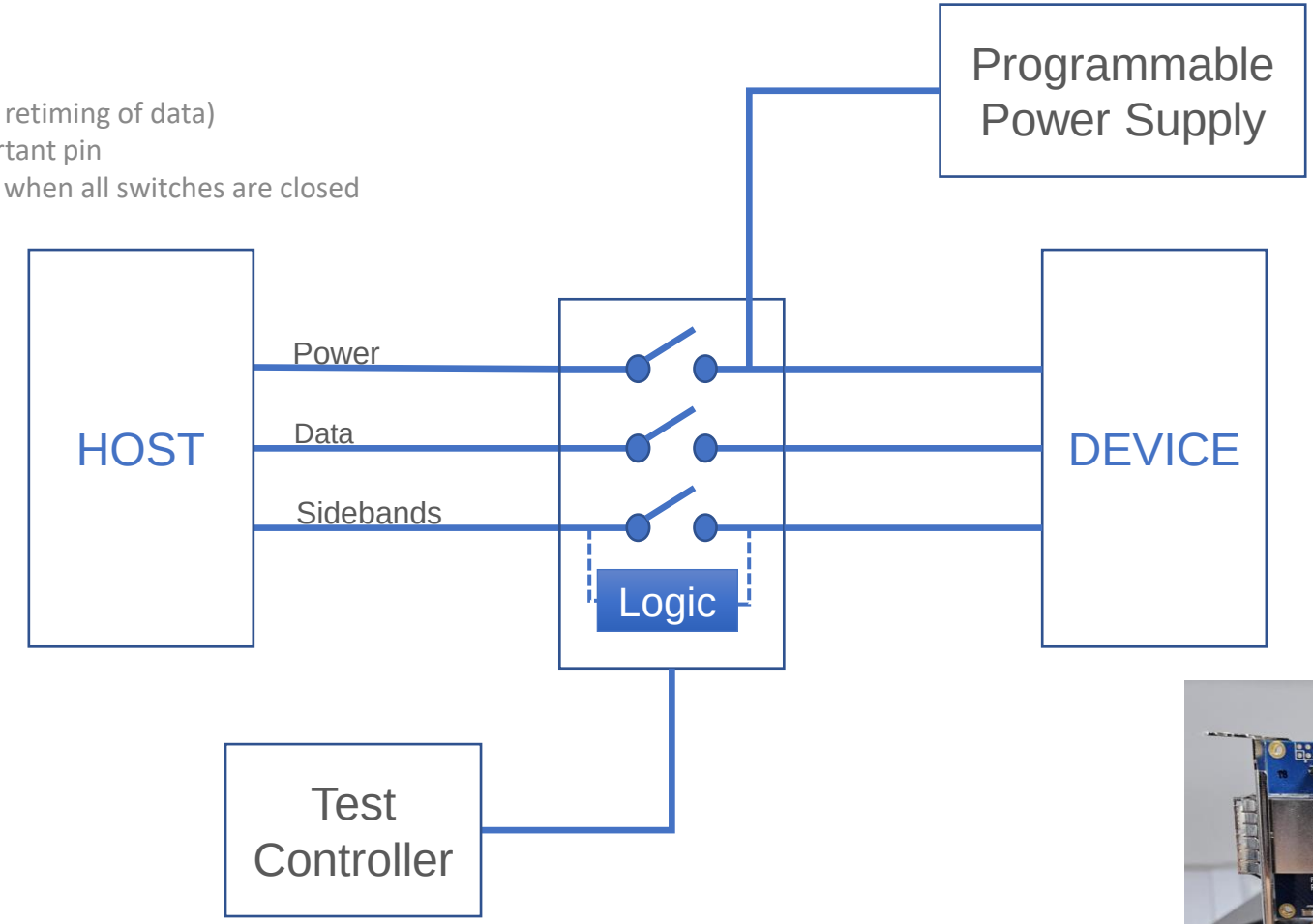
- Quarch Technology is a manufacturer of physical layer automation, fault injection, and power measurement equipment for Storage and Network Interfaces.
- Founded in 2006
- Based in Aviemore, Scotland

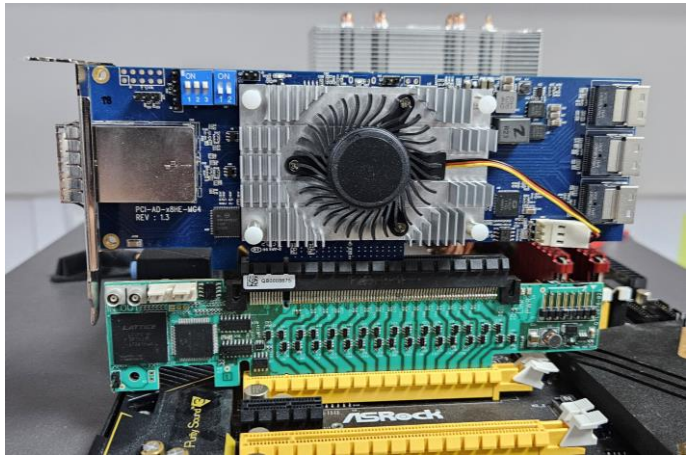
Physical Layer Testing



Physical Layer Testing

Passive interposer (no redriving or retiming of data)
Individual switching on each important pin
No effect on the system operation when all switches are closed





Physical Layer Testing

Pros:

- ✓ Cheap: Test hardware is relatively low cost and scalable, Once automated, testing can be repeated at very low cost across protocols, hardware, firmware and software revisions, and in customer systems
- ✓ Effective: Most bugs tend to be very repeatable, leading to fast diagnosis and fixes can be confirmed quickly
- ✓ Fast: No hardware modifications, no special builds, little inside knowledge required
- ✓ Real: Testing is performed on real systems and fw builds, the system is responding as it would in the field.
- ✓ Non-intrusive: Testing can be performed on high value and customer systems without low risk
- ✓ Transferrable: Tests are reusable and transferrable between platforms form factors, protocols and builds

  SAS Tests -> PCIe Tests -> NVMe Tests -> OCP Tests -> CXL Tests

Physical Layer Testing

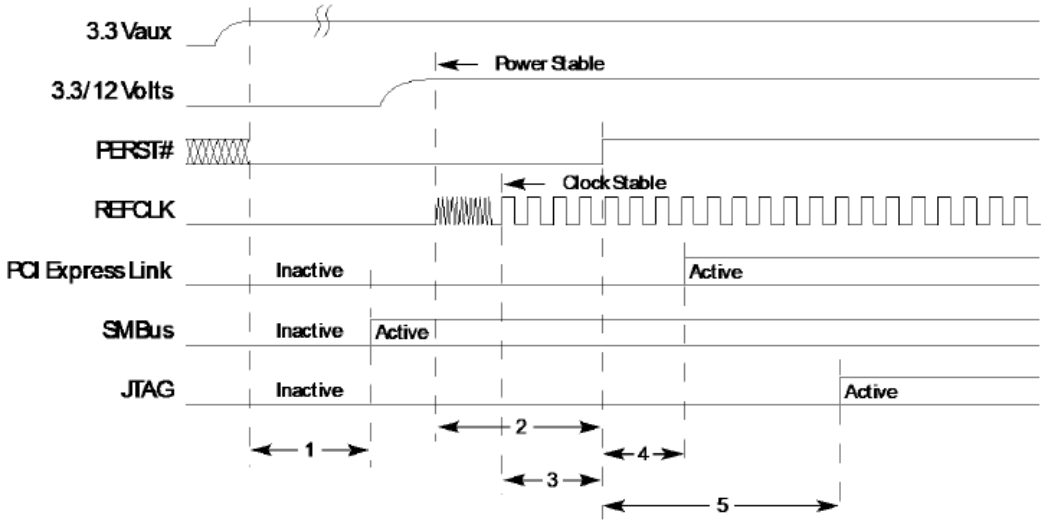
Cons:

✘ Dumb:	No knowledge of protocol without outside assistance. We don't know what data is going down the wire, although we can use triggers from other tools to overcome this to some extent.
✘ Blunt:	Switching times can be restrictive, fast RF switches have a switching time ~ 10 nS, some RF Switches take uS to switch at PCIe Gen6 one FLIT = 256 Bytes = 32nS, so creating correctable errors within a FLIT is not possible, but corrupting 1 or 2 FLITs is
✘ Limited:	Constrained by the limitations of the system, On a power up we can't make the refclk become valid any faster, or fix a poor system response
✘ Signal Integrity:	Becoming a real challenge for all test equipment at PCIe Gen6 and Gen7.

Common Issues #1 - Timing

Power up timing varies between platforms:

A vendor develops a device on Platform A, Customer Platform B has different power up timing and the device does not enumerate

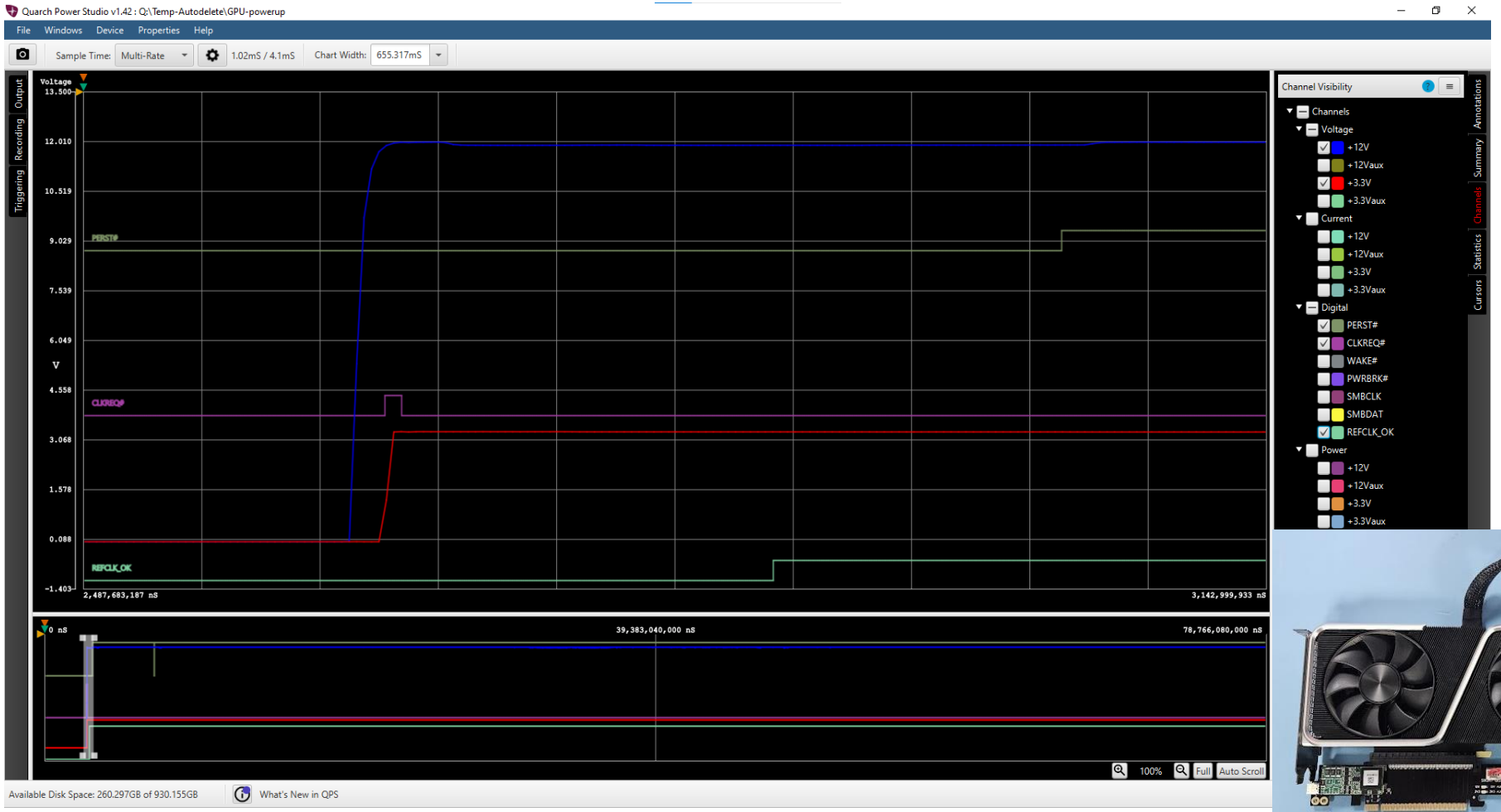


1. 3.3Vaux stable to SMBus driven (optional). If no 3.3Vaux on platform, the delay is from +3.3V stable
2. Minimum time from power rails within specified tolerance to PERST# inactive (T_{PVPERL})
3. Minimum clock valid to PERST# inactive ($T_{PERST-CLK}$)
4. Minimum PERST# inactive to PCI Express link out of electrical idle
5. Minimum PERST# inactive to JTAG driven (optional)

OM14742B

Figure 2-3: Power Up

Common Issues #1 - Timing



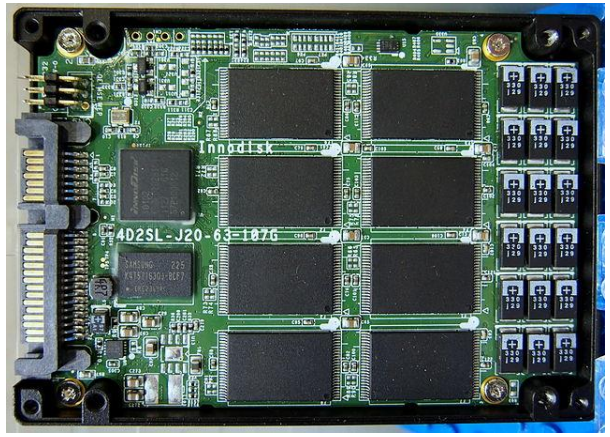
Every host is different, how do we test permutations?

Common Issues #1 - Timing

Hot Plug:	Test Fast / Slow / Incomplete Insertions by varying connection delay between pin lengths
Hot Removal:	Test Fast / Slow / Incomplete Insertions by varying removal delay between pin lengths
Power Up:	Emulate different power up sequences by delaying POWER / PERST / REFCLK
Power Down:	Emulate different power down sequences by accelerating POWER / PERST / REFCLK disconnection

Common Issues #2 – Power Failure

Power Loss:	Cut power to the device when idle, during workloads, firmware update, secure erase, etc
Crowbar:	Pull the device power hard to ground, to stress Power Loss Protection
Brownouts:	Margin power down and back up again to progressively lower voltages. Verify system/device recovery



Common Issues #3 – Error Injection

Data Errors:	Generate data glitches of increasing length and frequency, verify error reporting, recovery and performance – FEC will hide a lot of issues but performance will suffer
Clock Errors:	Generate reference clock glitches, remove refclk when testing SRIS/SRNS
Sideband Errors:	Glitch PERST / PWRBRK / SMBUS / I3C and verify recovery
Lane Down:	Degrade/disable lanes and verify system behaviour

Common Issues #3 – Error Injection

Packet Length and throughput on Ethernet during application of physical layer interruptions. The application here was tuning Firmware timeout values for performance

Common Issues #4 – Redundant Paths

Disable Data:	Disable data on each port, check behaviour, reporting and performance on the working port
Force Reset:	Force each port into reset (or multiple resets) and verify behaviour, reporting and performance on the working port
Performance:	Degrade one path by glitching data, check reporting, system performance

Thankyou!