Design of a 72-Channel, 40 Gbps PAM3 ATE-on-Bench Test System for GDDR7 Memories

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The GDDR7 Specification

A major step forward…

- 1 Tbps throughput on a single memory device
- 64 Gbit of storage on a single memory device

The GDDR7 Specification

A major step forward…

- 1 Tbps throughput on a single memory device
- 64 Gbit of storage on a single memory device

An unprecedented testing challenge…

- How to perform BERT-based I/O characterization
- How to perform memory cell testing

Focus of This Presentation

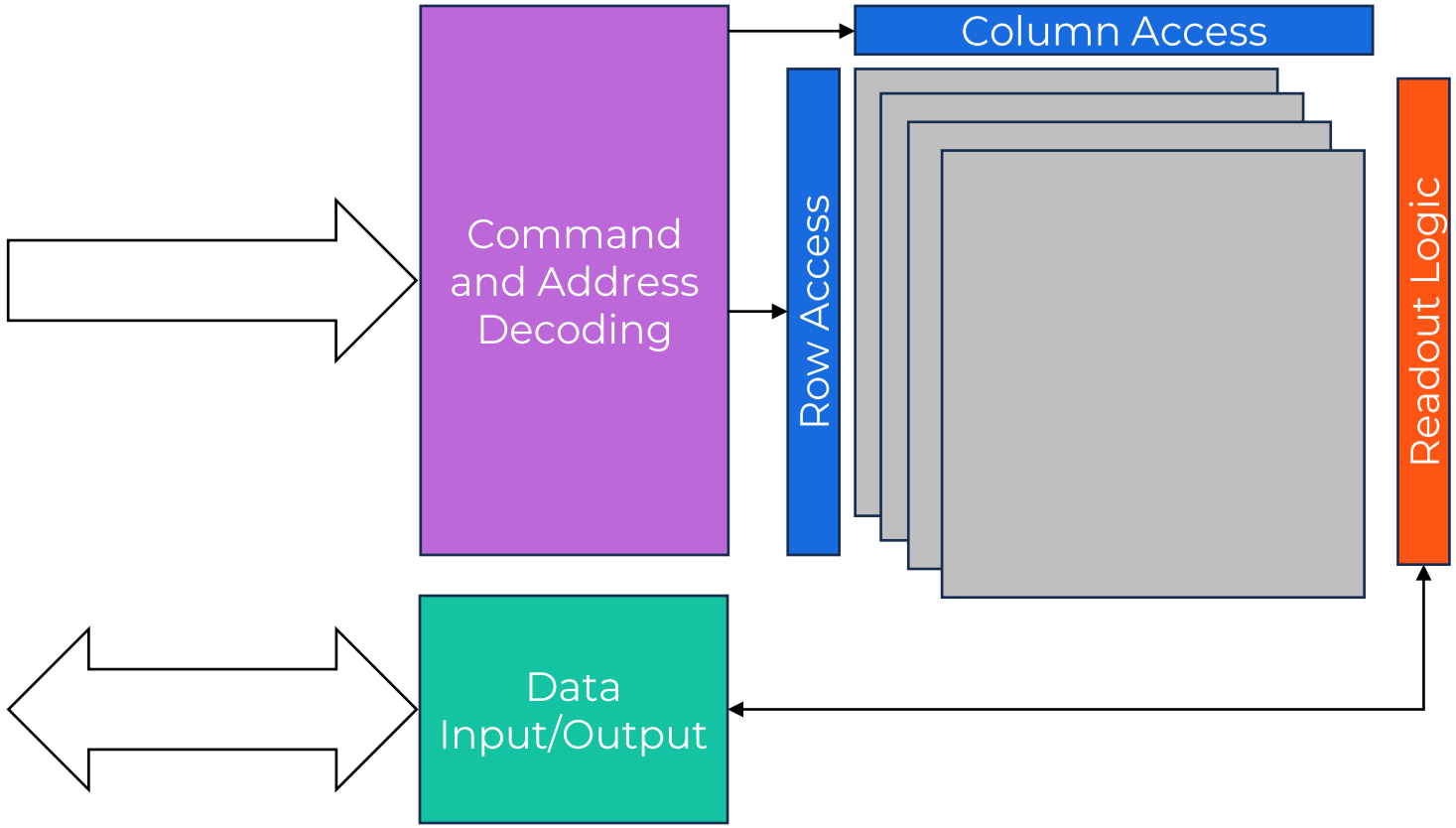
Design of an ATE on Bench Solution for GDDR7

Overview of the GDDR7 Specification

It still looks like a DDR memory interface

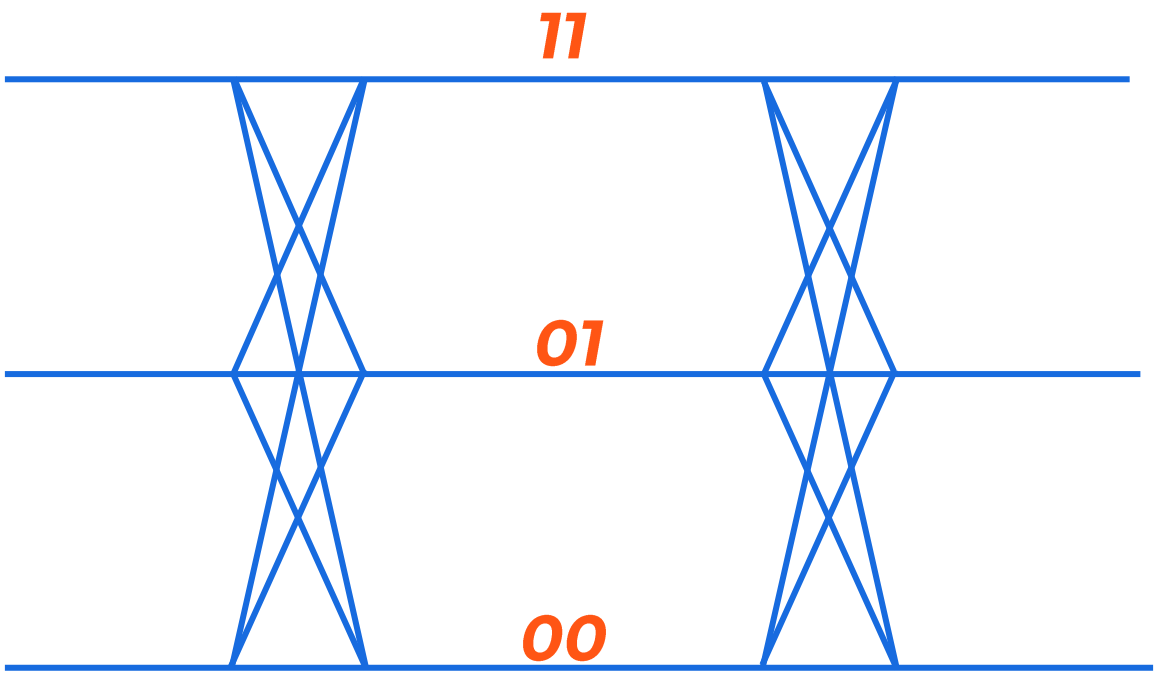
Source-synchronous command and address (CA) bus

Bidirectional burst-mode data bus



Overview of the GDDR7 Specification

It introduces PAM3 signaling



GDDR7 Is Unlike Other PAM3 or PAM4 Standards

High-Speed

Single-Ended

- Ethernet, USB, or PCIe are all high-speed, but they rely on differential signaling
- The GDDR7 DQ pins are all single-ended, and this requires more careful design

GDDR7 Is Unlike Other PAM3 or PAM4 Standards

High-Speed

Single-Ended

Bidirectional

PAM3

- Ethernet, USB, or PCIe all have separate Tx and Rx lanes, so the PHY implementation does not require bidirectional I/Os
- The GDDR7 DQ pins are all bidirectional I/Os, and this is a major design challenge

GDDR7 Is Unlike Other PAM3 or PAM4 Standards

High-Speed

Single-Ended

Bidirectional

PAM3

Burst-Mode

- Ethernet, USB, or PCIe all rely on CDR-based SerDes (with continuous data)
- The GDDR7 interface is burst-mode with very short burst sizes. So, it is not possible to use a CDR

GDDR7 Is Unlike Other PAM3 or PAM4 Standards

- High-Speed
- Single-Ended
- Bidirectional
- PAM3
- Burst-Mode

GDDR7 poses significant electrical test and characterization challenges

Protocol-Level Lane to Lane Interactions

CA Bus Training

DQ Bus Training

- Drive CA and measure DQ
- Drive CA, DQ and measure DQ
- DQ has both write and read training

Protocol-Level Lane to Lane Interactions

CA Bus Training

DQ Bus Training

PAM3 Encoders

- Three different PAM3 encoders (11b7s, 3b2s, 2b1s)
- PAM3 encoders are distributed across lanes

Protocol-Level Lane to Lane Interactions

CA Bus Training

DQ Bus Training

PAM3 Encoders

Data Integrity

- CRC on read/write transfers
- ECC on read/write transfers and on-die memory cells
- Command address parity

Protocol-Level Lane to Lane Interactions

- CA Bus Training
- DQ Bus Training
- PAM3 Encoders
- Data Integrity

GDDR7 poses significant protocol test and characterization challenges

Design of the ATE on Bench Solution

Parallel, Protocol-Aware BERT & Functional Memory Tester…

Goals of the Design

PHY Level Testing and Characterization

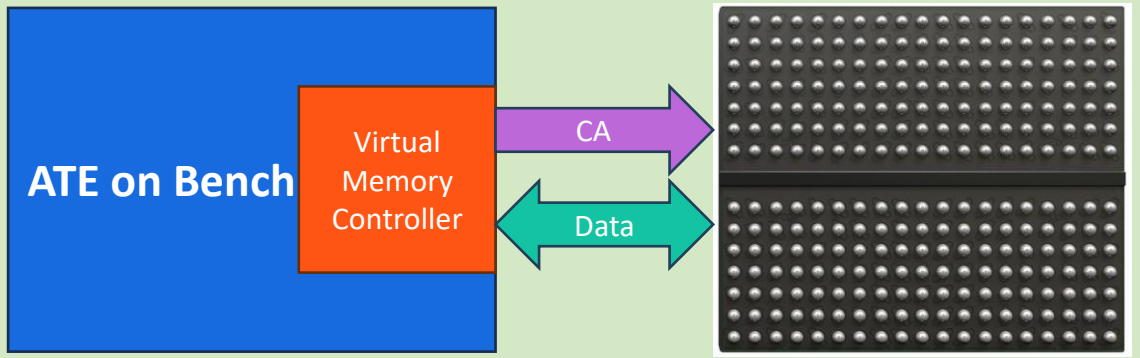
Adjustable voltage and timing parameters on all pins (including jitter injection)

Act as a high-performance, parallel, protocol-aware BERT

Virtual Memory Controller

Act as a CPU/GPU memory controller

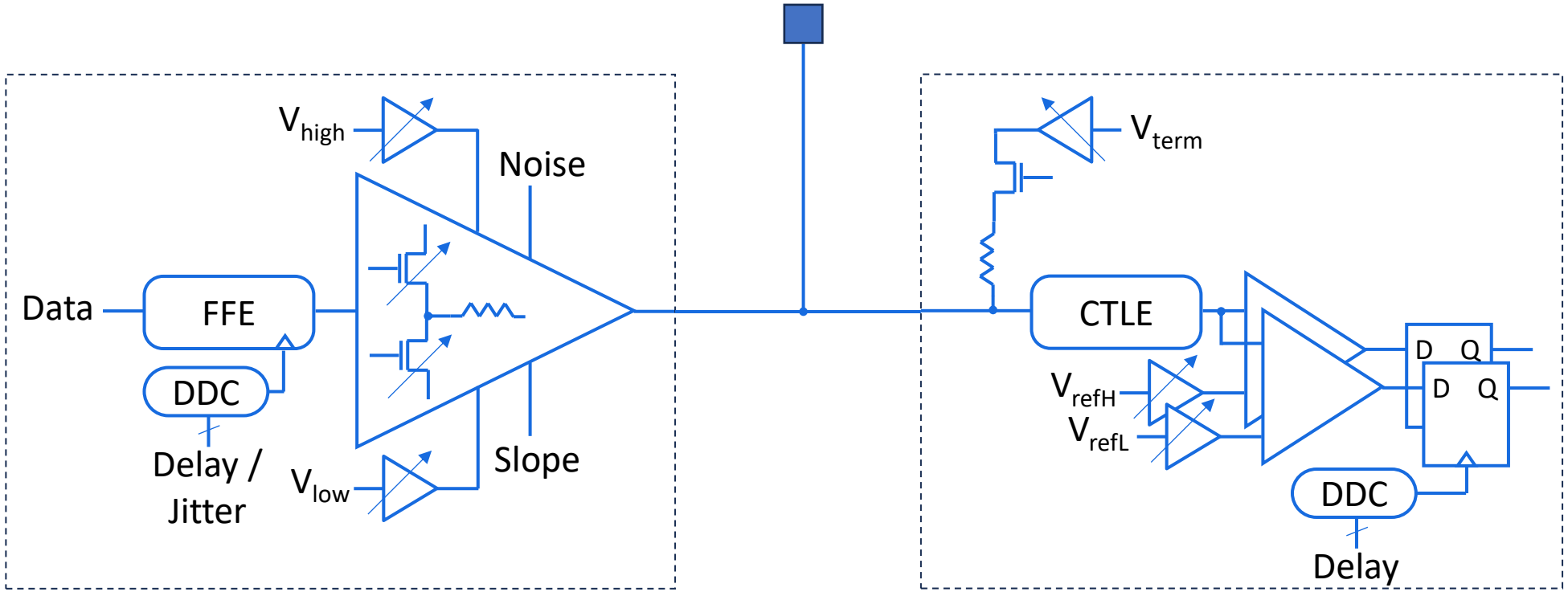
Protocol-compliant stimulus for all memory commands



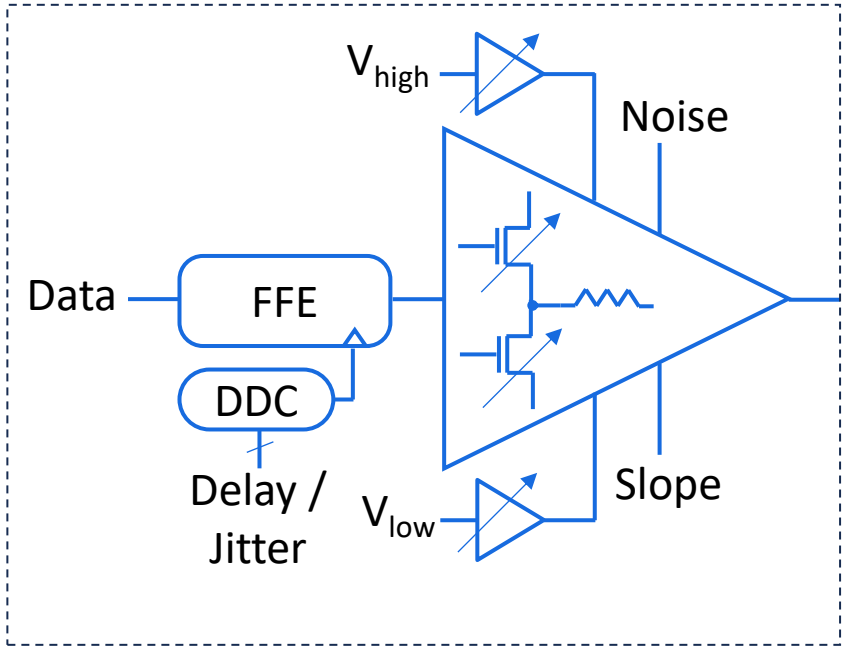
Functional Stress Testing

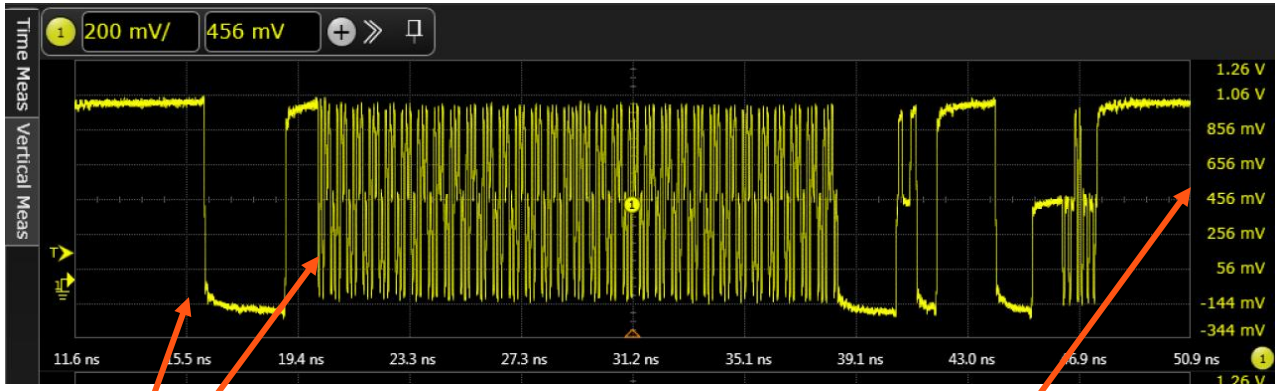
What are the limits of the device? Verify functional behavior while pushing command timings, data rate and other parameters out of spec

Pin Electronic Design



Pin Electronic Design – Cycle Level Control

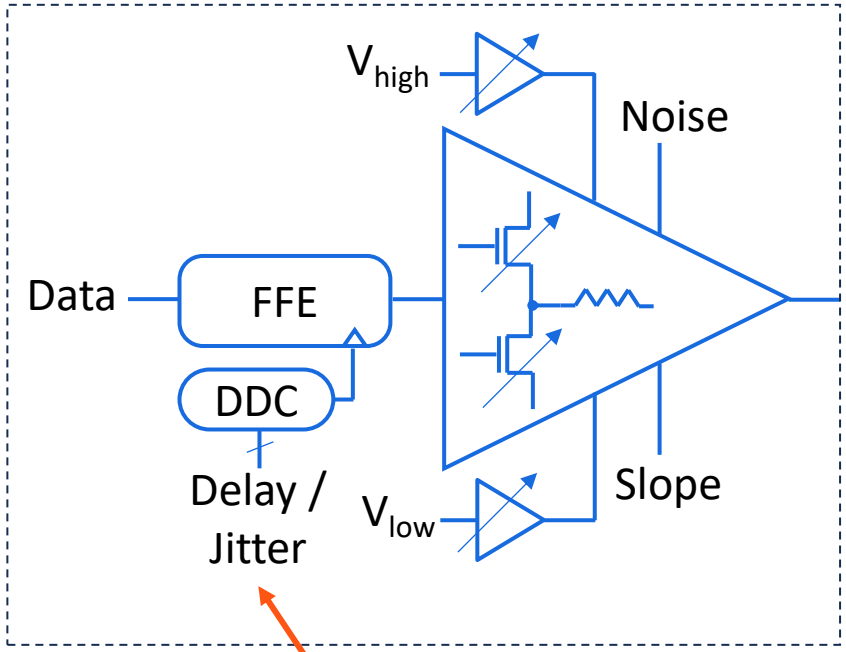


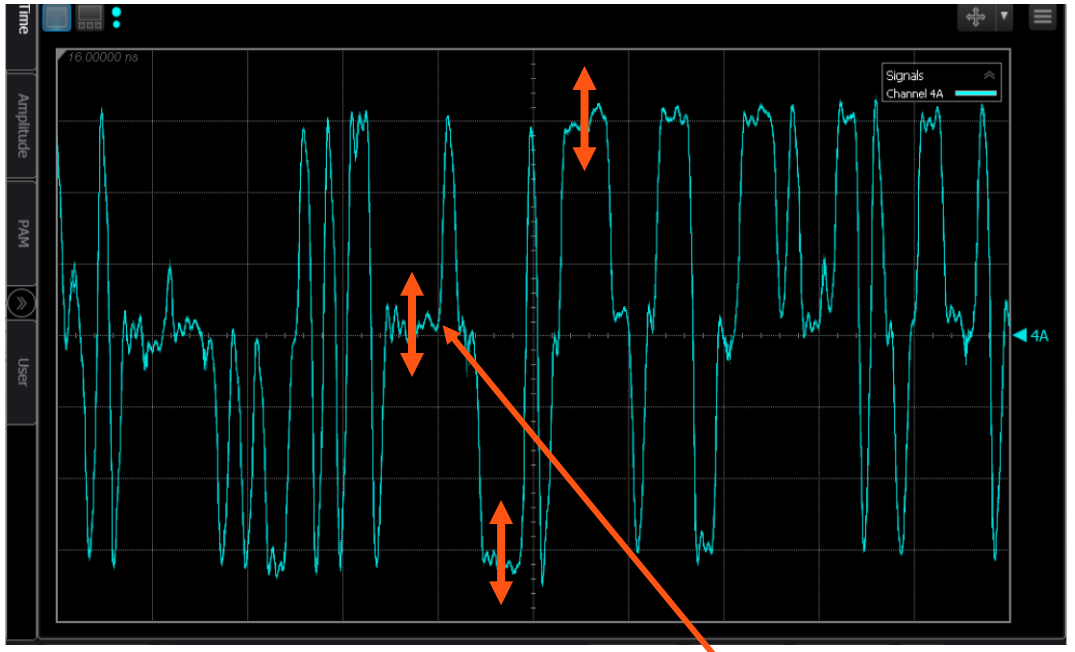


Arbitrarily switch between
NRZ and PAM3 signaling

Wide voltage range

Pin Electronic Design – Impairments

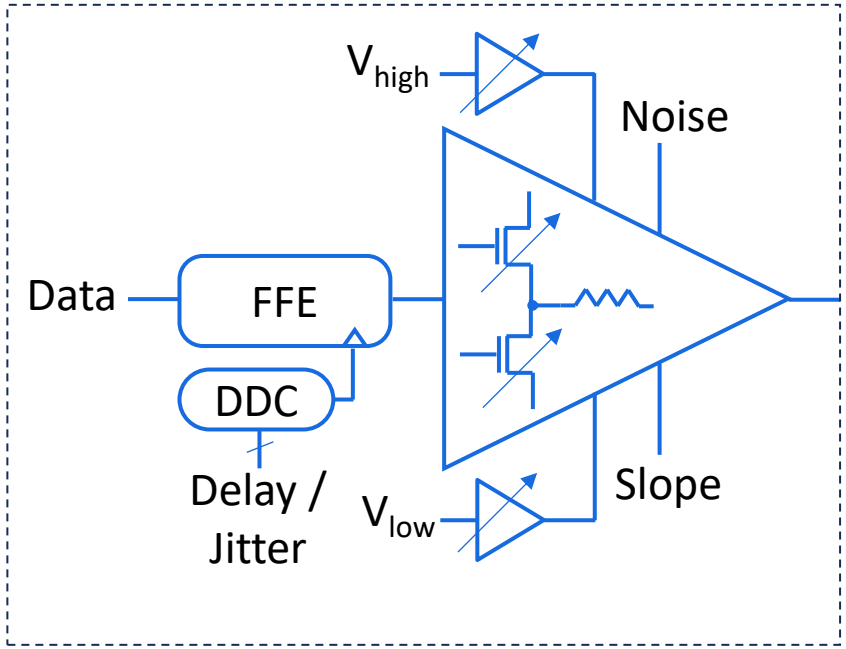


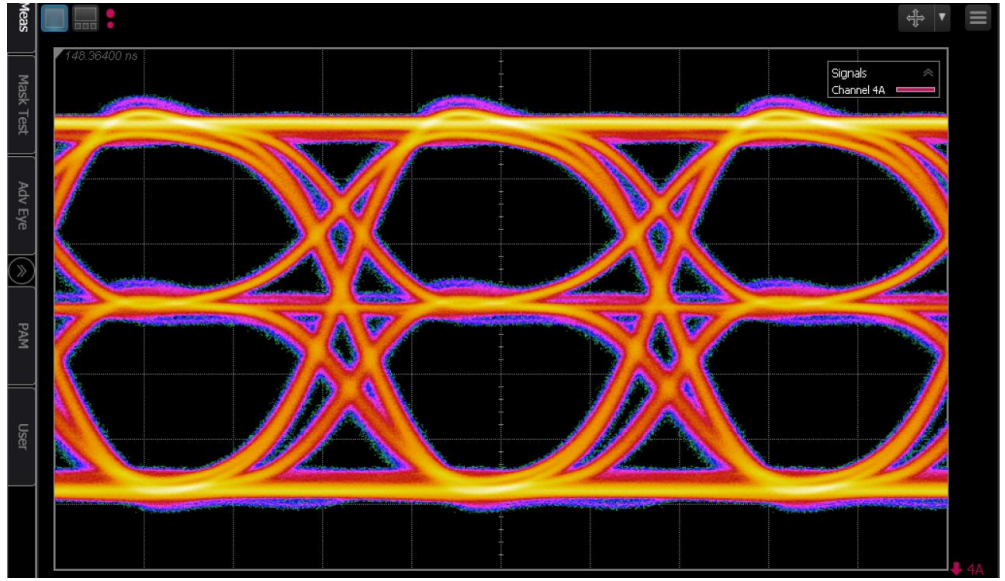


Digital to Delay Converter is used for programming both static skew and jitter

Individual control over low, mid, and high voltages

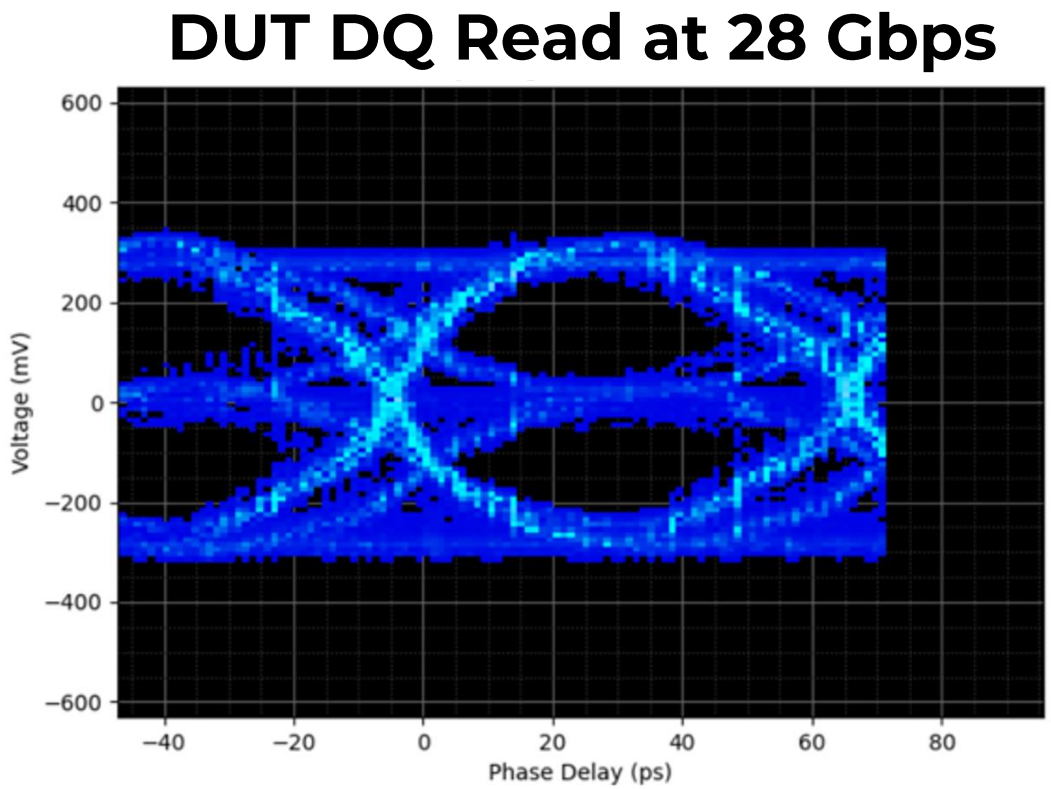
Pin Electronic Design – Designed for 40 Gbps

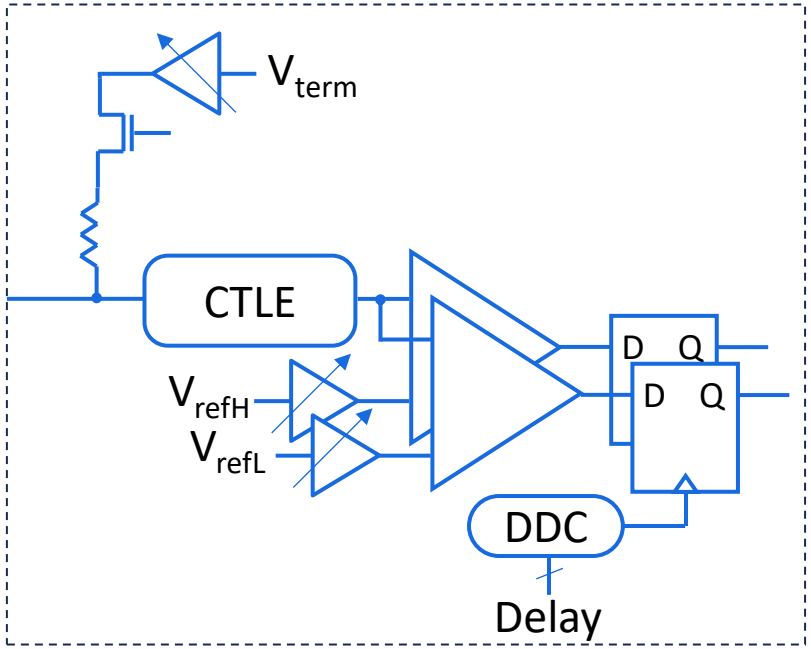




Superior signal integrity
at 28 Gbps and beyond

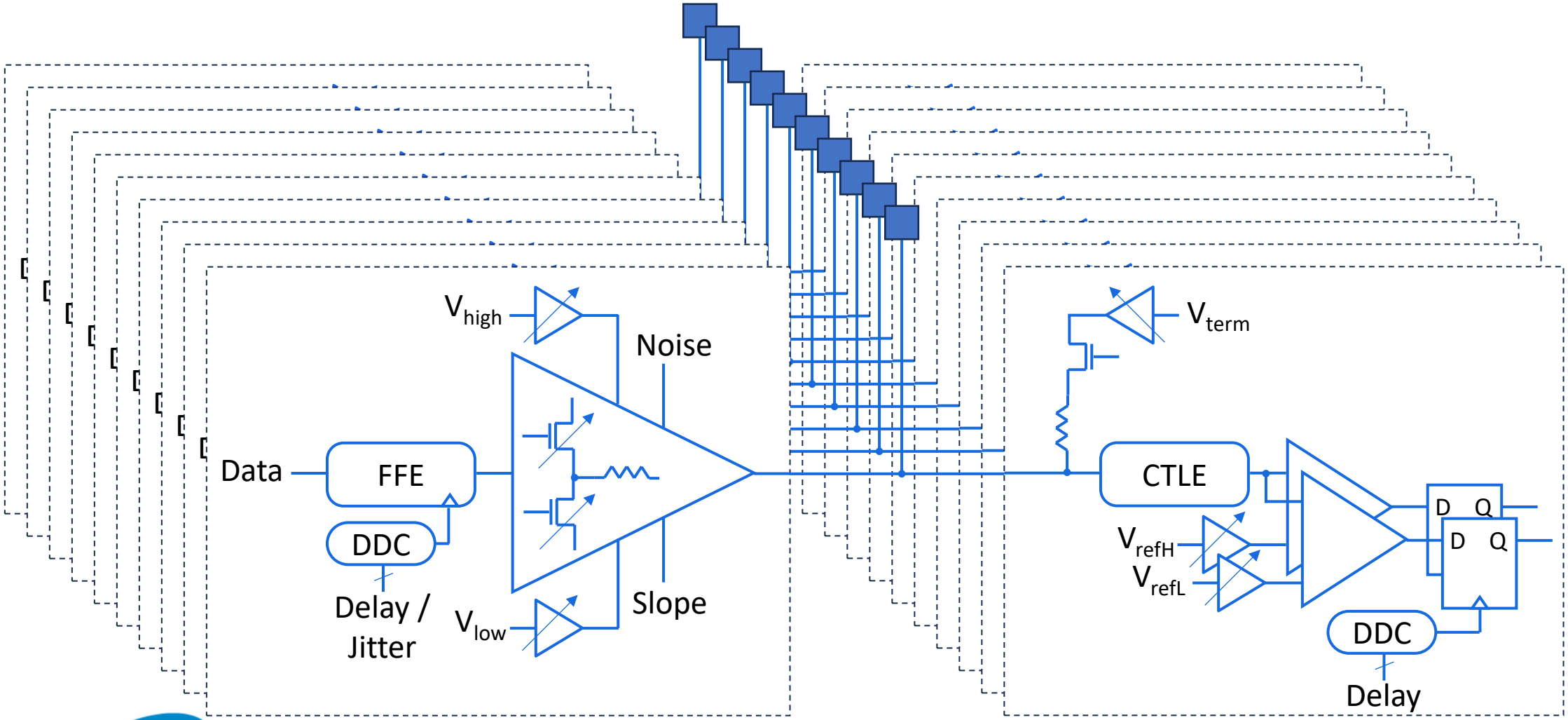
Pin Electronic Design – Shmoo Capability





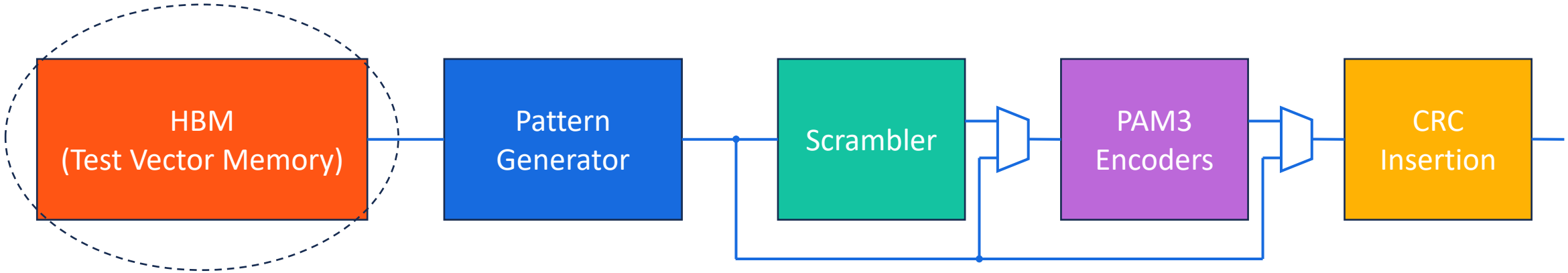
Receivers act as a window comparator to perform parallel PAM3 eye diagram measurement

All I/O Work as a Bus – 72 I/O per Package



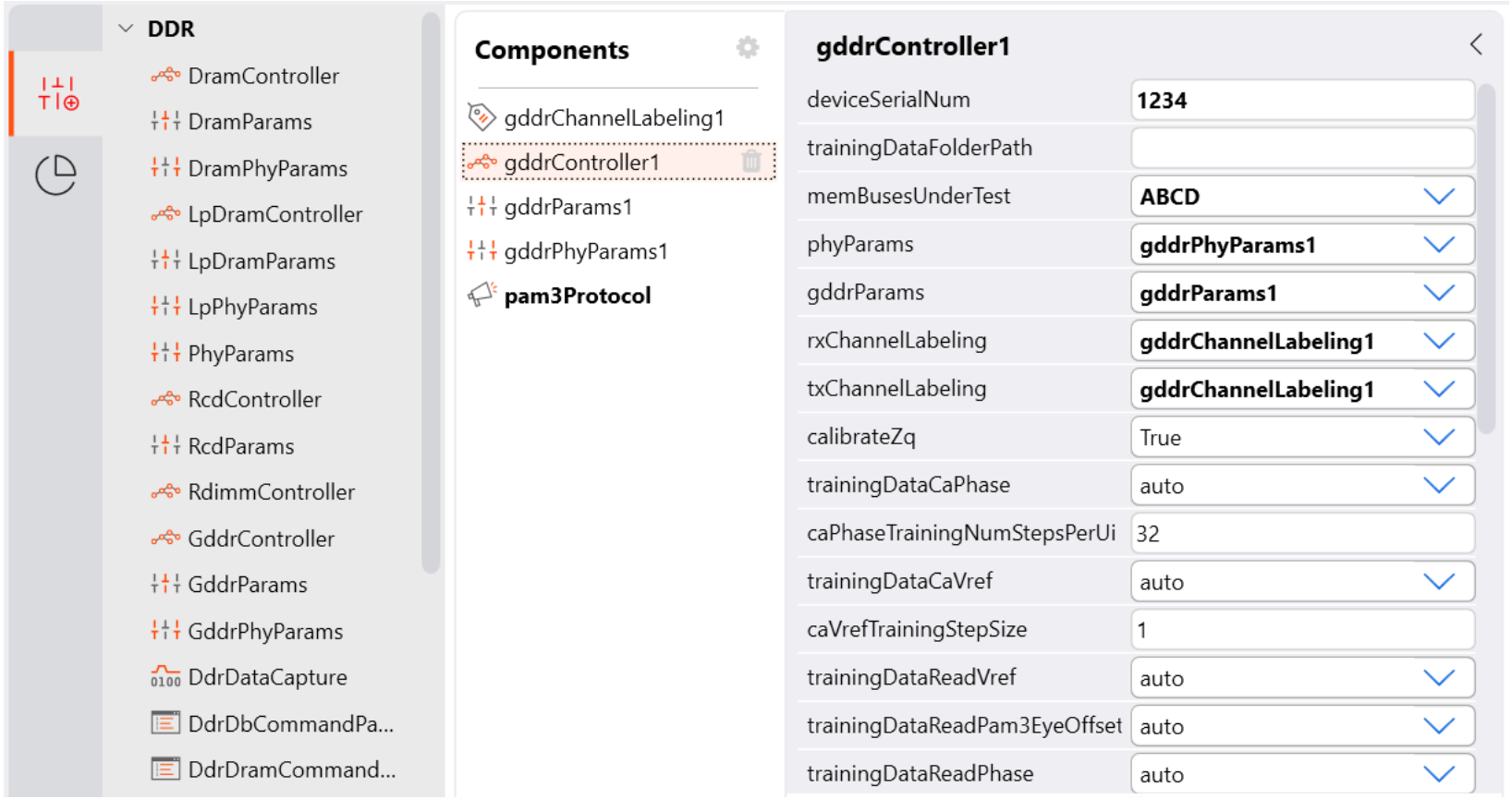
Auto calibration guarantees phase matching on Tx & Rx

Pattern Handling Architecture



- HBM memory is used behind all pins in order to sustain bandwidth
  - 2.88 Tbps of available test vector bandwidth
- Option for hardware-based or software-based scrambling, PAM3 encoding, and mapping
- Instruction sequencer includes “hold” and “idle” patterns

Software Architecture

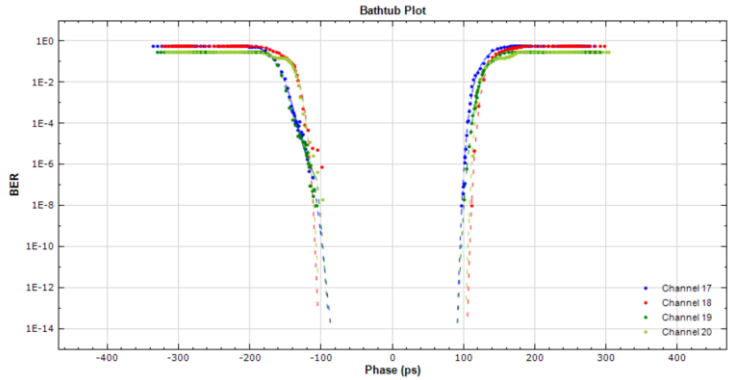


BERT:
Configure all impairments

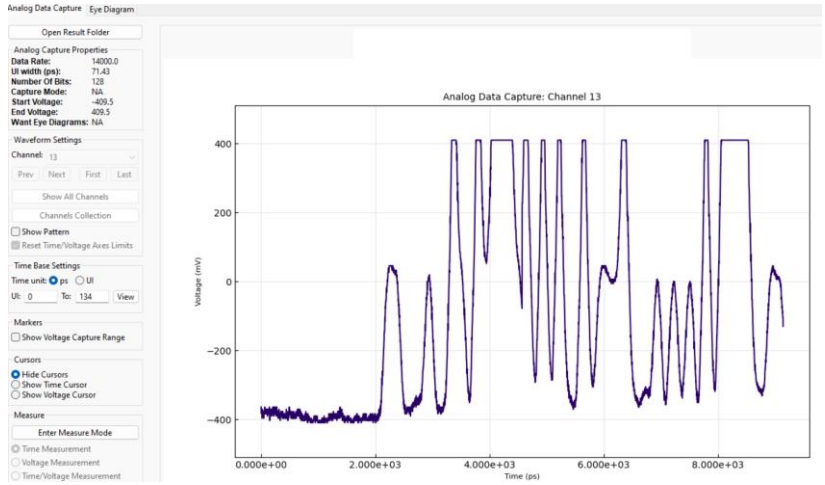
Virtual Memory Controller:
automatically initialize and train the interfaces

PHY Characterization – Transmitter Interfaces

- Clock to data skew measurement
  - RCK to DQ
- BERT measurements on clock and data
  - Long duration error rate tests
  - Eye diagrams
  - Jitter measurements
  - Slew rate measurements



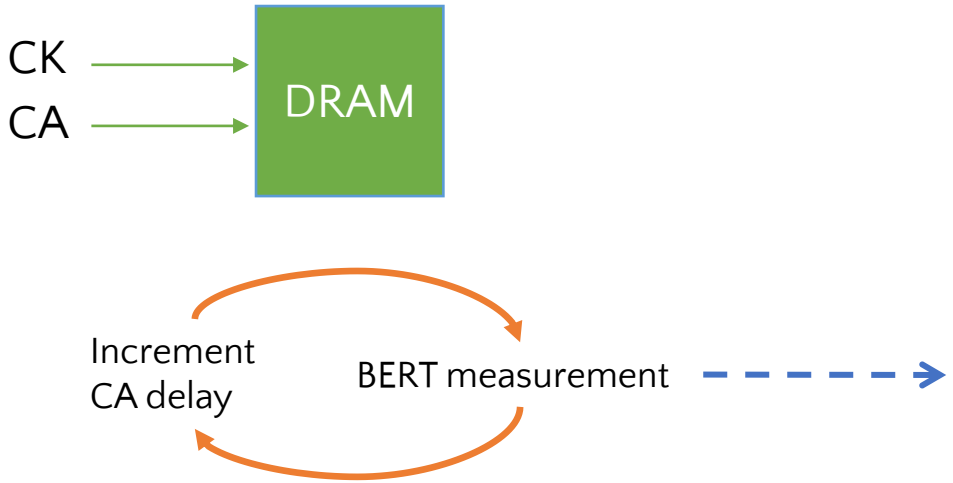
RCK and DQ jitter & skew measurement

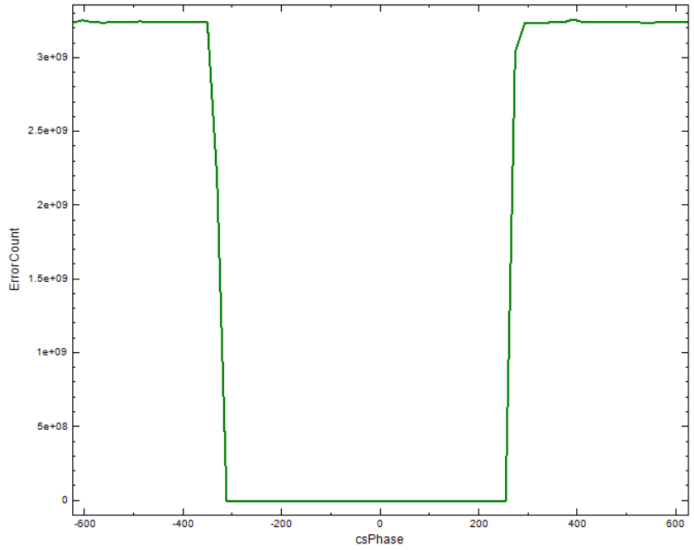


RCK and DQ waveform measurement

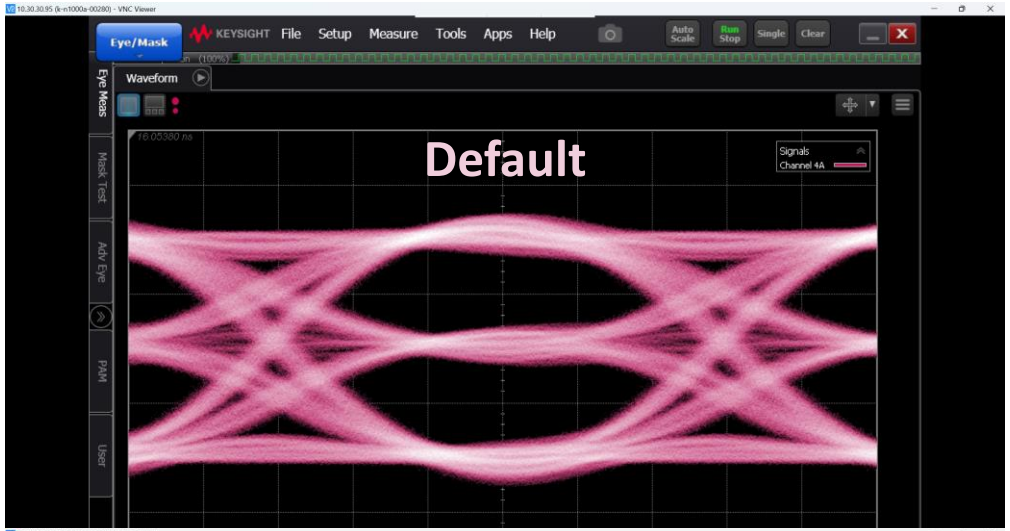
PHY Characterization – Receiver Interfaces

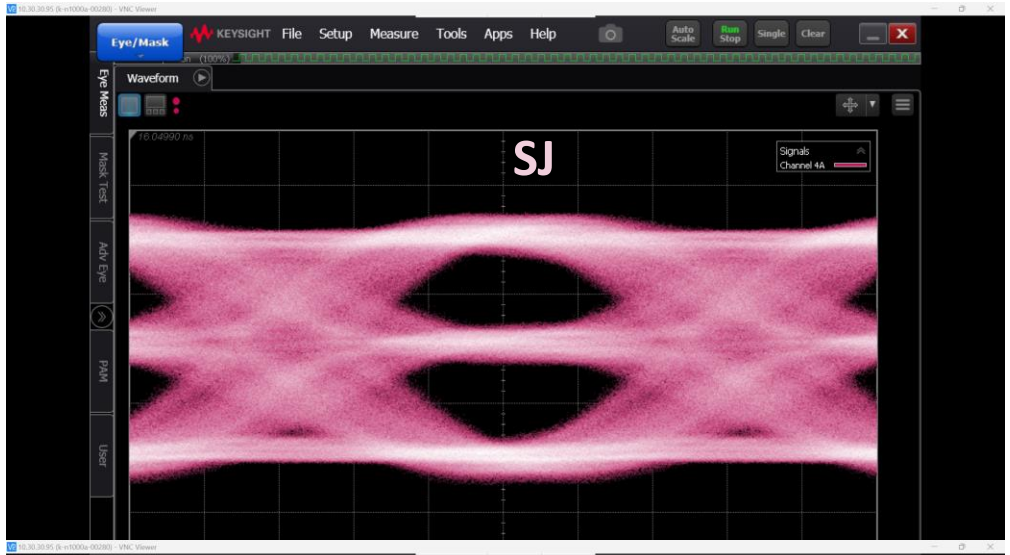
- Measure horizontal and vertical eye opening at receiver while applying different stressors
  - Timing & jitter sensitivity – clock to data
  - Voltage sensitivity
  - Stressed eye





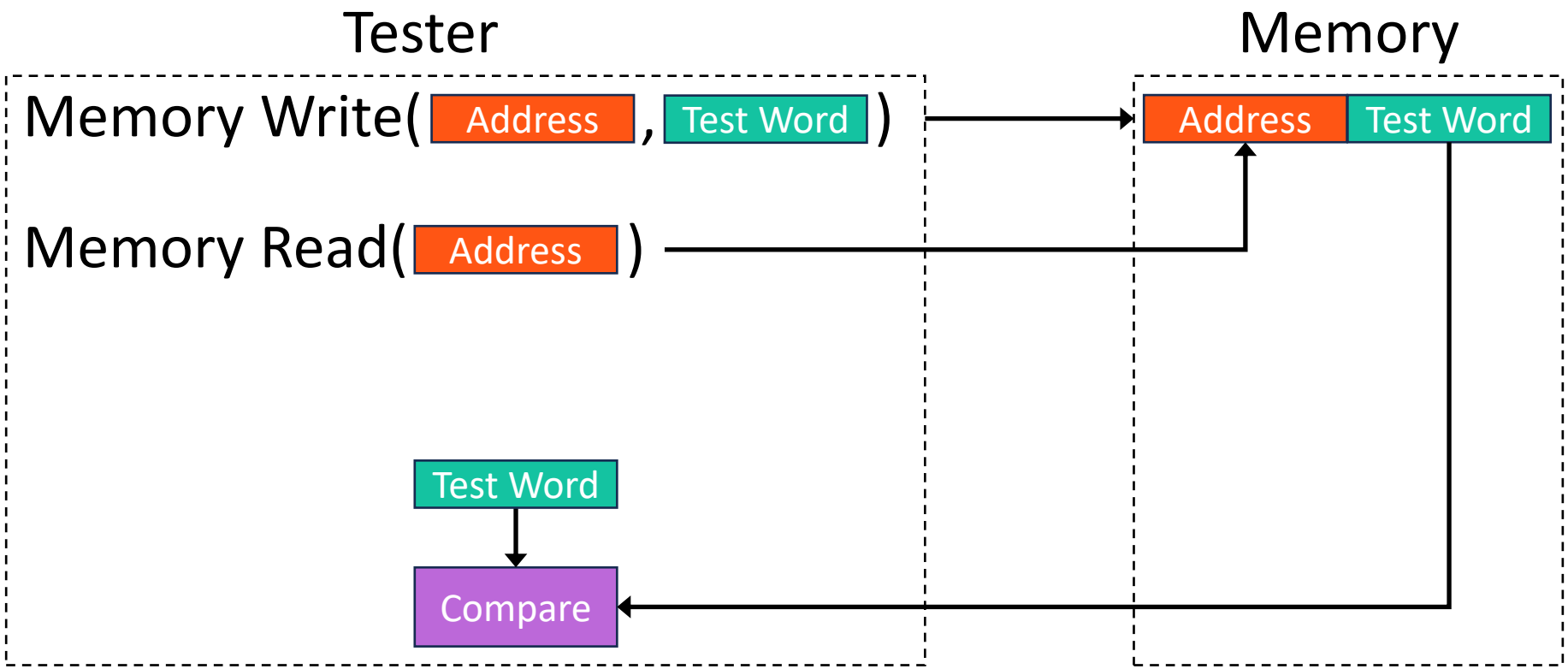
Receiver Stressed Eye Generation





Memory Stress Test Pattern Scheduling

- Write-read-compare at each memory location
- Data Pattern = User-configurable Test Word



Summary

- The high-speed, burst-mode, single-ended, bidirectional, PAM3 signaling in GDDR7 all present significant electrical design and validation challenges
- The multiple training modes in GDDR7 also present design validation and stress testing challenges
- We have presented the design of an ATE on Bench solution for testing GDDR7 memories
  - Acts like a high-performance BERT for electrical characterization
  - Acts like a high-speed memory ATE for functional memory testing

Thank You!

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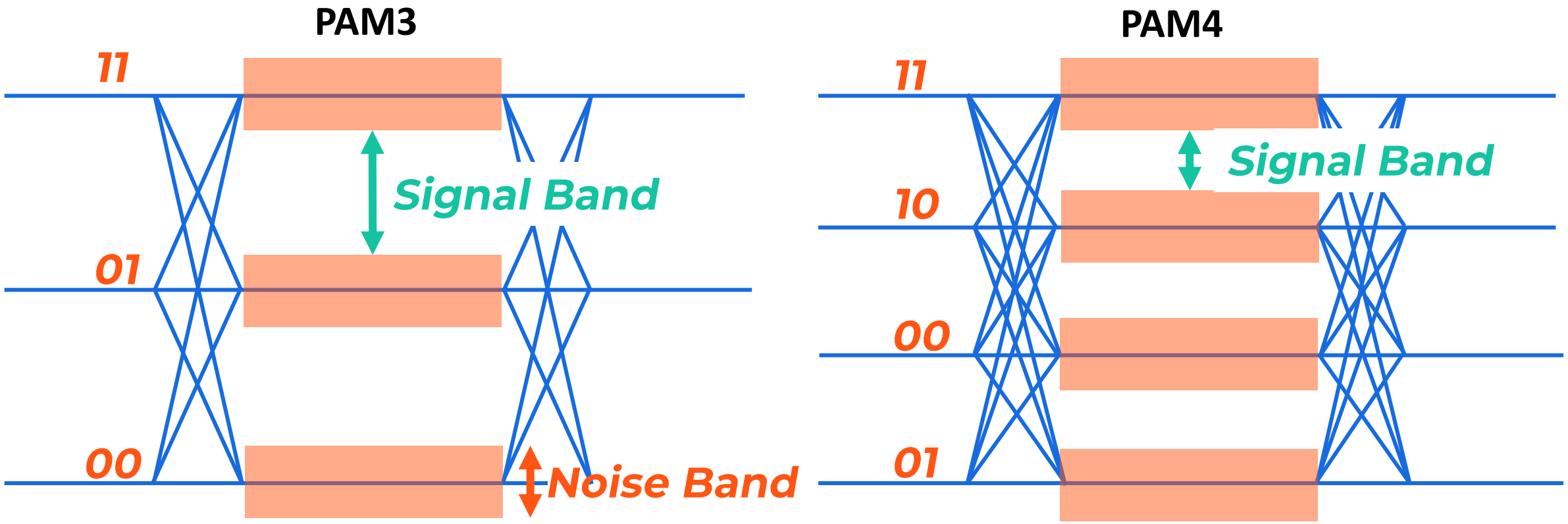
Backup

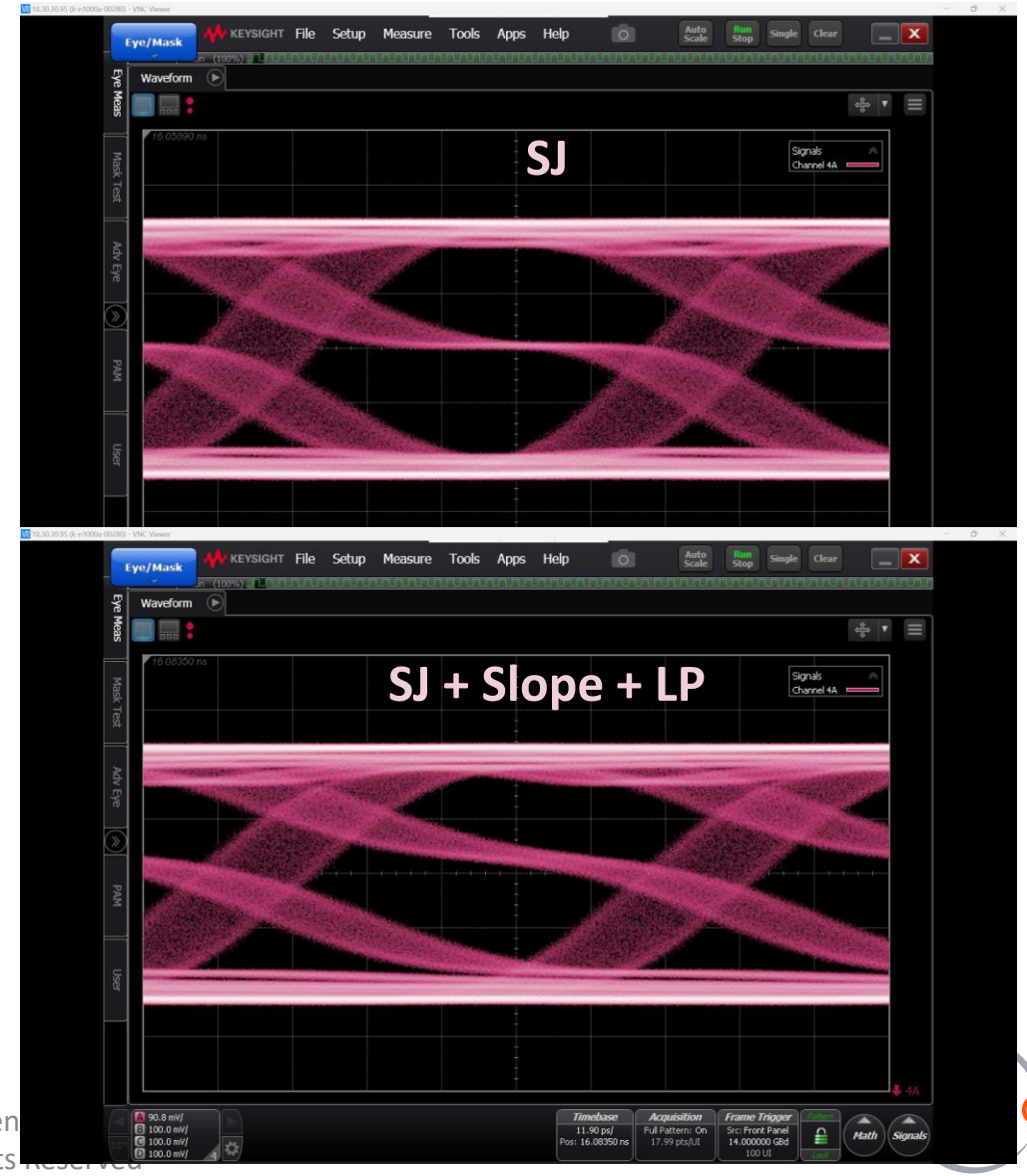
Why PAM3 and not PAM4?

Signal to noise ratio (SNR) is much better in PAM3



For the same noise level, the PAM3 signal eye is much larger

Stressed-Eye Generation With Simple Pattern



Progressively Degraded PAM3 Waveforms

Agenda

- Overview of GDDR7
- Goals of the ATE on Bench Design
- Pin Electronic Design
- Transmitter Characterization
- Receiver Characterization
- Memory functional stress testing