Considerations in PCIe Gen6 Electrical Validation, Device Margining and Characterization for HVM SSDs

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FMS the Future of Memory and Storage

Abstract

PCIe 6.0, a cutting-edge technology, delivers high-speed data transfer rates to cater to the demands of AI/ML applications that necessitate both ample bandwidth and minimal latency.

However, deploying a PCIe Gen6 SSD solution at scale introduces significant **electrical validation** challenges. Our exploration begins by delineating the scope of electrical validation, encompassing CEM, BER, margining, and Link testing.

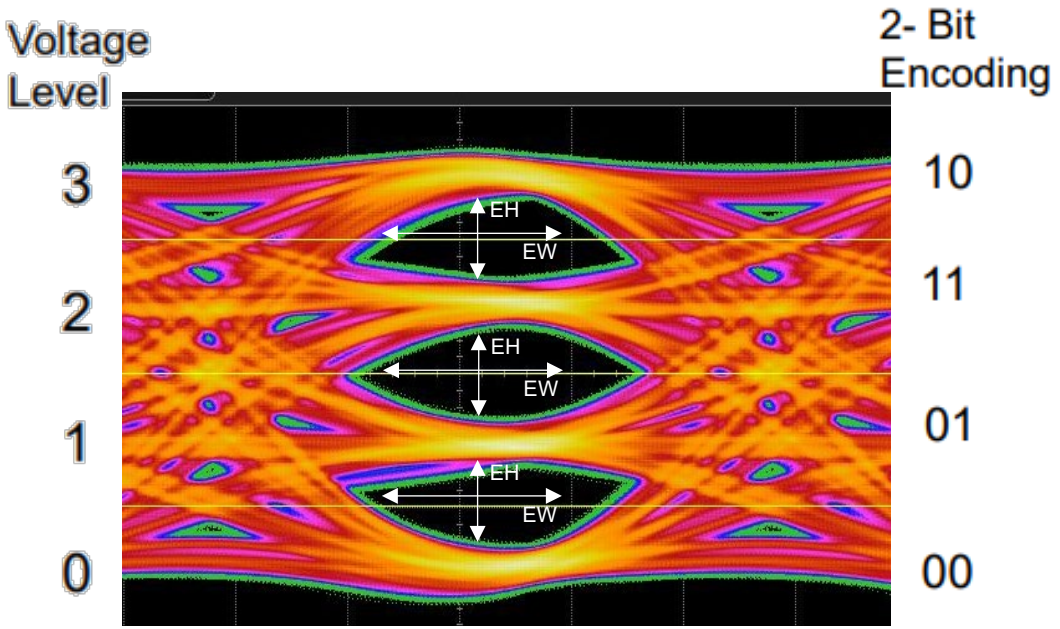
The work delves into the specific hurdles posed by Gen6. Additionally, we discuss best practices related to device margining features, link repeatability, time and frequency based End-to-End signal integrity simulation, and staged validation.

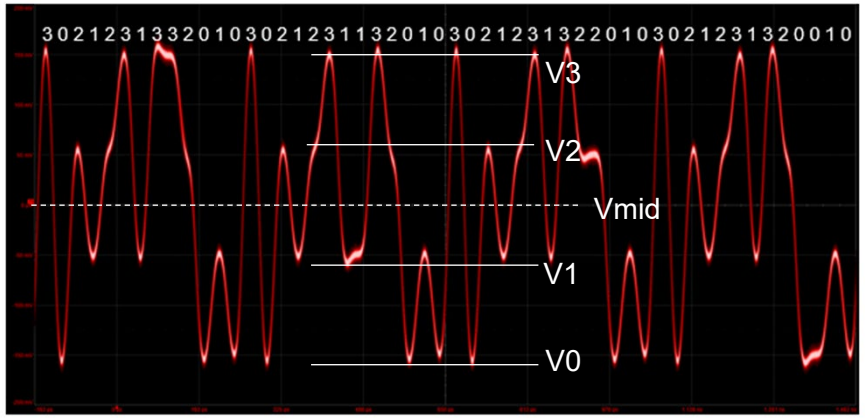
Agenda

- PCIe Gen6 unique challenges
- Channel Budget
- Frequency Requirements
- End-to-End Simulations
- Receiver Stressed Eye
- Power Integrity (PI) Simulations
- System Level Validation
- PHY Electrical Validation
- Characterization

PCIe Gen6 unique challenges

- **Signal to noise ratio**
  - With PAM4, the signal to noise ratio gets lowered by 33% (9.5 dB) which exacerbates the signal degrading effects.
  - To account for the higher noise sensitivity, starting with PCIe6, Forward-Error-Correction (FEC) becomes mandatory.
  - Reduced voltage levels (EH) and eye width (EW) increases susceptibility to errors – 3 eyes in same UI.
- **Linearity** on the 3 eyes, layout design and process variation becomes more critical to avoid asymmetrical eyes.
- **Flit mode** and **backwards compatibility.**
- **Power** challenges due to more complex equalization requirements
  - Tighter noise specification against PCIe5.
- **Jitter characterization**
  - The slew rates for the various transitions are now something to also consider.



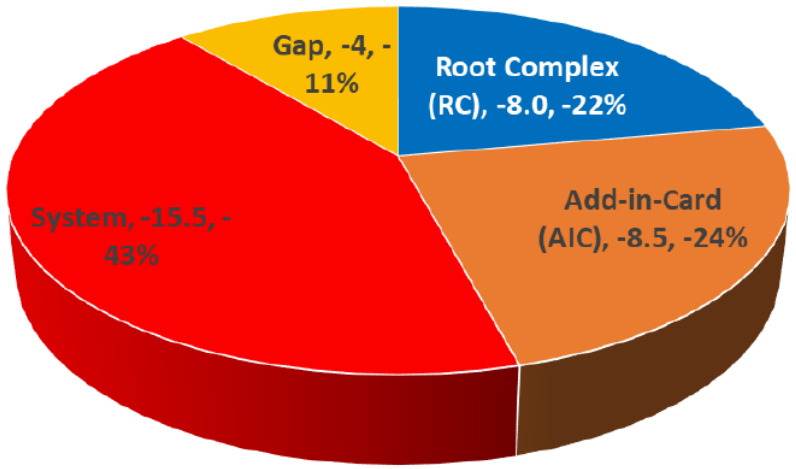


The Level Separation Mismatch Ratio

Channel Budget (CEM Spec)

Pad-to-Pad Loss and System Routing Length

Loss Parameters	PCIe 5.0 Rev 1.0 (dB)	PCIe 6.0 Rev 1.0 (dB)
Pad-to-Pad Loss at 16 GHz	-36	-32
Root Complex (RC)	-9.0	-8.0
Add-in-Card (AIC)	-9.5	-8.5
System	-17.5	-15.5



13”+ system routing requires -32 dB pad-to-pad loss support and PCB loss <= 1.0 dB/in

Courtesy : PIC Sig website

Frequency Requirements

- The Insertion loss, Return loss spec requires to include the PCB routing right after **the connector + controller package and Die loading**.
- Full design optimization is required on all the components.

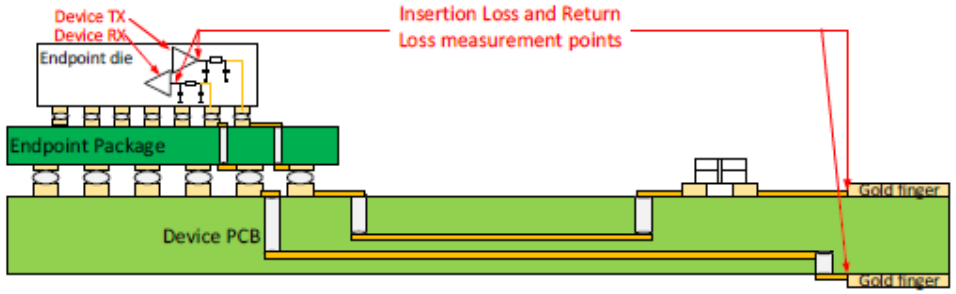
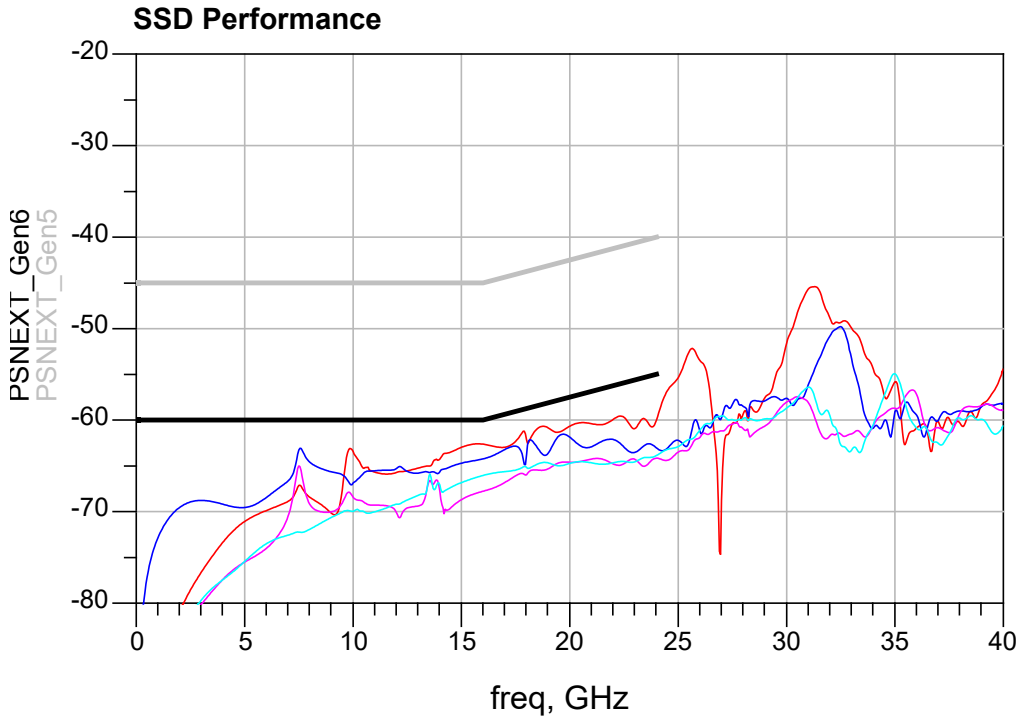


Figure 8-2. Example of Circuit Contributions to Insertion Loss and Return Loss

Table 8-1. Summary of Signal Integrity Requirements

Line Rate	Insertion Loss (IL)	Return Loss (RL)	Power Sum Near End Crosstalk (PSNEXT)[1]	Power Sum Far End Crosstalk (PSFEXT)[1]
16.0 GT/s	-5.5 dB (f = 0 to 8 GHz)	≤ -10 dB (< 4 GHz) ≤ -7 dB (4 to 24 GHz)	≤ -40 dB (0 to 12 GHz)	≤ -40 dB (0 to 8 GHz) ≤ -48 + 1.0 * f dB (f = 8 to 12 GHz)
32.0 GT/s	≥ -0.2 - 0.425 * f dB (f = 0 to 16 GHz) ≥ 5 - 0.75 * f dB (f = 16 to 24 GHz)		≤ -45 dB (0 to 16 GHz) ≤ -55 + 0.625 * f dB (f = 16 to 24 GHz)	≤ -36 dB (0 to 16 GHz) ≤ -44 + 0.5 * f dB (f = 16 to 24 GHz)
64.0 GT/s	≥ -1.5 - 0.28125 * f dB (f = 0 to 16 GHz) ≥ 6 - 0.75 * f dB (f = 16 to 24 GHz)	≤-15dB (< 1.25 GHz) ≤-10dB (1.25 to 24 GHz)	≤ -60 dB (0 to 16 GHz) ≤ -70 + 0.625 * f dB (f = 16 to 24 GHz)	≤ -50 dB (0 to 16 GHz) ≤ -60 + 0.625 * f dB (f = 16 to 24 GHz)

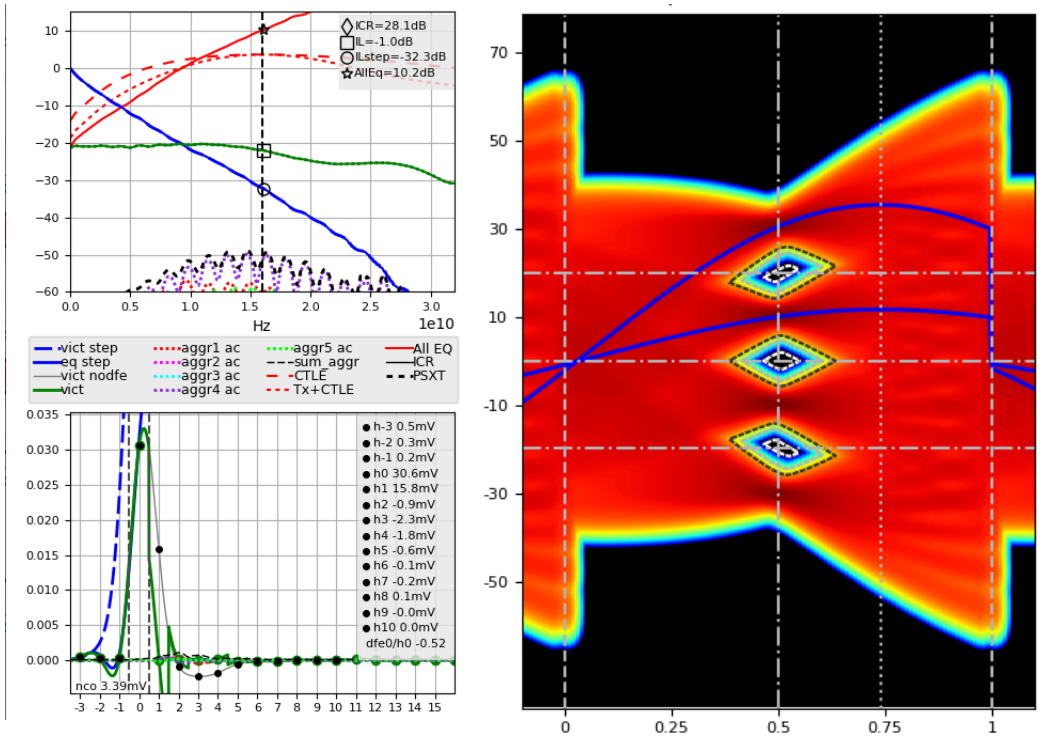
Courtesy : SFF Spec (DRAFT_SFF-TA-1009_R3.1.4)



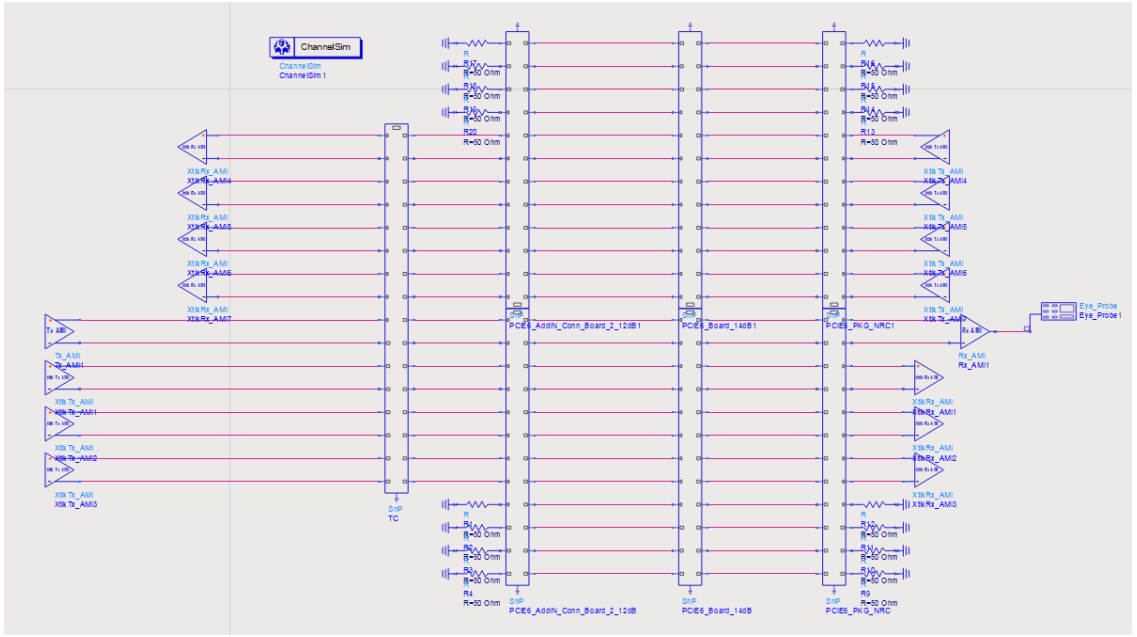
End-to-End Simulations

- Signal-integrity includes the following:
  - S-Parameter models of all the channel components.
  - IBIS-AMI models of RX and TX for signal integrity simulations.
  - Simulations to match with better than 1e-6 BER.

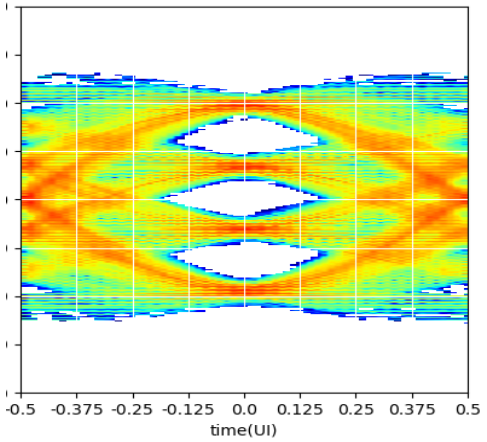
SEASIM



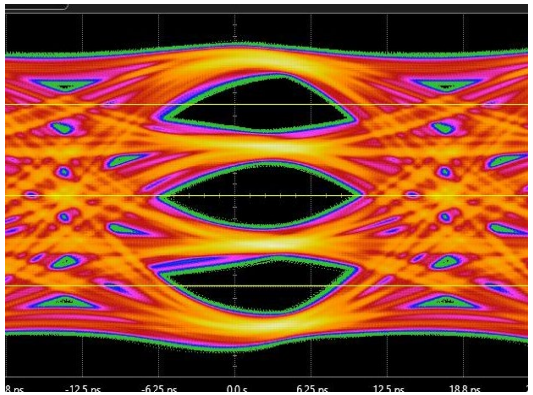
IBIS AMI



Simulated

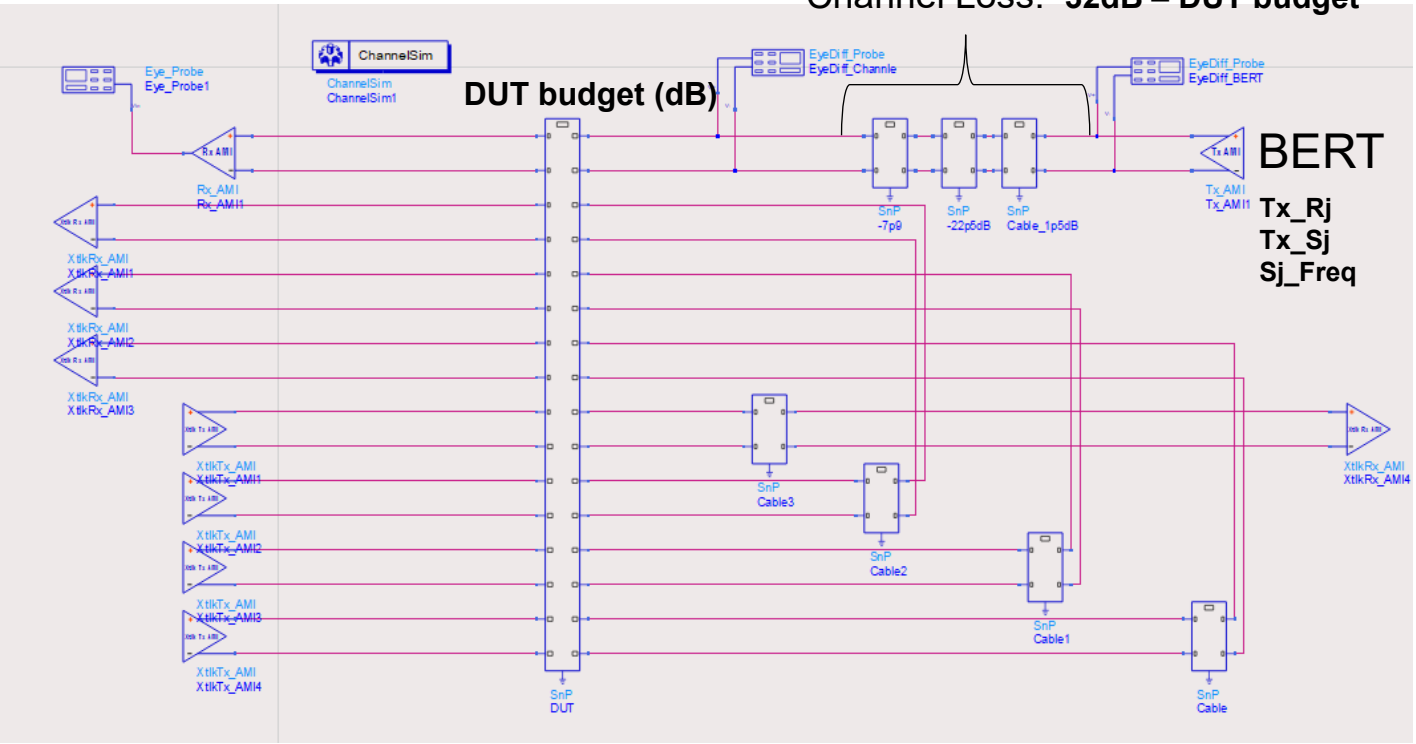


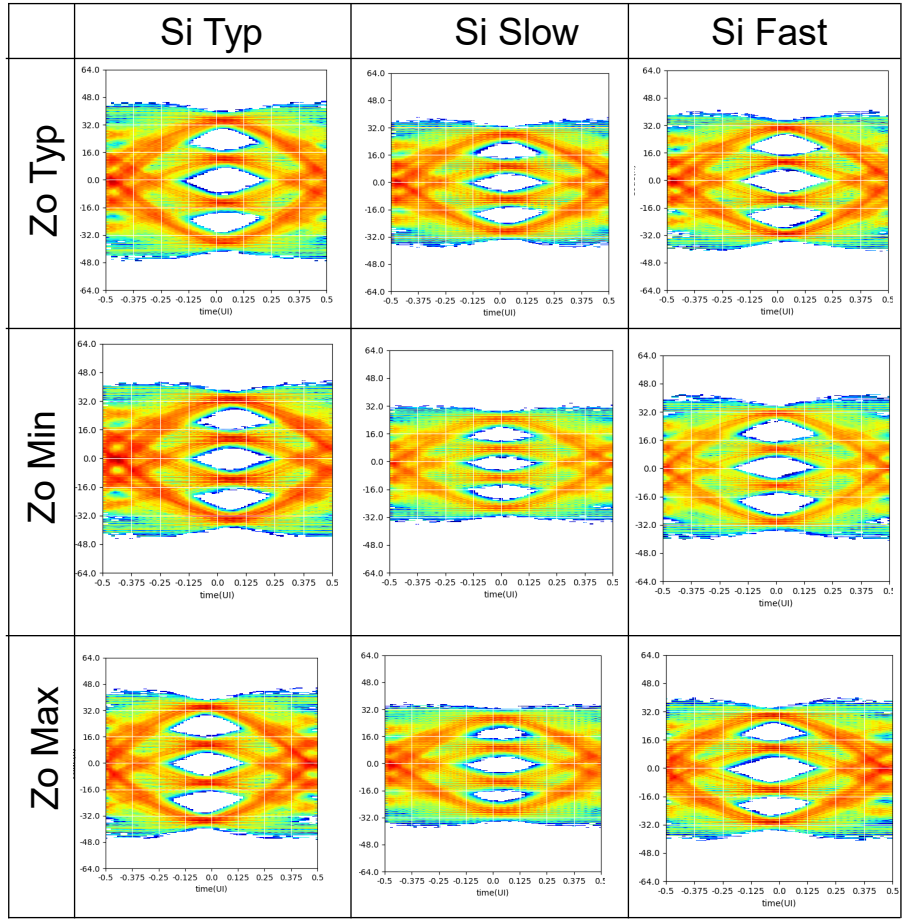
Measured



Receiver Stressed Eye (JTol)

Channel Loss: **32dB – DUT budget**



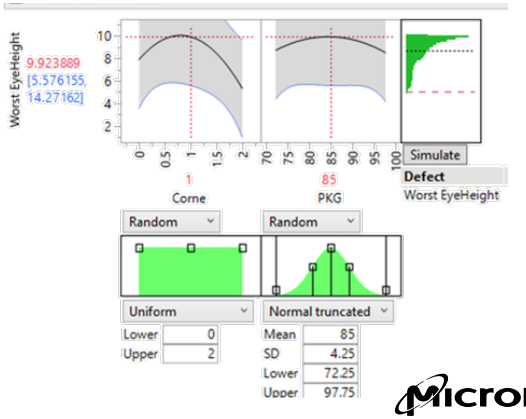


All Receiver are tested by means of a stressed eye applied over a calibration channel that approximates the near worst-case loss characteristics encountered in an actual channel.

PCIe Eye spec

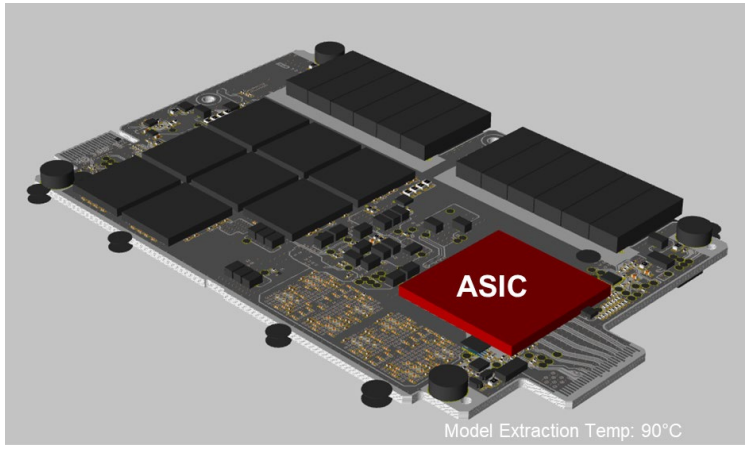
Symbol	Parameter	Value	Units
$V_{RX\text{-}CH\text{-}TOP\text{-}EH\text{-}64G}$	Top Eye height	6 (min)	mVPP
$T_{RX\text{-}CH\text{-}TOP\text{-}EW\text{-}64G}$	Top Eye width at zero-crossing	0.1 (min) 3.12ps	UI

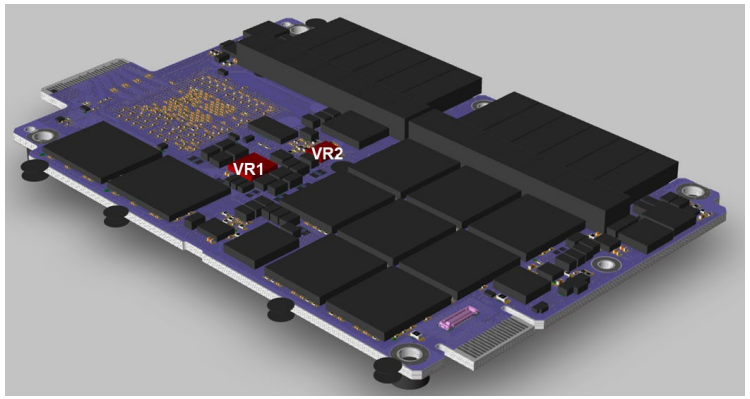
High-Volume Jtol statistics



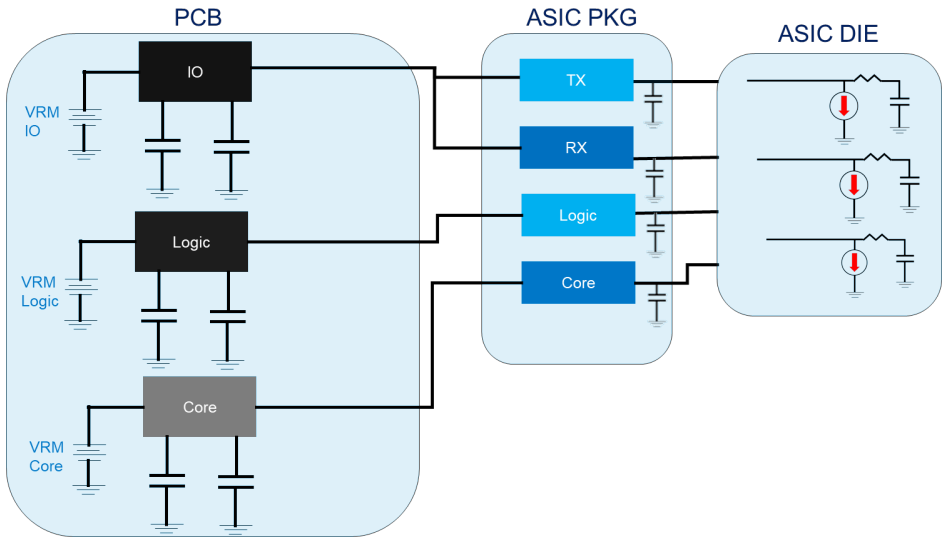
Power Integrity Simulations

- End-to-End Power Integrity simulation from Voltage Regulator (VR) up to Silicon including the full Power Delivery Network (PDN).
- Including End of Life (EOL) models and deratings factors.
- Temperature effects and Electromigration on PCB and PKG.



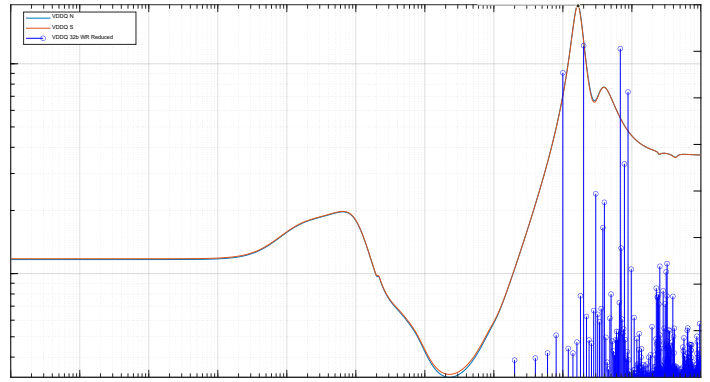


EDSFF Implementation

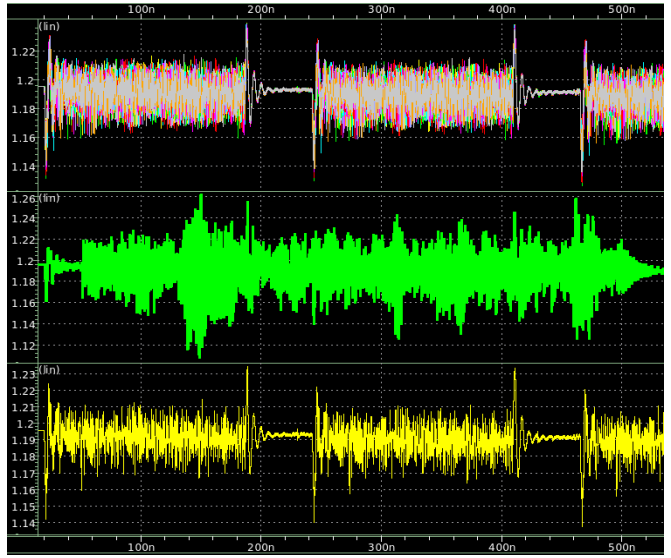


End-to End PDN Modeling

Impedance Response



Time Response

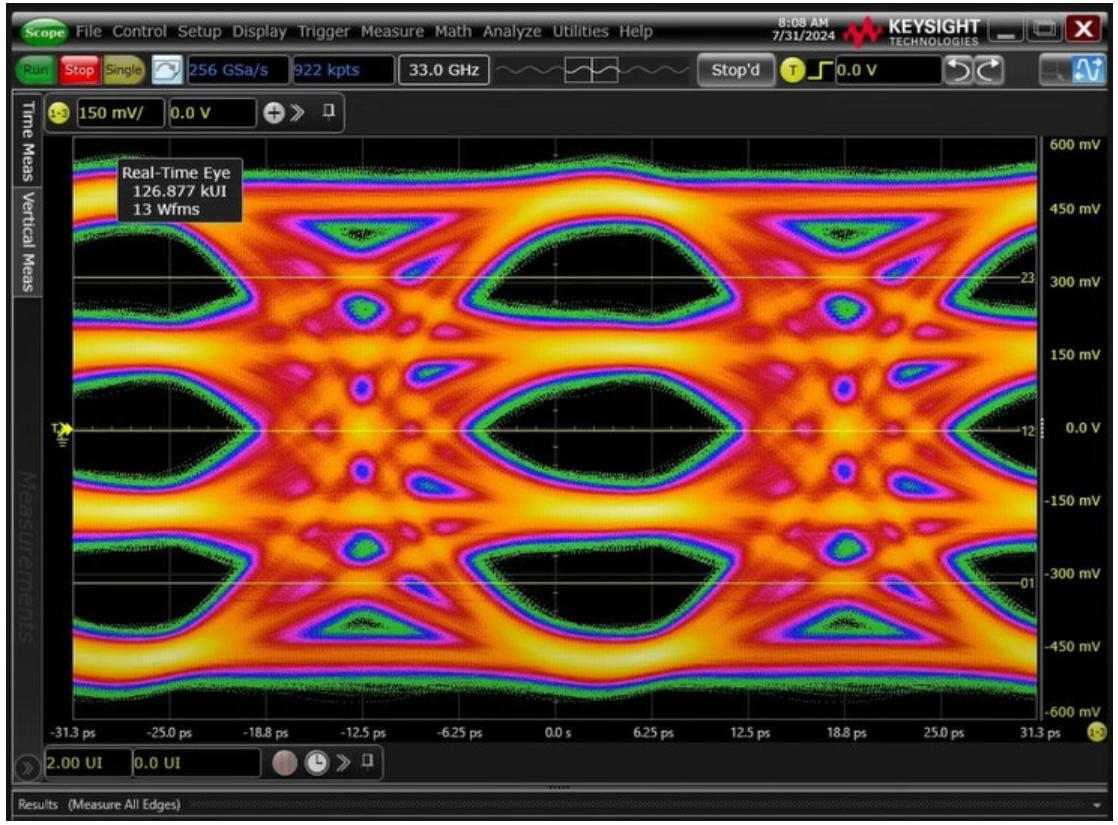


System Level Validation

- Link Stability
  - Check for correctable errors and/or BER
  - Are link recoveries occurring – can cause latency issues
- Link Repeatability
  - Does the link reliably come up over many iterations of link up
  - Do the equalization settings reliably converge to similar values
- Link Quality
  - Industry standard Lane Margining
  - Internal validation tools such as full eye diagrams, destructive margining

PHY Electrical Validation

- Margin Receiver using industry standard bit error rate tester (BERT)
  - PCIe spec defines minimum eye height and width requirements and a corresponding bit error rate
  - How much margin to the spec do we have
  - Verify that performance matches simulation
- TX Signal Quality
  - PCIe has industry standard requirements that must be met to ensure link compatibility with all partners
  - Check over Process, Voltage Temperature



Characterization

- Issues can arise as channel lengths vary
  - Shorter is not always better
  - Receiver architectures designed around worse case
- Need a method to qualify SSDs in customer systems and provide guidance to the quality of the link
  - Can quantify known bit error rates using BERT and correlate to receiver eye metrics
  - Can correlate various calibration and adaptation values over multiple channel lengths and signal quality conditions