UCIe 2.0 Specification: Advancing an open ecosystem for on-package chiplet innovation

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Chairman of UCIe Consortium

UCIe™
Universal Chiplet Interconnect Express

Agenda

- Introducing UCIe
- UCIe 1.0/1.1 Specifications: Recap
- UCIe 2.0: Vertical Chiplets with UCIe-3D
- UCIe 2.0: Addressing SIP challenges through common infrastructure
- Future Directions and Conclusions

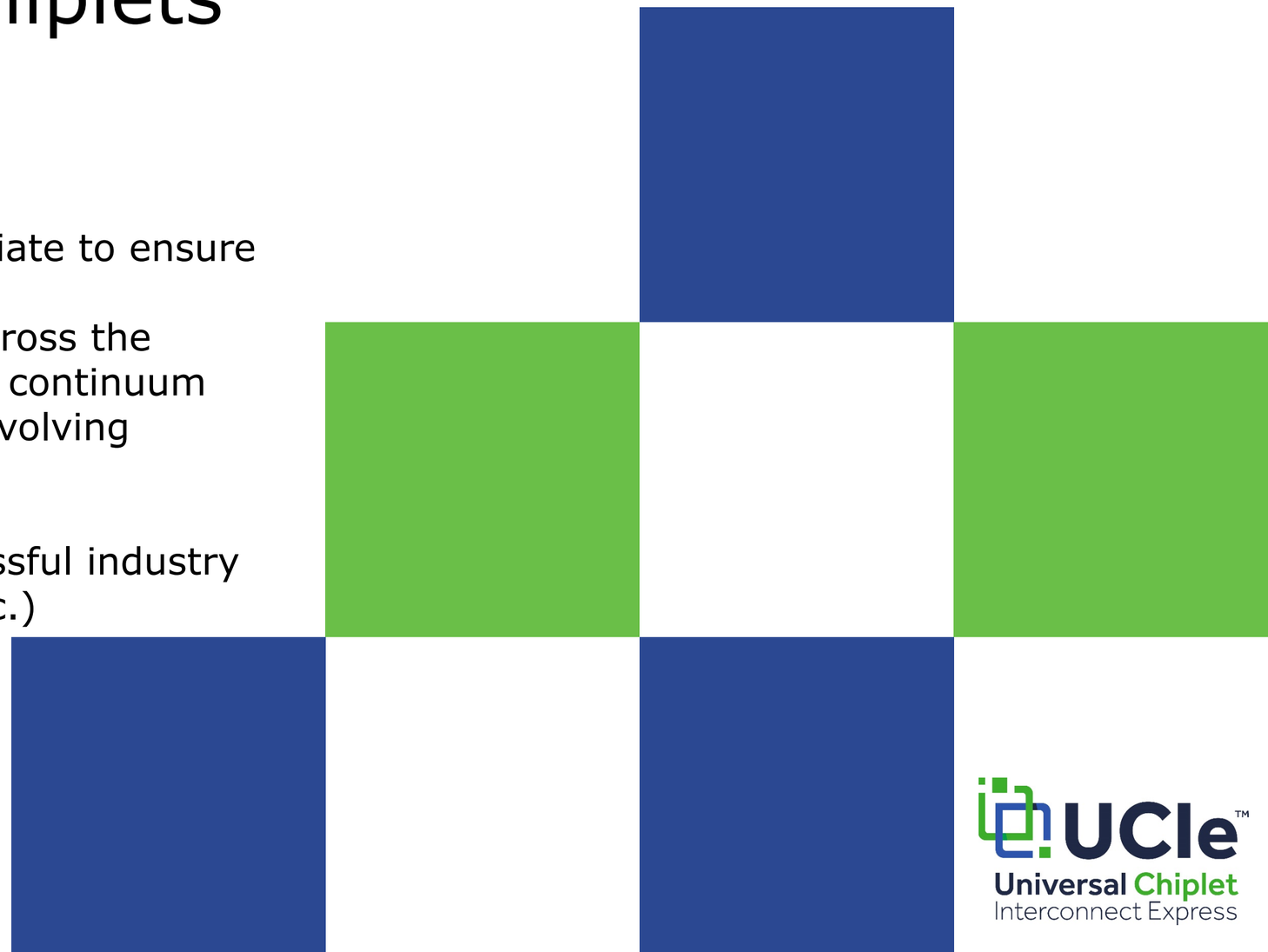
Universal Chiplet Interconnect Express™ (UCIe):

An Open Standard for Chiplets

<u>Guiding principles of UCIe</u>

1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)



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Universal Chiplet
Interconnect Express

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive
The open chiplet ecosystem.

JOIN US!

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Universal Chiplet Interconnect Express

130+ Member Companies…and growing!

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Advanced Micro Devices

Advanced Semiconductor Engineering, Inc.

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Akrostar Technology Co., Ltd

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Amkor Technology, Inc.

Ampere Computing

Analog Devices Incorporated

AP Memory Technology Corporation

Applied Materials, Inc.

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Atron (Chongqing) Technologies, Limited

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Ceremorphic, Inc.

ChangXin Memory Technologies, Inc.

Ciena Corporation

CoMira Solutions Inc

Credo Semiconductor, Inc

Deca Technologies, Inc.

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DreamBig Semiconductor Inc.

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e-Infochips Inc (An Arrow Company)

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Ericsson AB

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The MathWorks, Inc.

Thine Electronics, Inc.

Tongfu Microelectronics Co., Ltd

Toyota Motor Corporation

Truechip Solutions PVT LTD

Tsavorite Scalable Intelligence, Inc

Unisoc (Shanghai) Technologies Co., Ltd

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Universal Chiplet Interconnect Express

UCIe Consortium is Open for Membership

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level.**

- **UCIe** was founded in March 2022, incorporated in June 2022. Two levels of memberships: Contributor and Adopter

- **Contributor Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board
  - Participate in the technical working groups
  - Influence the direction of the technology
  - Access the intermediate (dot level) specifications
  - Election to get to the Promoter Class/ Board every year when the term of half the board completes

- **Adopter Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board

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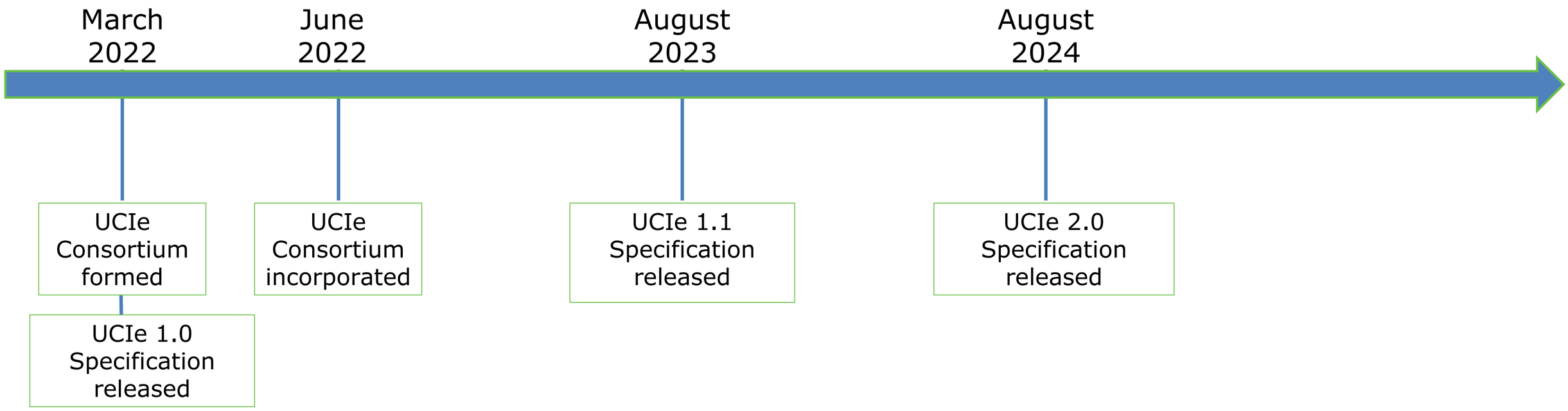
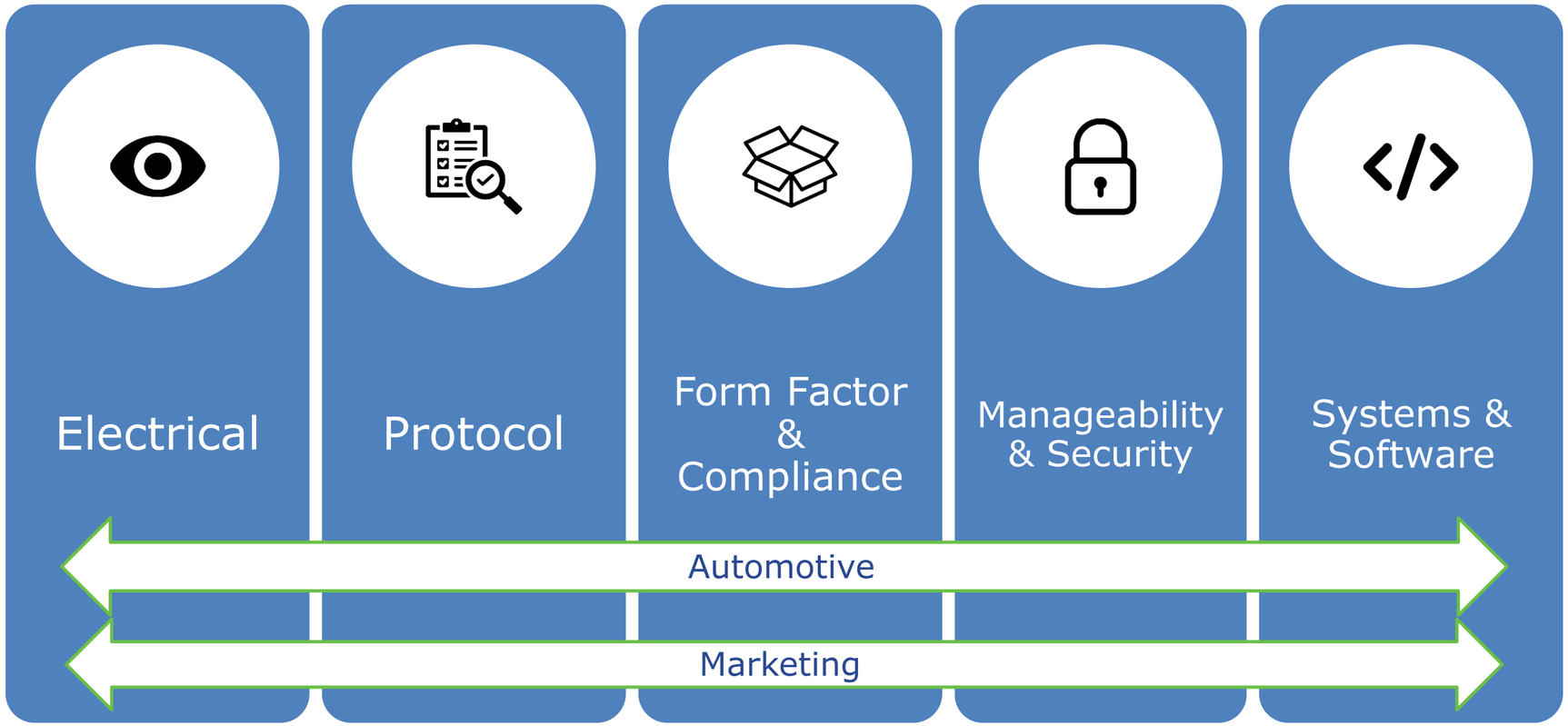
Member Driven Evolution



UCIe Consortium Working Groups

Working Groups are identifying and addressing the demands of a complete, full-stack solution for strengthening the open standards-based ecosystem.



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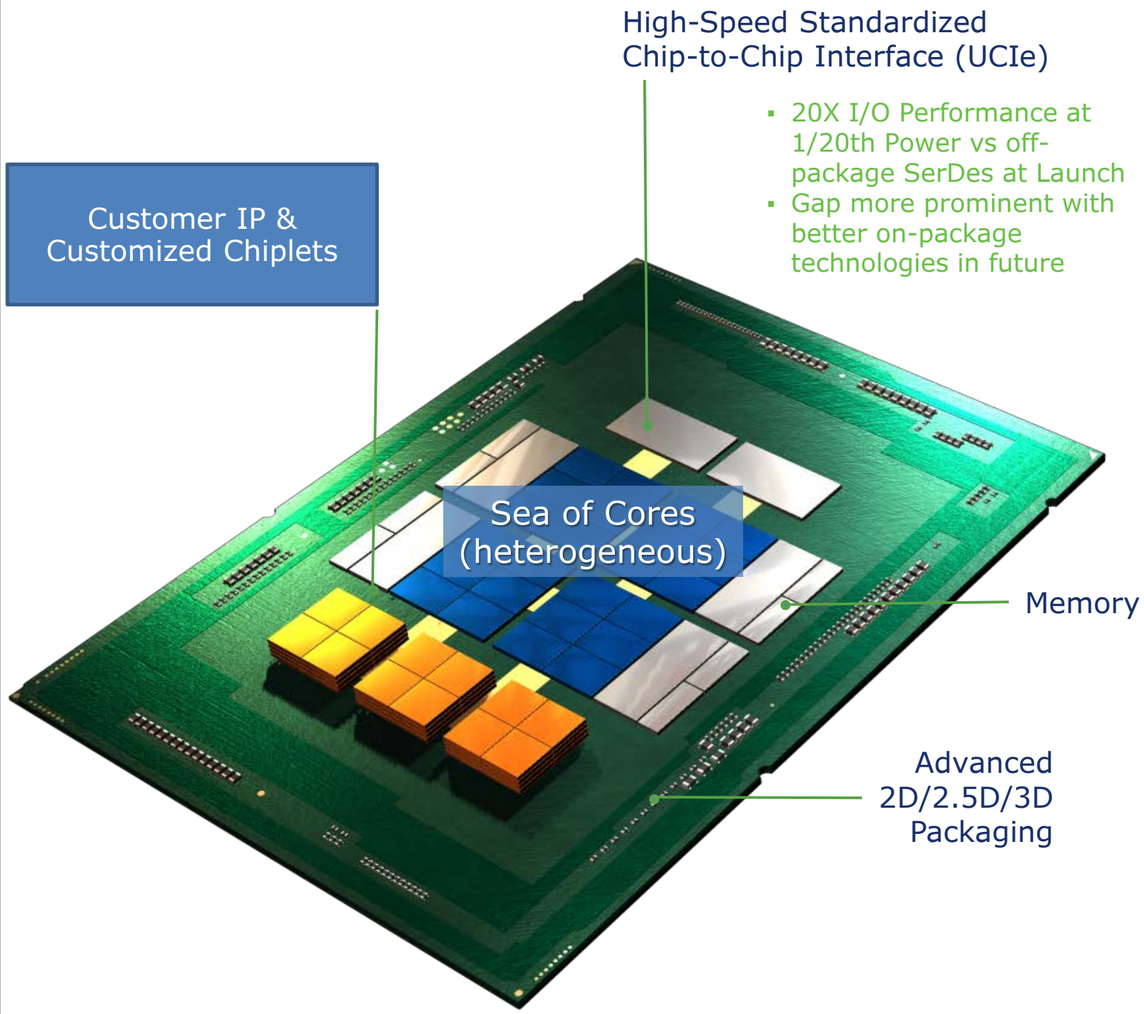
Motivation

OPEN CHIPLET: PLATFORM ON A PACKAGE



Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

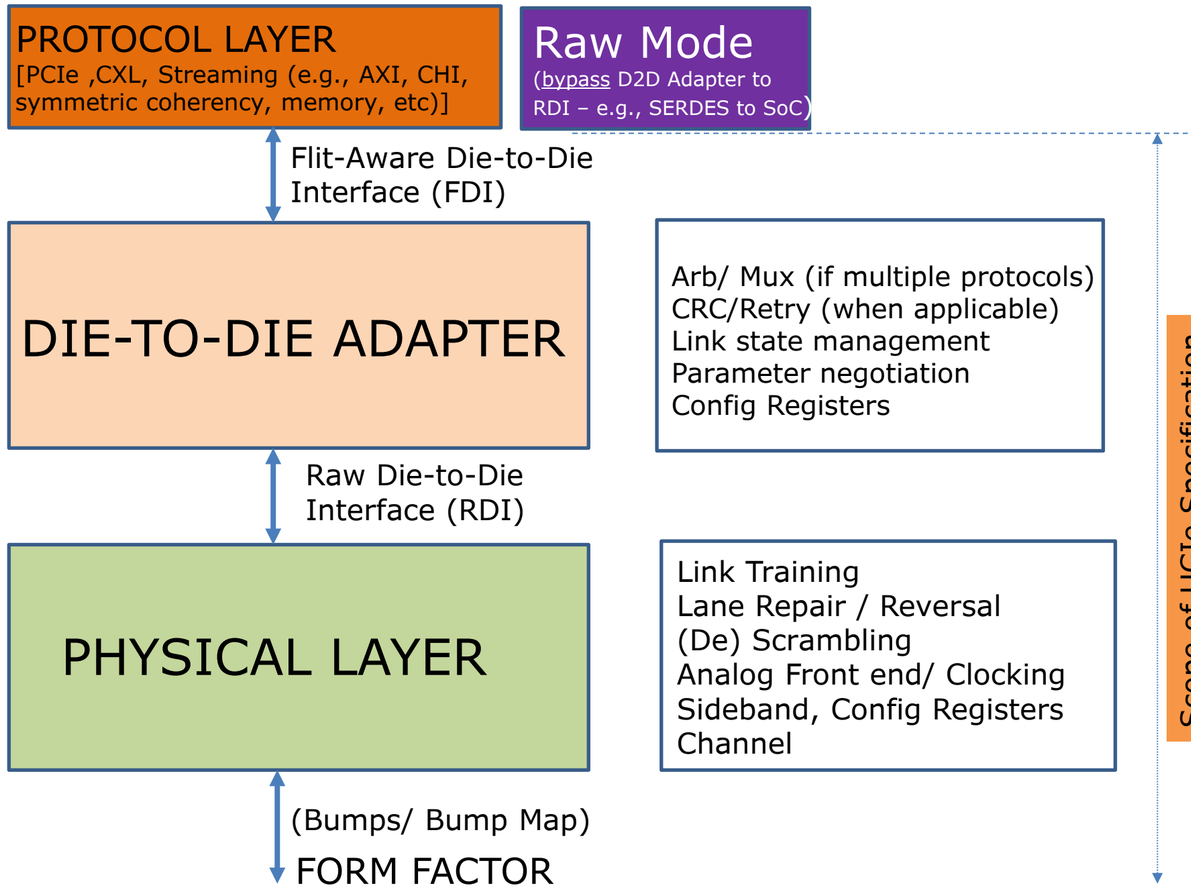
Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing/ process locked IPs)

UCIe™ Universal Chiplet Interconnect Express

UCIe 1.0 Specification

- **Layered Approach with industry-leading KPIs**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:** Reliable delivery
  - Support for multiple protocols: bypassed in raw mode
- **Protocol:** CXL/PCIe and Streaming
  - **CXL™/PCIe® for volume attach and plug-and-play**
    - SoC construction issues are addressed w/ CXL/PCIe
    - CXL/PCIe addresses common use cases
      - I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/ etc)
    - Raw Mode only
- **Well defined specification**: interoperability and future evolution
  - Configuration register for discovery and run-time
    - control and status reporting in each layer
    - transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



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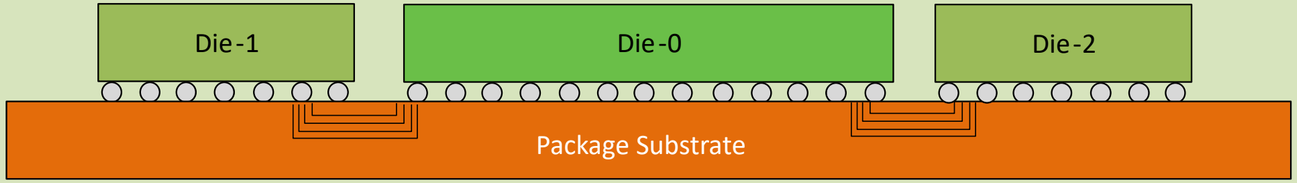
UCIe 1.0: Supports Standard and Advanced Packages

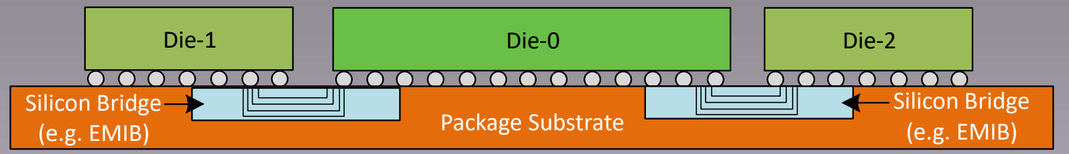


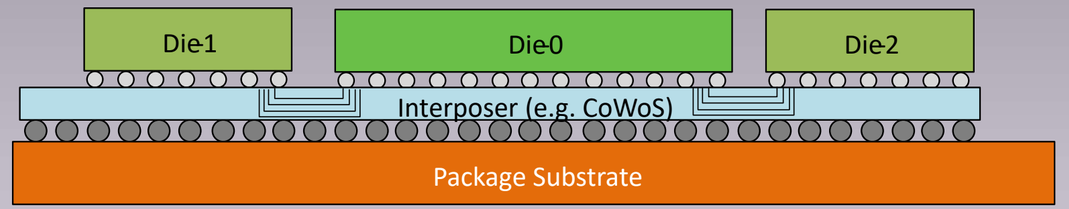
(Standard Package)

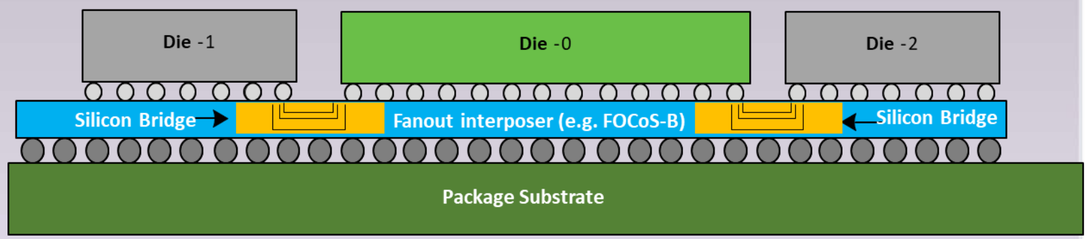
Standard Package: 2D – cost effective, longer distance

Advanced Packages: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer







(Advanced Package Choice Examples)

One UCIe 1.0 spec supports **different flavors** of packaging options to build an open ecosystem

UCIe 1.1 Enhancements

Enhancements for **Automotive Segment** Usage

New Usages: Streaming Protocols with Full Stack

Cost Optimization for **Advanced Packaging**

Enhancements for **Compliance Testing**

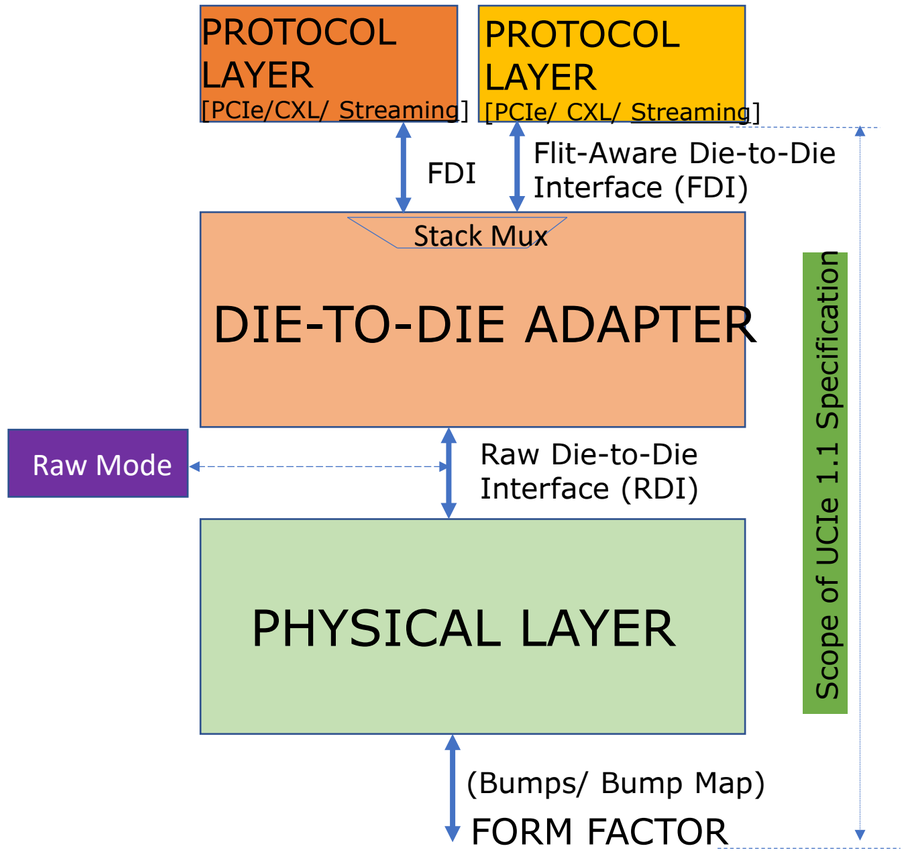
UCIe 1.1 is fully backward compatible with UCIe 1.0

UCIe 1.1: Automotive Enhancements

- Preventive Monitoring:
  - Added new registers to capture Eye Margin (eye width and eye height, if applicable) information in a standard format from training
  - SW can trigger periodic retrain of the link to get eye margin info using existing UCIe 1.0 mechanism
- Run-time Testability of Link Health
  - Existing mechanism in UCIe 1.0: Periodic parity Flit injection and checking for monitoring health of each Lane in mission mode
  - Enhancements in UCIe 1.1: Per-Lane error Log/ counter with ability to send interrupt
  - Usage: Software can inject periodic parity Flit and monitor the UCIe 1.1 error log register to assess the health of each Lane to assess the Link health and repair if needed
- Field Repairability
  - Already present with UCIe 1.0 (mask Lane, retrain, etc) – so no changes in this area
- We will continue to monitor and meet the automotive needs

UCIe 1.1: Streaming Protocols on Full Stack

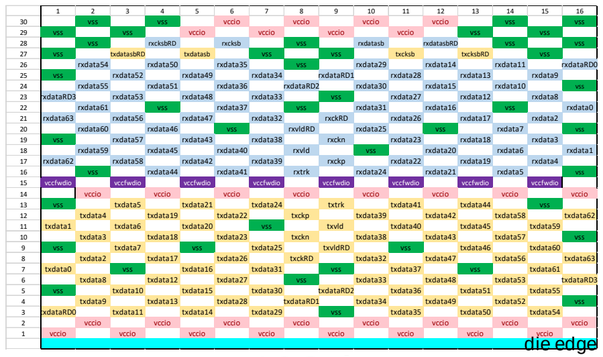
- UCIe 1.0 supports Streaming Protocol (e.g., AXI, CHI, SMP coherency protocols, SFI, CPI) only in Raw Mode
- Two enhancements with UCIe 1.1 (raw mode still supported)
  1. Streaming Protocols can use the D2D adapter
     - Enables them to reuse the CRC, Retry etc.
     - Mechanism: map streaming to existing Flit Formats at FDI interface
  2. Streaming Protocols can multiplex with other protocols with on-demand interleaving
     - Enables co-existence of multiple protocols (e.g., streaming for processing, PCIe for discovery, DMA, TLB, error reporting, interrupt, etc.) for different use cases
     - Mechanism: Protocol muxing for Streaming protocol with existing Flit Formats at FDI interface



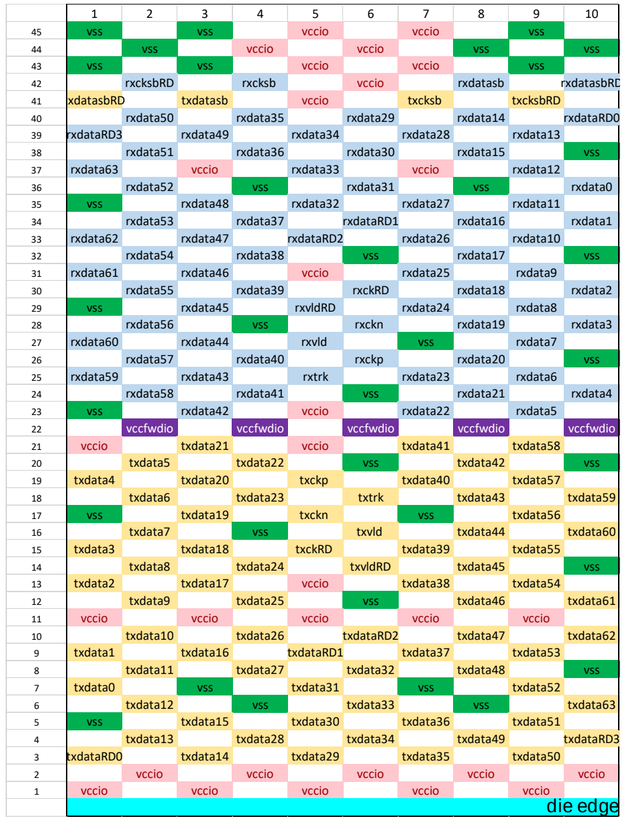
UCIe-A Bump Map Optimization

- Two newly introduced bumpout configurations for maintaining optimized BW/mm^2 across allowable bump pitch range
  - Existing bumpout : 10-column
  - New: 8-column, 16-column
  - Suggested usage guideline:

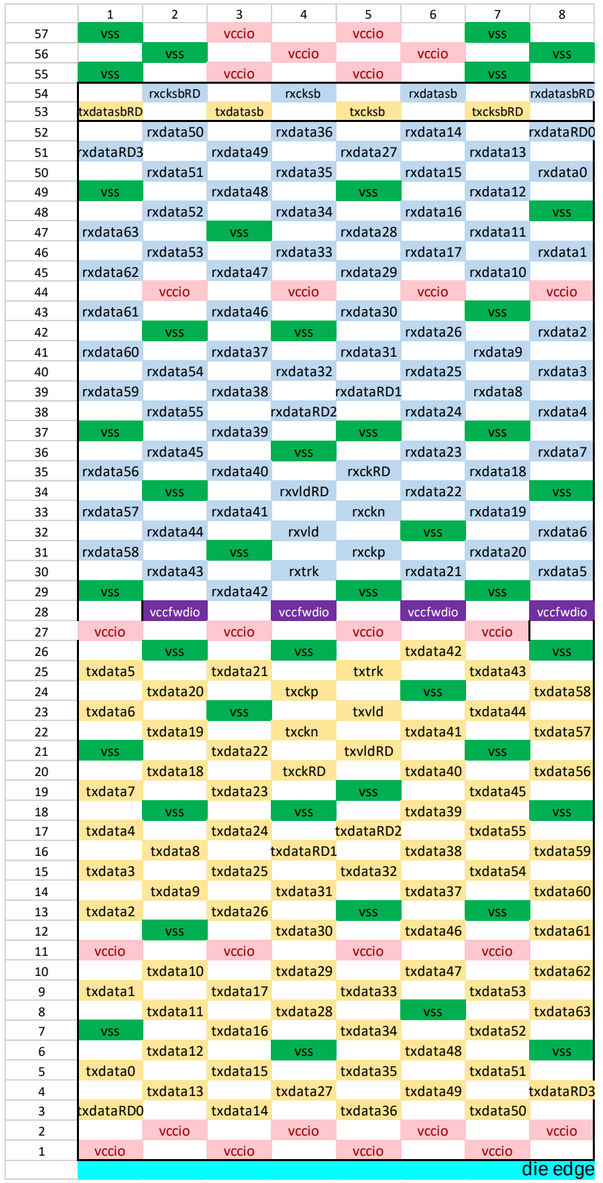
BP	Max Data Rate by Spec	Columns within 388.8 shoreline
25-30	12	16
31-37	16	
38-44	24	10
45-50	32	
51-55	32	8



16Col
Recommended for
25-37um bump pitch

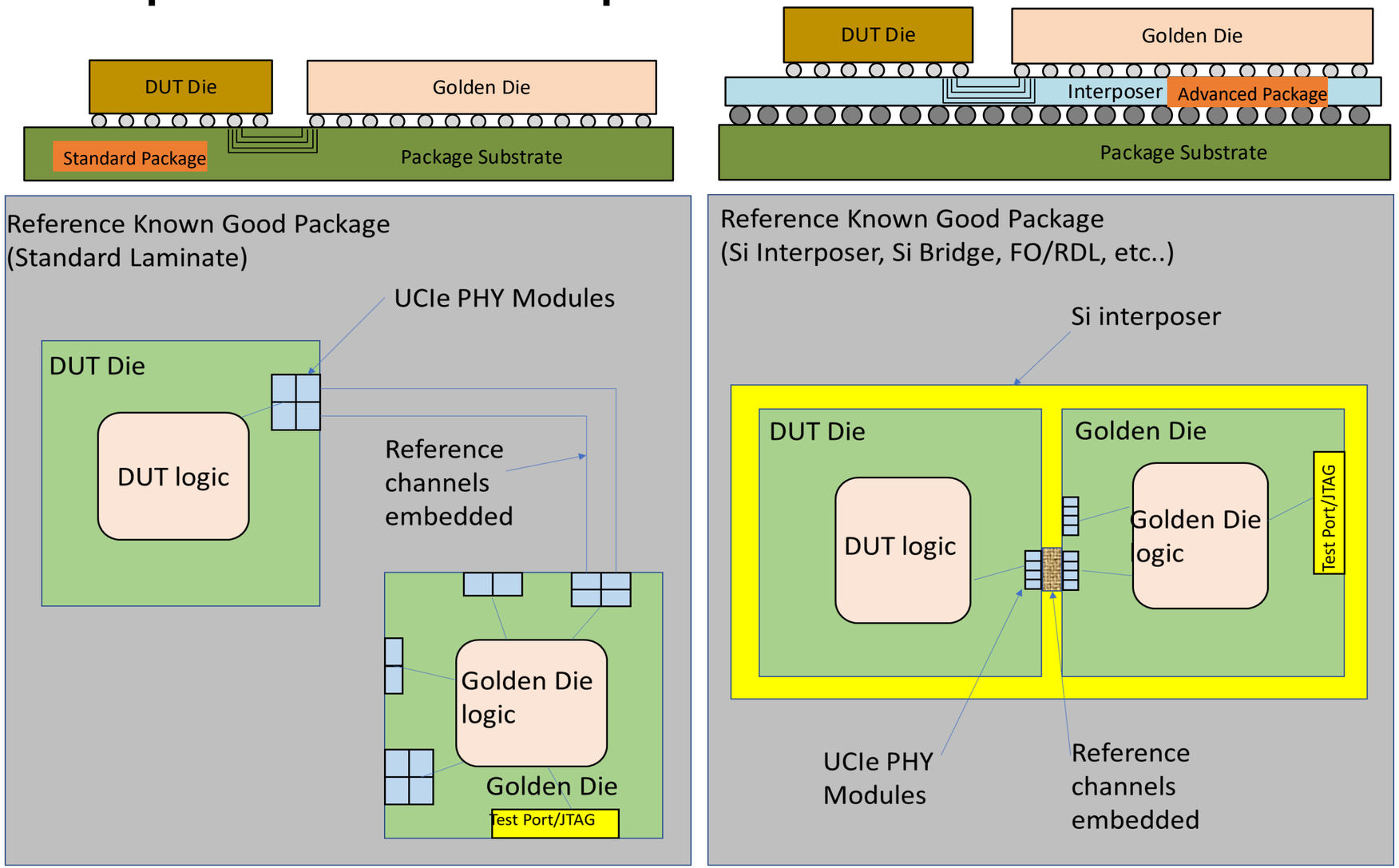


10Col (in spec 1.0)
Recommended for
38-50um bump pitch



8Col
Recommended for
51-55um bump pitch

UCIe Compliance: Setup



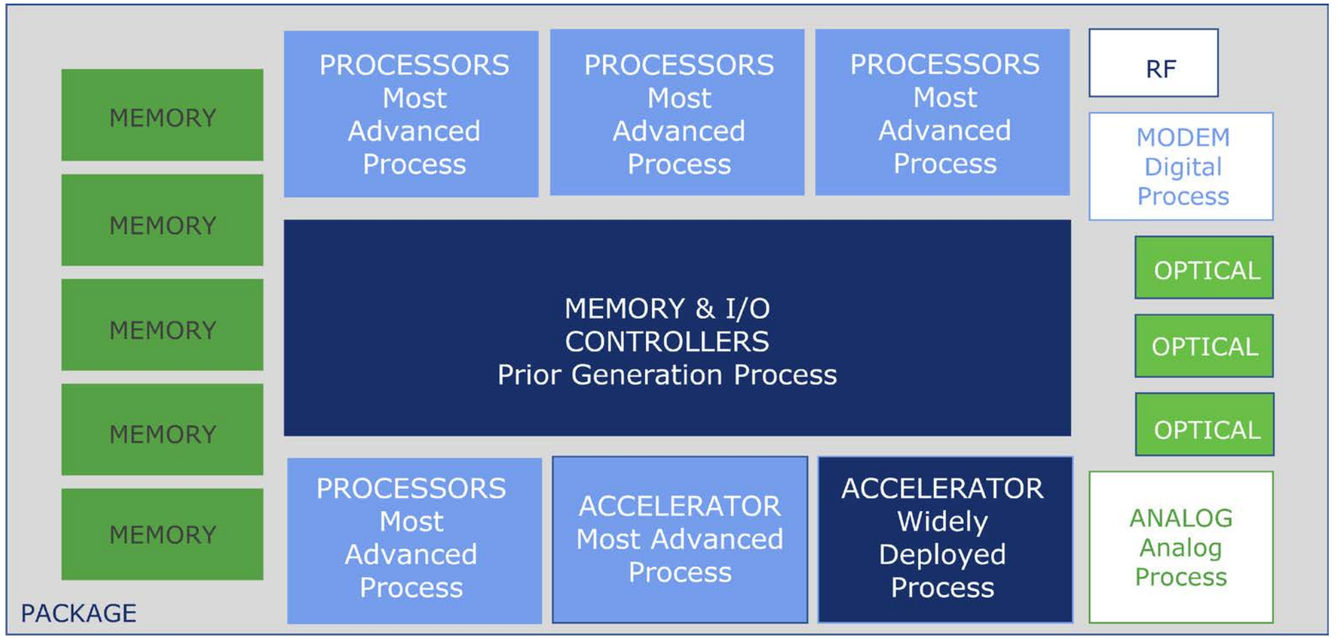
Ingredients: Reference known good package with Reference Channels, Golden Die, DUT

UCIe 1.1 Enhancements: Compliance

- PHY level Compliance:
  - Timing/ Voltage margin, BER measurement, Lane to lane skew, Even/Odd eye asymmetry, Tx EQ – register based control
  - Golden die: all above plus ability to inject errors/ cause timeouts in various phases of training
- D2D Adapter Compliance:
  - DUT: Register based injection of NOP/Test Flit, Replay etc.
  - Golden Die: Support all formats, ability to inject the above, error in sideband, etc
- Protocol Compliance: Expected to be orchestrated through an FPGA / dedicated silicon connected to the golden die
  - Leverage PCIe and CXL protocol compliance as defined by those specifications
  - Streaming Protocols: Use their respective compliance

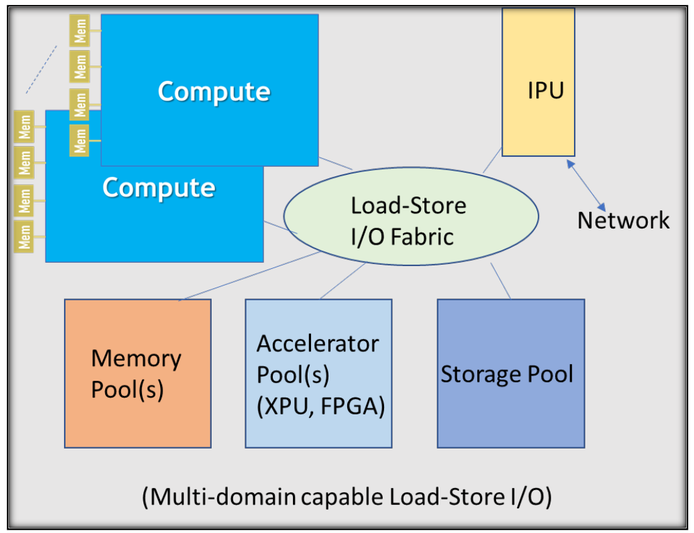
Usage Models for UCIe: SoC at Package level

- SoC as a Package level construct
  - Standard and/ or Advanced package
  - Homogeneous and/or heterogeneous chiplets
  - Mix and match chiplets from multiple suppliers
- Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, Automotive, IoT, etc
- UCIe PHY and D2D adapter common
  - PCIe/CXL protocol for plug-and-play
  - Streaming for others (similar to board level connectivity today where scale-up systems are on PCIe PHY)
  - Similar to PCIe/ CXL at board level

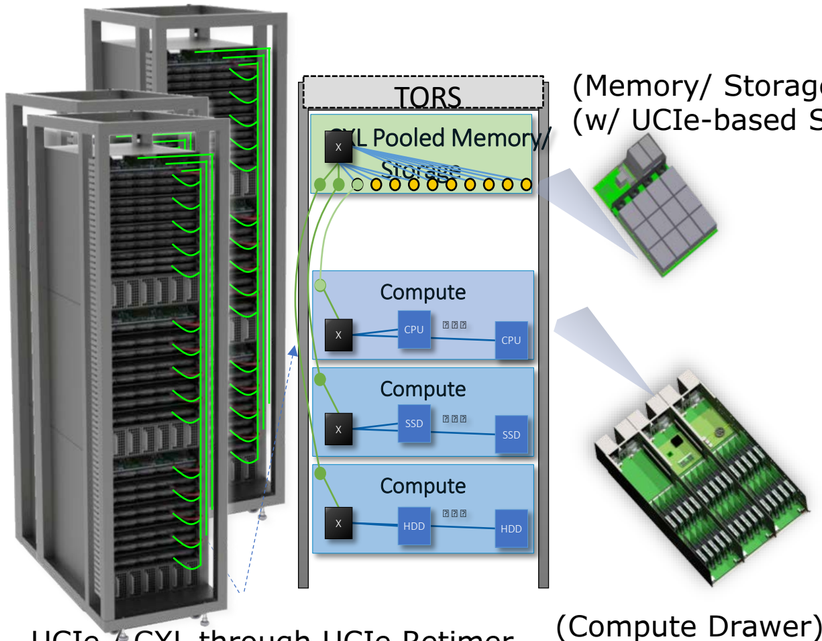


Processors: symmetric coherency protocol mapped on UCIe through FDI
Memory: CXL.Mem mapped on UCIe through FDI
Accelerators: PCIe/ CXL mapped on UCIe through FDI
Modem/ RF/ Optical: Raw mode on UCIe

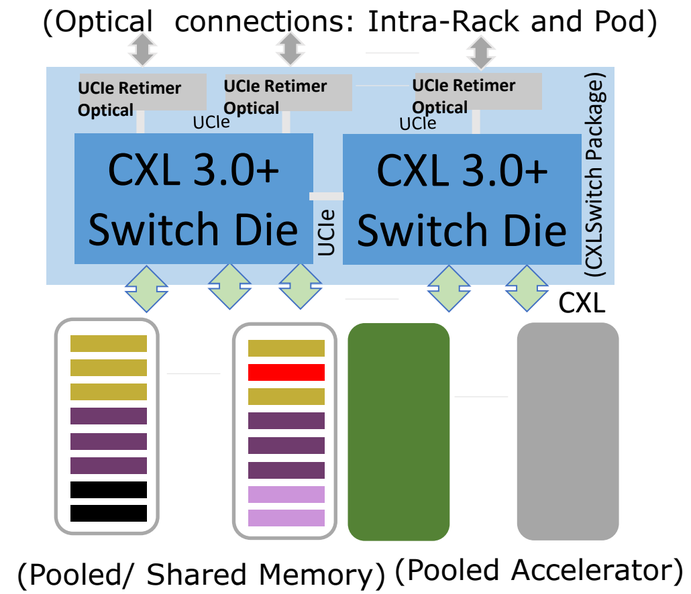
UCIe Usage: Off-package Connectivity w/ Retimers



(Use Case: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/ sharing as well as message passing)

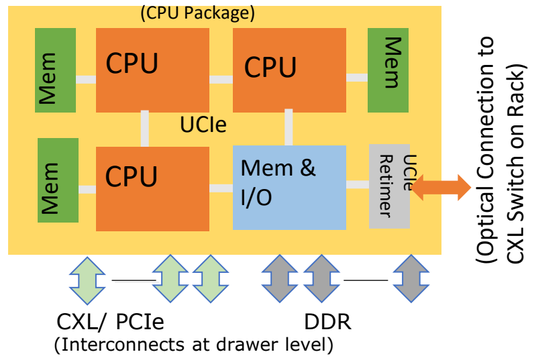


Provision to extend off-package with UCIe Retimers connecting to other media (e.g., optics)

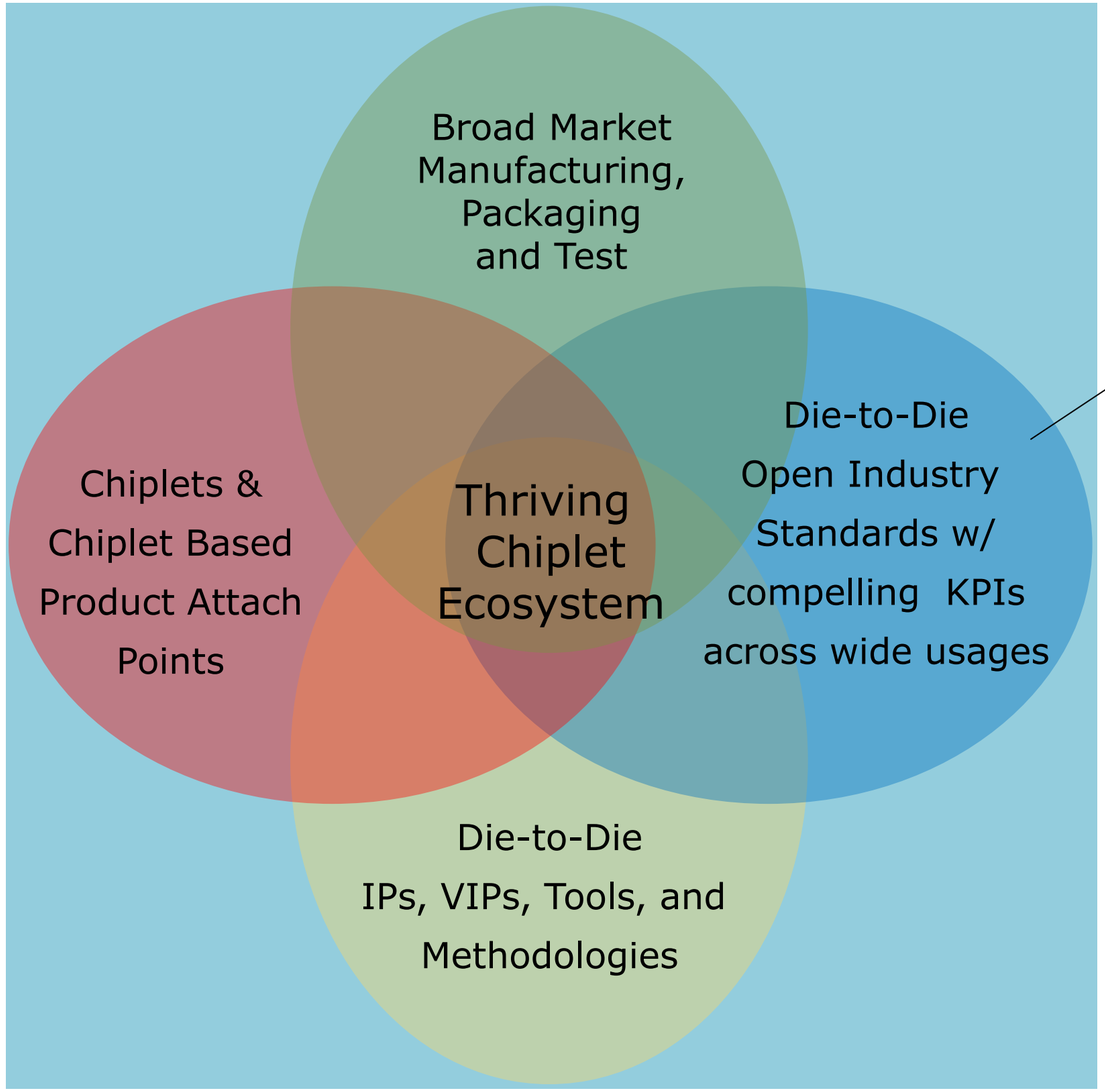


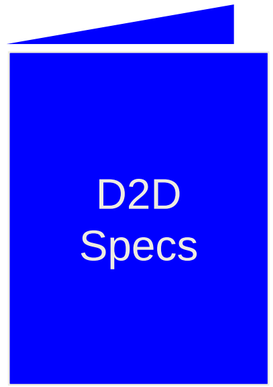
(Switch dies connected through UCIe PHY + Adapter Running a proprietary switch internal protocol)

(Another example can be multi-terabit networking switches Constructed from UCIe-based co-packaged optics and partitionable networking switch dies connected through UCIe on package



Ingredients for a Broad Inter-operable Chiplet Ecosystem



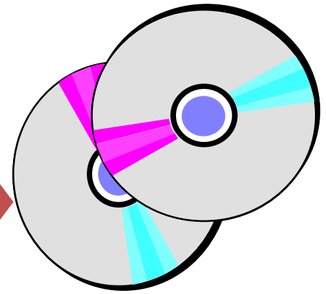


Well-defined Specs

(Electrical, Logical, Protocol (e.g., PCIe/ CXL) Software, Form-Factor, Management)

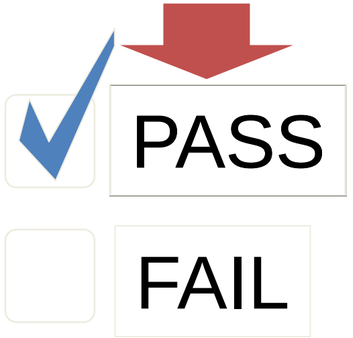
Test criteria based on Specs

(Test Definitions, Pass/Fail Criteria: Electrical, Logical, Protocol, Software)



Test Tools And Procedures

<u>Test H/W & S/W</u>
Validates
Test criteria
- Compliance
- Interoperability



Predictable path to design compliance with UCIe

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- UCIe – Key Metrics
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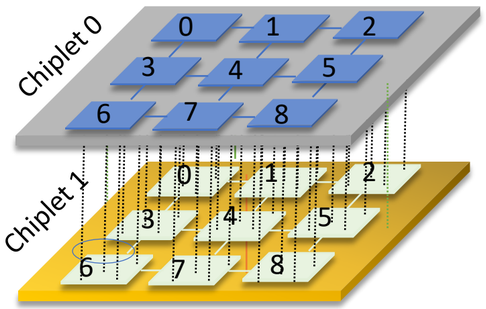
UCIe-3D: Opportunities and Challenges

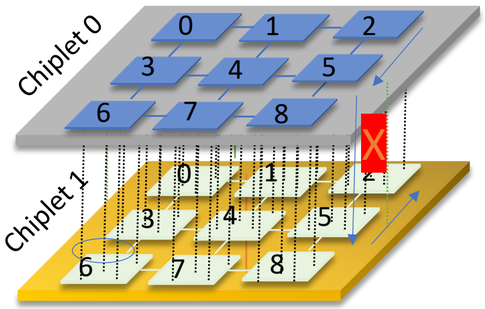
- 3D deployed in commercial offerings (Memory, CPU)
  - Hybrid bonding (HB) looks promising
  - Standardize for constrained interop (e.g., bump pitch match)
- High bandwidth density
  - 3D => areal connectivity (vs shore-line in 2D/ 2.x D)
  - Bump pitches aggressively shrinking
    - Number of wires increases inversely as the square of bump pitch
  - Must ensure we continue to be bump-limited
- Low power
  - Reduced interconnect distance (~0) between dies, electrical parsitics
  - Simple circuits and lower frequency are essential
- Better power, bandwidth, and latency than UCIe 2.5D

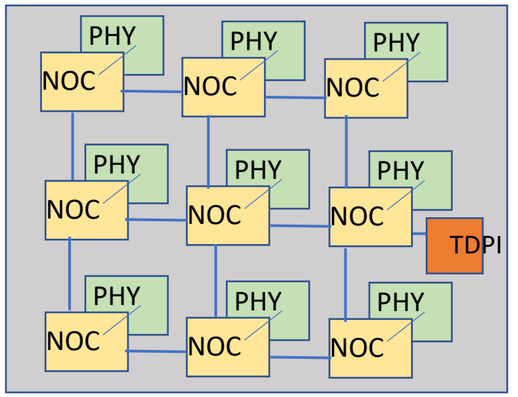


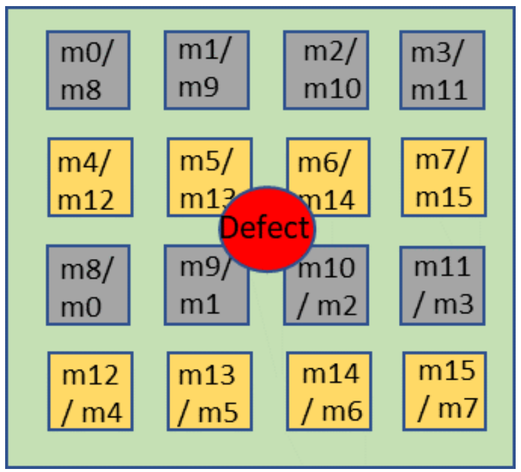
3D can deliver power-efficient performance comparable/ better than large monolithic die

UCIe-3D Approach: Towards Compelling KPIs

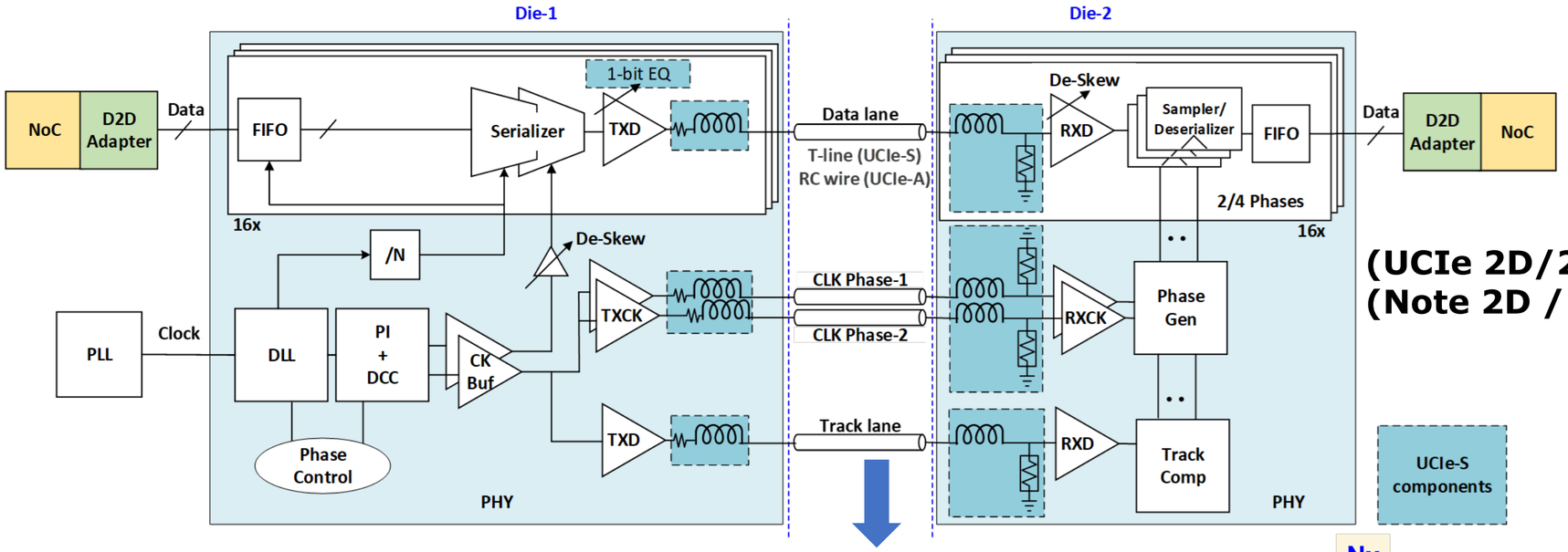
- PHY: unidirectional, forwarded clock, Hard IP
  - No ESD, inverter-based design
  - Lower frequency for lower power/area
  - No (de)serialization .. No deskew
- No D2D Adapter: NOC directly connected to PHY
  - BER 1E-27 -> 1E-30 – no CRC/ Replay
  - Repair: cluster level - a defect may impact multiple ubumps
- Centralized (chiplet) level function
  - Test, Debug, Pattern gen/ check Infrastructure (TDPI)
  - Amortizes overhead since there will be multiple Links



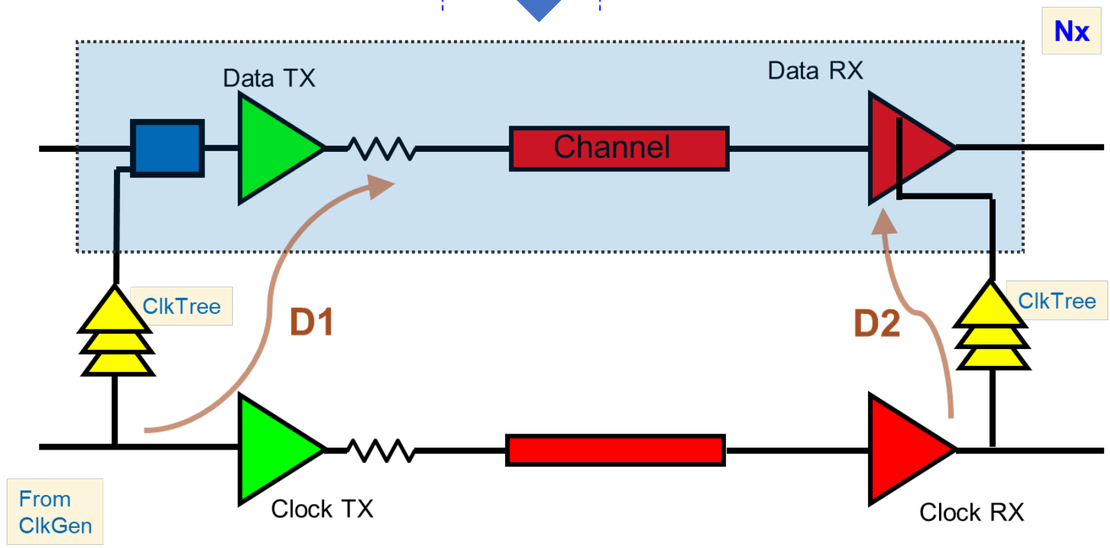




UCIe-3D: Significant Simplification over UCIe 2.5D/2D



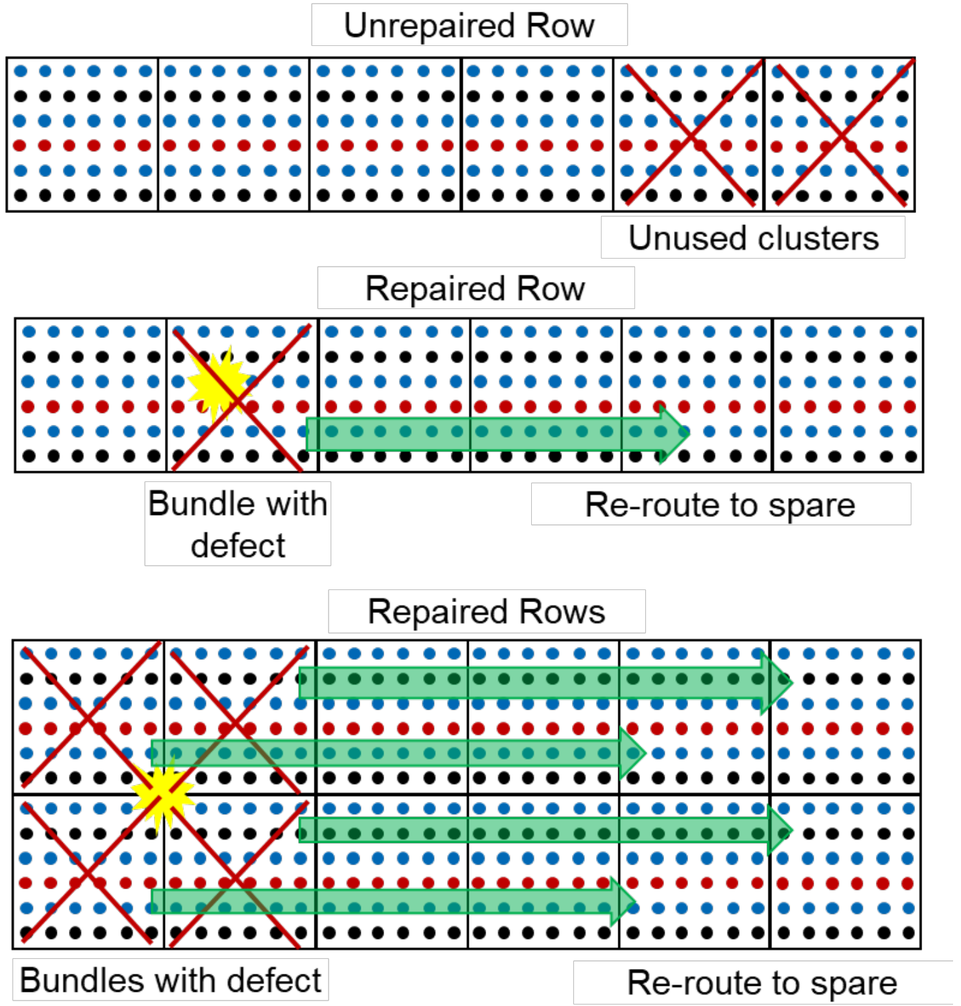
(UCIe 2D/2.5D Circuits)
(Note 2D / UCIe-S has more components)



(UCIe-3D Circuit)

Repair: Baseline Approach

- Reserve modules in SoC for repair, reroute to the backup module when there is a failure.
  - To address cluster failure mode. Defects are larger than bumps. For example, one defect can take out 5x5 bump area.
- UCIe3D: Each Module has one TX bundle (x64 TX + Clock) and one RX bundle (x64 RX + Clock). Bundle layout is roughly a square, ~ 100um x 100um for 9um bump pitch.
- For densely packed 2D UCIe Module array, reserve 2 full Modules (4 bundles) to repair one failure cluster.
  - Assume alternating TX, RX bundle in at least one direction.



Key Metrics: Expanding Industry Leading KPIs to UCIe-3D

Characteristics / KPIs	UCIe-S (2D)	UCIe-A (2.5D)	UCIe 3D	Comments for UCIe 3D
Characteristics				
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Up to 4	= SoC Logic frequency – power efficiency is critical
Width (each cluster)	16	64	80	Options or reduced width to 70, 60…
Bump Pitch (µm)	100 – 130	25 – 55	≤ 10 (optimized) > 10 – 25 (functional)	Must scale so that UCIe-3D fits within the bump area, must support hybrid bonding
Channel Reach (mm)	≤ 25	≤ 2	3D vertical	FtF bonding initially; FtB, BtB, multi-stack possible
Target for Key Metrics				
BW Shoreline (GB/s/mm)	28 – 224	165 – 1317	N/A (vertical)	
BW Density (GB/s/mm^2)	22 – 125	188 – 1350	4,000 – 300,000	4TB/s/mm^2 @ 9µm, ~12TB/s/mm^2 @ 5µm, ~35T/s/mm^2 @ 3µm, ~300T/s/mm^2 @ 1 µm
Power Efficiency Target (pJ/b)	0.5	0.25	<0.05 at 9µm -> 0.01 at 1 µm	Conservatively estimated at 9µm pitch <0.02 for 3µm pitch
Low-Power Entry/Exit	0.5nS ≤ 16G, 0.5-1nS ≥ 24G		0nS	No preamble or post-amble
Reliability (FIT)	0 < FIT (Failure in Time) << 1		0 < FIT << 1	BER < 1E-27
ESD	30V CDM		5V CDM → ≤ 3V	5V CDM at introduction, no ESD for W2W hybrid bonding possible

UCIe-3D will deliver compelling power-efficient performance

UCIe™
Universal Chiplet Interconnect Express

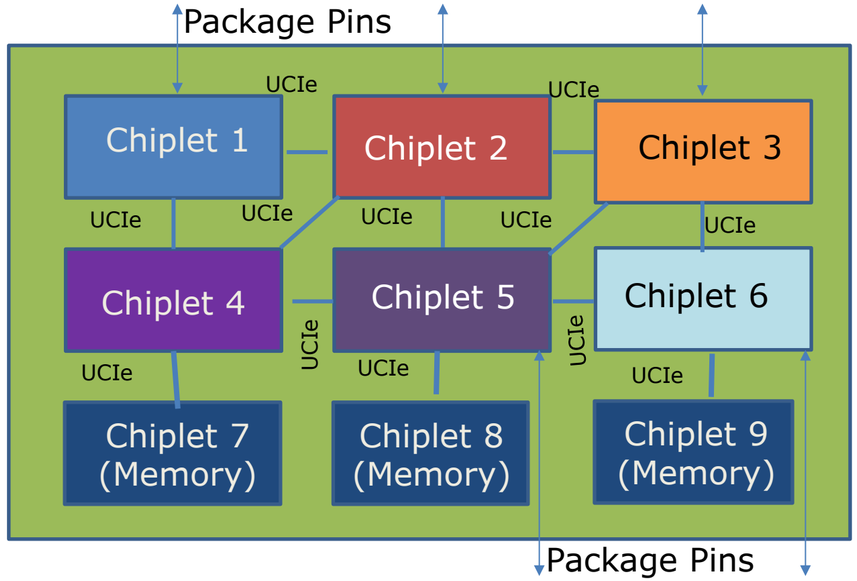
Agenda

- Introducing UCIe
- UCIe 1.0/ UCIe 1.1 Specifications: Recap
- UCIe 2.0: Vertical Chiplets with UCIe-3D
- UCIe 2.0: Addressing SIP challenges through common infrastructure
- UCIe – Key Metrics
- Future Directions and Conclusions

SiP Challenges: Testability, Debug, Telemetry, and Manageability: Design for Testability/ Debug/ Manageability (DFx)

- UCIe 1.0/1.1 already has several mechanisms in place for DFx at the interconnect level
  - E.g., lane margin, loopback, compliance, fault reporting, sideband, etc
- Need to look at the entire chiplet/ package in a holistic manner to ensure a thriving chiplet-based plug-and-play ecosystem
- Test: Die / Sort, Package / Bond
  - Micro-bumps can not be probed => Use other bumps (e.g. JTAG, UCIe-S)
- Debug in lab and field (e.g., can not use a scope/ logic analyzer)
- Manageability w/ security (e.g., repair, firmware upgrades)
- Some chiplets may not have access to package pins
  - Use UCIe to access remote chiplets from chiplets with package pins (dedicated UCIe-S/ muxed)
- Wide range of bandwidth demands

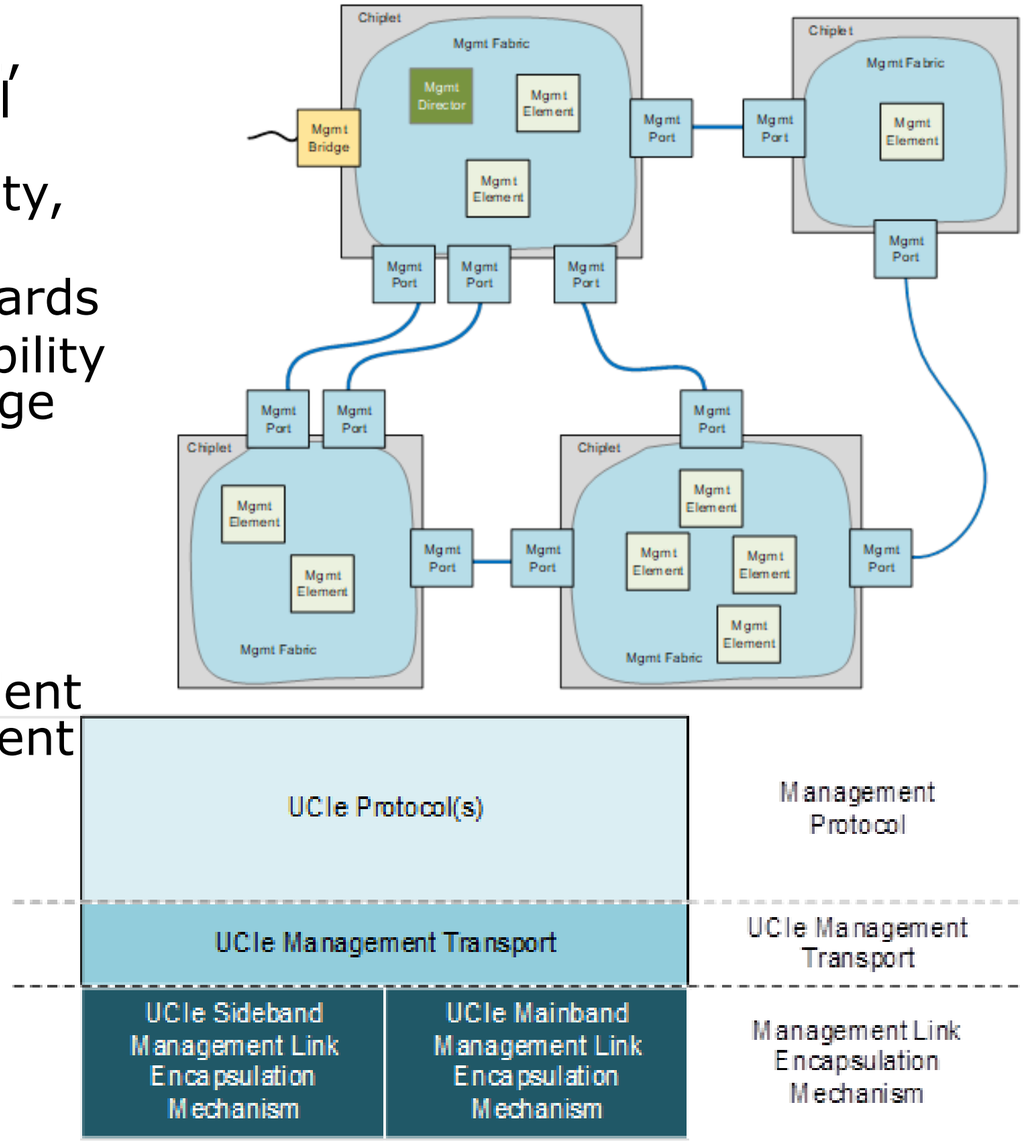
Common infrastructure for entire lifecycle.
Leverage existing package pins and standards
Added SB-only as well as x8 UCIe-S dedicated port for DFx



Interface	Bandwidth
UCIe-S x16	512 Gb/s/dir main @ 32G (800 Mb/s/dir sideband)
PCIe6.0 x16	1024 Gb/s/dir
USB 4.0	80 Gb/s/dir
JTAG (IEEE 1149.1)	5-100 Mb/s/dir
IEEE 1838	>100 Mb/s/dir with FPP
I2C/SMBus	400 Kb/s
I3C	33 Mb/s/dir

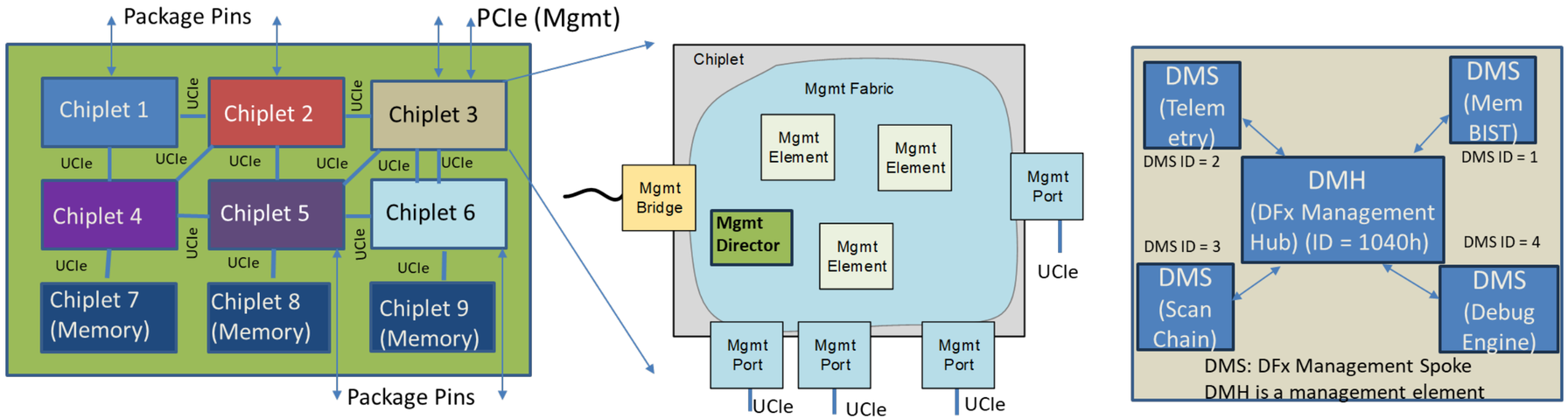
UCIe 2.0 Manageability Baseline Architecture

- Mechanisms supported : Discovery of chiplets and their configuration, initialization of chiplets and parameters (e.g., EEPROM replacement), firmware download, power/ thermal management, error reporting, telemetry, retrieval of crash dump log, test and debug, various aspects of chiplet security, etc.
- Protocol-agnostic – builds on top of existing industry standards
- Management domain: chiplets that support UCIe manageability are interconnected through management ports, with a bridge to an external package pin (e.g., SMBus, PCIe)
  - Chiplets that don't support UCIe management are outside the domain
  - Management director: discovery, configuration, coordination of overall management within SiP, root of trust for manageability
- UCIe Management Transport – end-to-end media-independent protocol for management communication on the management network (management entities within/ across chiplet(s))
- UCIe Management Transport Packet for communication
  - Sideband and Mainband
  - Up to 8 VCs, each with (un)ordered semantics
  - Credit based – negotiated during link training

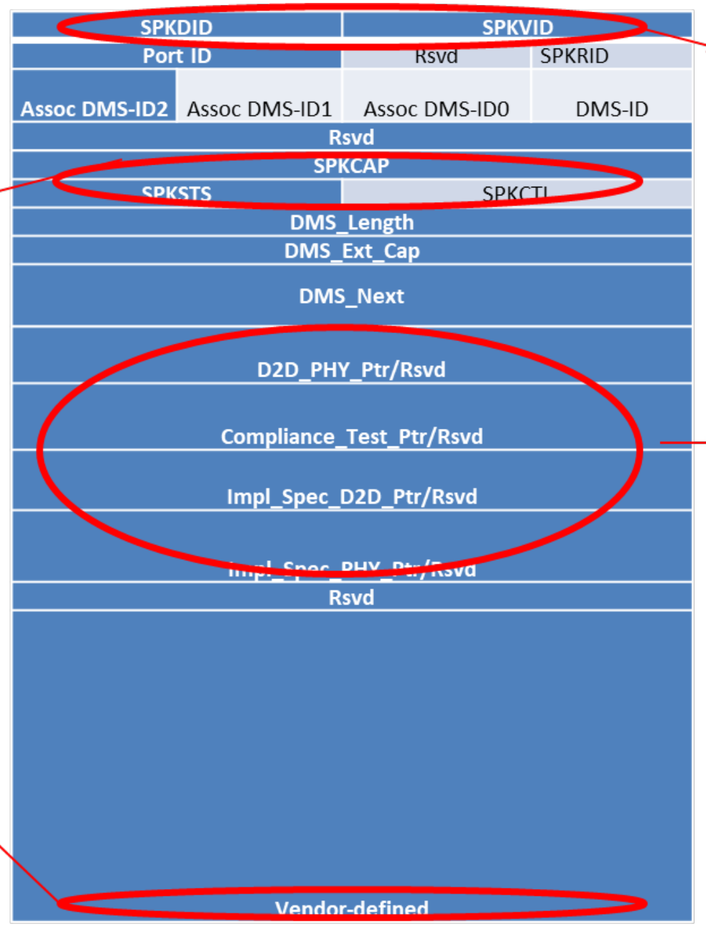


UCIe DFx Architecture (UDA): Common Infrastructure

- UDA comprehends test, telemetry, debug – covered through the management fabric
- Hub and Spoke(s) inside each chiplet
- DFx Management Hub (DMH) is a management element
  - Gateway to access test, debug, telemetry capability inside each chiplet
  - Routes the management transport packets to Spokes (DFx Mgmt Spoke: DMS)
  - Routes to other chiplet (DMH)
- DMS: test, debug, telemetry functions
  - E.g., Scan controller, Mem BIST, SoC Fabric debug, trace protocol engine, etc.
- Architected configuration registers on top of existing registers – basically a UCIe wrapper on top of existing registers
- UCIe issued Vendor ID, Device ID , RID for spoke



Standardized Configuration for Test, Debug, Manageability



Basic Cap/Cntrl/Sts – E.g., Spoke type, UDM payload size supported/Control.

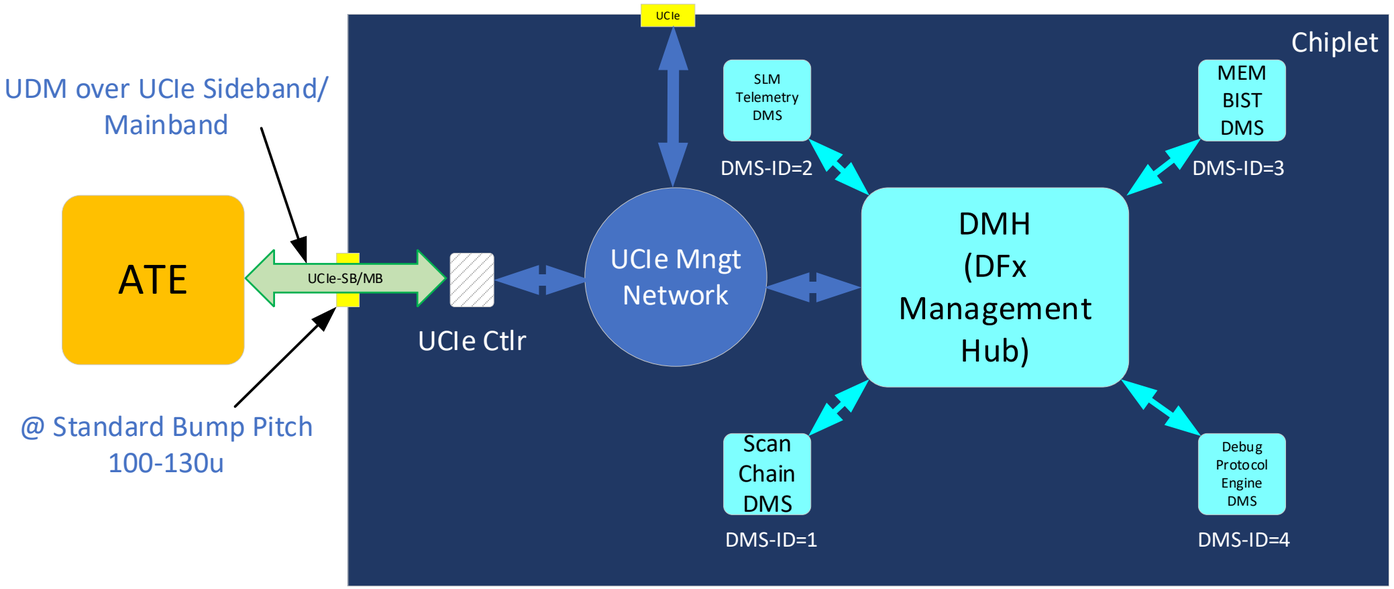
- Identifies SpokeVID/DID/RID
- Different vendors in one chiplet (e.g., RAMBIST, PCIe, UCIe PHY, etc)
- Notion of a driver that knows how to use the underlying functionality based on VID/DID

- Pointer to UCIe link registers, if Spoke associated with a UCIe link

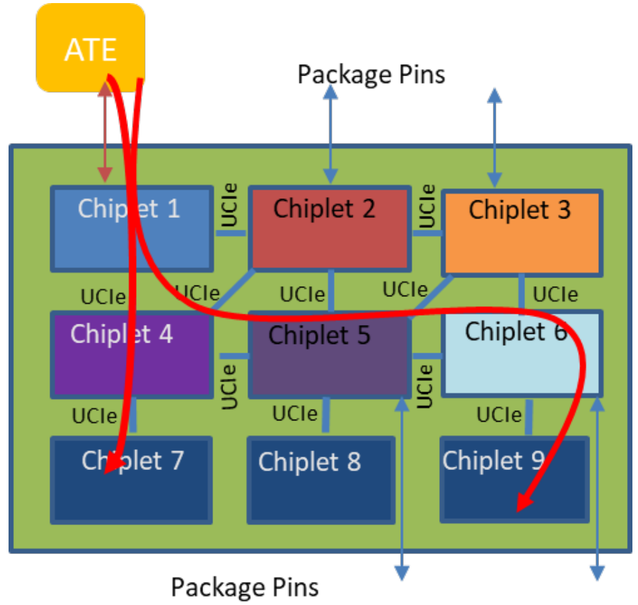
Vendors do what they want. E.g., map prop. debug registers, map internal debug array etc.

UDA: Simple, minimal standard header for DMS; rest is vendor-defined

Example Usages of UDA



(a: ATE testing during sort using UCIe-S pins: sideband and/or mainband)

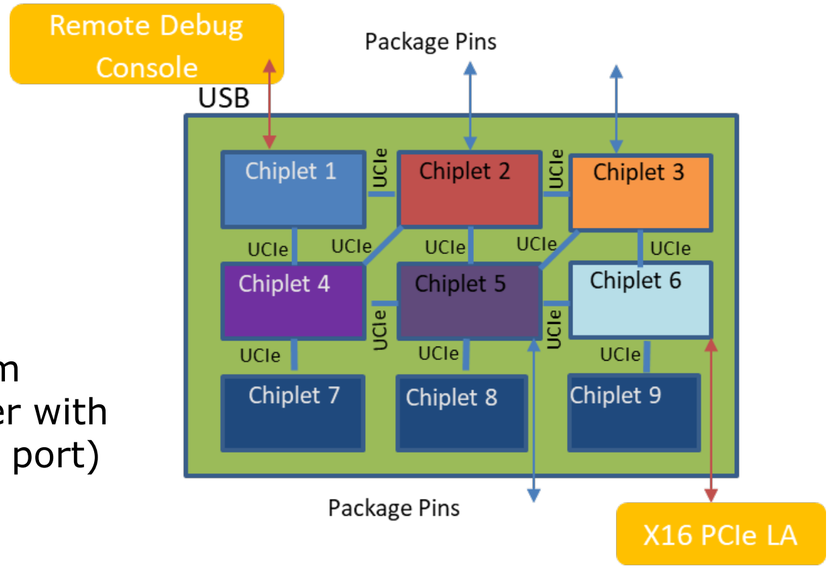


(b: ATE testing after packaging using UCIe-S pins: sideband/mainband)

Package pins used for Test & Debug

Package pins used for functional purposes

(c: Routing multiple sets of debug signals from Chiplets through UCIe to a PCIe Logic Analyzer with The remote debug console (control) on a USB port)



Summary

- UCIe Consortium continues to evolve UCIe technology in a backward-compatible manner comprehending new usage models, additional cost optimization, and towards a robust compliance mechanism.

- UCIe is an open industry standard that establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.
  - Tremendous support across the industry with several companies announcing IP/VIP availability
  - Evolving as *the* interconnect of SoCs just as PCIe and CXL at the board level
  - UCIe 2.0 Specification is available to the public https://www.uciexpress.org/specification

- UCIe Consortium welcomes interested companies and institutions to join the organization at the Contributor or Adopter level.

- 6 Technical Working Groups (Electrical, Protocol, Form Factor/Compliance, Manageability/Security, Systems and Software, Automotive) alongside the Marketing Working Group are driving the technology toward the future.
  - Incredible innovation happening in the Consortium!

- Get involved! Learn more by visiting www.UCIexpress.org

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Thank You

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