Embedded OTP Memory Solution Towards 3nm Generation: High Security Purposes

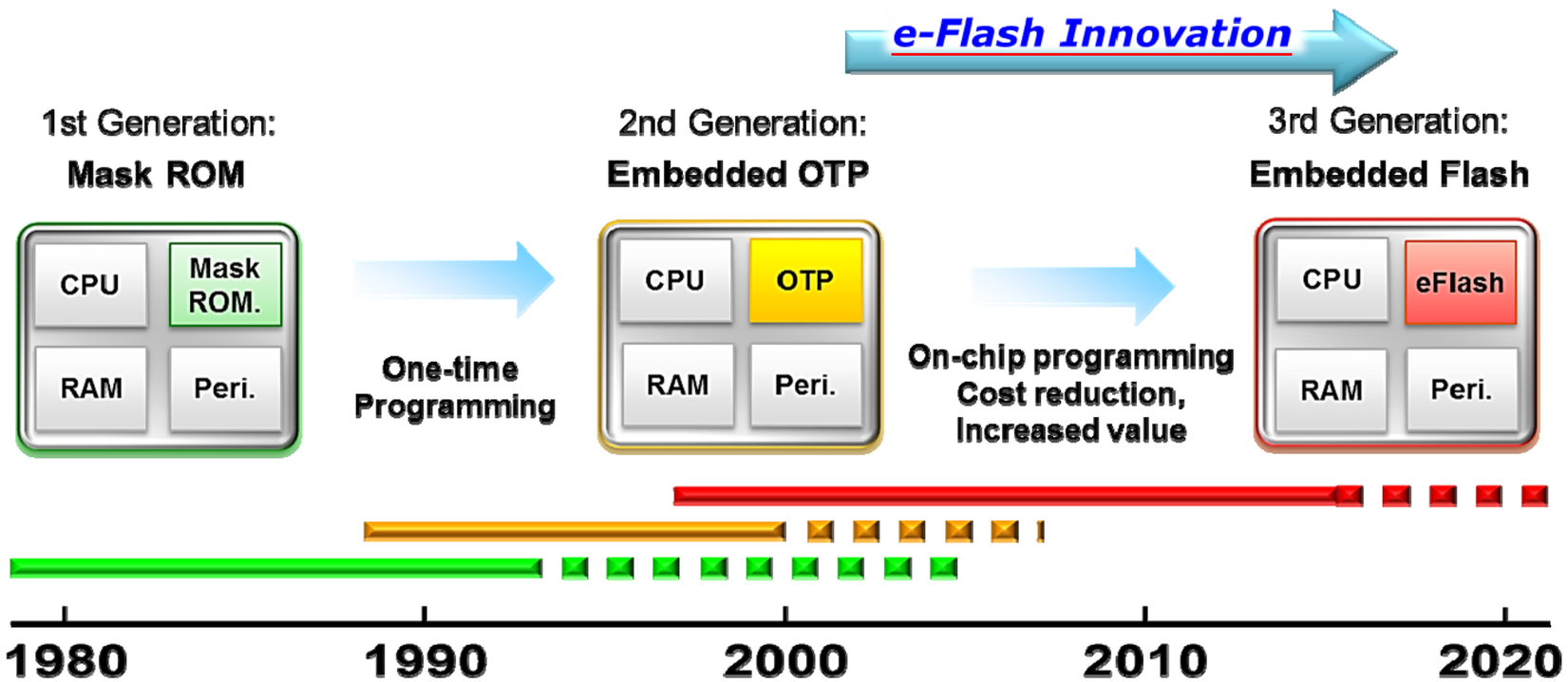
Steve S. Chung
Chair Professor
National Yang Ming Chiao Tung University

Outline

- Introduction
  - Motivation- General & application
  - Two Conventional OTP Structure
- Unit Cell Design of OTP Memory
  - Operation Mechanism – Dielectric fuse
  - Macro Design and Validation
- Another Application
  - Realization in FinFET Generation
  - PUF
- Summary and Conclusions

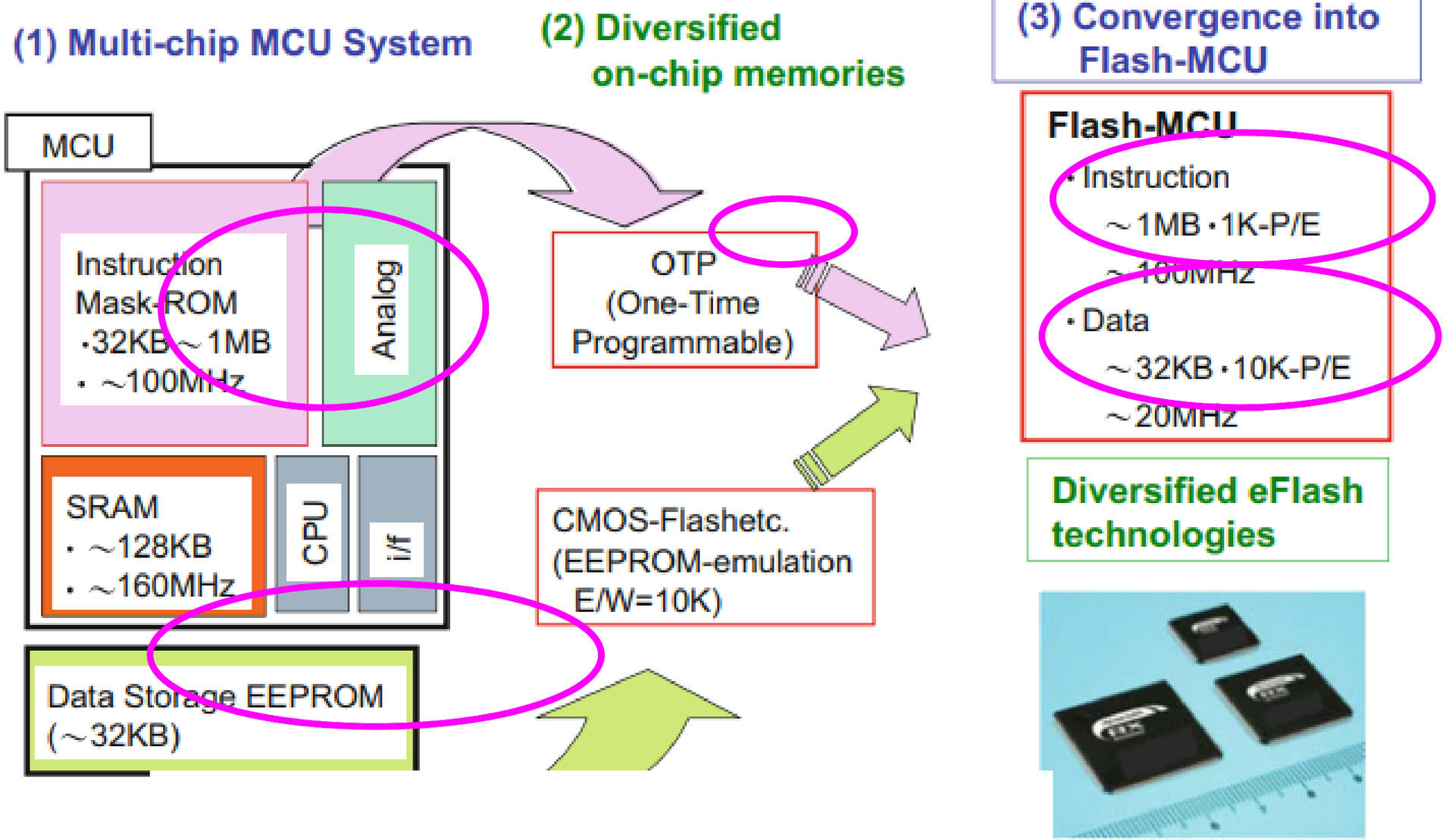
Embedded NVM

- NVM mounted on MCU and SoC chips with other IPs (CPU etc.).
- Market Size ~ $20B /Worldwide
- Multiple time programmability innovates MCU development and delivery.



[modified from] Y. Tiaito, 2018 VLSI-TSA Short Course

System Level Design

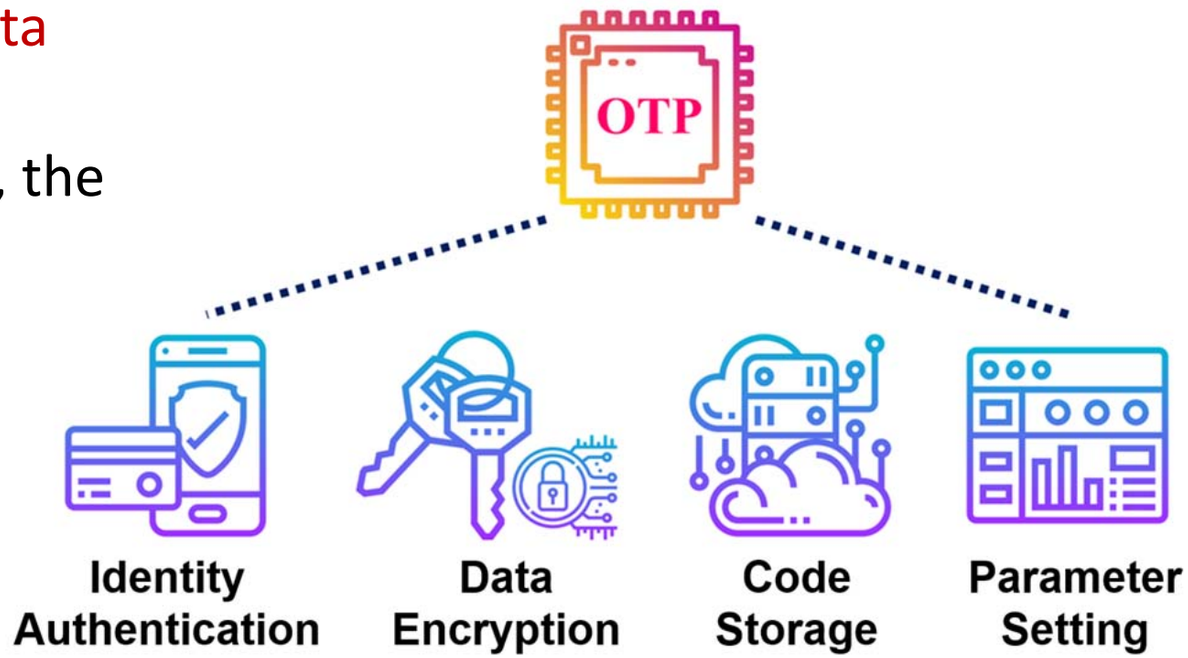


H. Hitaka
Springer 2018

Fig. 2.6 Convergence into a standard flash-MCU configuration

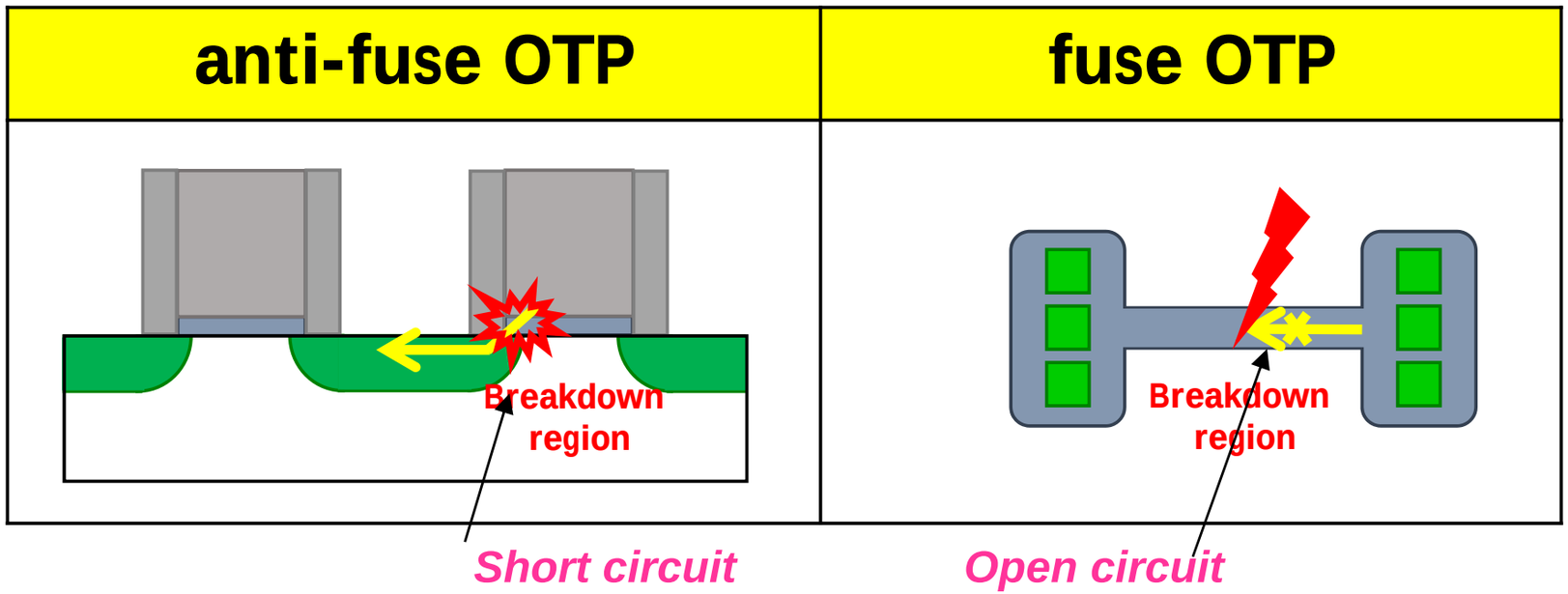
OTP (One-Time-Programmable) Memory-
Electrically programmable nonvolatile memory, write ONCE but multiple-read

- Applications for identity authentication data encryption in state-of-the-art technology
- To be embedded with existing logic CMOS, the process must be compatible with CMOS fabrication.



*E R. Hsieh, S. S. Chung et al., "…. a Newly Found Dielectric Fuse Breakdown," **IEDM, 2015**, pp. 3.4.1- pp. 3.4.4.*

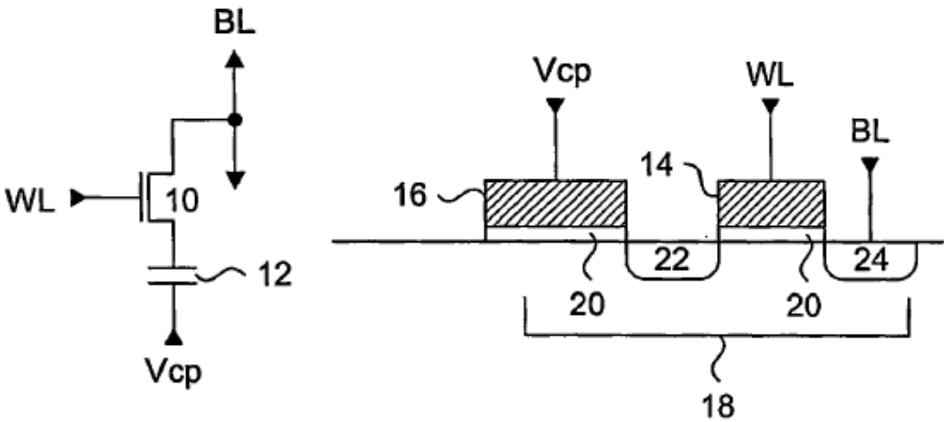
Two types of conventional OTP operation

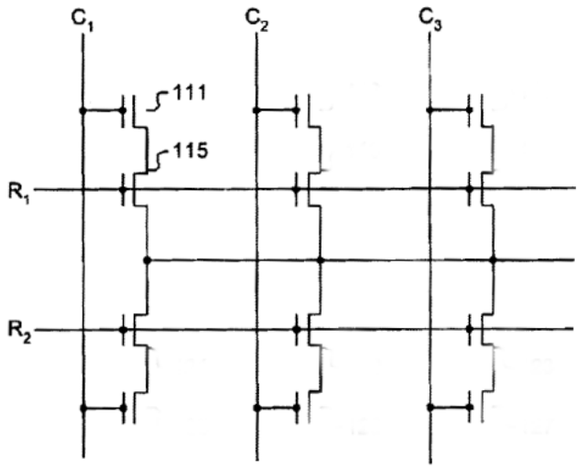


- Anti-fuse breakdown: an electron device that changes state from non-conducting to conducting, i.e., form permanent gate dielectric breakdown
- Fuse breakdown: use a narrow link of metal or poly-silicide wire.

Prior Arts

J. Peng et al., US patent 6,667,902, *2003*





One Transistor + Capacitor

– Use breakdown to short the capacitor.

- Source floating

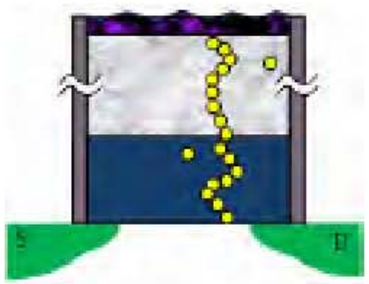
⇒ *Anti-fuse*

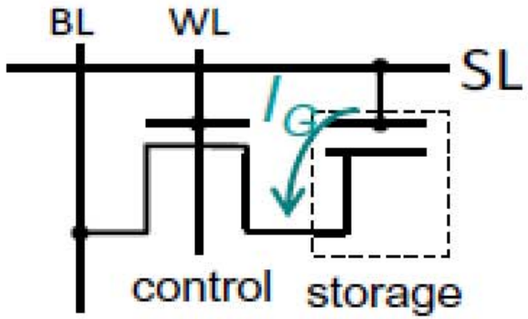
Outline

- Introduction
  - Motivation- General & application
  - Two Conventional OTP Structure
- Unit Cell Design of OTP Memory
  - Operation Mechanism – Dielectric fuse
  - Macro Design and Validation
- Another Application
  - Realization in FinFET Generation
  - PUF
- Summary and Conclusions

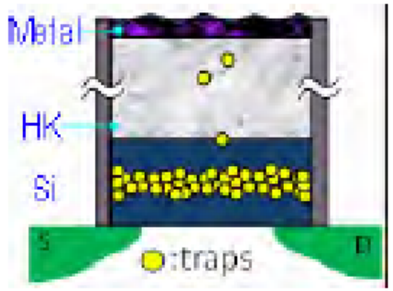
New Gate Dielectric Fuse Breakdown

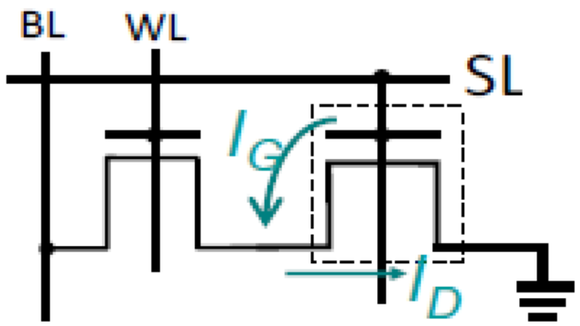
E R. Hsieh, S. S. Chung et al.,
"…. a Newly Found Dielectric Fuse Breakdown,"
IEDM, 2015, pp. 3.4.1- pp. 3.4.4.



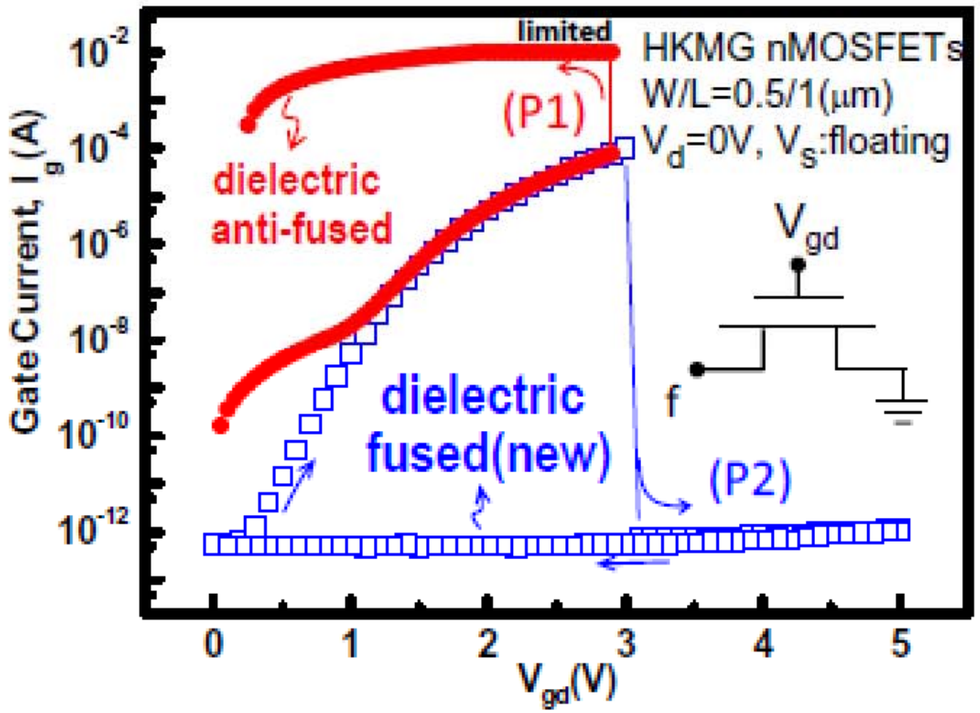


(a) Conventional OTP (anti-fuse)





(b) NEW (dielectric fuse)

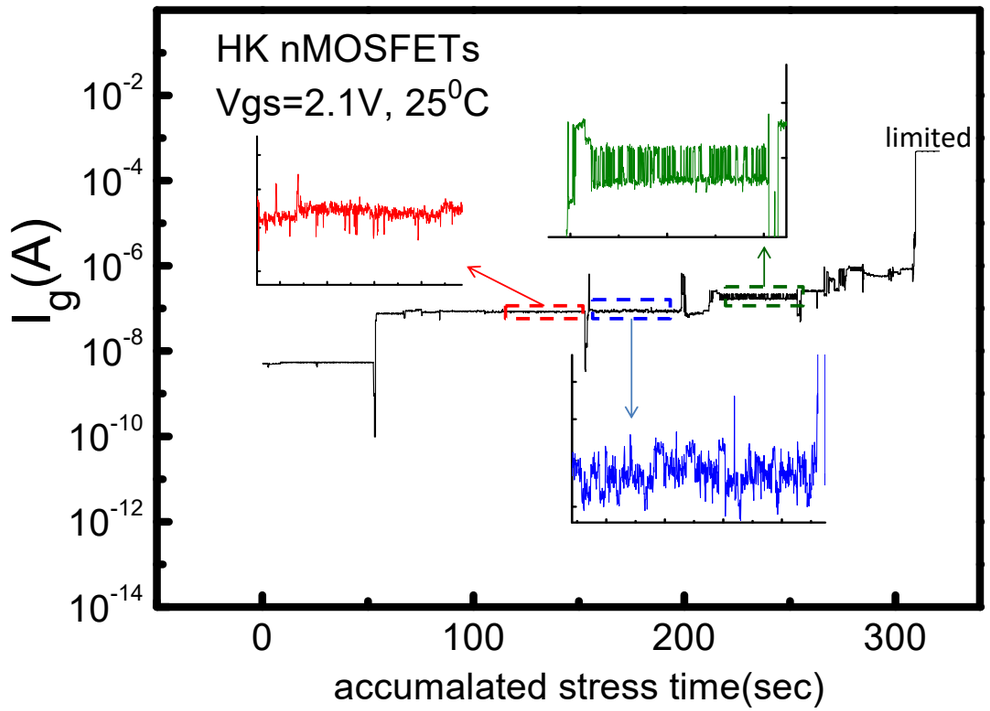


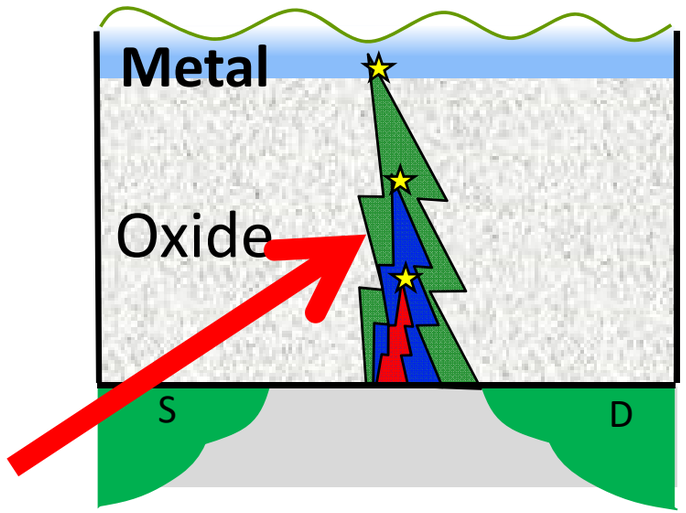
- After anti-fuse, the gate current increases rapidly(P1); after fusing, it is blocked(P2).

The Observation from TDDB

- TDDB (Time Dependent Dielectric Breakdown)

➡ *Ig-transient*

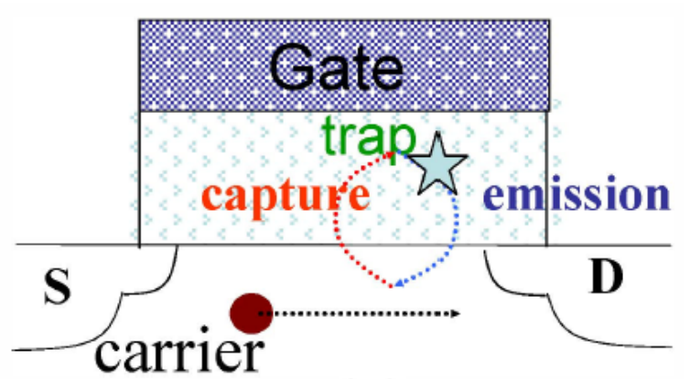


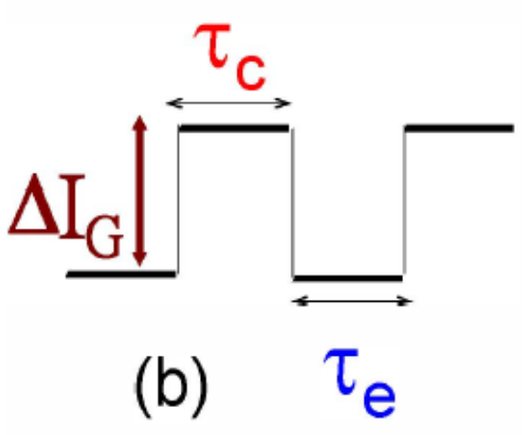


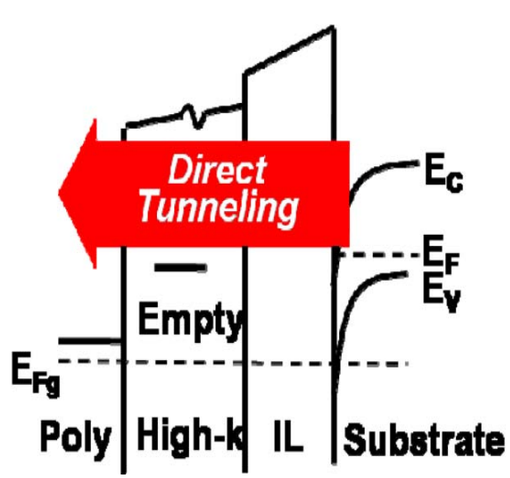
Measuring trap generation as a function of time, we may trace the leakage path.

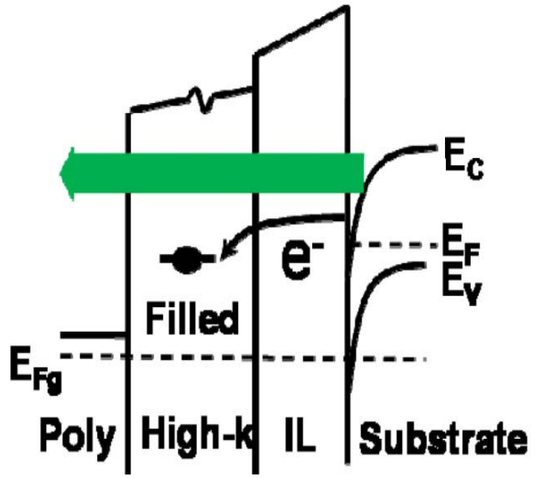
The Principle of Ig-RTN 1.0 (Random Telegraphy Noise)

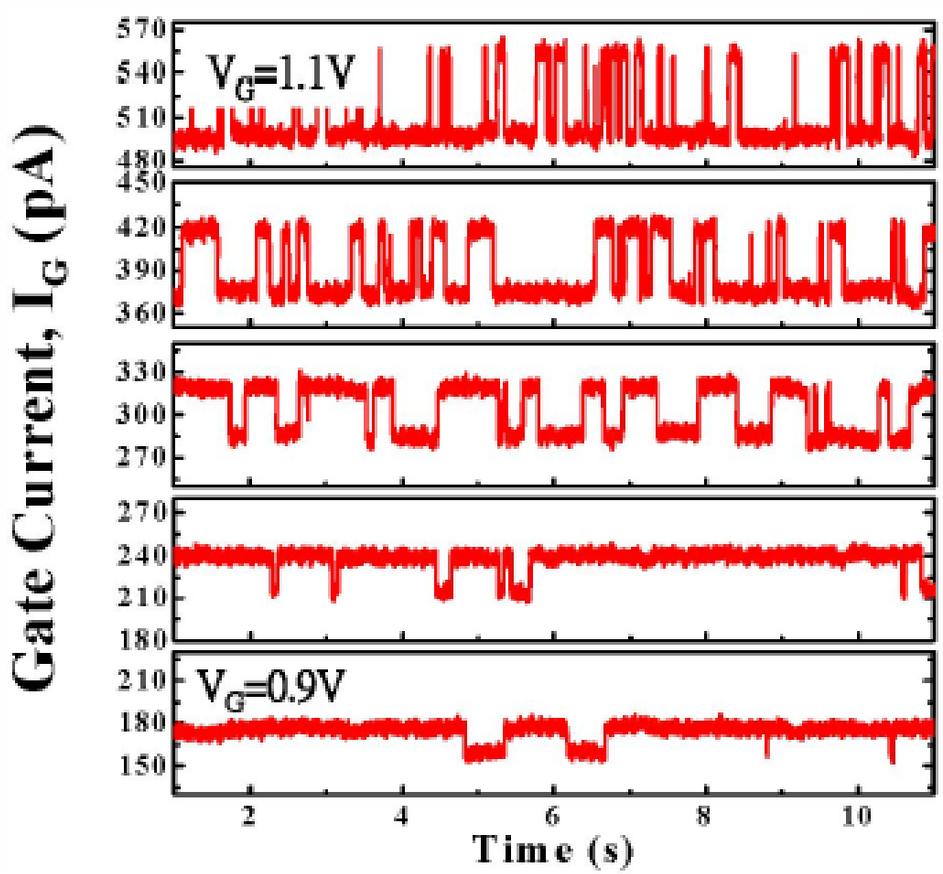
C. M. Chang, S. S. Chung, IEDM 2008.



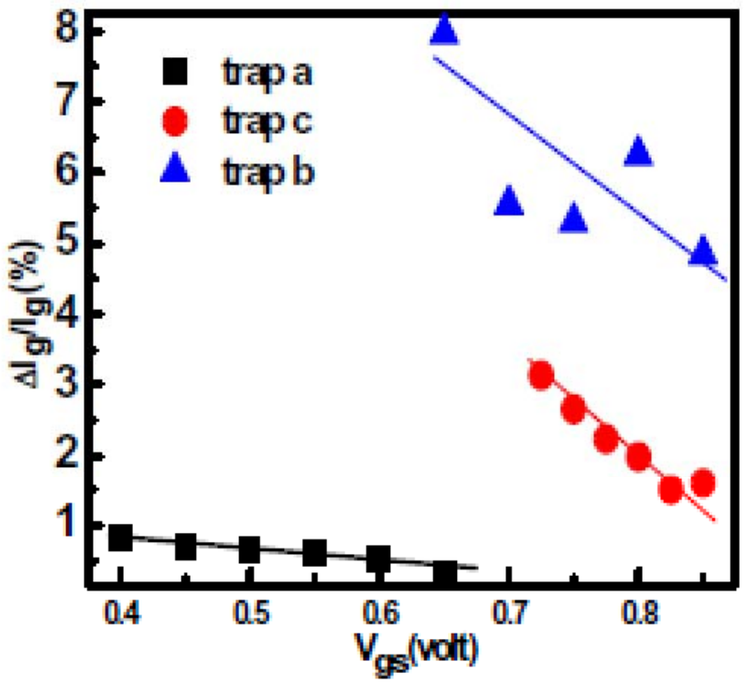


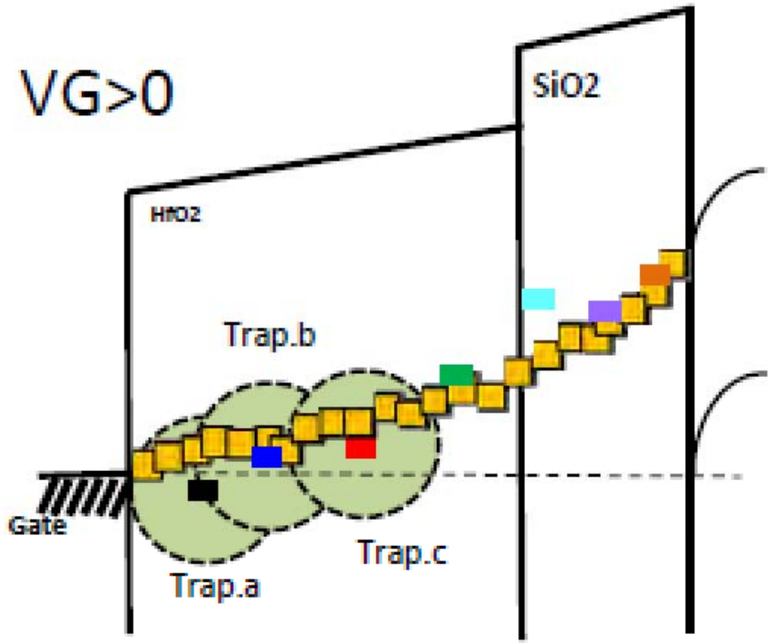






The Leakage Path in n-channel MOSFET





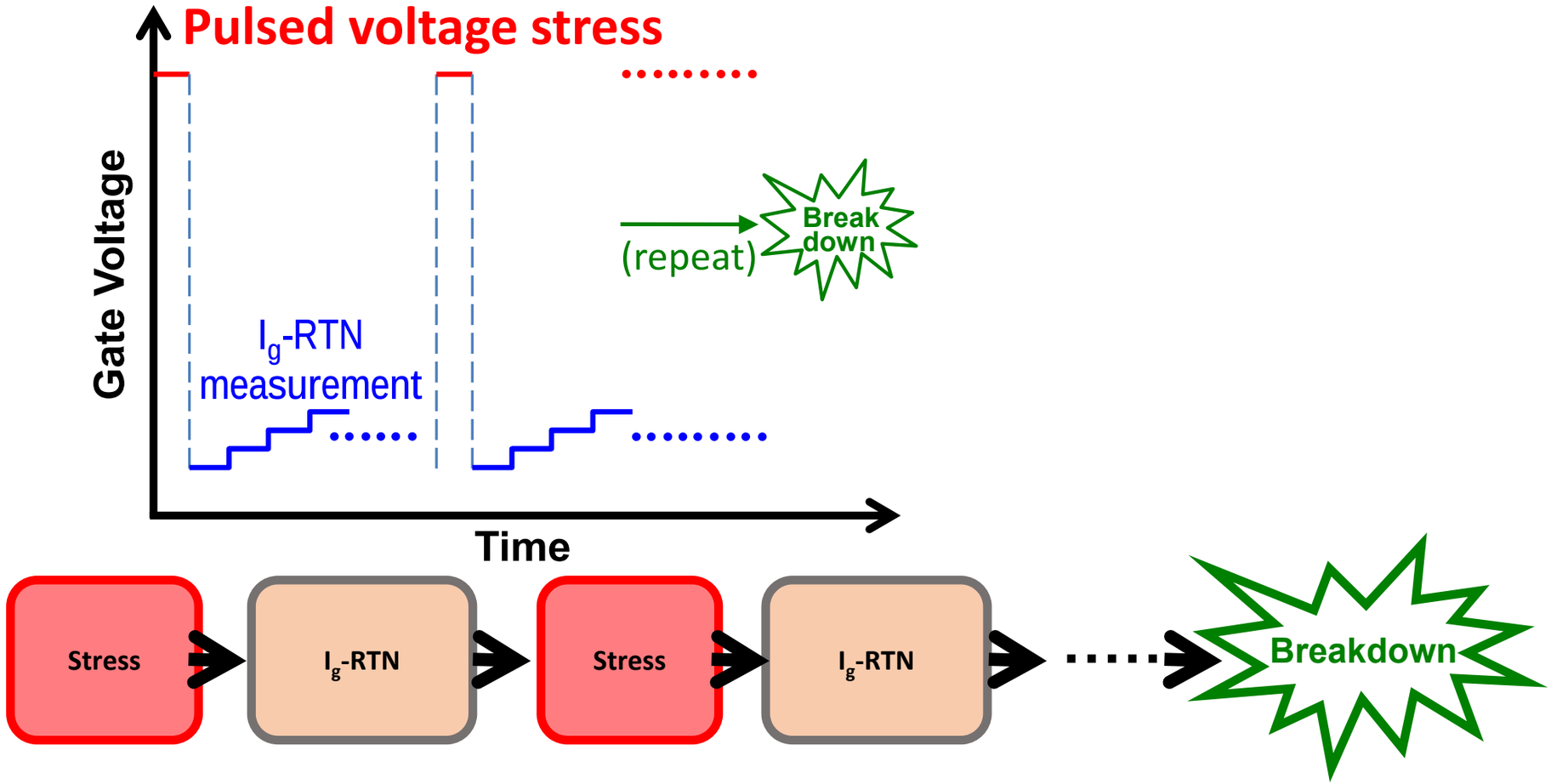
- The conceptual leakage path based on the gate current fluctuation under inversion region.
- The closer the RTN trap is to the leakage filament, the larger the current fluctuation will be.

Ig-RTN Measurement- Version 2.0

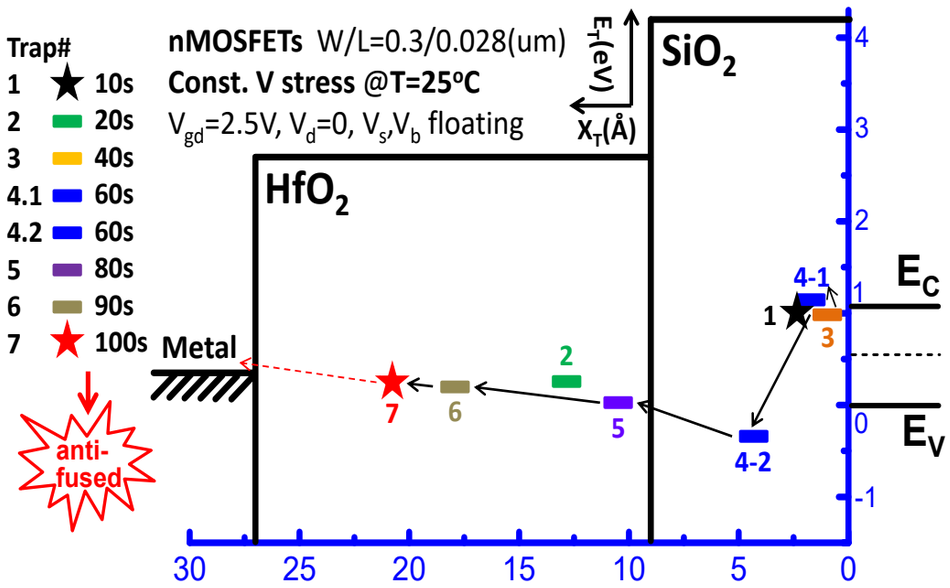
The Observation of Trap Generation as Function of Time

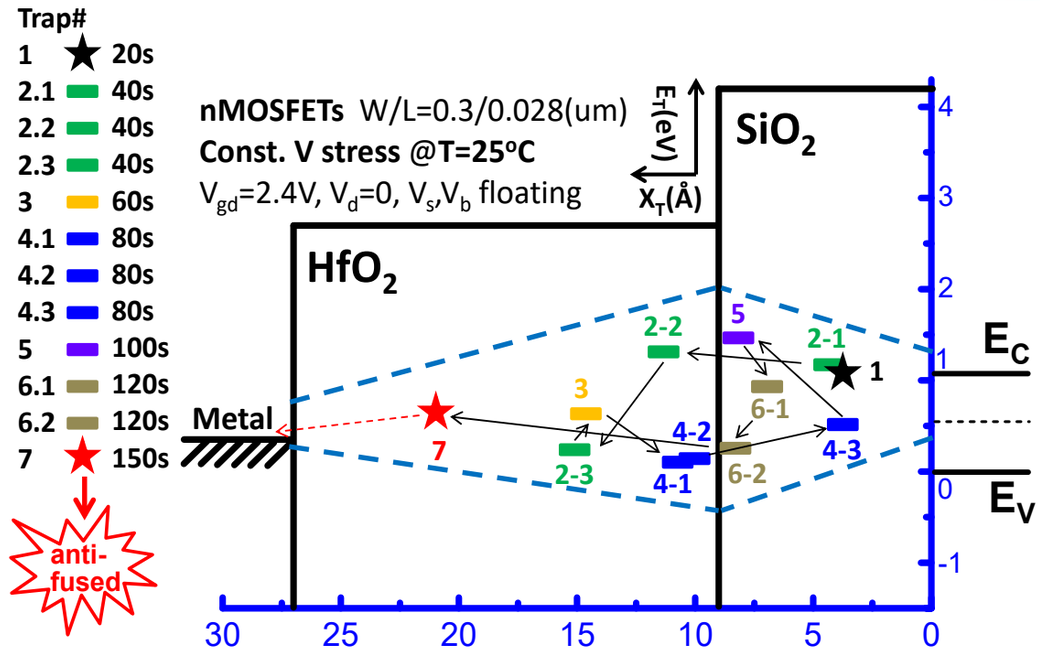
*E R. Hsieh, S. S. Chung et al., **VLSI Tech. Symposium**, 2014, pp. 12.4.1-12.4.2.*

Experimental Procedure

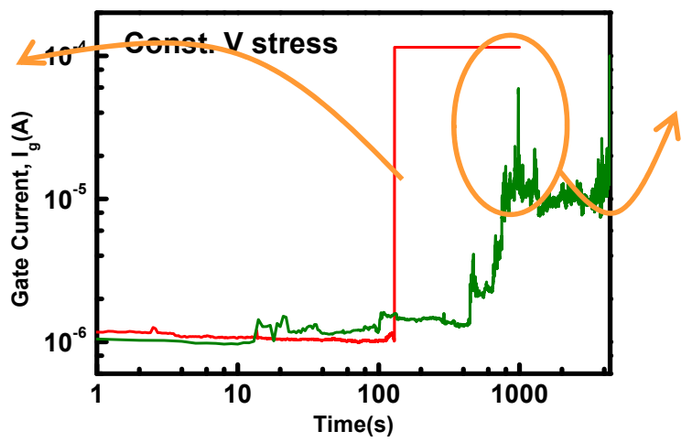


Dielectric Anti-fuse Breakdown



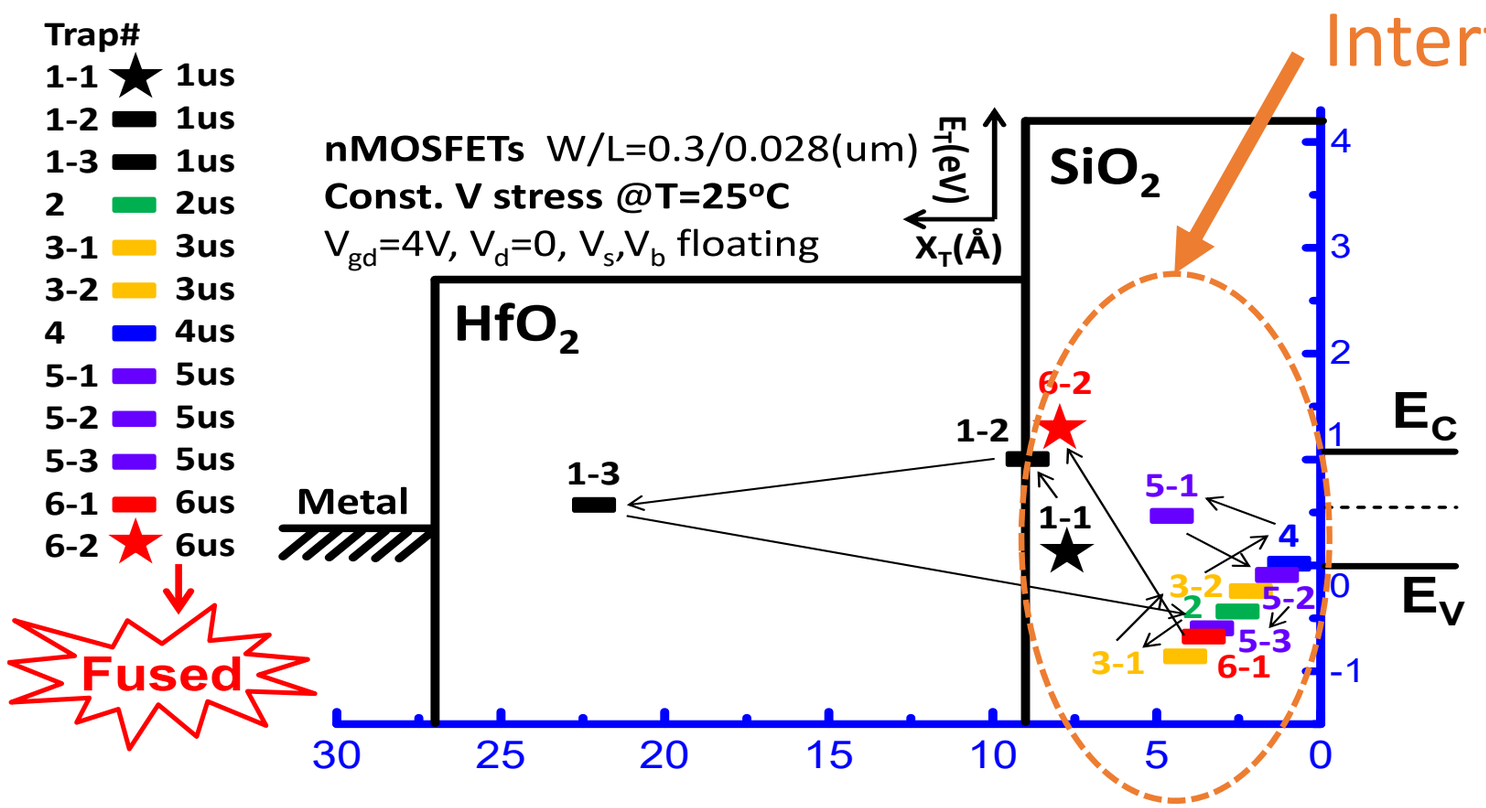


Hard-breakdown: the breakdown path behaves as a snake path.



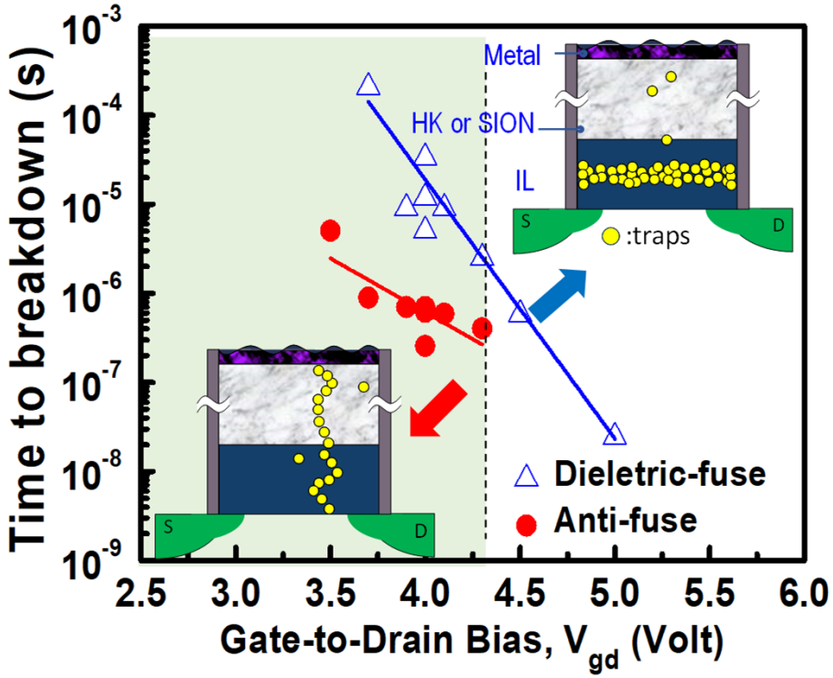
Soft-breakdown: the breakdown path forms as a spindle shape.

Dielectric Fuse Breakdown- dFuse

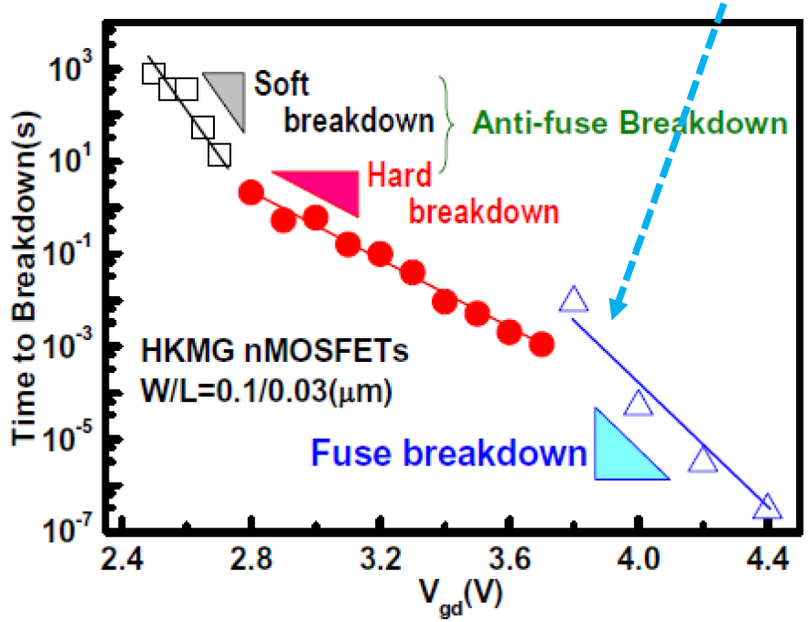


- Fuse-breakdown at room temperature: the traps are highly concentrated near the interface between the IL and channel.
- As the oxygen ions in SiO_2 layer are pulled out, the oxygen vacancies are left as traps and create a gap to block the current path.

Time-dependent Dielectric Breakdown

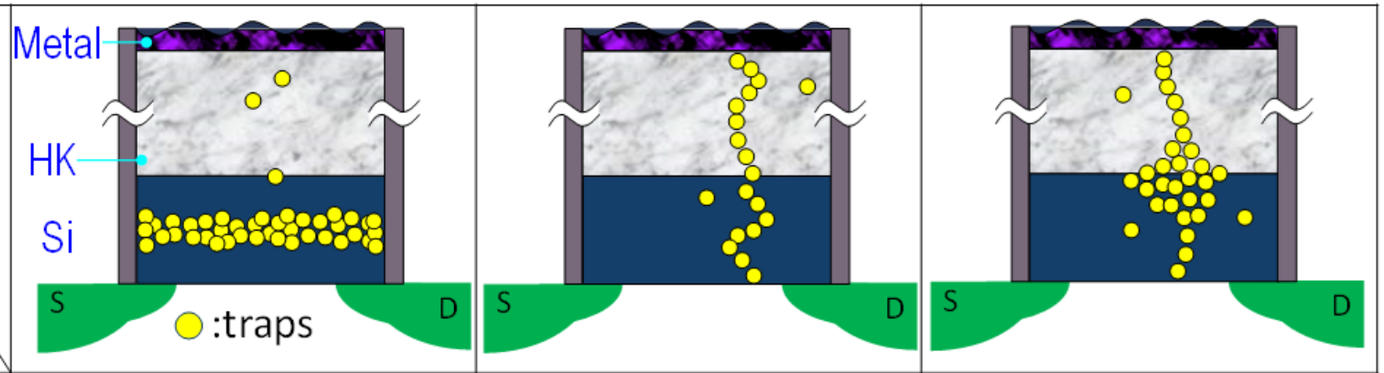


3rd breakdown (dielectric Fuse)



- At V_{gd}= 4.3V, anti-fuse appears first and followed by dFuse, in which anti-fuse generates a hard-breakdown with shorted G-to-D, while dFuse creates a porous SiO_2 interfacial layer.

Different Breakdowns in the Gate Dielectrics

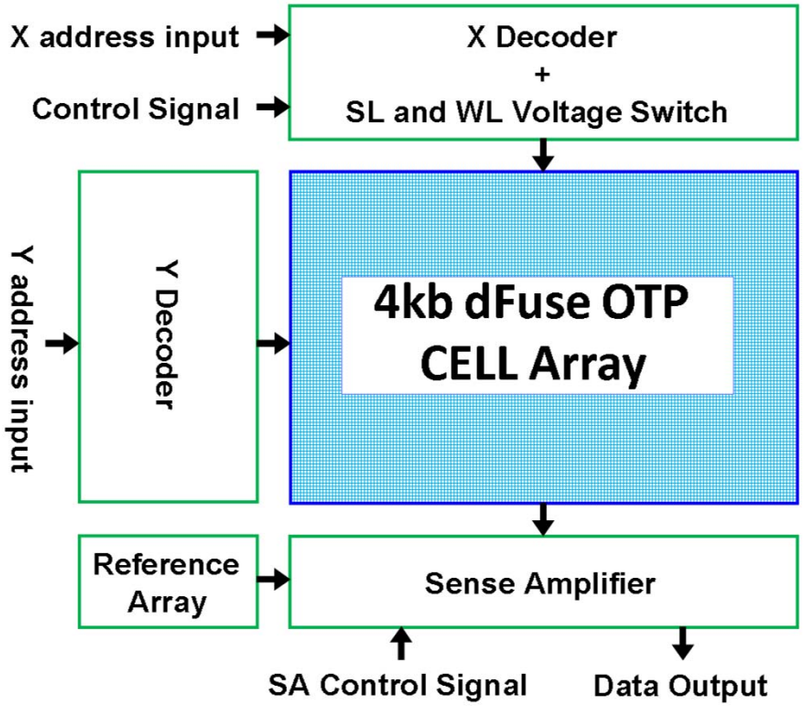
Type / Property			
Dielectric Breakdown Mechanism	**Fuse Breakdown** (porousness of SiO_2)	**Anti-fuse Breakdown**	
		Hard	**Soft**
Field to breakdown	>38MV/cm	>38-27MV/cm	<27MV/cm
Time to breakdown	<1ms	Few 10s~1ms	>few 10s
Breakdown path	**Internal Closed Loop**	**External connecting loop**	

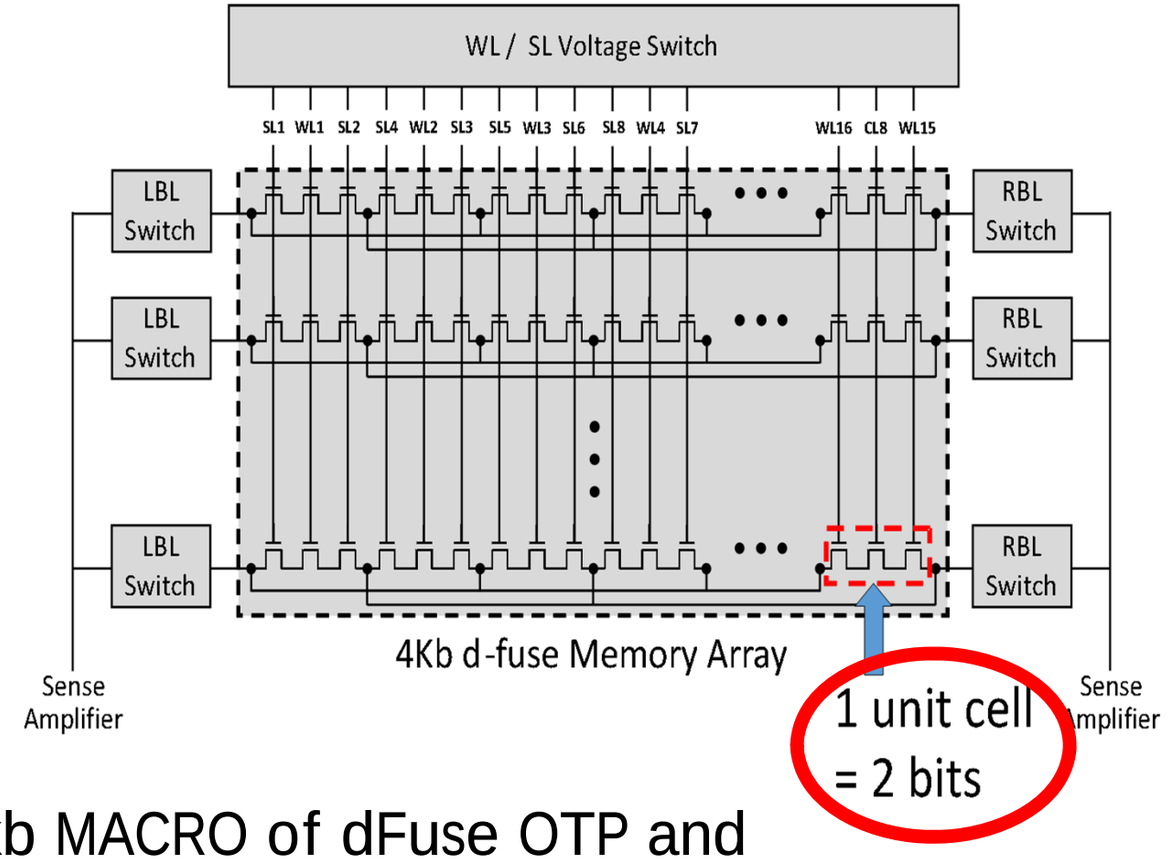
- (column 1) dFuse: the gate dielectrics become porous in the IL, leading to I_G~ 0.
- (columns 2 or 3): Hard breakdown creates a shorted path in the gate.

Outline

- Introduction
  - Motivation- General & application
  - Two Conventional OTP Structure
- Unit Cell Design of OTP Memory
  - Operation Mechanism – Dielectric fuse
  - Macro Design and Validation
- Another Application
  - Realization in FinFET Generation
  - PUF
- Summary and Conclusions

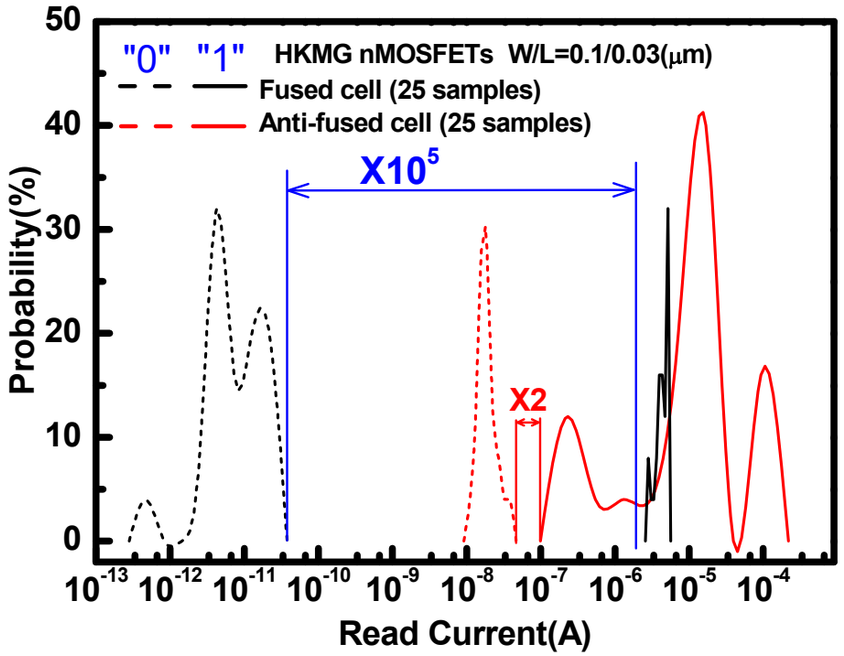
Block Diagram and Architecture of OTP chip

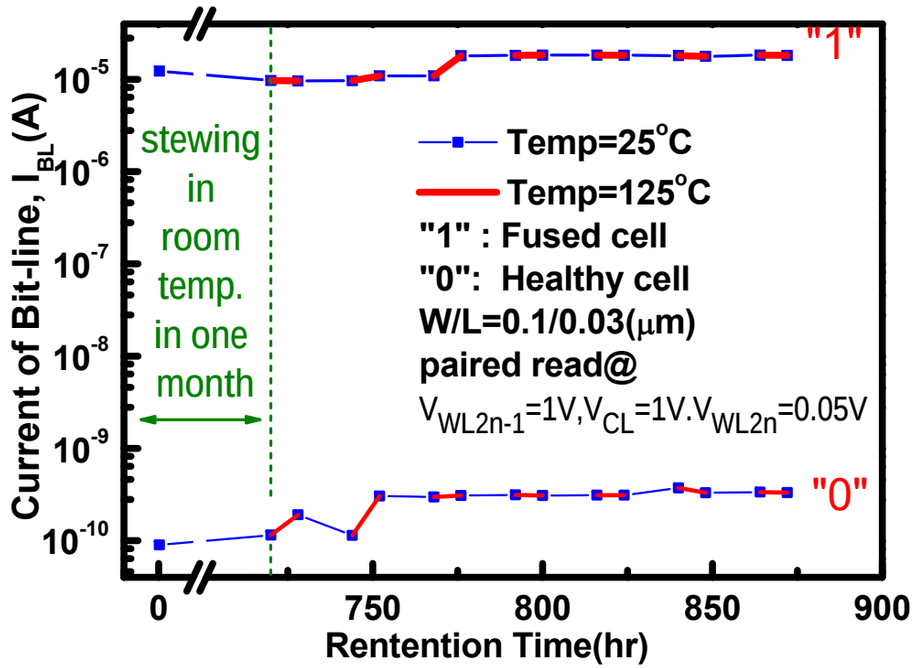




- (Left) The block diagram of 4kb MACRO of dFuse OTP and associated peripheral circuits.
- (Right) Two storage transistors share a single control transistor (at the center), i.e., one bit equals to 1.5T.

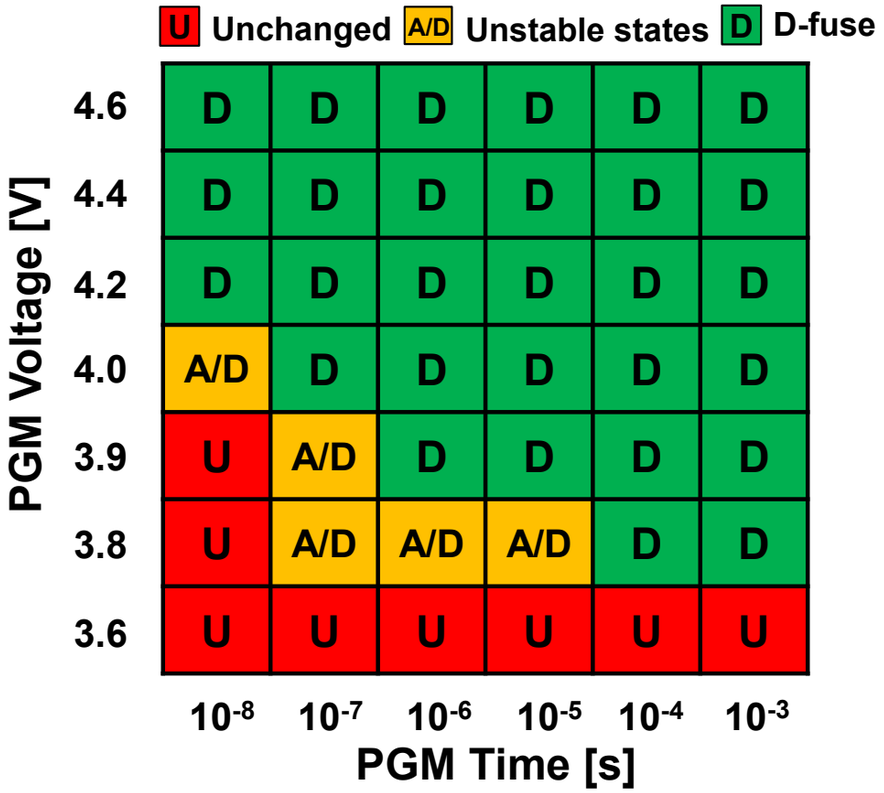
Reliability of dFuse OTP

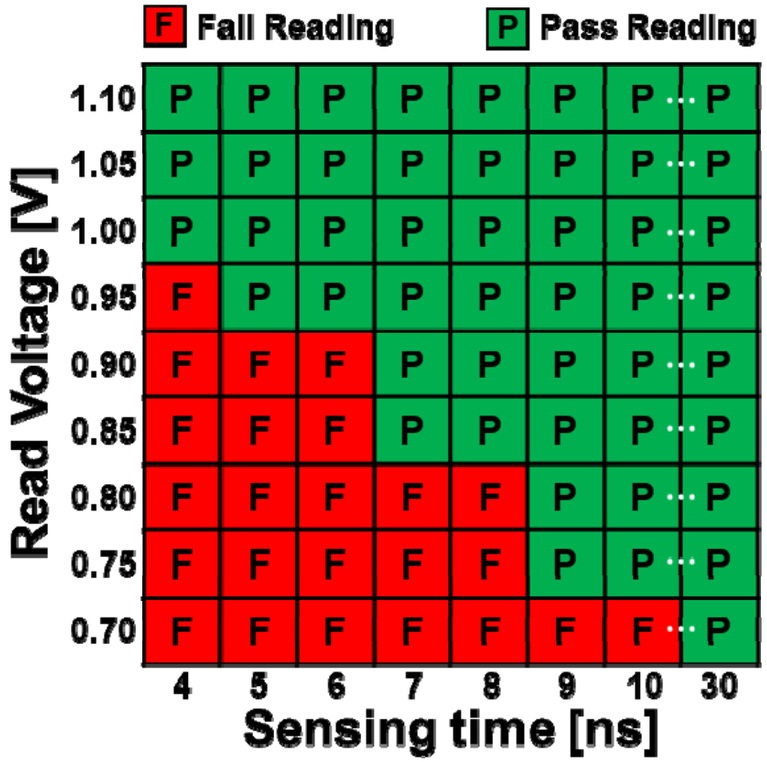




- The window of the dielectric-fuse cell is much larger than that of the anti-fuse one, up to 10^5 times.
- The data-retention during one month still remains distinct and clear 1 and 0 states.

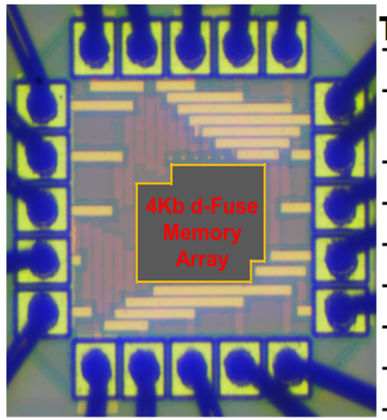
Shmoo Plots of Program and Read





- The dFuse OTP can achieve successful programming of 4V in 100ns.
- The reading operation can be completed within 4ns under 1V or down to 0.7V for 30ns.

Chip Photo and Key Parameters



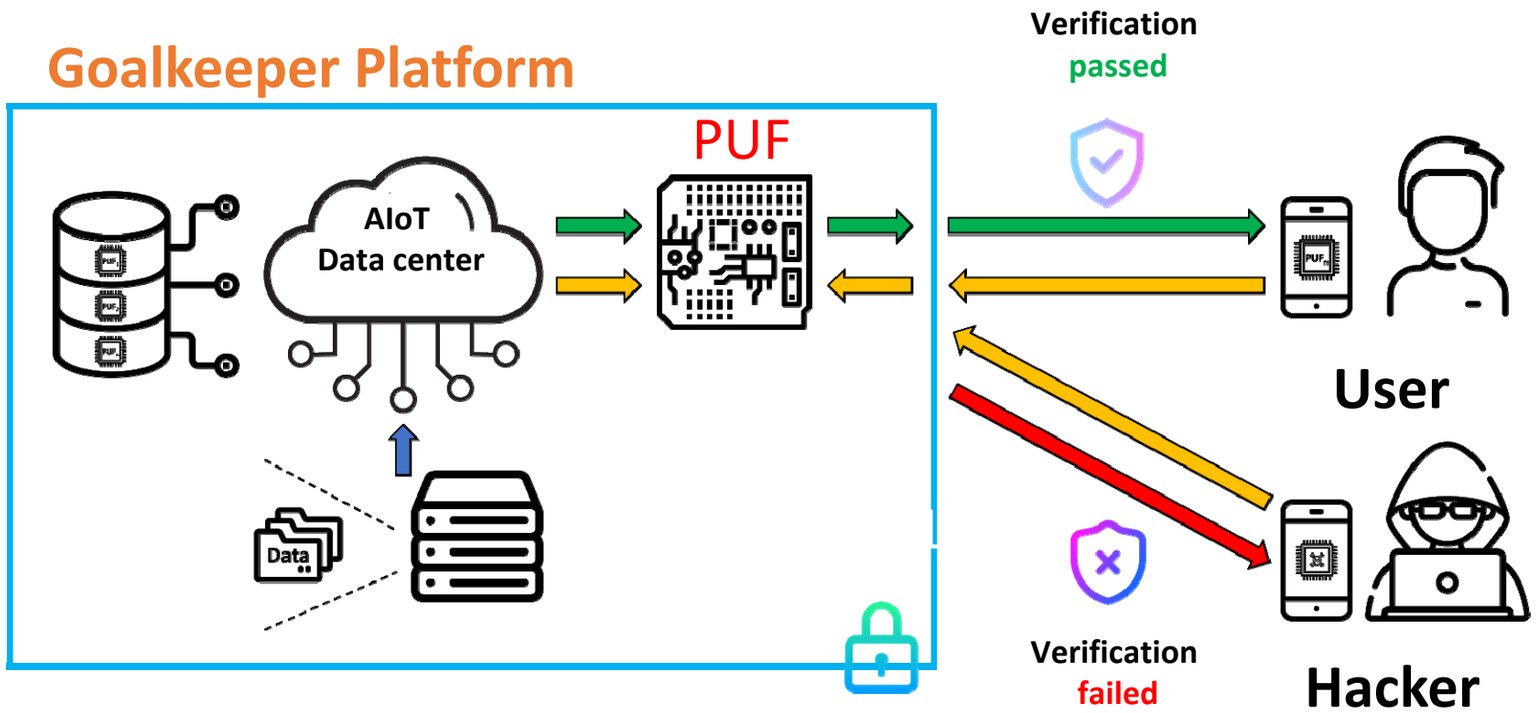
TECHNOLOGY KEY PARAMETERS	
Process	28nm HKMG
Mechanics	Dielectric Fuse Breakdown(dFuse)
Min. Bit Size	1.5T, 0.0585um^2
Program Voltage	3.8~4V
Program Pulse	10~100ns
Sense Voltage	0.7~1.1V
Sense Time	<10ns
Retention Time	>1month@150℃

	VLSI2016[7] Z. Chen et al.	ISSCC2017[8] S. Chou et al.	TED2015[9] W. Y. Hsiao et al.	This Work
Process	14nm Tri-gate	10nm FinFET	28nm HKMG	**28nm HKMG**
Mechanism	Electro-migration	Anti-fuse	Anti-fuse	**dFuse**
Bit Cell	1T1R 0.9um^2	2T 0.028um^2	2T 0.0441um^2	**1.5T 0.0585um^2**
PGM Voltage	2.1~2.4V	5.4V	4V	**3.8 ~ 4V**
PGM Time	20us	7us	20us	**10 ~100ns**
Read Voltage	0.75~1.2V	N/A	1.5V	**0.7 ~ 1.1V**
Read Time	N/A	N/A	N/A	**<10ns**
Retention	N/A	150℃ 0.25 month	150℃ >1month	**150℃ > 1momth**
Reliability Assessment	N/A	yes	N/A	**yes**

Outline

- Introduction
  - Motivation- General & application
  - Two Conventional OTP Structure
- Unit Cell Design of OTP Memory
  - Operation Mechanism – Dielectric fuse
  - Macro Design and Validation
- Another Application
  - Realization in FinFET Generation
  - PUF
- Summary and Conclusions

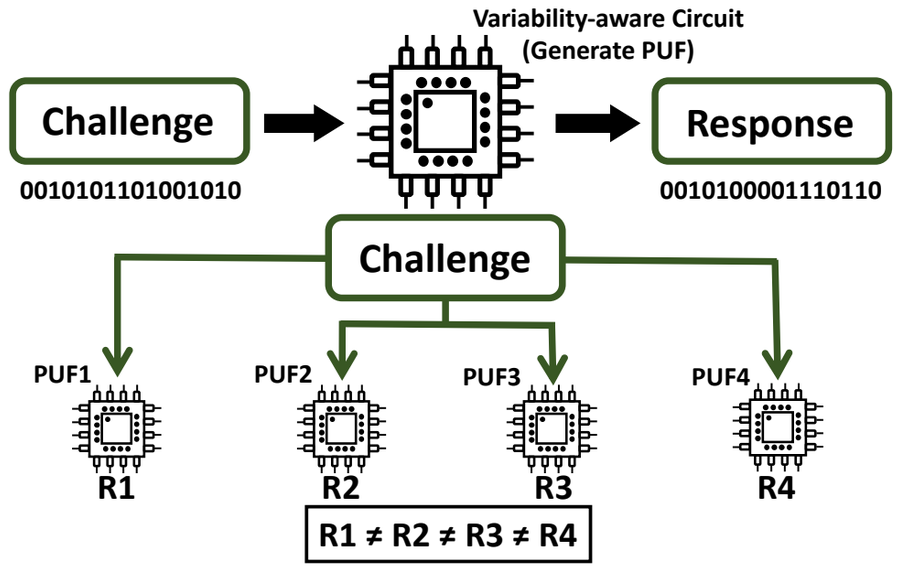
Application The Concept of Hardware Security



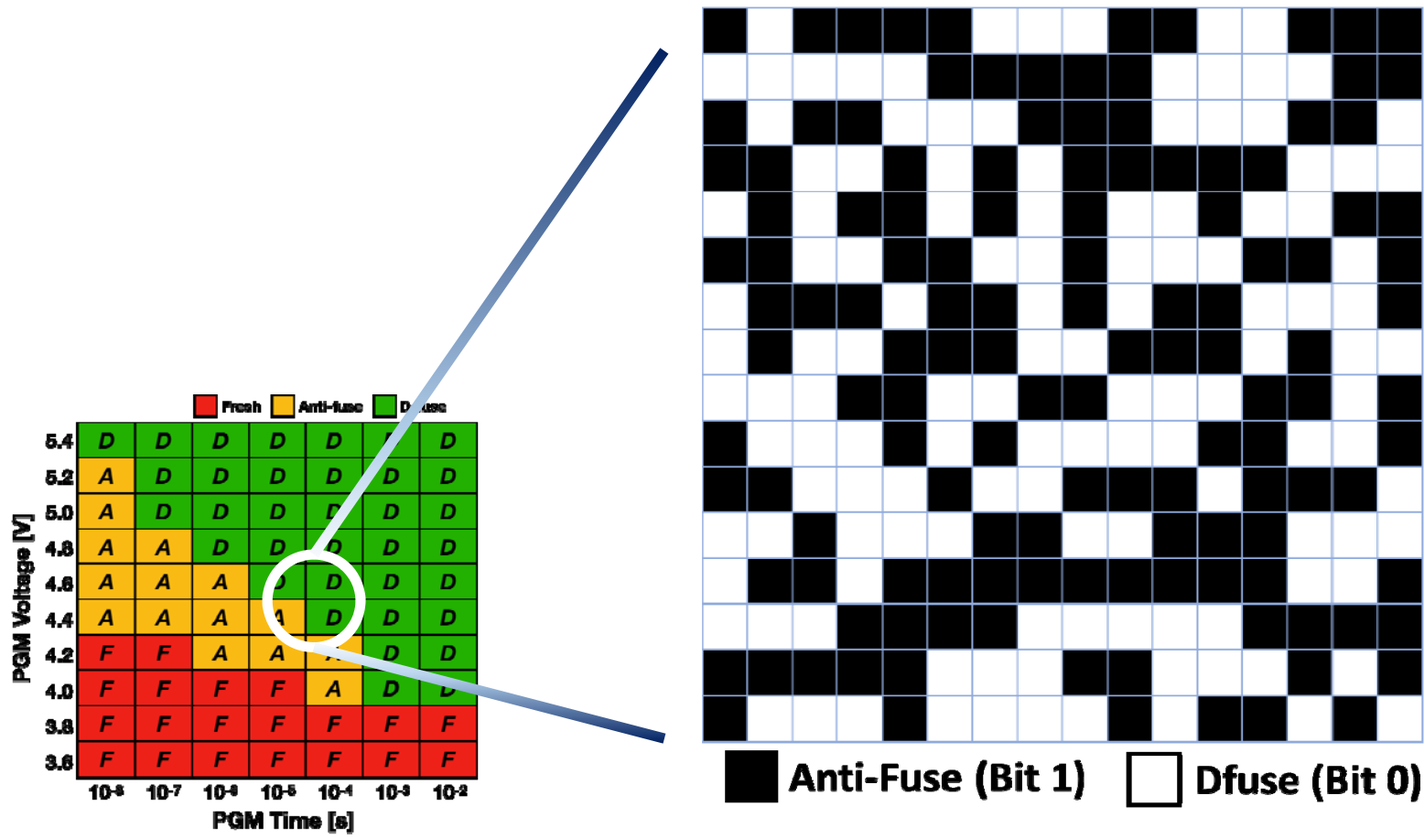
- The architecture of Goalkeeper composed of the cloud server and the edge device demonstrates identity authentication in IoT communication.
- PUF: embedded into the Goalkeeper platform so that the cloud server can recognize the difference between users and hackers to avoid data breaches.

Physical Unclonable Function

- **PUF (Physical Unclonable Function) Definition**
  - **Unique physical characteristics from process/device variations**
- **Challenge Response Pair (CRP) in a device or circuit, generating encryption**
- **PUF Requirements**
  - **Randomness, Uniqueness: No relation between elements**
  - **Unclonability, Unpredictability: Extremely hard to obtain and reproduce**
  - **Robustness, Reliability: Reliable over the whole product lifecycle**



The Generation of PUF Strings

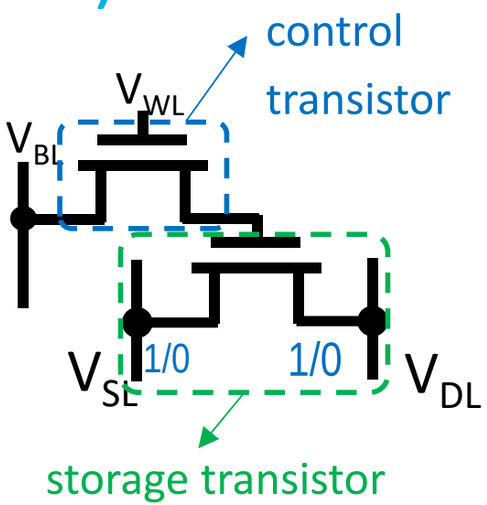


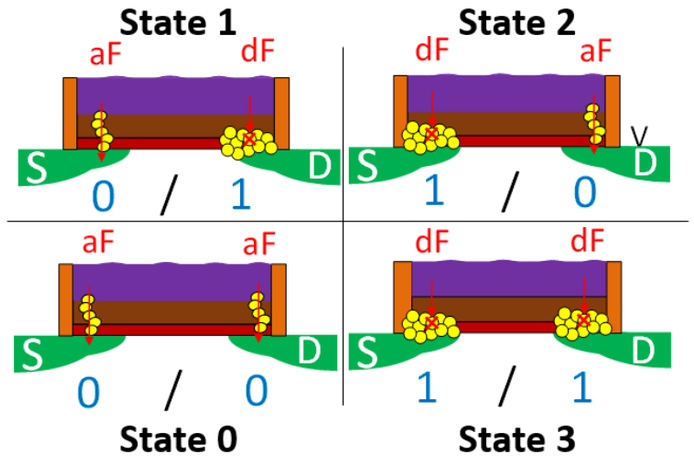
- When the PGM voltage is 4.5V and the pulse width is $5.6x10^{-6}$, the anti-fuse state accounts for 51% of the overall mosaic map.

2-bit-per-cell OTP-based PUF array (14nm FinFET)

E. R. Hsieh, H. W. Wang,, S. S. Chung et al., "Embedded PUF on 14nm FinFET……," VLSI, 2019, T118-T119

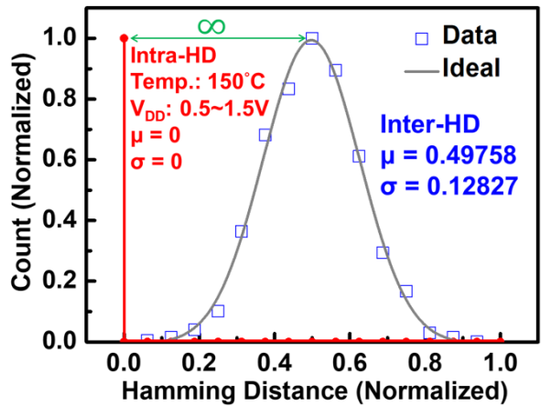
OTP based PUF



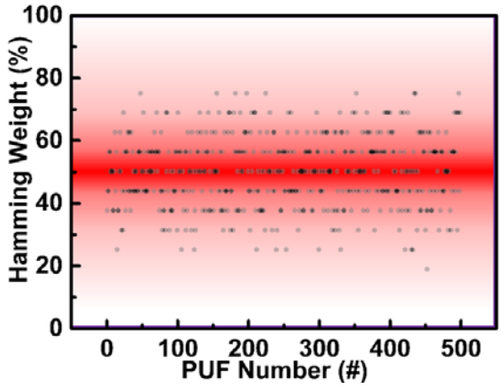


(aF: anti-fuse; dF: dFuse)

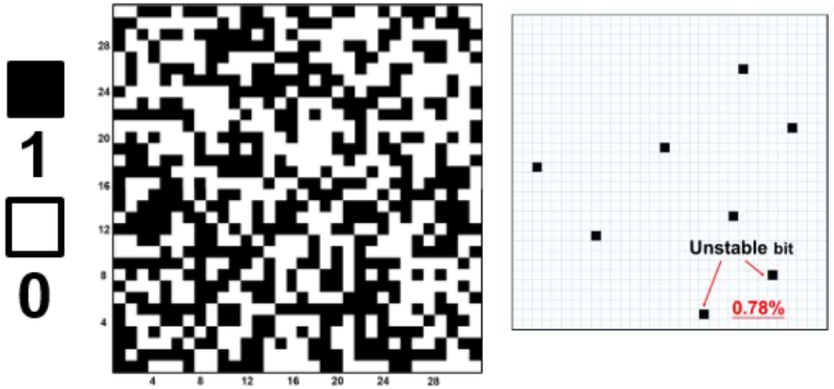
Randomness: Hamming distance



Randomness: Hamming weight



PUF array- Mosaic map



After reading 10,000 times, only two unstable bits were observed.

Outline

- Introduction
  - Motivation- General & application
  - Two Conventional OTP Structure
- Unit Cell Design of OTP Memory
  - Operation Mechanism – Dielectric fuse
  - Macro Design and Validation
- Another Application
  - Realization in FinFET Generation
  - PUF
- Summary and Conclusions

Summary and Conclusions

- OTP equipped with a unique dFuse scheme has been successfully developed, well suited for advanced HKMG/FinFET CMOS generations.
  - 28nm and 14nm were demonstrated
  - FinFET Extendable to 3nm ⇒ OTP is still available
- Ig-transient RTN measurement technique has been introduced to understand the breakdown mechanism
  - A third-type breakdown: Dielectric Fuse (dFuse)breakdown
  - Anti-fuse breakdown: hard-breakdown
- In hardware security, one more application
  - A very advanced PUF is developed in 14nm FinFET platform.

More applications in mobile phones (e.g., power management, cryptography, key generation, and encryption), MCU, safety of AI devices, storages etc.