



# CXL<sup>®</sup> Attached Flash Memory Economics

**Mahinder Saluja**  
Director of Strategy, SSD BU  
KIOXIA America, Inc.

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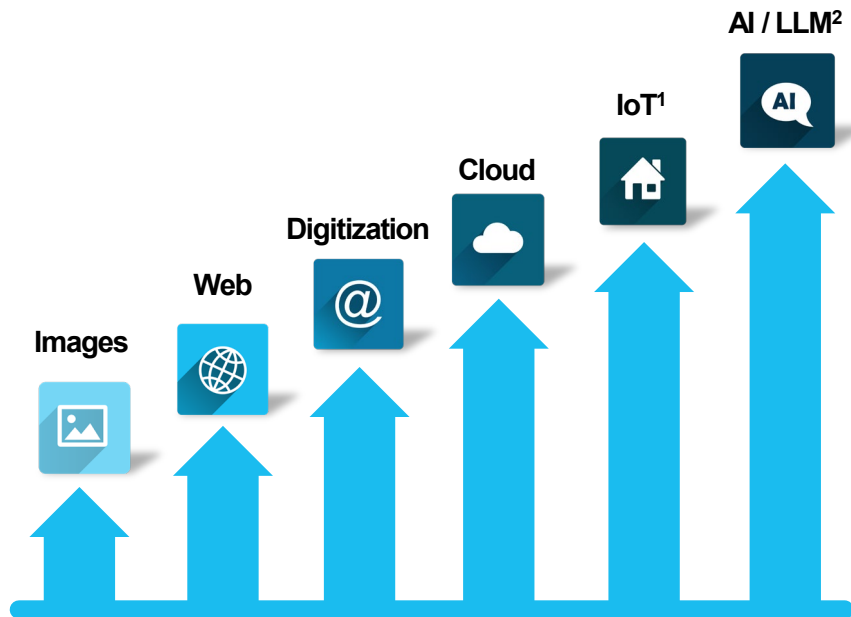
# Agenda



- **Why Memory Expansion?**
- **CXL<sup>®</sup> Attached Flash Memory**
- **Performance and Cost**
- **Challenges and Opportunities**

# Why Memory Expansion?

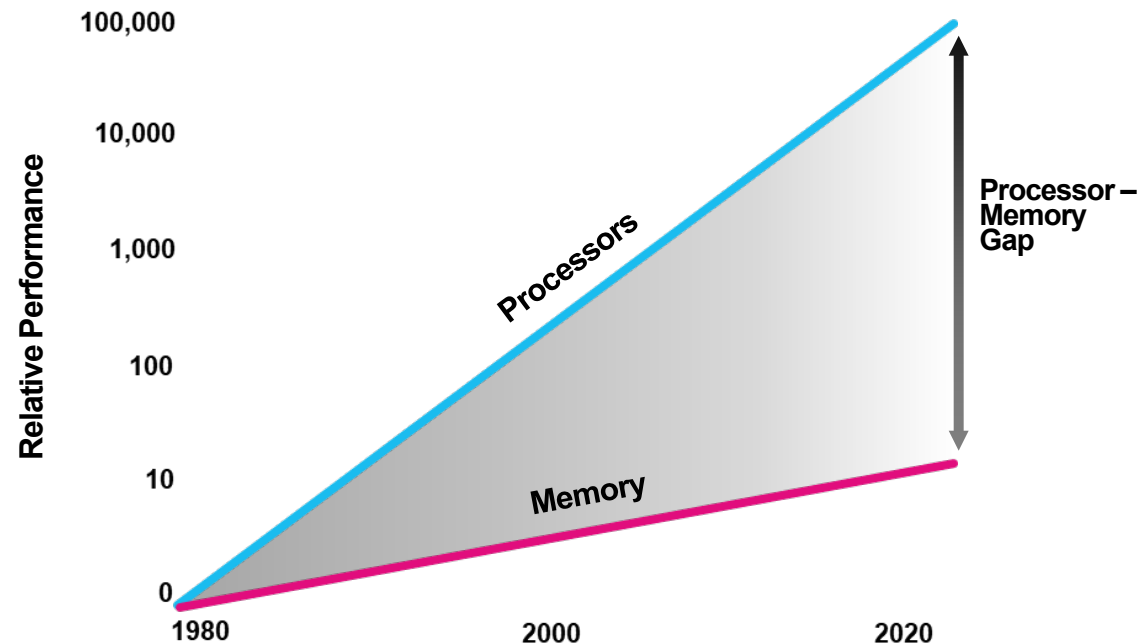
Today's data center workloads require increased memory capacity and bandwidth.



<sup>1</sup> that Internet of Things (IoT) <sup>2</sup> Artificial Intelligence (AI) / Large Language Models (LLM)

Central processing unit (CPU) / graphics processing unit (GPU) core idles due to gap in density growth compared to memory capacity and bandwidth

- Memory ~40%-50%\* of total server cost



# Memory Expansion with Flash

- **CXL® Benefits**

- Cost effective memory capacity and bandwidth expansion
- Enables memory pooling and sharing with DRAM
- Abstracts memory media interface

- **CXL® Technology Creates the Perfect Opportunity to...**

- Explore alternative to costly DRAM
- Flash media to jump over the semantic wall

But can flash media jump over the semantic wall and reduce cost?

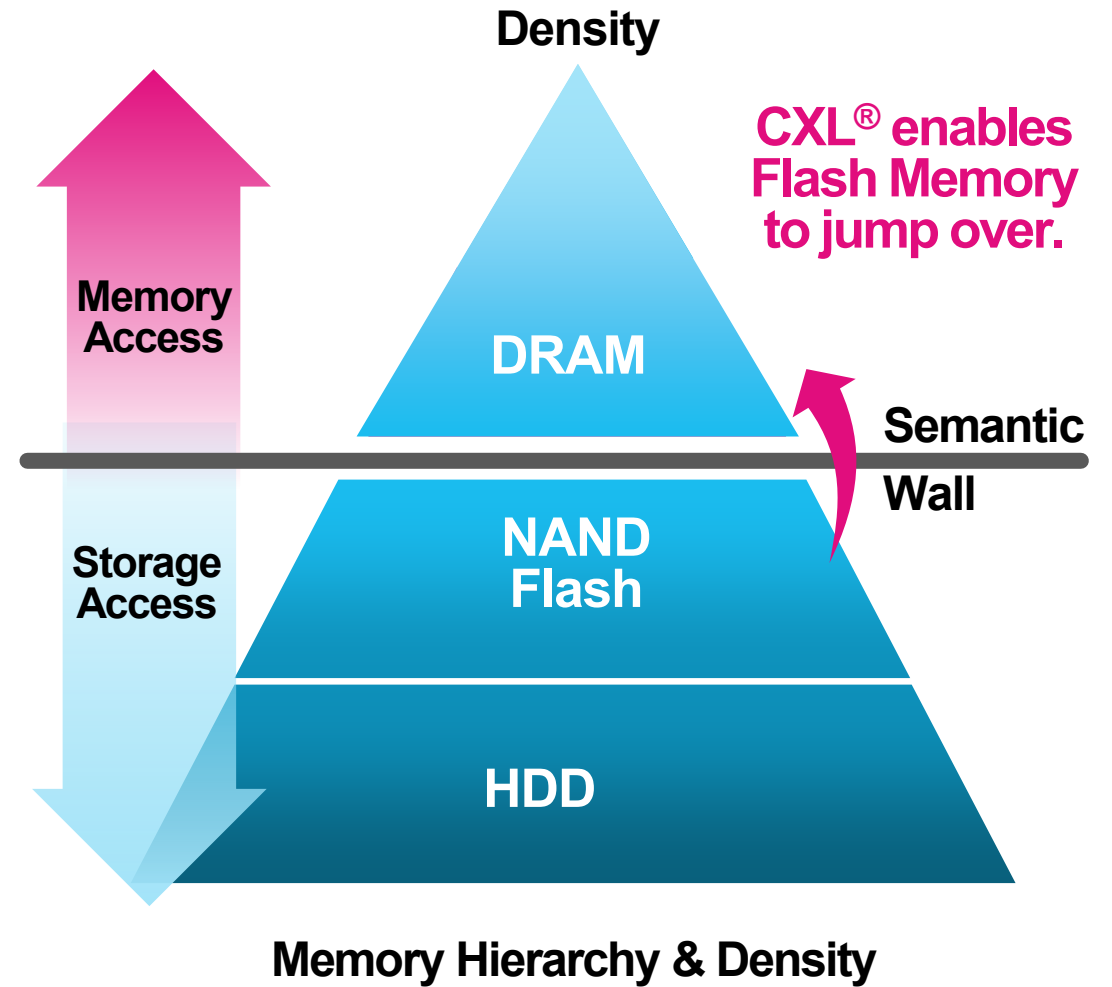


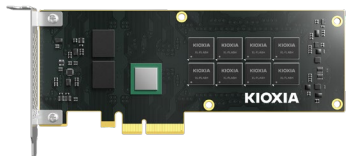
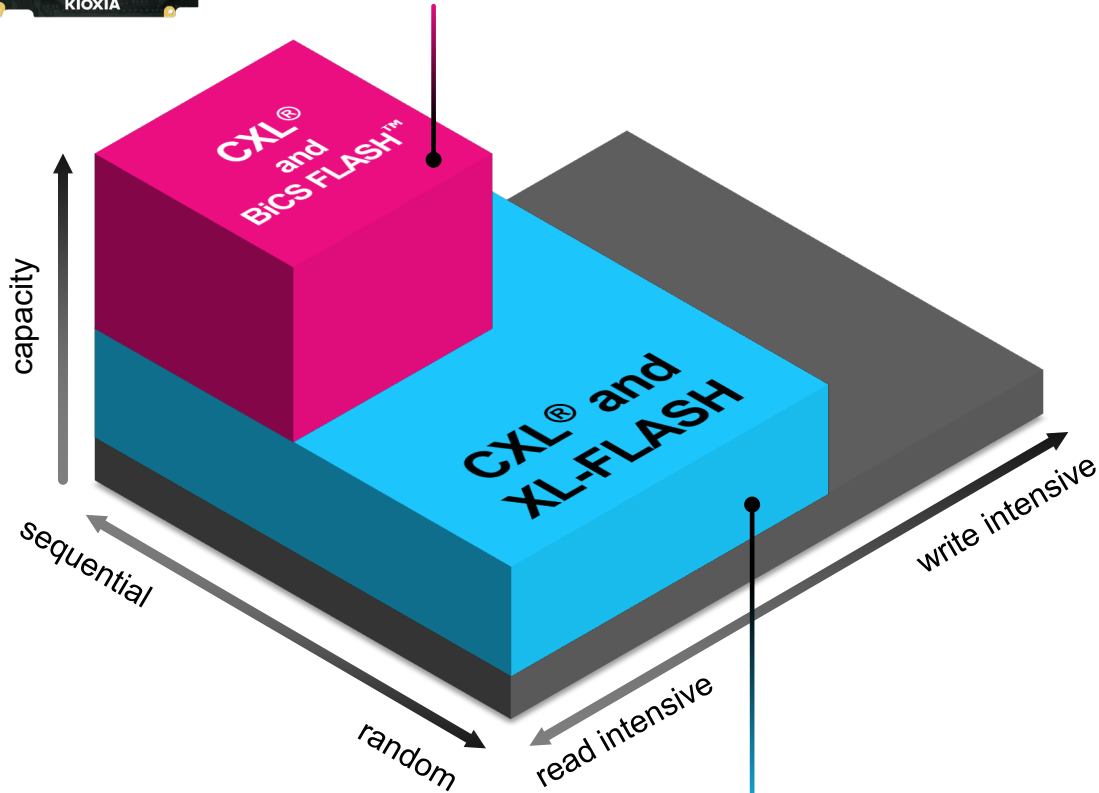
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# KIOXIA CXL<sup>®</sup> Flash Memory Exploration



## Combination of CXL<sup>®</sup> and BiCS FLASH<sup>™</sup> technologies

Read intensive high capacity and high bandwidth memory



## Combination of CXL<sup>®</sup> and XL-FLASH technologies

Random read/write access memory expansion

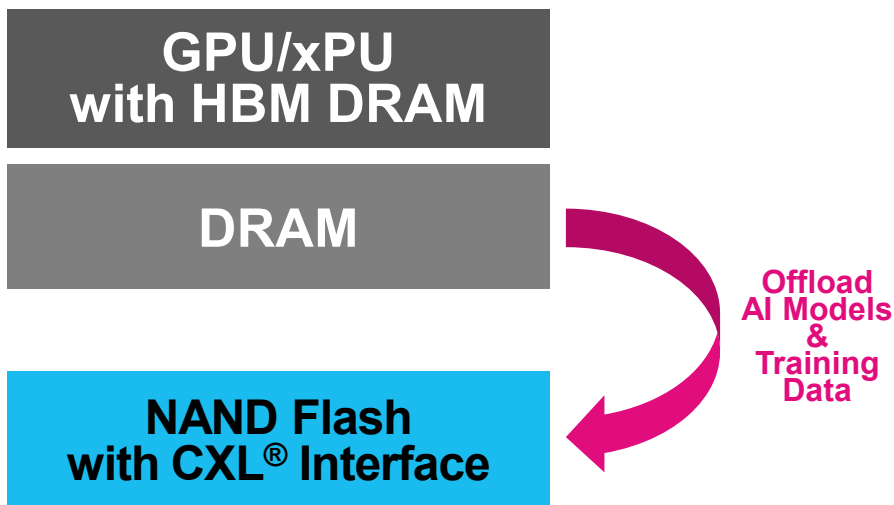
	CXL <sup>®</sup> and XL-FLASH Technologies	CXL <sup>®</sup> and BiCS FLASH <sup>™</sup> Technologies
<b>Media</b>	BiCS FLASH <sup>™</sup> (XL-FLASH)	BiCS FLASH <sup>™</sup>
<b>Value Pillar</b>	Low latency (<5us (single-level cell), <10us (multi-level cell); DRAM cache tier)	High bandwidth and High capacity
<b>CXL Access</b>	CXL.mem, CXL.io	CXL.mem, CXL.io
<b>Capacity</b>	>256 gigabytes (GB)	> 1 terabytes (TB)
<b>Suitable Applications</b>	Artificial intelligence (AI) / machine learning (ML) inference, In-memory data bases (DB), graph processing, cache, tiering	AI/ML training & inference, big data analytics

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# CXL<sup>®</sup> and BiCS FLASH<sup>™</sup> Application

## Generative Artificial Intelligence (AI) Inference & Training

Large Language Models (LLMs) require large memory to refill HBM DRAM on GPU



Memory Requirements by AI Model Size

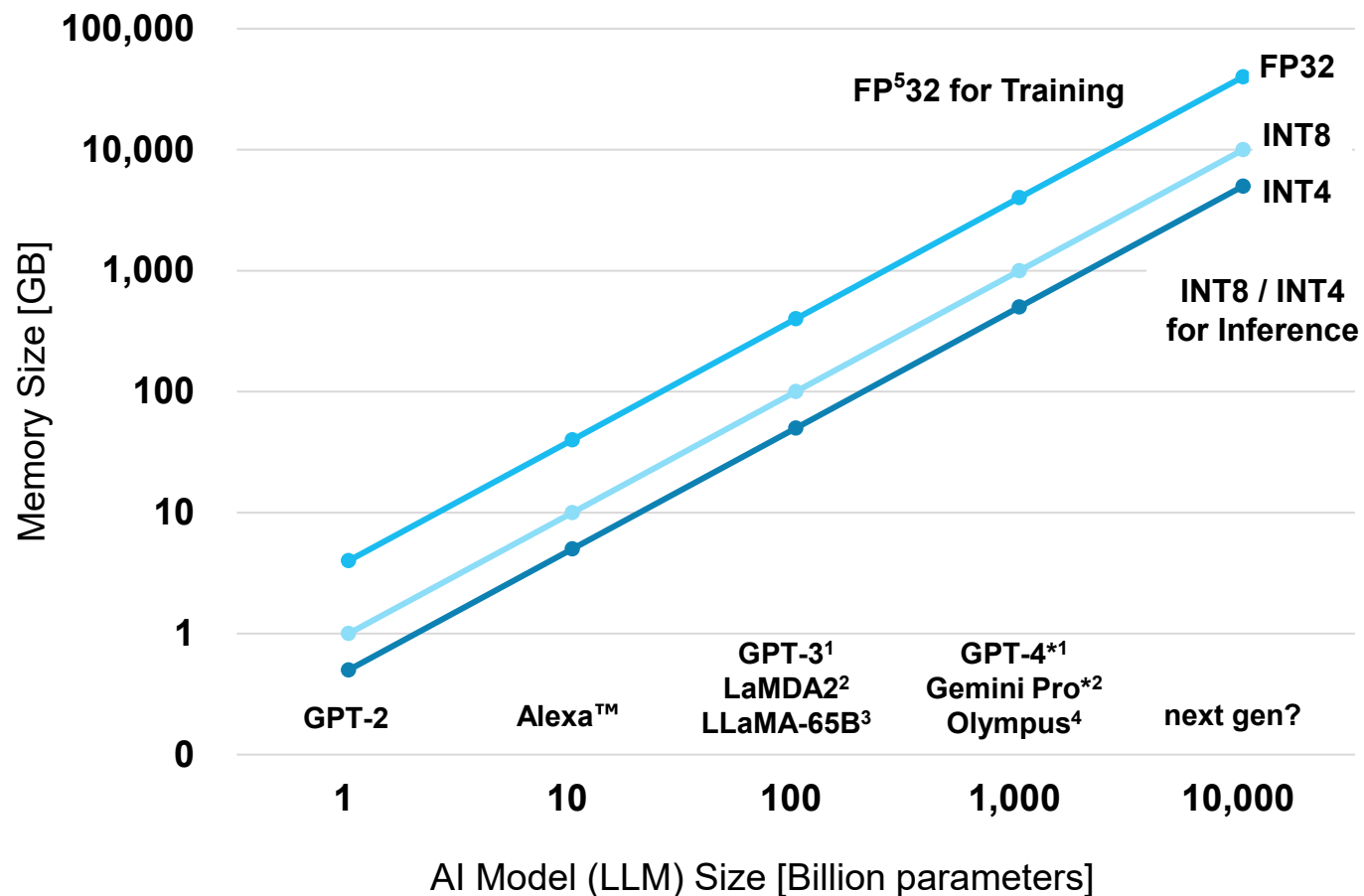
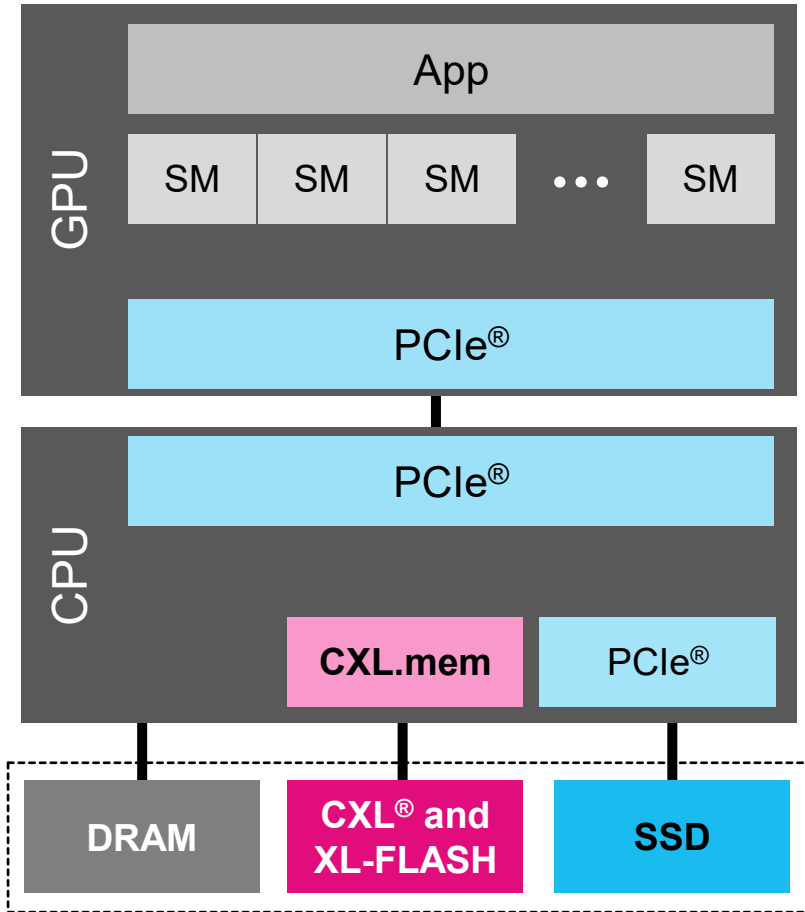


Image and graph source: created by KIOXIA

\* Some model sizes are estimated by KIOXIA

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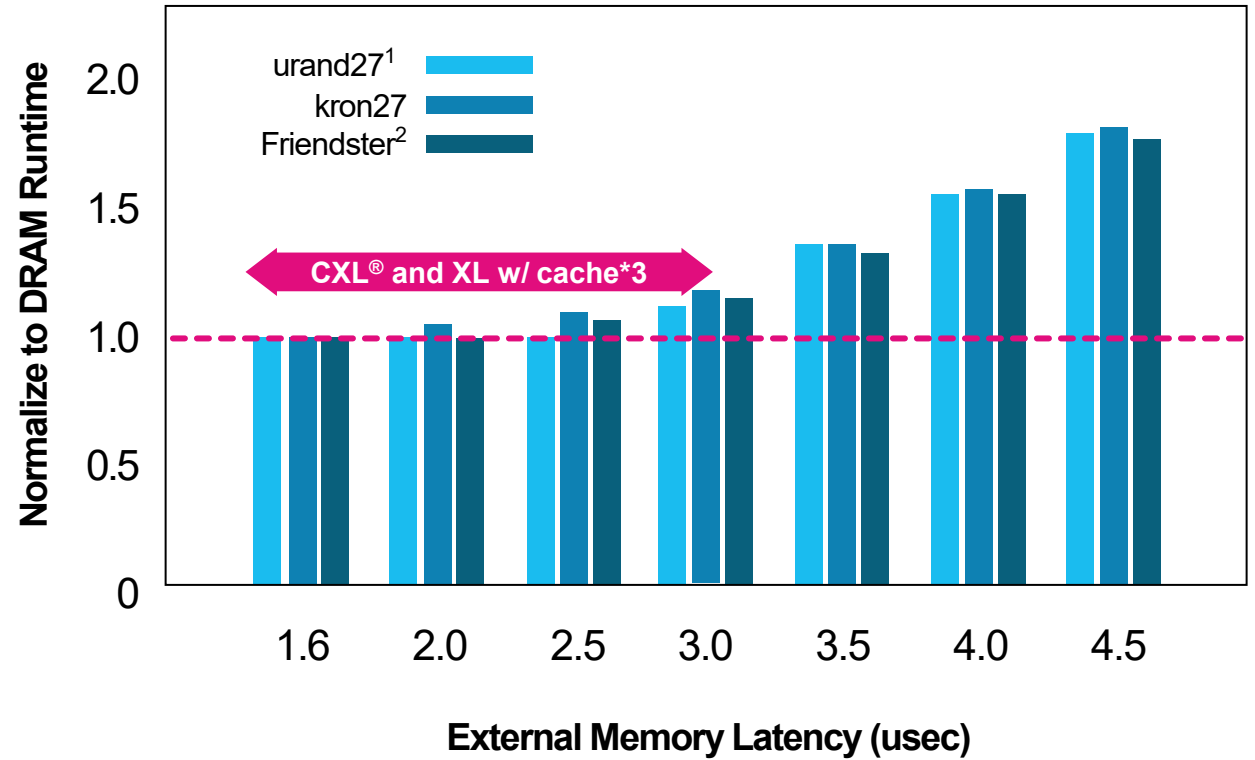
# GPU Graph Processing with Low Latency Flash



External Memory for GPU

Image and graph source: created by KIOXIA

## BFS (Breadth First Search)



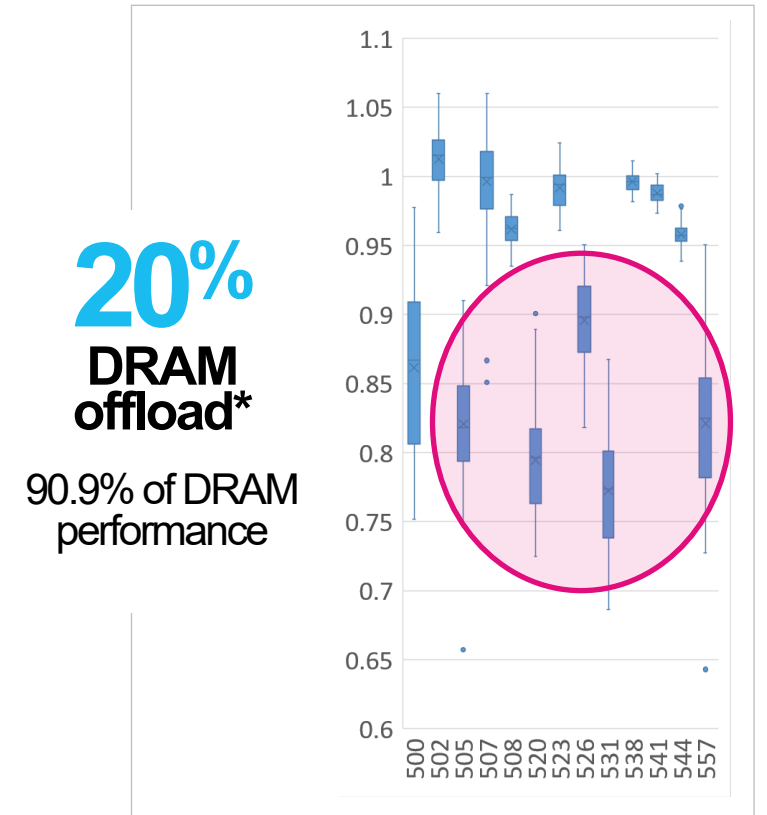
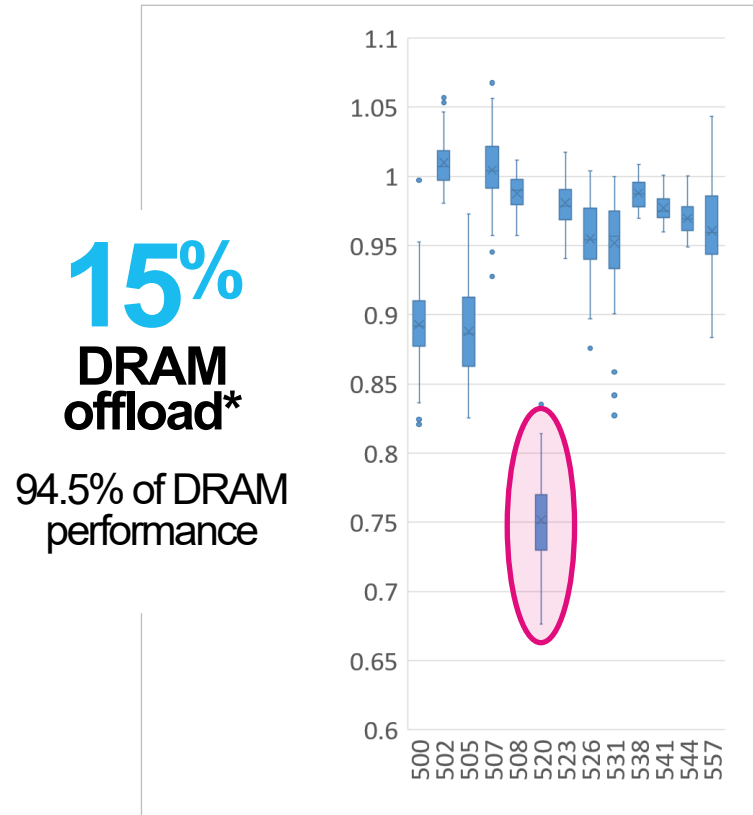
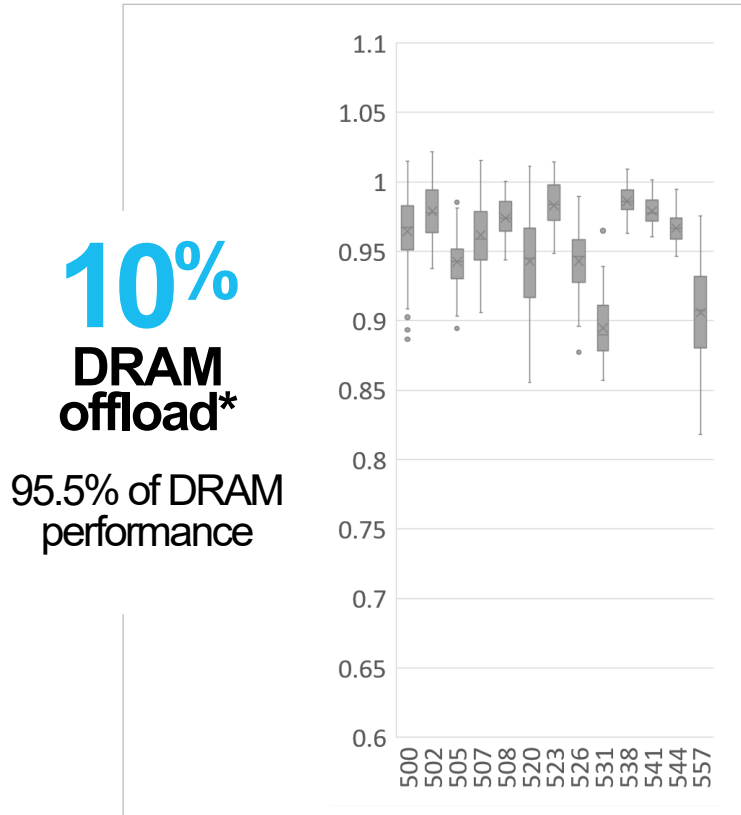
GPU Graph Processing on CXL<sup>®</sup>-Based Microsecond-Latency External Memory (SC23 MSTA)

**Low latency XL-FLASH with cache can deliver DRAM-like application performance.**

# SPEC CPU® Benchmark with Low Latency Flash

**SPEC CPU:** SPEC CPU is a benchmark suite designed to measure and compare the performance of CPUs, memory subsystems, and compilers through a series of compute-intensive tests.

**Test Setup:** 32 copies x 4 hours, 10%, 15% & 20% offload



\*FPGA emu. for memory offload

Image and graph source: created by KIOXIA

**Low Latency XL-FLASH can offload memory with nominal performance degradation.**



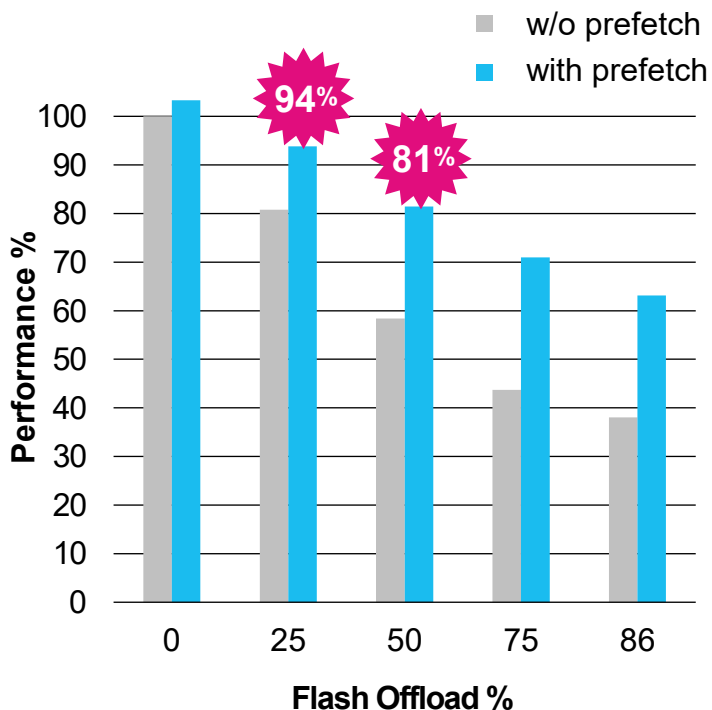


# Redis™ In-Memory Database with Low Latency Flash

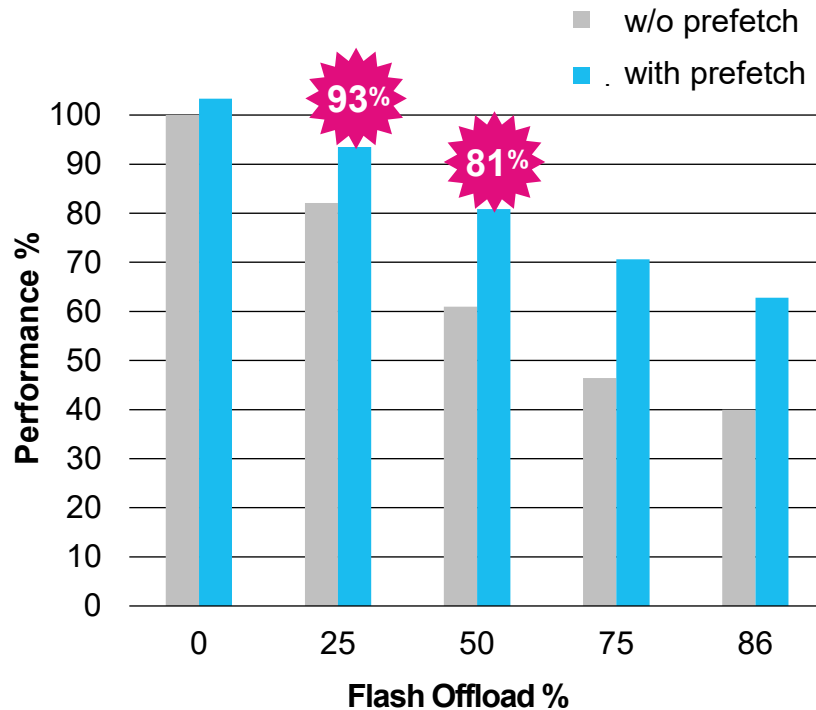
Tested with Yahoo!™ Cloud Serving Benchmark (YCSB) tool  
Setup: 10M records(14 GB), 32 client threads

Data Type: 100B\*10 fields/record  
Offload with Linux® TPP (Transparent Page Placement)

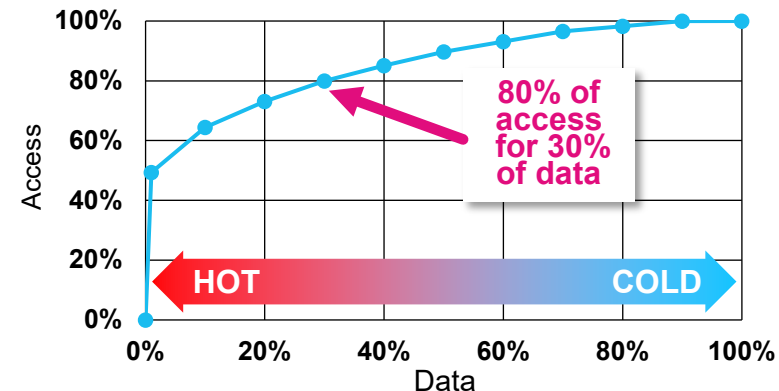
### Test C: Get 100%



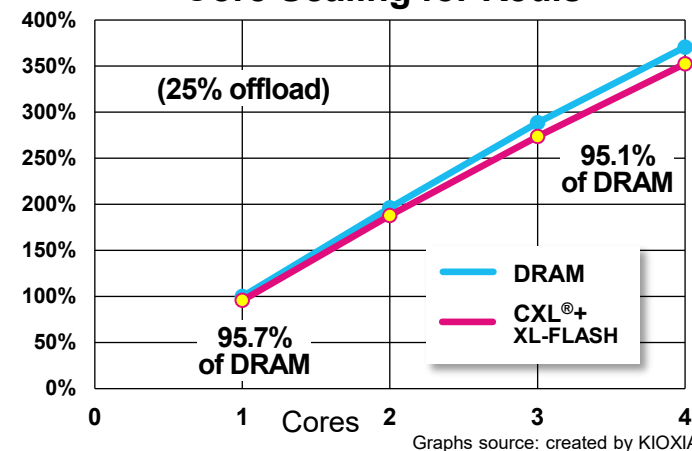
### Test A: Get 50%, Put 50%



### Zipf Distribution Workload A,C



### Core Scaling for Redis



Graphs source: created by KIOXIA

**YCSB demonstrates CXL® and XL-FLASH technologies can offload 25% of memory with ~5% of performance degradation.**



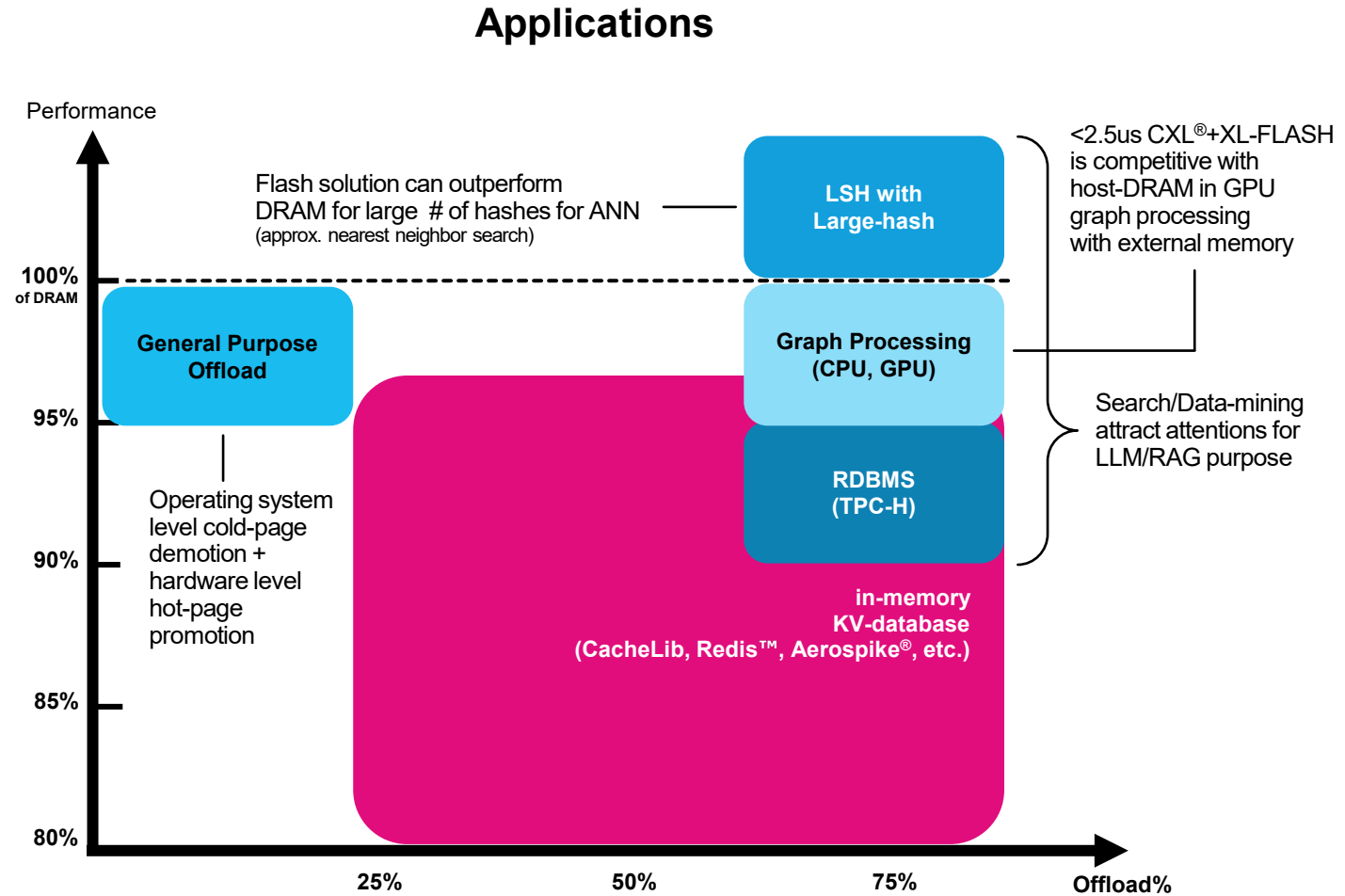
# Challenges and Opportunities with CXL<sup>®</sup> Attached Flash Memory

## All Applications Are Not The Same

- It is not suitable for latency/bandwidth sensitive applications
- Application not tuned for leveraging memory hierarchy optimally

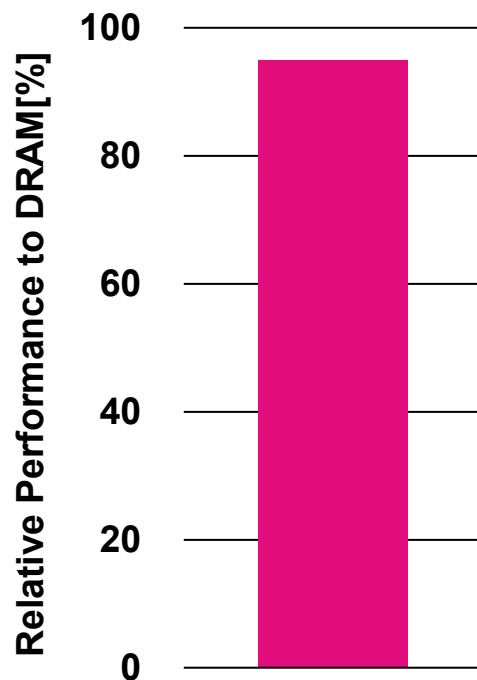
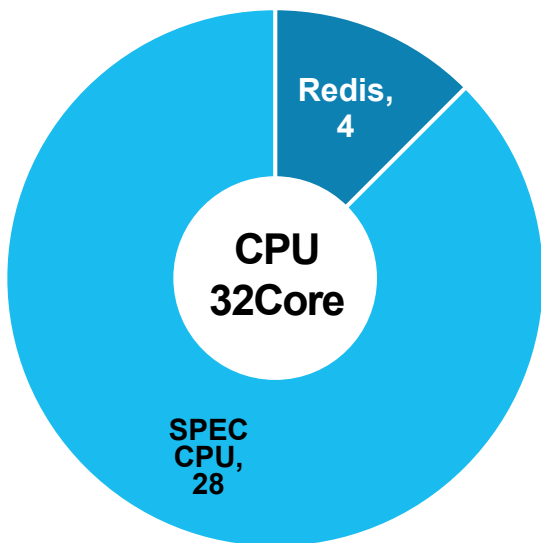
## Leverage Industry Efforts

- Transparent Page Placement - Automatically manages large memory pages
- Transparent memory tiering solutions optimizes data placement across different memory types
- Application specific libraries can further increase the efficiency and reduce cost

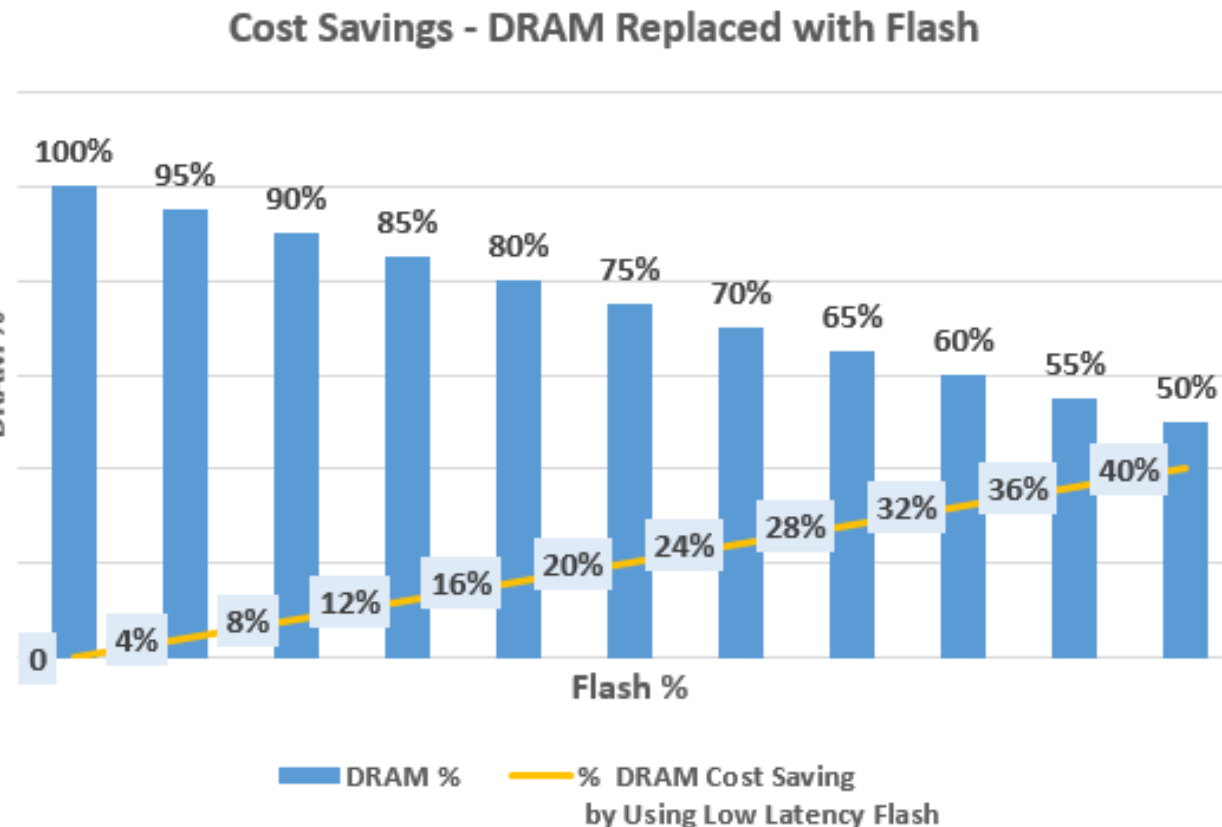


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# Application and TCO

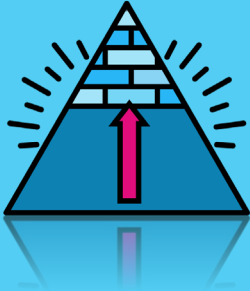


Case B	Offload	Performance
Redis™ x 4 cores	25%	94%
SPEC CPU® x 28 cores	15%	95%
<b>total</b>	<b>23%</b>	<b>95%</b>

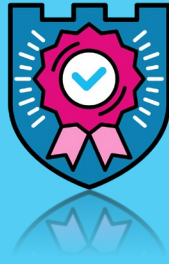


KIOXIA assumption: Price of Low Latency Flash is 1/5 DDR Price.

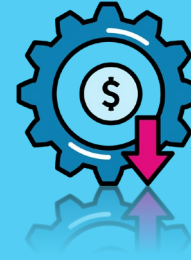
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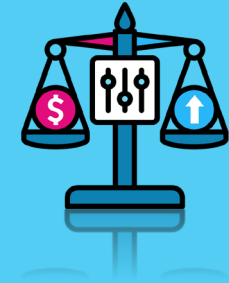
Flash memory can jump the semantic wall.



Flash memory is proven and reliable media.



Flash memory lowers the system TCO.



Flash memory can further perform and reduce cost with software.

If you are working on large memory intensive applications like **Data Mining, Artificial Intelligence (AI), Machine Learning (ML), Analytics, High Performance Computing (HPC), Graph Processing Applications**, Please visit **KIOXIA Booth #307** for collaboration opportunities.



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