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Reliability Testing of Emerging Non-Volatile Memories
How to Shorten Time-To-Result

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Non-Volatile Memories Pervasive Presence

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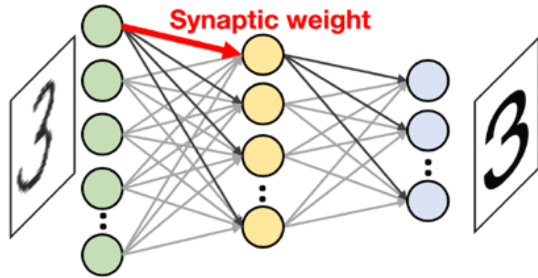
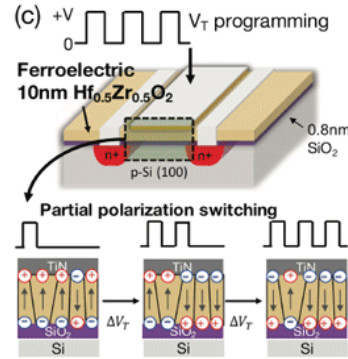
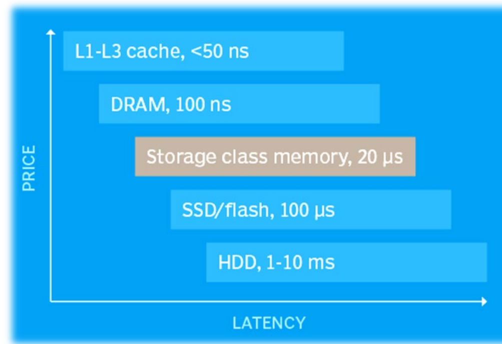






NVMs are used everywhere

- In-memory and analog computing
- Embedded code/data
- Tiering of storage technologies

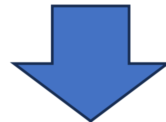
NVMs have unlimited applications

- Client, Edge, Data Center, AI/ML
- Consumer, Industrial, Automotive
- Mission Critical, Space

Reliability Test Taking Too Much Time

NVM technology innovation is pushing many boundaries

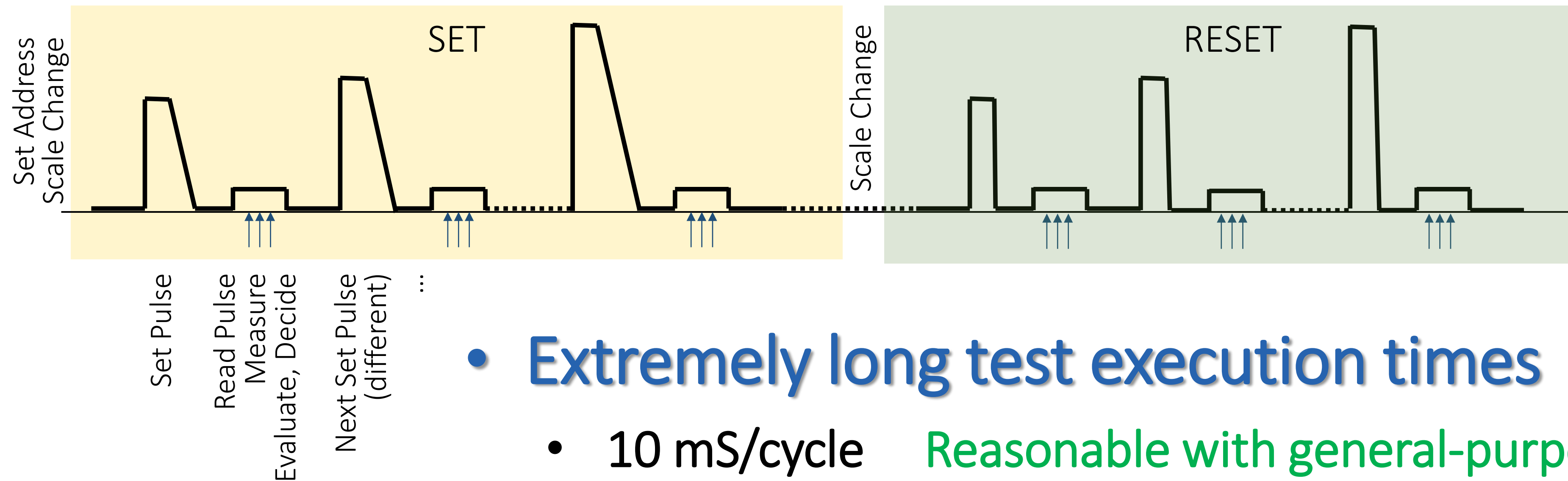
- Analog signals have more complex sequences and shapes
- Signals timing gets much faster
- Reliability evaluation on memory array test chip is highly analogic
- Algorithms for Set/Reset and Read operations get more sophisticated
- Endurance can reach 10^6 cycles … and beyond
- Stress worsens because of broad applications and environmental conditions



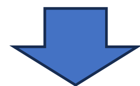
Reliability Test Can Take Several Months

The Speed Challenge

Memory array endurance loop: millions to billions of times on hundreds to thousands of cells



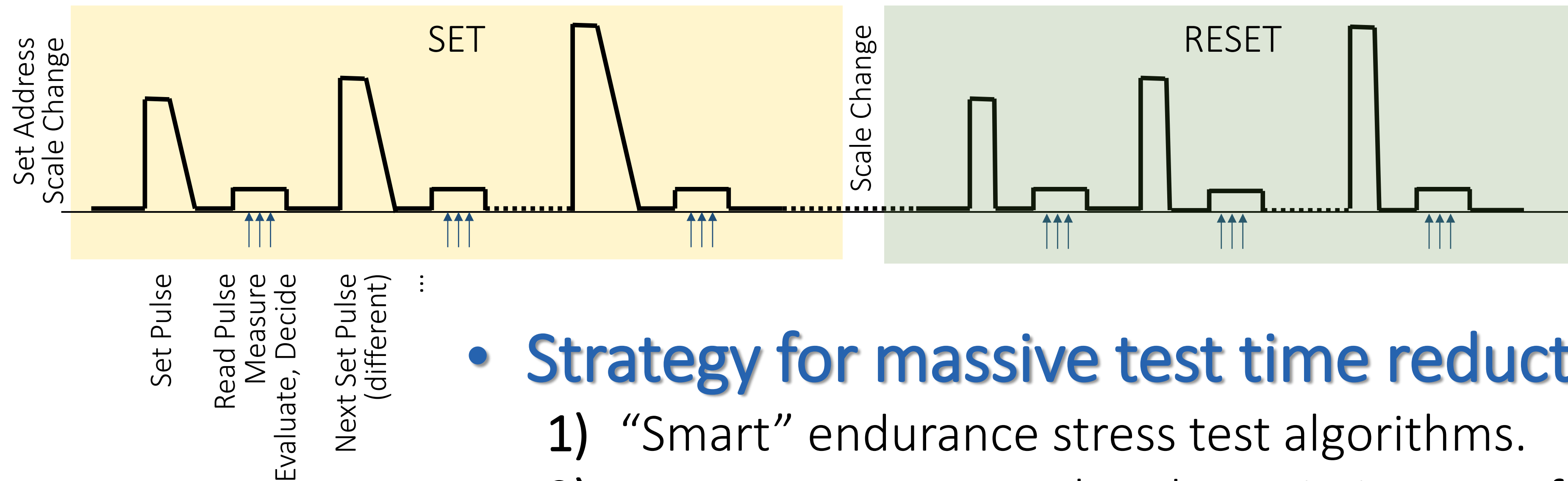
- Extremely long test execution times
  - 10 mS/cycle Reasonable with general-purpose instruments
  - 1M cycles
  - 1k cell test chip array



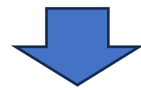
  - 4 months Too long for a Reliability test

The Speed Challenge

Memory array endurance loop: millions to billions of times on hundreds to thousands of cells



- **Strategy for massive test time reduction**
  1) "Smart" endurance stress test algorithms.
  2) Low test system overhead. Maximize test efficiency



- **Can we reduce by 1,000x to ~10uS per Cycle?**

How do we achieve 1,000x? ... with TESTMESH!

A system designed explicitly for NVM

- 2nd Generation of NVM technologies tester for Flash, ReRAM, PCM, FeRAM, MRAM.
- System with composable instrumentation designed for speed and signals complexity of emerging NVM
- Multiple configurations for different NVM stages:
  - From Cell and Memory array technology evaluation
  - To Production qualification and quality monitoring

How do we achieve 1,000x – Part 1

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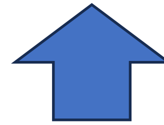
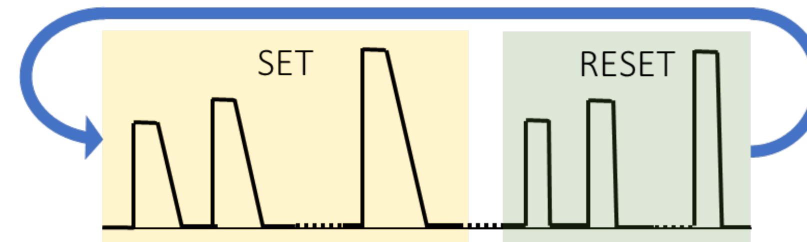
“Smart” endurance stress test algorithm

- Do only what is needed. Focus on what matters for stress
- Simplify/Minimize time-consuming sequences



- Fixed S/R pulses per cell: no Read/Measure/Decide time
- Memory map with S/R pulses required by each cell
- Recompute periodically the S/R pulses required by each cell



How do we achieve 1,000x – Part 2

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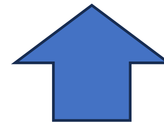
Low Test System Overhead

- Maximize Test System Efficiency



- High-speed Algorithmic Waveform Generator (5nS Step) powered by real-time embedded processor.
- Very fast switch (<1uS) between Analog sequences
- High-Speed (100 MHz) Digital Sequences generator
- Tight synchronization between Analog and Digital instrumentation.
- Very fast PMU sampling time (10nS) with range switch time <10uS.

More on actual results with TESTMESH

PCM test array

- 9,000x increase: 3 minutes vs. 43 hours test time of a system with general-purpose instruments
- Many experiments, evaluations, and analyses were done with a 3-minute test duration.

ReRAM test array

- Ultra-fast cycling of semi-blind S/R loop with instruments programmable algorithmic sequences
- Very good reliability matching between the semi-blind S/R and full S/R sequence.

Test Program and Algorithmic Sequences

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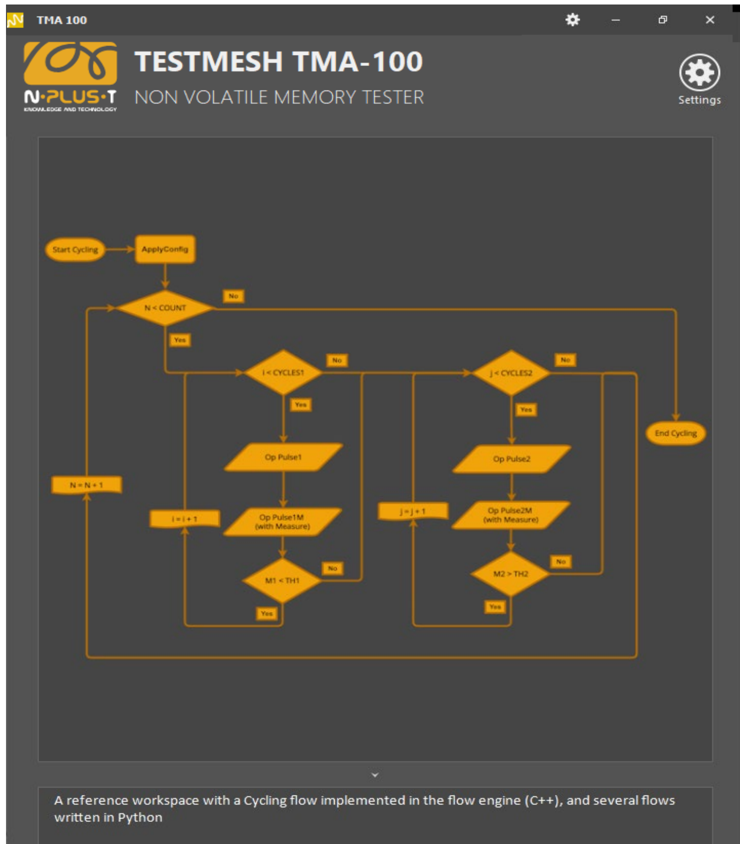

• High-Level Test Flow in Python

- Test Program runs on a motherboard with local PCIe interfaces to instrumentations
- Easy to use (everybody knows Python), productive, reliable results.
- Run-time development/debugging supported with Visual Studio Code

• Low-Level Instrument Algorithmic Sequences in C/C++

- Timing critical Sequences running on the instrumentation's real-time embedded controller
- Very low overhead on low-level timing critical sequences
- Large set of library functions with reference memory operation sequences

TESTMESH Standard Configurations

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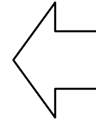
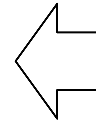
NVM Cell
Wafer level



TMS-100
- Single Cells

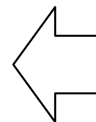
TMA-100
- Single cells
- Multi-cell structures
- Mini-arrays w/ decoders

Mini Array
Test Chip



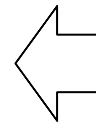
TMC-100
- Crossbar arrays
- Memristor networks

Embedded Macro
Test Chip



TMY-100
- IP Macros with digital interface
- uC/SoC with embedded memories
- NVM memory components

Product
SoC, Component



Standard NVM Test Systems Configurations

Configurations	TMS-100	TMC-100	TMA-100	TMY-100
Target DUT	Single Cell	Crossbar and Memristor Array	Single Cell and Mini-Array	Embedded Macro, Component
Capabilities	• Set/Reset/Program/Erase • Analog pulses and measurements	• Set/Reset/Program/Erase • Analog pulses and measurements • Array parameters bitmap • Memristor specific selectors/decoders • Configurable connections to DUT	• Set/Reset/Program/Erase • Analog pulses and measurements • Array parameters bitmap • Cell address decoder • Configurable connections to DUT	• JTAG, SPI, I2C, parallel,.. protocols • Analog measurements • Array parameters bitmap • Pass/Fail and internal digital information readout
Waveform Generators	4	4, 8	4, 8, 12	-
Measurement Units	1	2, 3	2, 3, 4	1
Digital IOs	-	32	32, 64	64
Power Supplies	-	4	4	4
Vref	-	2 global, 16 for rows	2	2
Iref	-	1	1	1
DUT Signal Interface	Direct	Multiplexers Bank	Switch Matrix	Direct (custom)
DUT Connection	4 SMB	Socket Board	34 SMB	Socket Board

A tester conceived for NVM technologies can achieve 1,000x time reduction over a system with general-purpose instrumentation

- Millions of Cycles can be achieved in hours instead of months.
- Exceptional analog performances in a speed-optimized test system architecture
- Programmable test flows, sequences, and algorithms “Memory Bitmap Aware” running full speed
- Architected to support from Cell to Array to Memory chip with proprietary instruments configurations
- Come to see us at the Exhibits @ booth 749, www.n-plus-t.com