Memory Technologies : How Chiplets Change Everything
Rev 1

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the Future of Memory and Storage

Overview

- New Memory Technology Review
- Barriers to Implementation
- SRAM Scaling Challenges
- Chiplets to the Rescue
- Financial and Strategic Examples
- Summary

New Memories

- In previous presentations (FMS) we have shown WHY Emerging memories do not ever really emerge
- They need to be Niche, Embedded, or no cost adder to DRAM/NAND
  - There is not …and there never will be…. a “universal memory”
  - “Nature” and “Science” will have articles promoting universal memory.
- Optane showed that even with billions spending and support for ecosystem, mass acceptance is too slow to build a fab around
  - We have spreadsheets to explain why finances don’t make sense.
- Hence most end up as niche or abandoned

Memory Technologies Reviewed

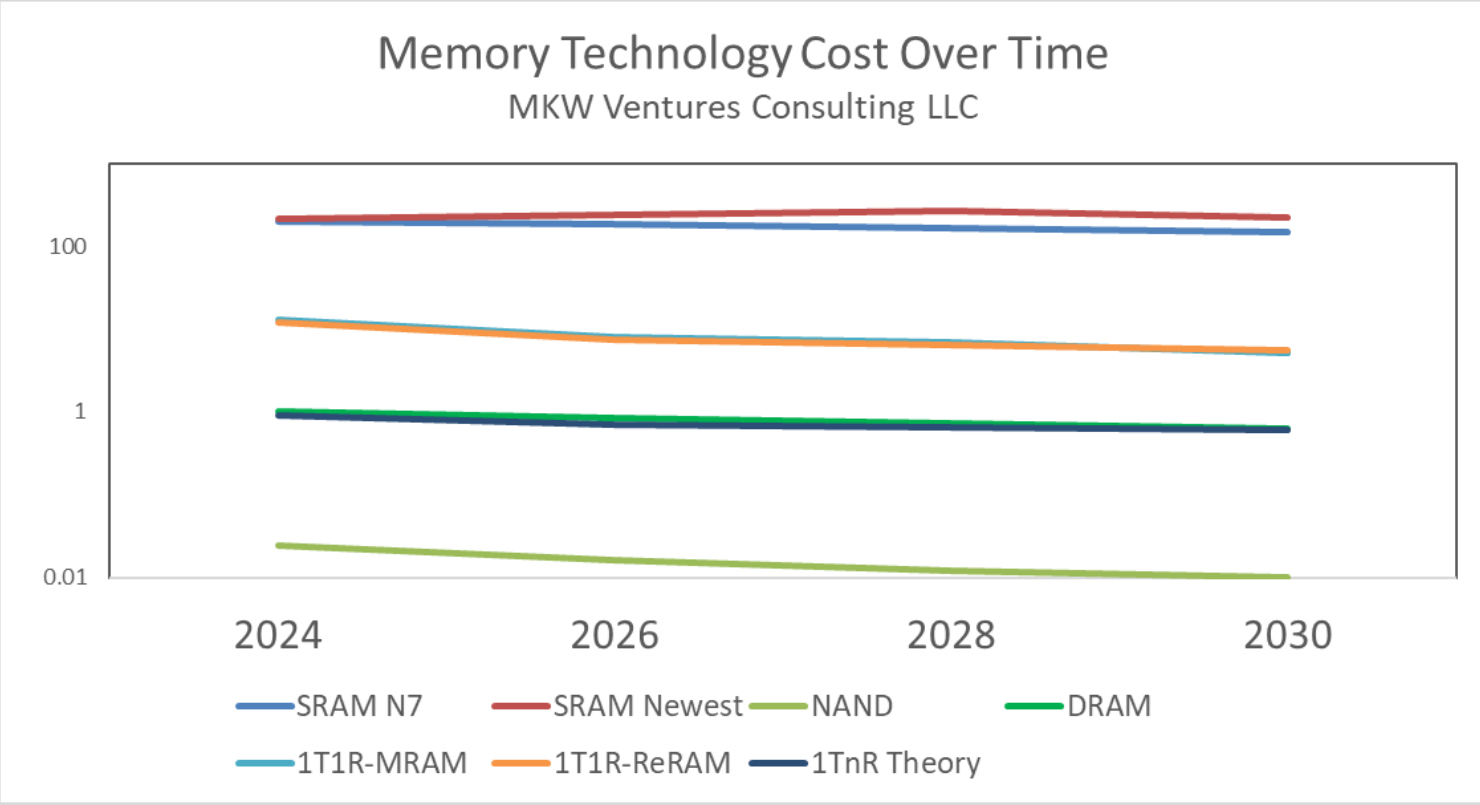
UPDATED Scorecard: We don't need Universal … Lots of Yellow!

	Latency	Density	Cost	HVM ready
DRAM	*****	***	***	*****
NAND	*	*****	*****	*****
SRAM	*****	*	*	*****
NOR	***	**	**	*****
MRAM	****	**	**	****
RRAM	***	**	**	****
PCM (1T1R)	***	**	**	****
FE RAM (Gb)	***	**	***	*
Other	***	**	**	*

MKW Ventures Model

Costs for All Memory Technologies Over Time

- Memory costs differ by orders of magnitude. Huge tradeoffs.
- SRAM on leading edge cost increases. SRAM on N-2 node cost decreases



MKW Ventures Cost Model

NOTE: SRAM is based on cost of 2MB L2 Cache macro based on bit cost

Some Challenges (Pros/Cons)

- DRAM: Fast/Volatile
- NAND: Cheap/Slow
- SRAM: Really Fast/Expensive, not scaling
- NOR: Mature NVM/lower density
- MRAM: Fast NVM/Cost
- RRAM/PCM(1T1R): NVM/Medium density
- FeRAM (Gb): Potential/not HVM
- Other (Gb): Potential/10 years from HVM

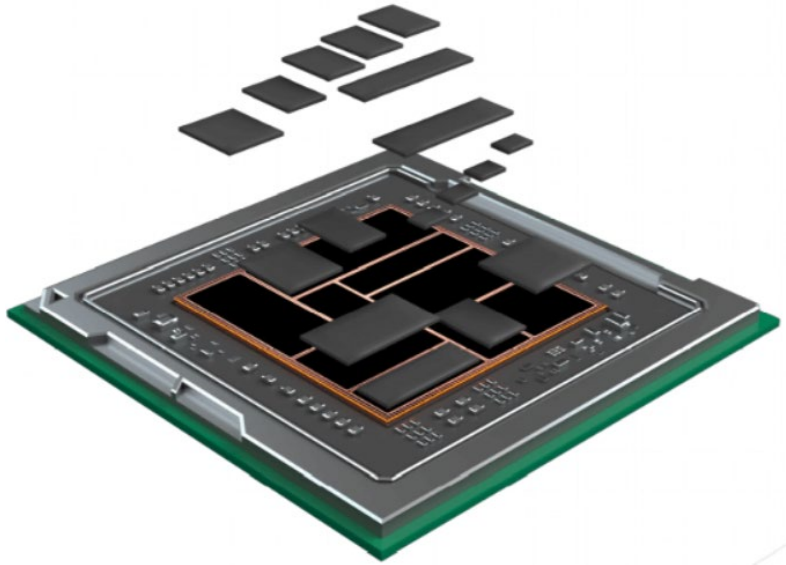
SRAM Scaling

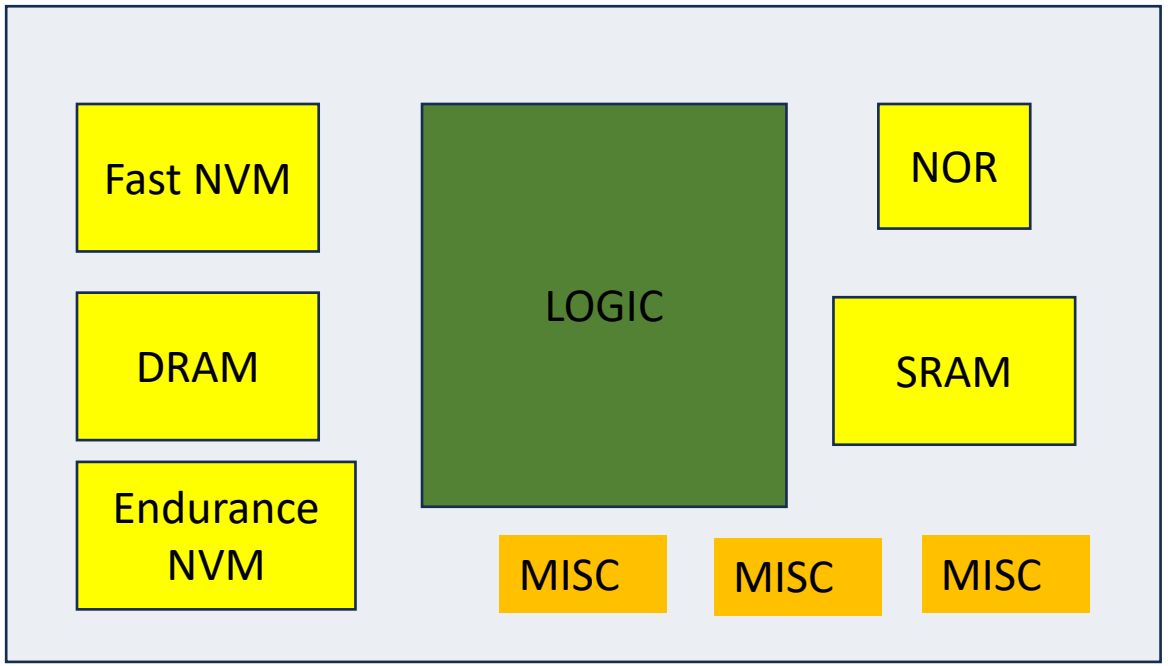
- SRAM is fastest memory and comes free with logic process
- The Cell Size has gone from 40F to 200F over the years
- Very smart people said it wouldn’t scale below 16nm
  - It scaled by a factor of 4 in the 8 years since.
  - But it looks like 3-5nm it did stop (TSMC N5 is .02u^2)
- So L2-L4 Cache needs solutions

Chiplets Solve Many Problems

- Wont cover logic benefits, that is well know
- E-flash processes are too expensive for large chips. Doesn’t Scale
- Embedding MRAM/RRAM adds complexity when it might be <5% of chip area (adds wafer cost)
- SRAM isn’t scaling, why use 3nm chip area?
- eDRAM required optimization for small area of Chip
- Connecting with a bus is too slow.
- SOLUTION: Optimized by need and purpose and “only pay for what you need”

Chiplet Hypothetical





NAND/CXL DRAM off Chip

The Results: Cost and Strategy

- Often we want a feature for a small portion of Chip
  - NOR for boot and XIP code. SRAM for Cache, MRAM/Fast NVM
- BEFORE: Needed to choose a process or choose to access by PCI, DDR, CXL
- Chip designers can now choose ANY memory feature without requiring embedded process.
- Memory suppliers can provide supply without leading edge silicon or high volume
  - The costs didn’t work out before, they do now. 40nm NOR, 22nm MRAM
- Chip made of Chiplets allows all options, optimized cost and modifications in future revisions
  - Ex: Start with NOR, Move to MRAM. Add AI optimized memory (weighting)

Cost Options Examples

Design	
Logic Chip with SRAM one die N3 process, 24MB SRAM	$46
N3 Logic, N7 SRAM 24MB CHIPLET	$42
N3 Logic, 8MB N7 SRAM, 128MB LPDDR4, 2MB NOR CHIPLET	$40
N3 Logic, 8MB N7 SRAM, 16MB MRAM, 1GB LPDDR CHIPLET	$47
28nm 1MB NOR 25mm2 EFLASH Process [1]	$2.40
28nm 1MB NOR 25mm2 CHIPLET [1]	$3.50

[1] On small die/Mature wafer, the wafer cost optimization does not outweigh the increased packaging cost of Chiplets

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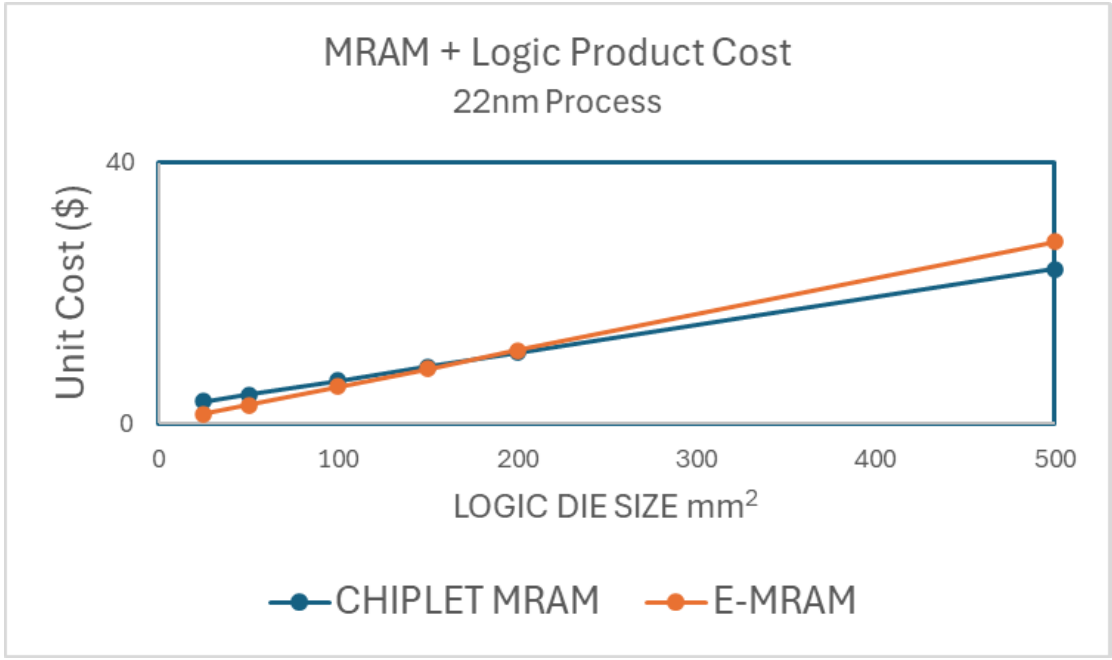
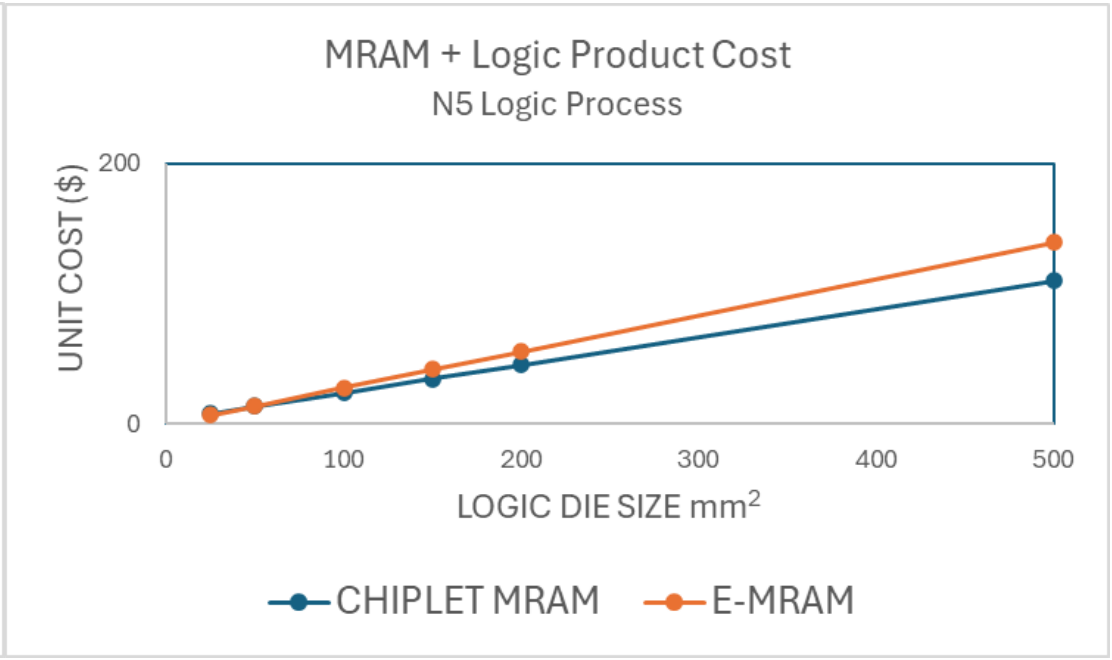
Examples: Cost by Die Size for Logic+MRAM

Small Die, Inexpensive Processes Don't Benefit from Chiplets





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Summary

- Chiplets allow chip designers to implement multiple memories including “niche memories” as trades offs require
  - Mix memories and have options for revisions over time
- L2/3 SRAM Can be optimized for cost separately from logic
  - 10% cost savings from SRAM optimization
- For large logic die on advanced processes, the cost trades are beneficial. Small die are penalized by packaging cost
- From strategy point of view, this adds many memory options to chip designer vs typical eMemory or discrete.

Follow up

- Lots of details available on website and in follow up discussions
- Spreadsheets to discuss trade off numbers available for discussion

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