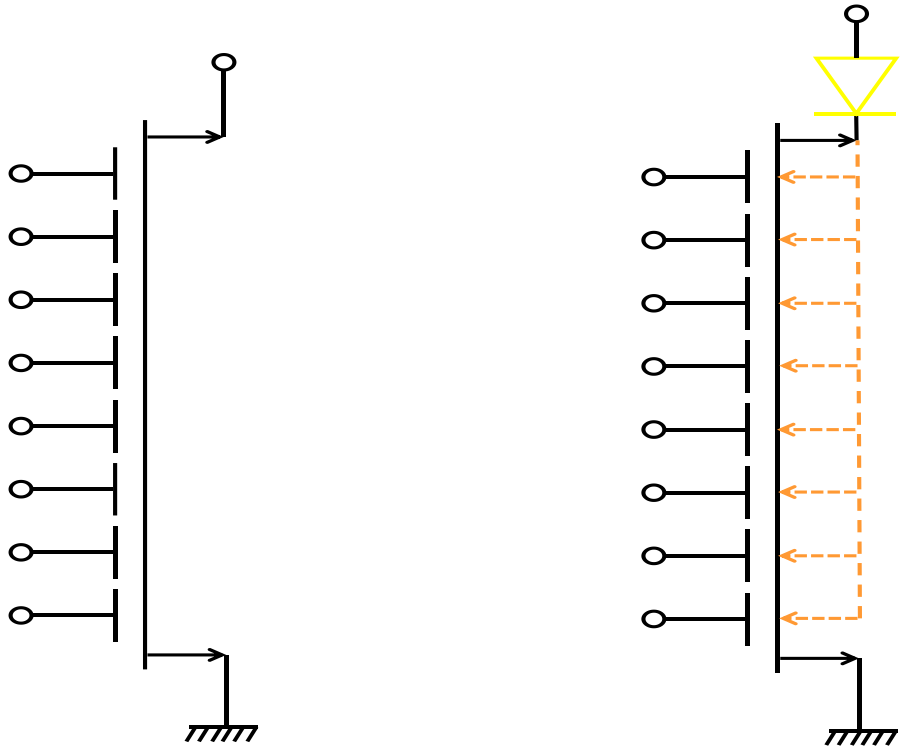
Ultra-High Speed Photonic NAND FLASH

Presenter: James Pan Ph.D.

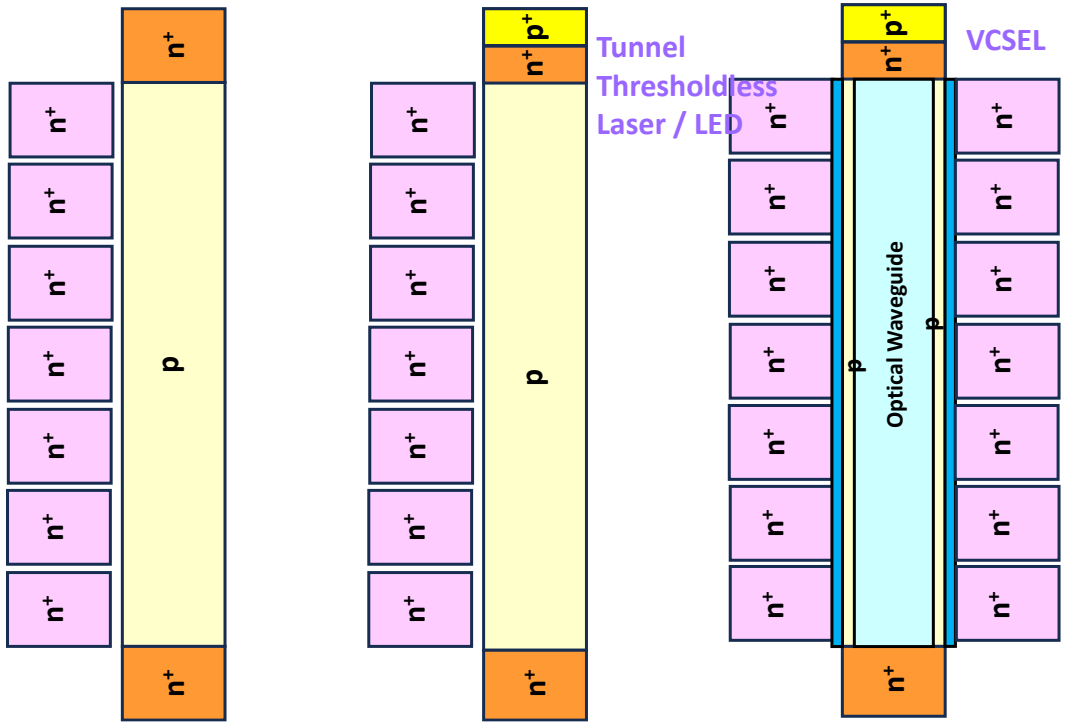
American Enterprise and License Company

Equivalent Circuit



- Left: Traditional NAND FLASH
- Right: Photonic NAND FLASH

Cross Sections

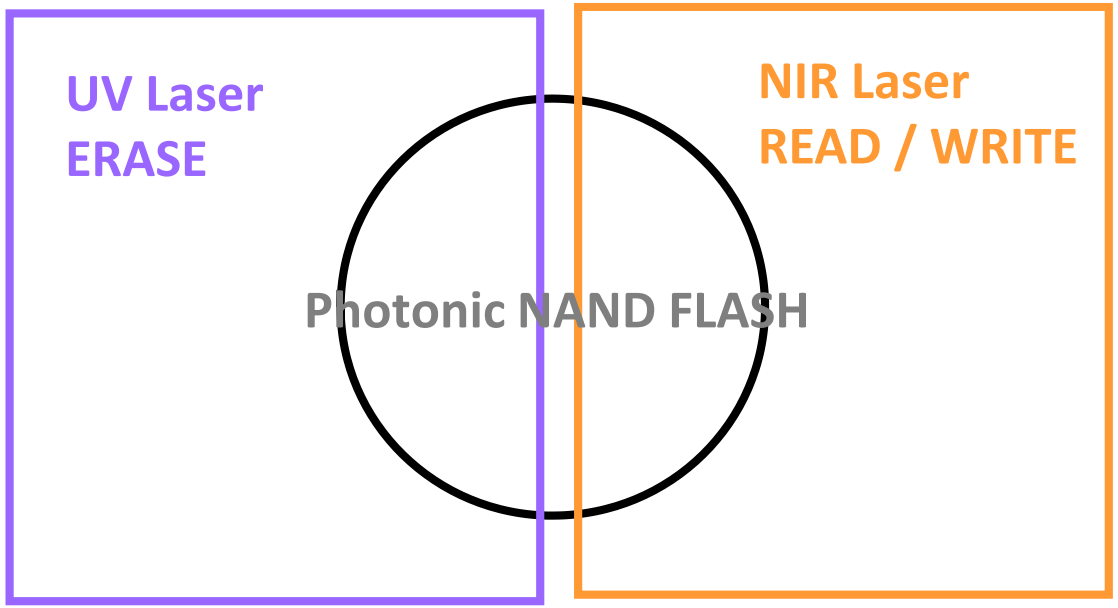


(a) Traditional NAND FLASH

(b) Photonic NAND FLASH

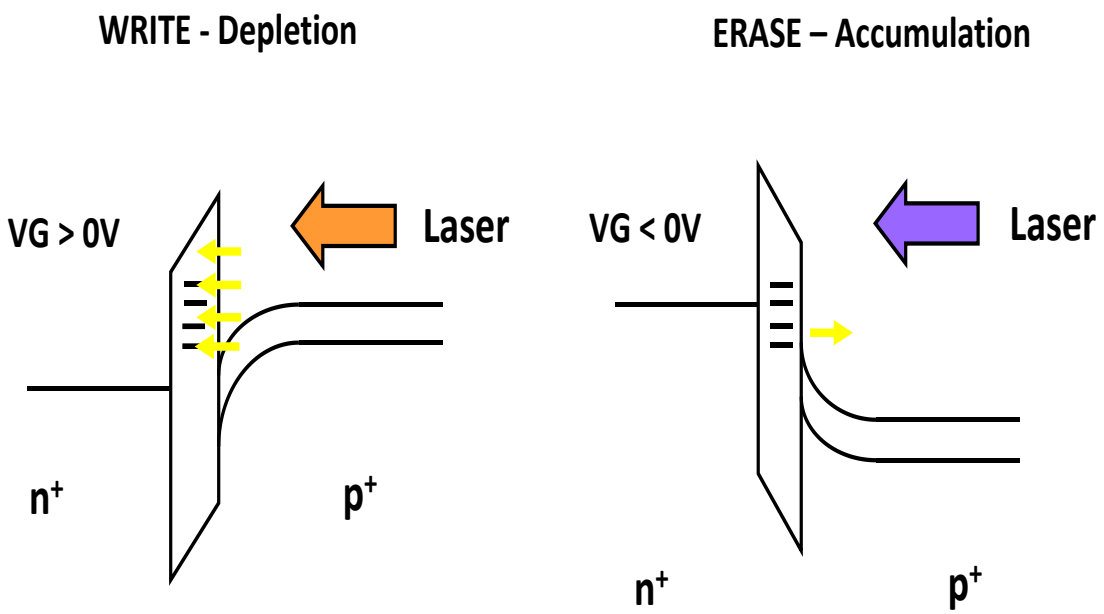
(c) Photonic NAND FLASH with VCSEL

Top Down View



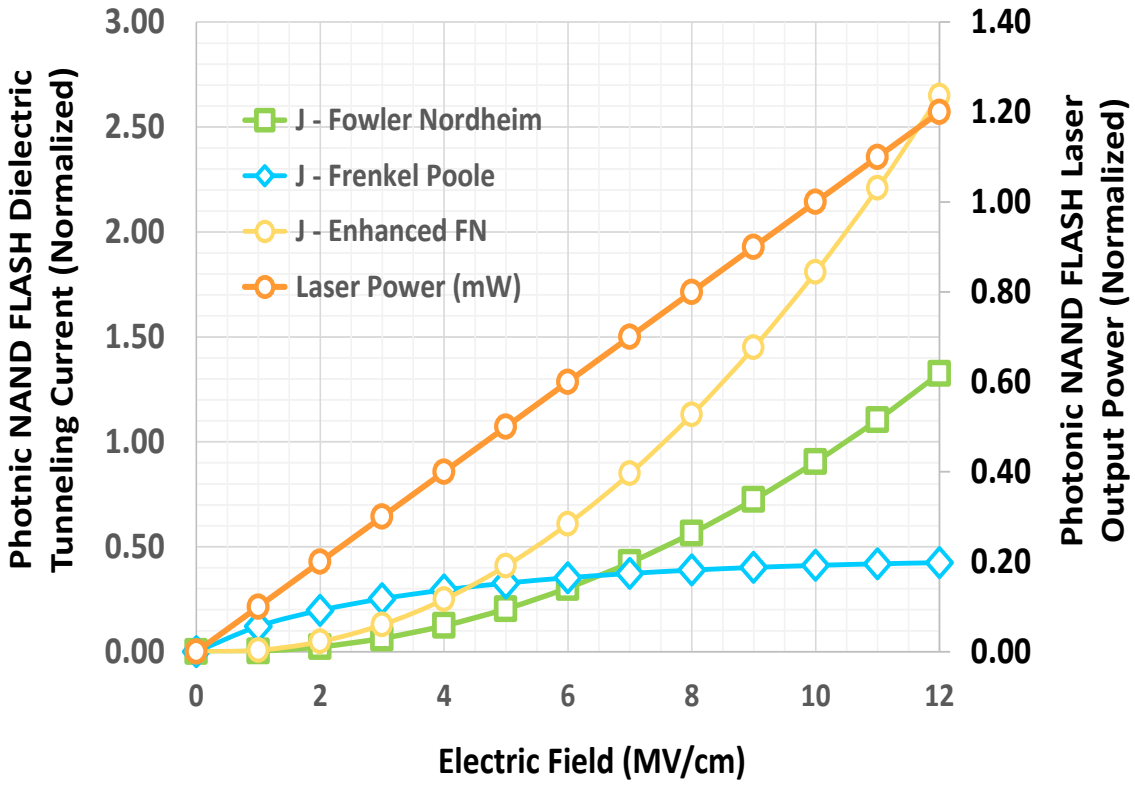
- Top-down view (Layout Design) of a Dual VCSELs Photonic NAND FLASH.

Operations



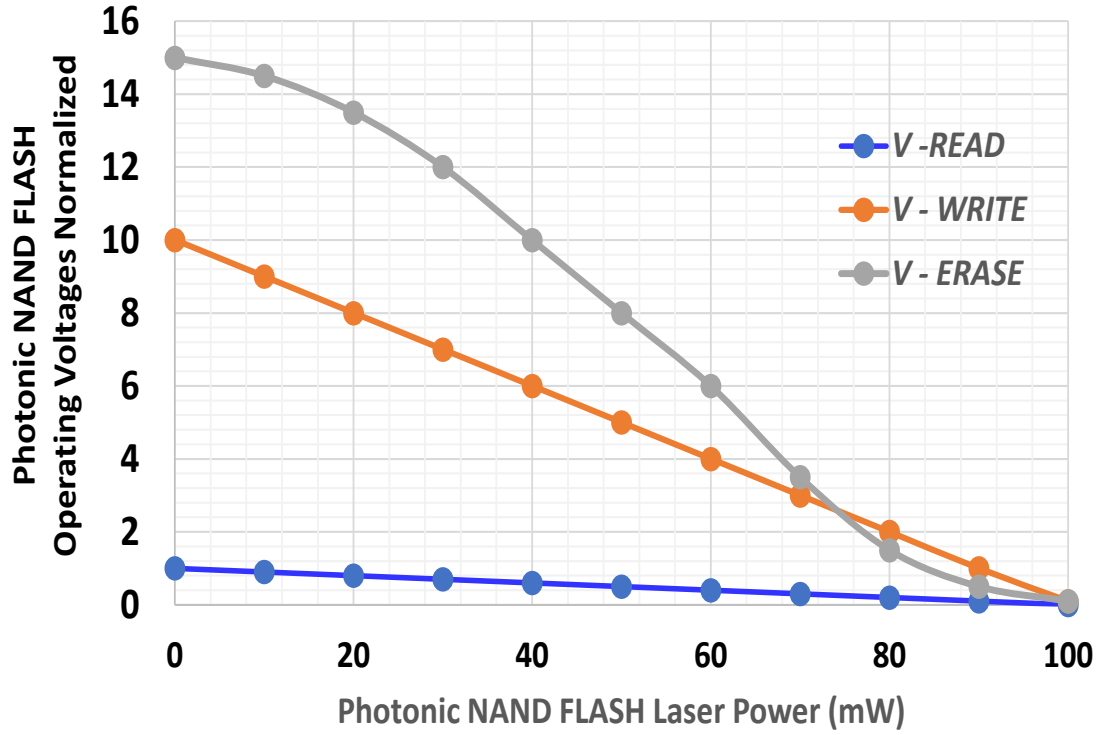
- Energy band diagrams for the WRITE and ERASE cycles of Photonic NAND FLASH.

Tunnelling Mechanisms



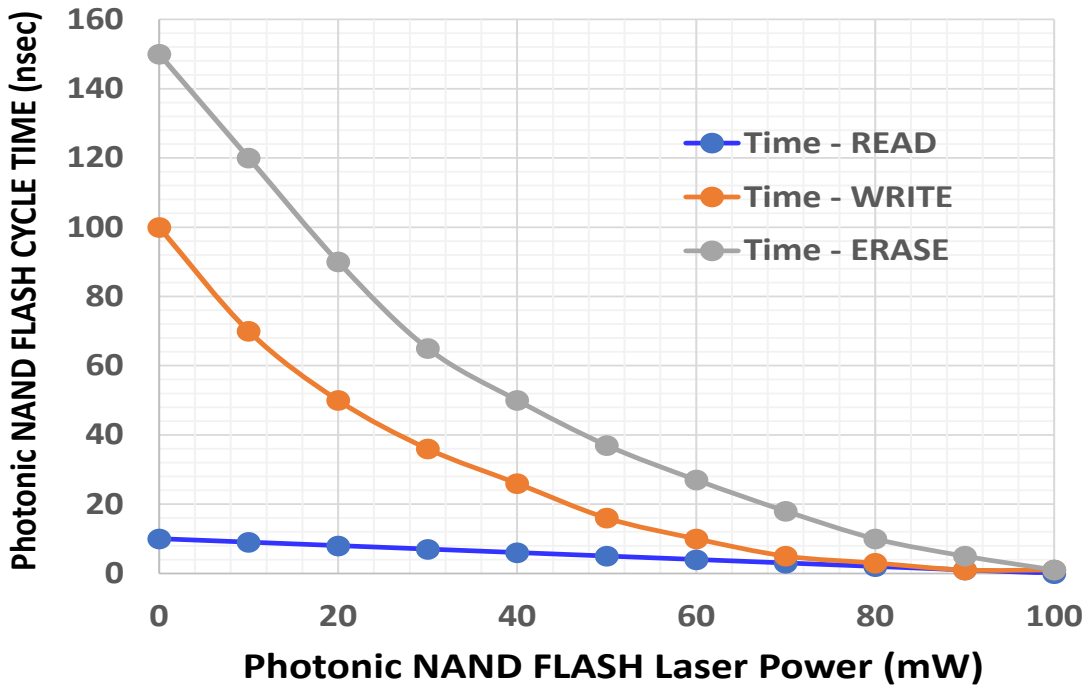
- Fowler Nordheim Tunneling, Frenkel Poole Tunneling, Traps-Enhanced FN Tunneling, and Photon-Enhanced Tunneling for Photonic NAND FLASH.

Power Consumption



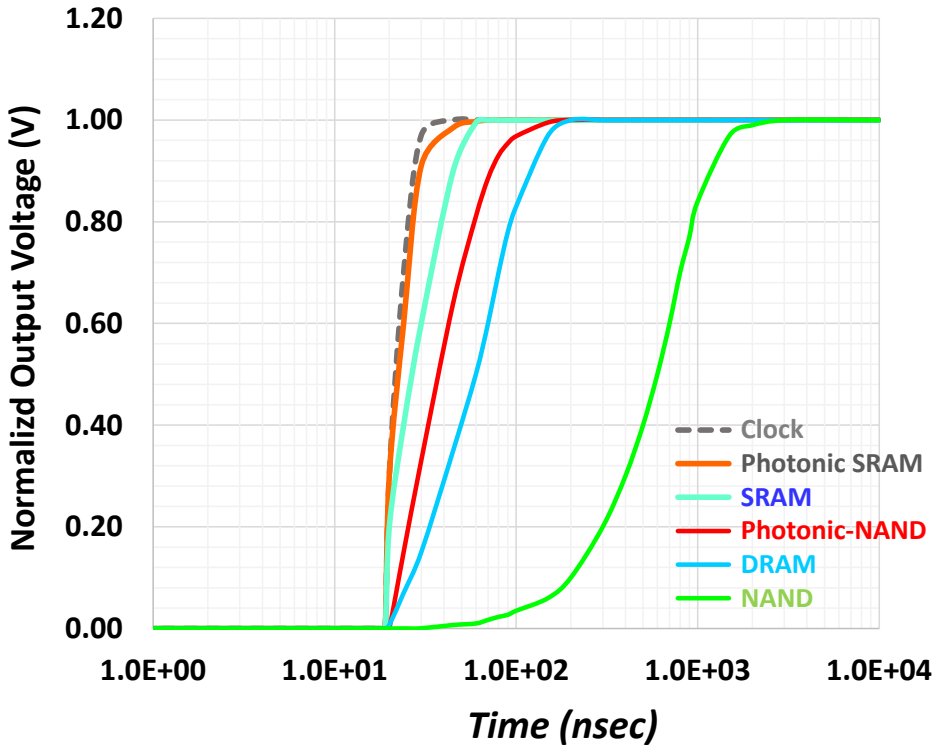
- Photonic NAND FLASH Voltage. vs. Laser Power.

Photonic NAND FLASH Operations



- Photonic NAND FLASH READ / WRITE / ERASE times vs. Laser Power

Photonic NAND FLASH Operations



- Simulated Response

Conclusion

- Ultra-high-speed operations with much lower voltages and power consumption can be achieved with the Photonic NAND FLASH technology. Process integration is compatible with available NAND FLASH process flows. Potentially Photonic NAND FLASH could outperform DRAMs.