ULTRARAM™
ULTRA-EFFICIENT MEMORY

QuInAs Technology

ULTRA**RAM**™: Progress and prospects

Professor Manus Hayne
Chief Scientific Officer, Quinas Technology Ltd

FMS the Future of Memory and Storage

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Outline

- Introduction to ULTRA**RAM**™
- Progress and challenges (scaling, arrays)
- Prospects

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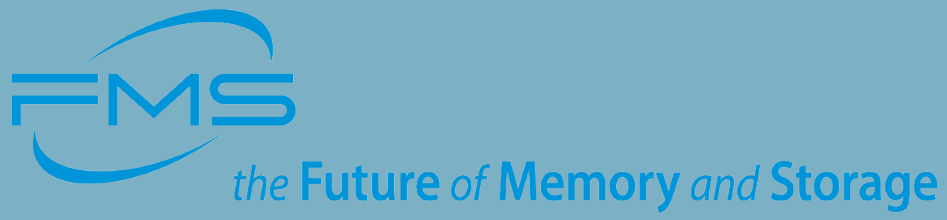
Introduction to ULTRA**RAM**™



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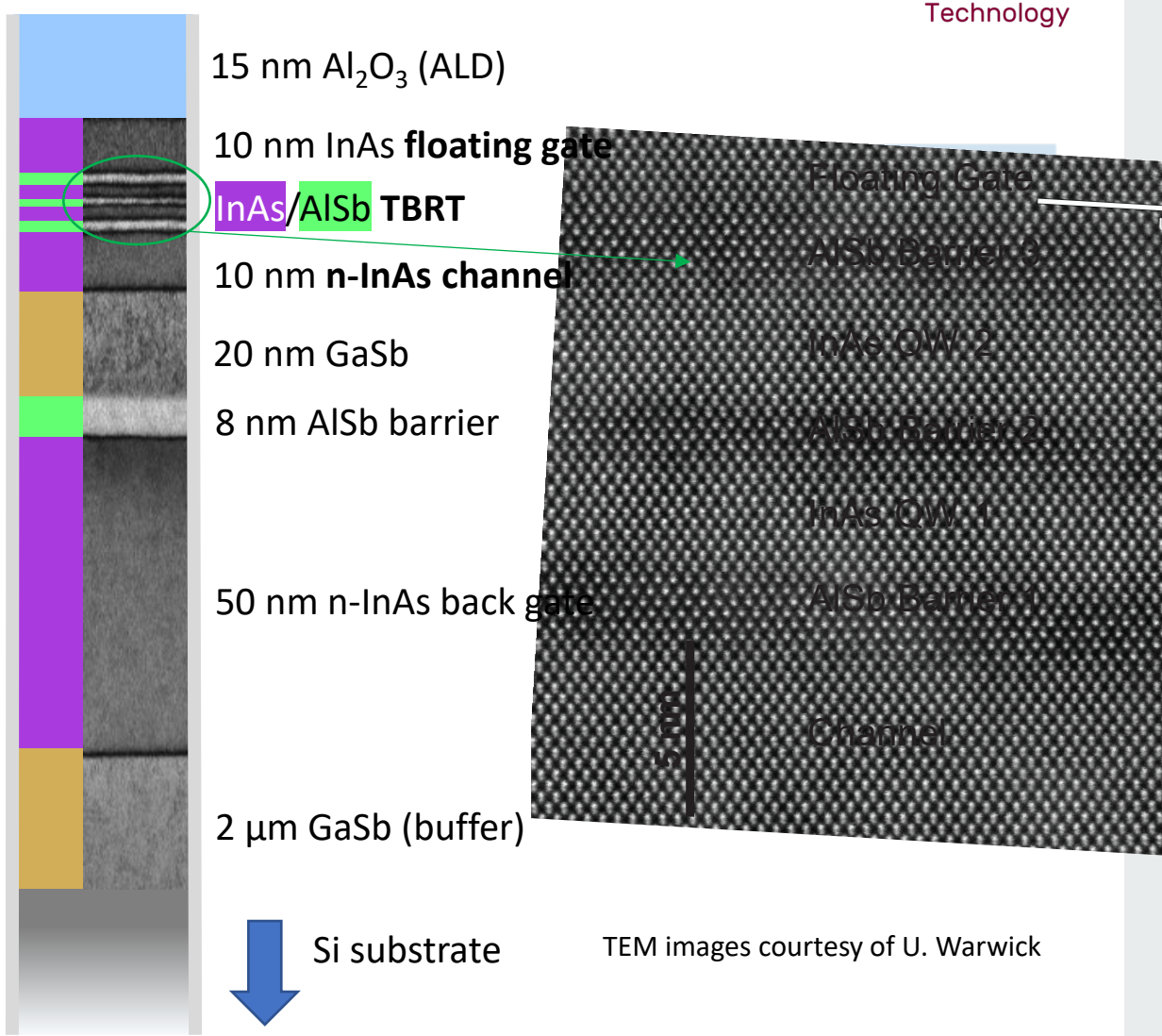
ULTRA**RAM**™ concept

US10243086B2, US11929120B2 + pending

- Floating gate memory (like flash)
- Compound semiconductor based
- High-mobility InAs channel
- Grown on silicon substrates
- Oxide tunnelling barrier is replaced by a

Triple barrier resonant tunnelling structure (TBRT)



TEM images courtesy of U. Warwick

ULTRA**RAM**™ cell

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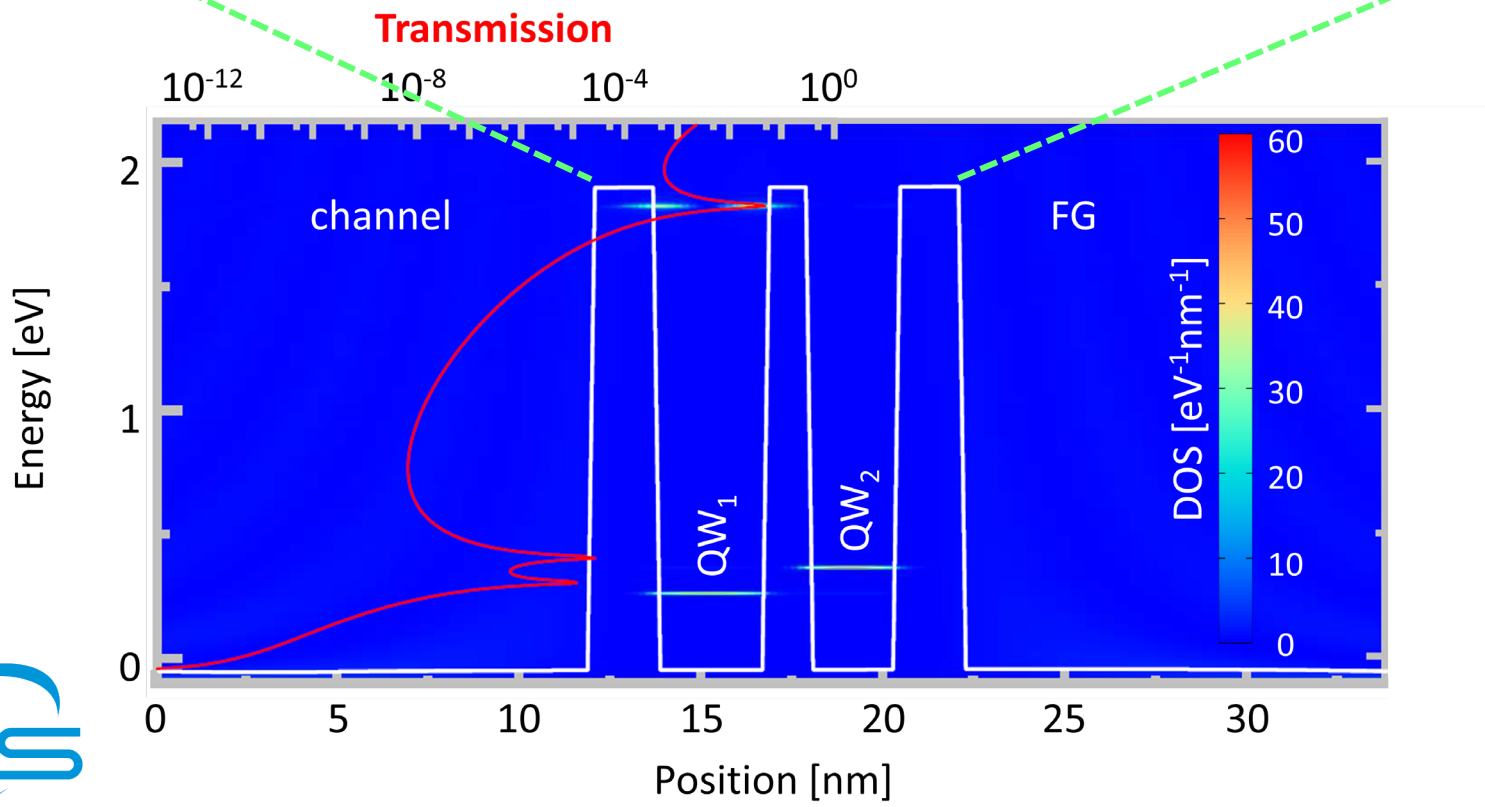
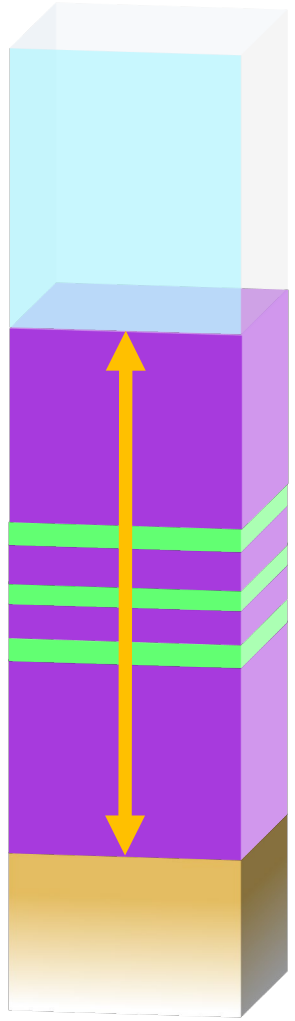
Charge retention (no bias)

1.8 nm AlSb / 3.0 nm InAs / 1.2 nm AlSb / 2.4 nm InAs / 1.8 nm AlSb





blocking barrier oxide

floating gate (**FG**) InAs

TBRT region InAs/AlSb

channel InAs

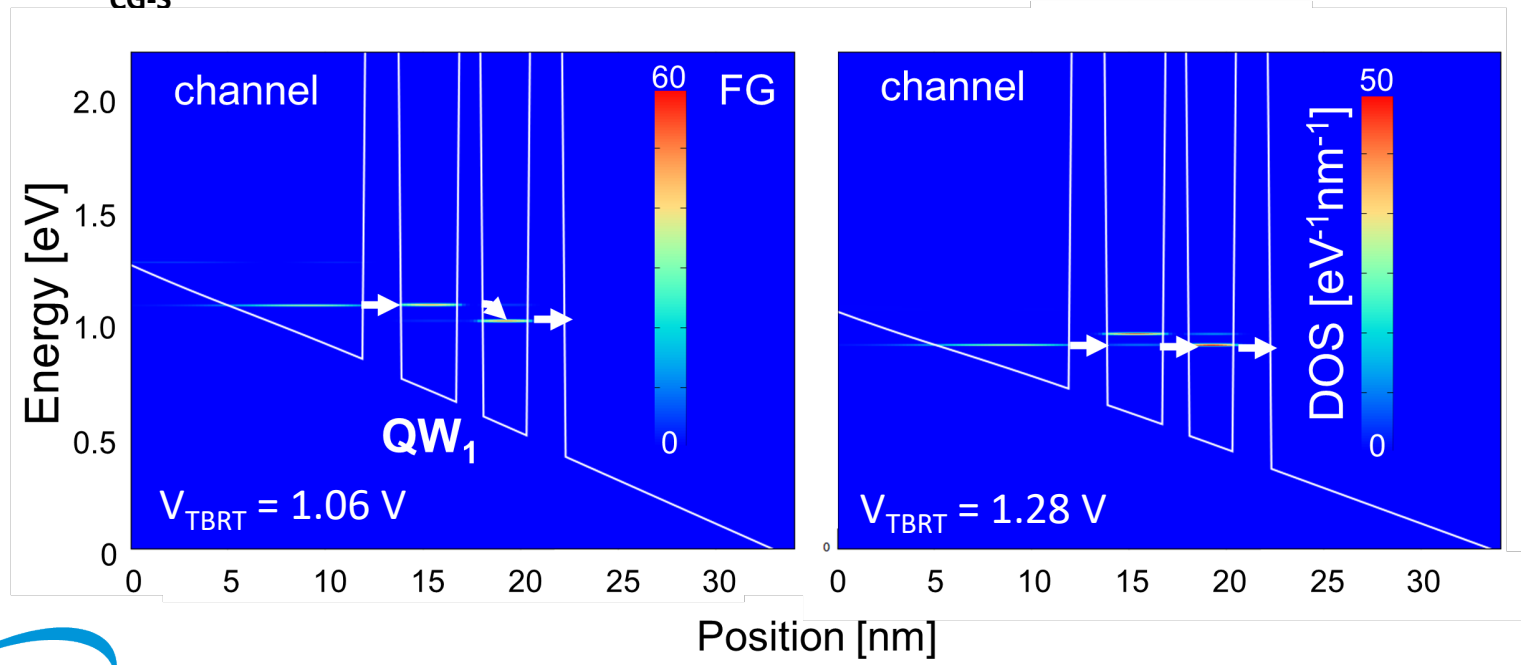
back gate (BG) and substrate layers

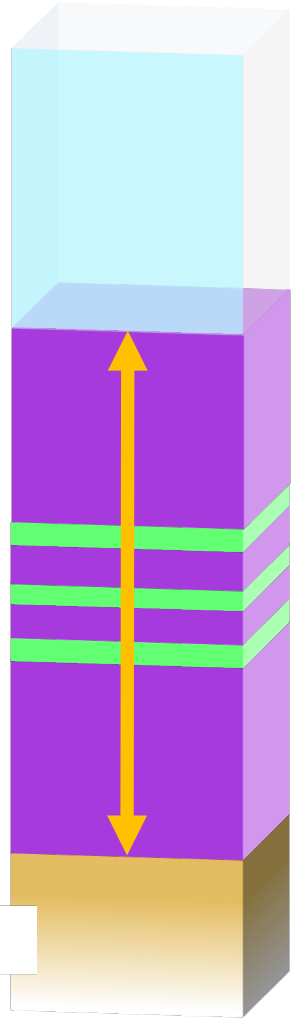
Lane and Hayne, J. Phys. D: Appl. Phys. **54**, 35104 (2021)

Program and erase (≤2.5 V)

Program (P) cycle: add electrons to the floating gate

V_{CG-S} < +2.5 V





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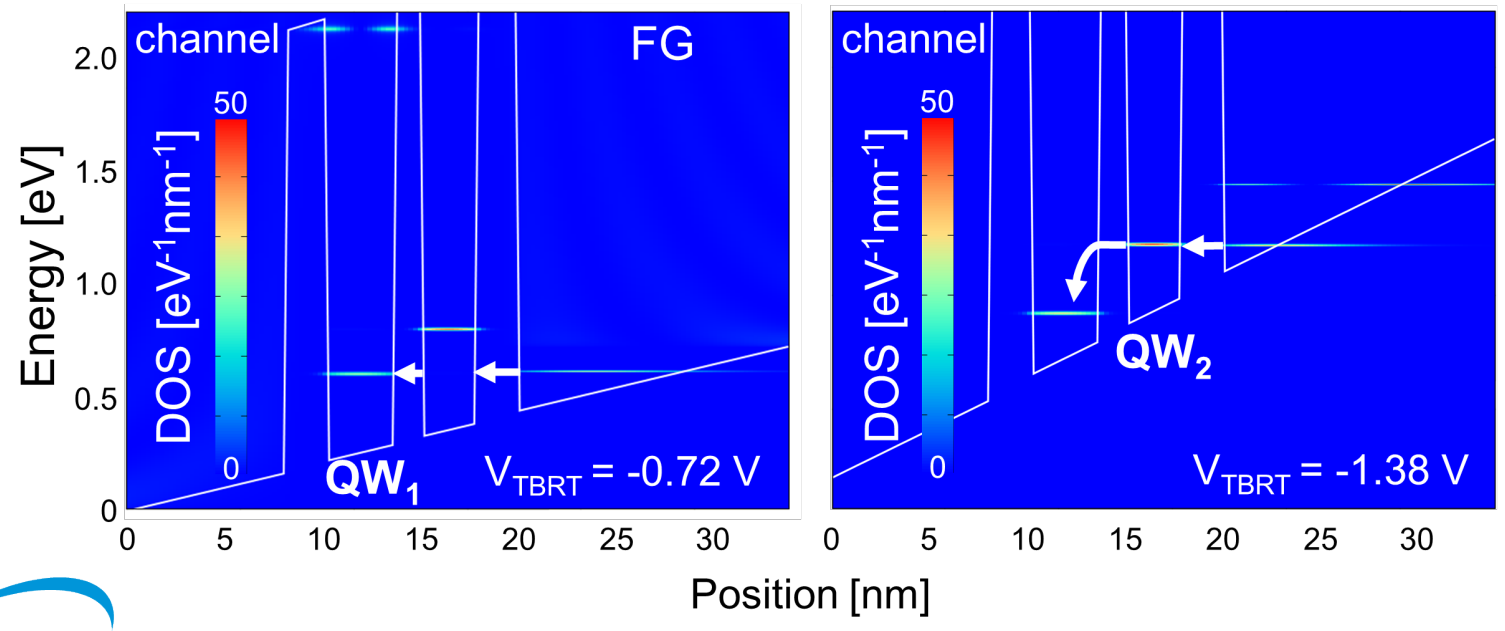
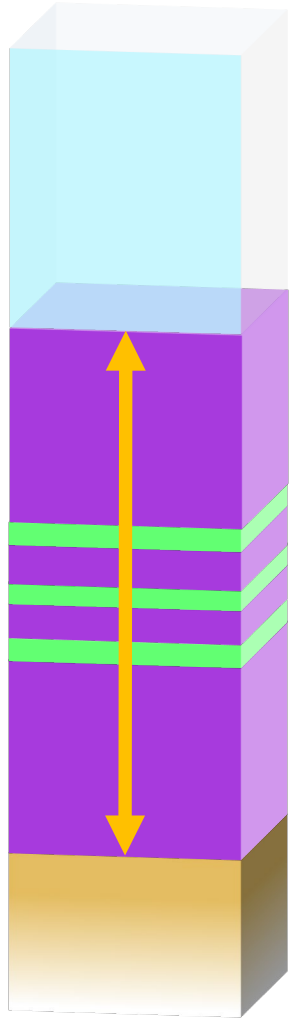
Lane and Hayne, IEEE Trans. Electron Devices **67**, 474 (2020).
Lane and Hayne, J. Phys. D: Appl. Phys. **54**, 35104 (2021).

Program and **erase** (≤2.5 V)

Erase (E) cycle: remove electrons from the floating gate
V_{CG-S} < -2.5 V





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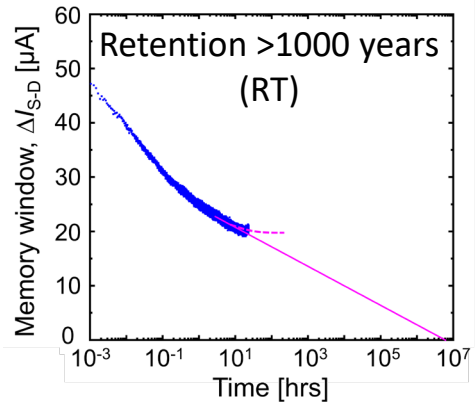
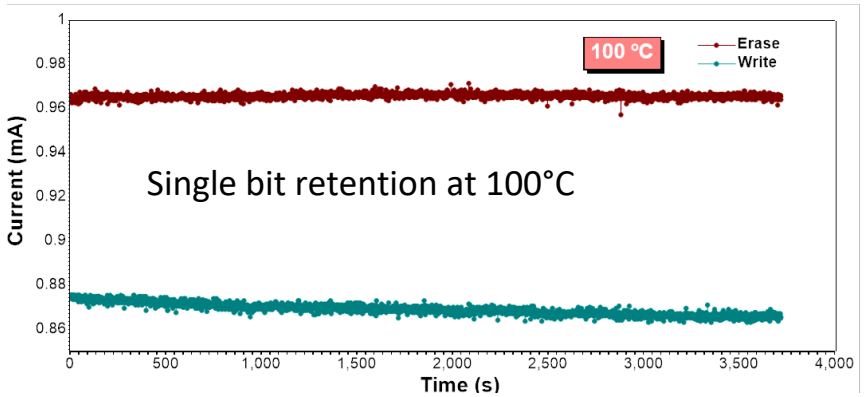
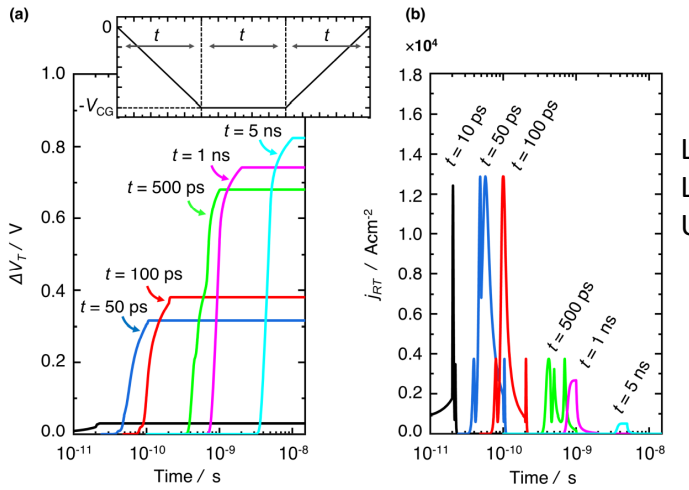
Key ULTRA**RAM**™ features



Hodgson *et al.*, Adv. Electron. Mater. 2101103 (2022)

- Charge-based memory, like DRAM, flash, SRAM (99% of market)
- Lowest switching energy (½CV^2: low capacitance, low voltage)
- Very robust charge storage
  (unaffected by material defects, TBRT variations, temperature, light…)
- Intrinsically fast (resonant tunnelling)





Lane, PhD Thesis, Lancaster University (2021)

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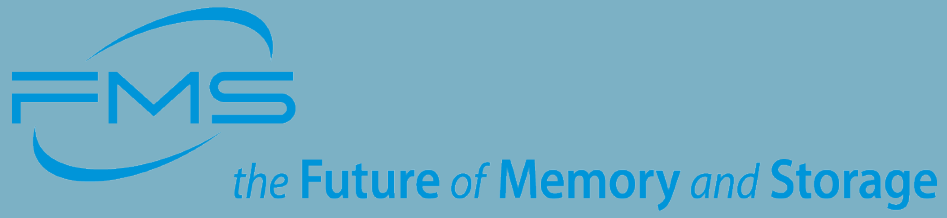
Progress and challenges



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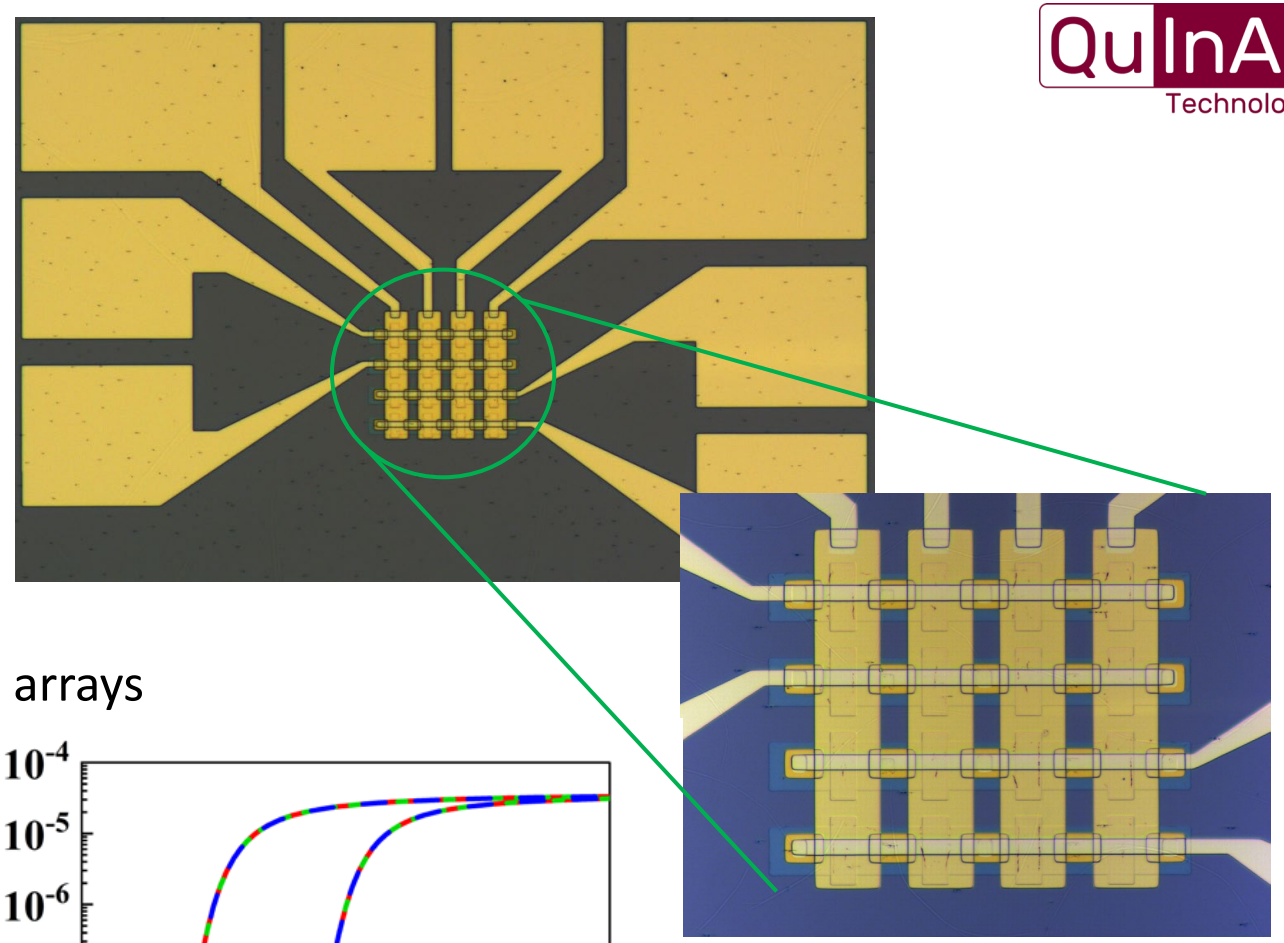
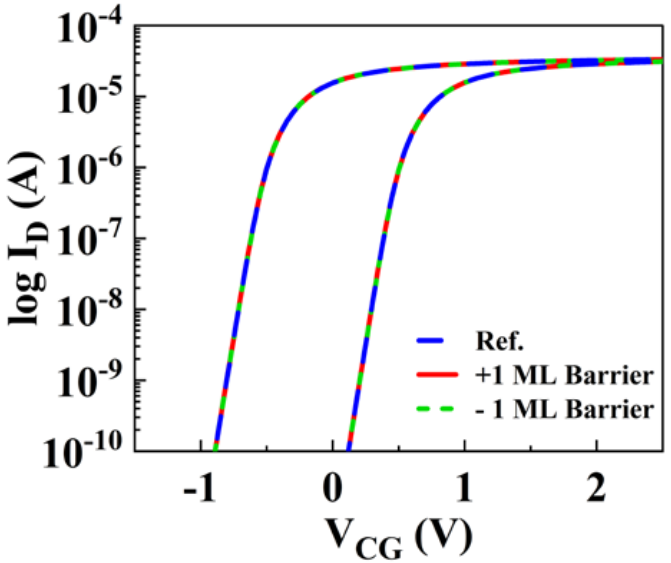
ULTRA**RAM**™ arrays



- Under active development
  - 4/16, 16/64 bare arrays
  - FEI logic for decoding (pat. pending)
  - Then 256, 256^2, 256^2 x 16, etc. decoded arrays
- Architecture (NOR-like) well understood
- Main challenge is 0/1 contrast ratio, which is << than the 10^5 predicted



Kumar *et al.*, submitted IEDM (2024)

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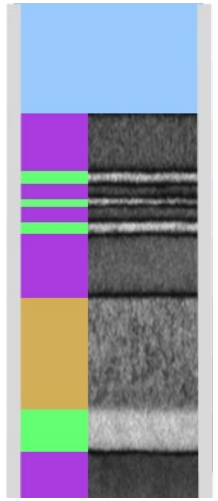
ULTRA**RAM**™ scaling



15 nm Al_2O_3 (ALD)

10 nm InAs **floating gate**

InAs/AlSb **TBRT**

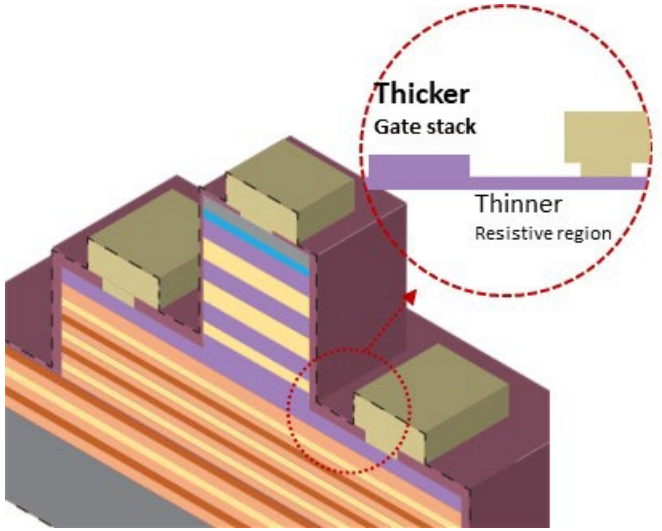
10 nm **n-InAs channel**

20 nm GaSb

8 nm AlSb barrier

Dry etching to the <10 nm InAs channel is challenging, and over-etching is inevitable

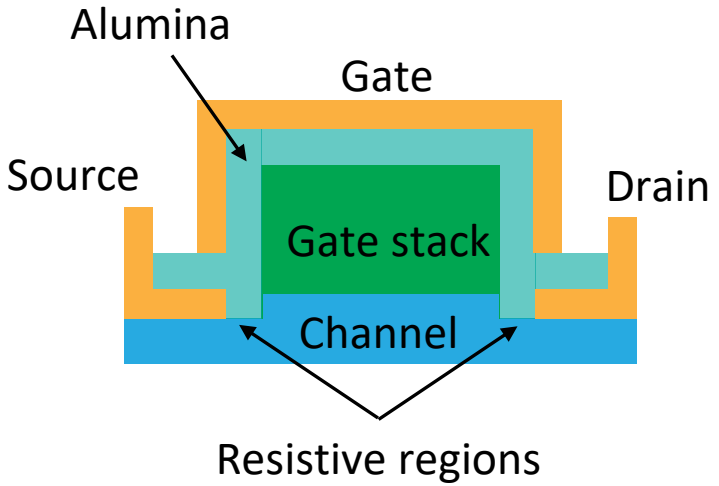
This creates a large parasitic resistance that dampens 0/1 readout contrast

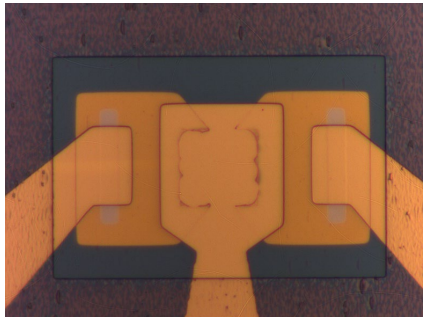


ULTRA**RAM**™ scaling

The solution is to minimise the distance between channel contacts and the gate stack by insulating with a thin layer

An overlapping gate contact can further enhance conductivity in this small region, for the target device only





Device fabrication using this patent-pending process is underway

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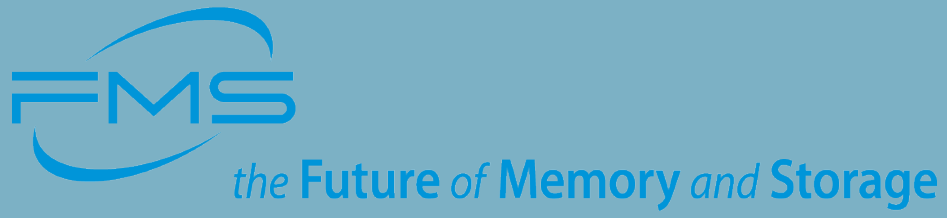
Prospects



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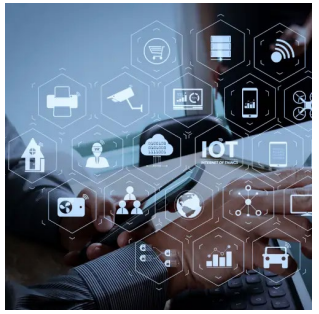
Beachhead ULTRA**RAM**™ markets

While the ambition is to compete with DRAM, we are identifying applications that take advantage of ULTRA**RAM**™'s remarkable properties

- Ultralow energy consumption
- Very robust data storage
- Operation at high and/or the lowest temperature

We are also developing In-ULTRA**RAM**™ computing for analogue MAC operations in AI



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