杭州电子科技大学
HANGZHOU DIANZI UNIVERSITY

Trends in Matching NVM Technology to the Right Application

Presenter

Jianjun Luo

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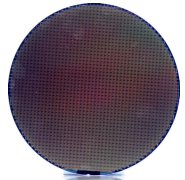

FMS

【BIO】

- Jianjun (Jerome) Luo is a professor at Hangzhou Dianzi University in China.
- I founded and served as Chairman of Sage Microelectronics, a company specializing in integrated circuits and solutions for digital storage and data security applications. Prior to establishing Sage Microelectronics, I was the Director of R&D at Initio Corporation in San Jose and Eastcom in China. With over 30 years of experience in communication and storage IC design, I brought extensive expertise to my roles.
- I earned a PhD in semiconductor technology from Zhejiang University in China, a Master's in Microelectronics from the Hangzhou Institute of Electronics Engineering, and a Bachelor's in Electronics Engineering from Shanghai Jiaotong University.
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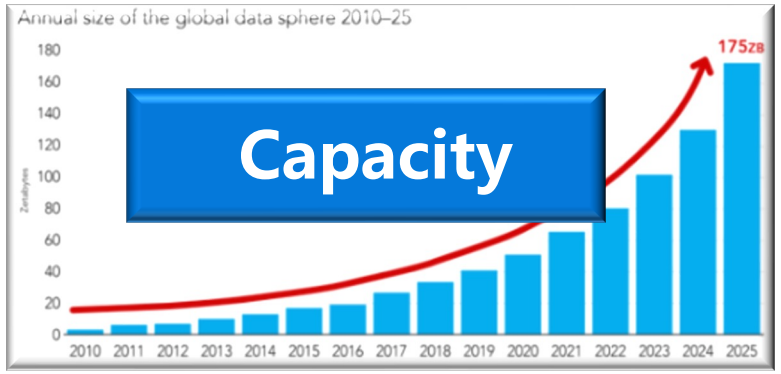
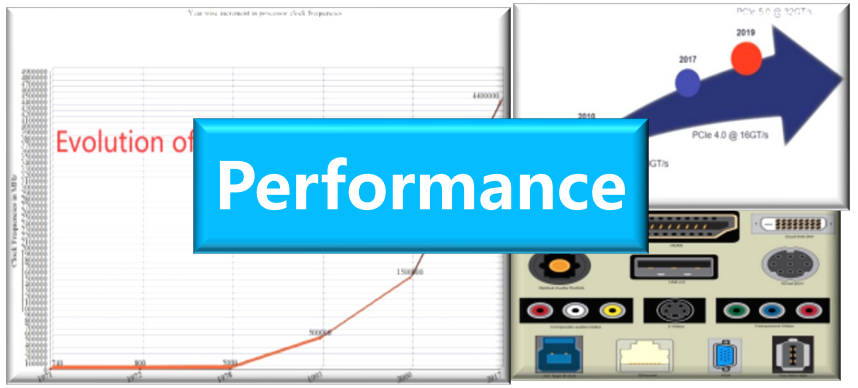
Data Storage facing Challenges

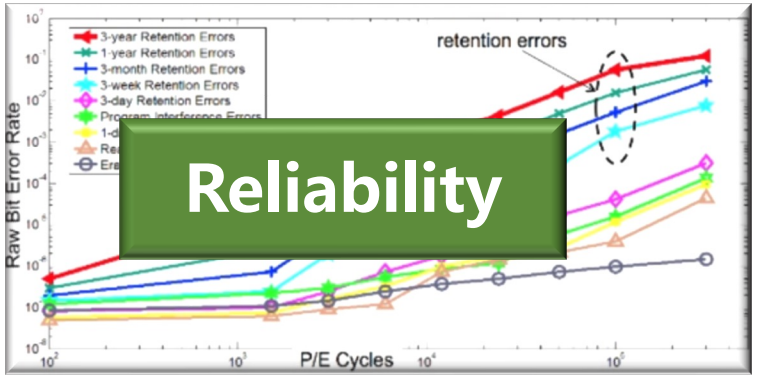
① Data Volume ➔ Exploring



② High Performance Computing ➔ Extreme faster

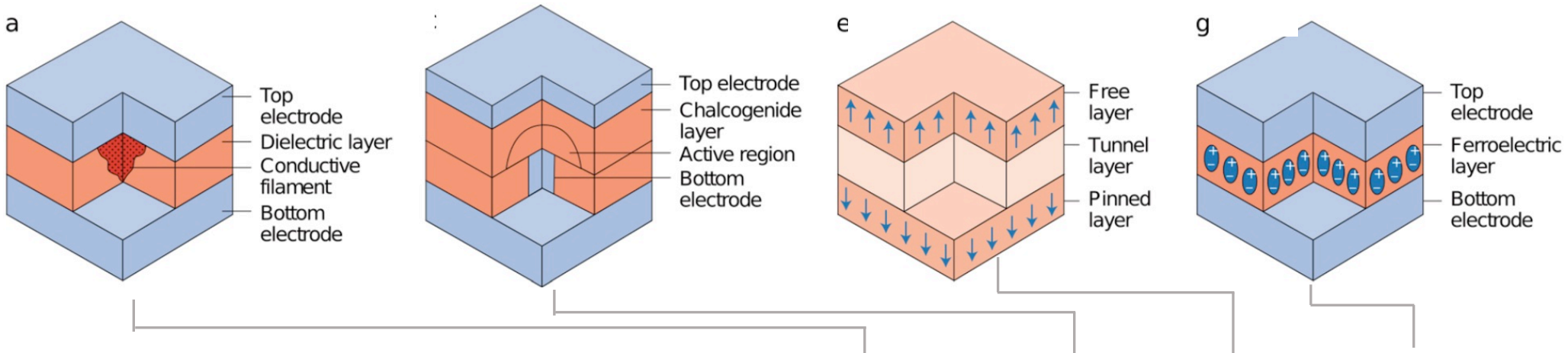


③ High Desnity vs. High Reliability ➔ Conflicting



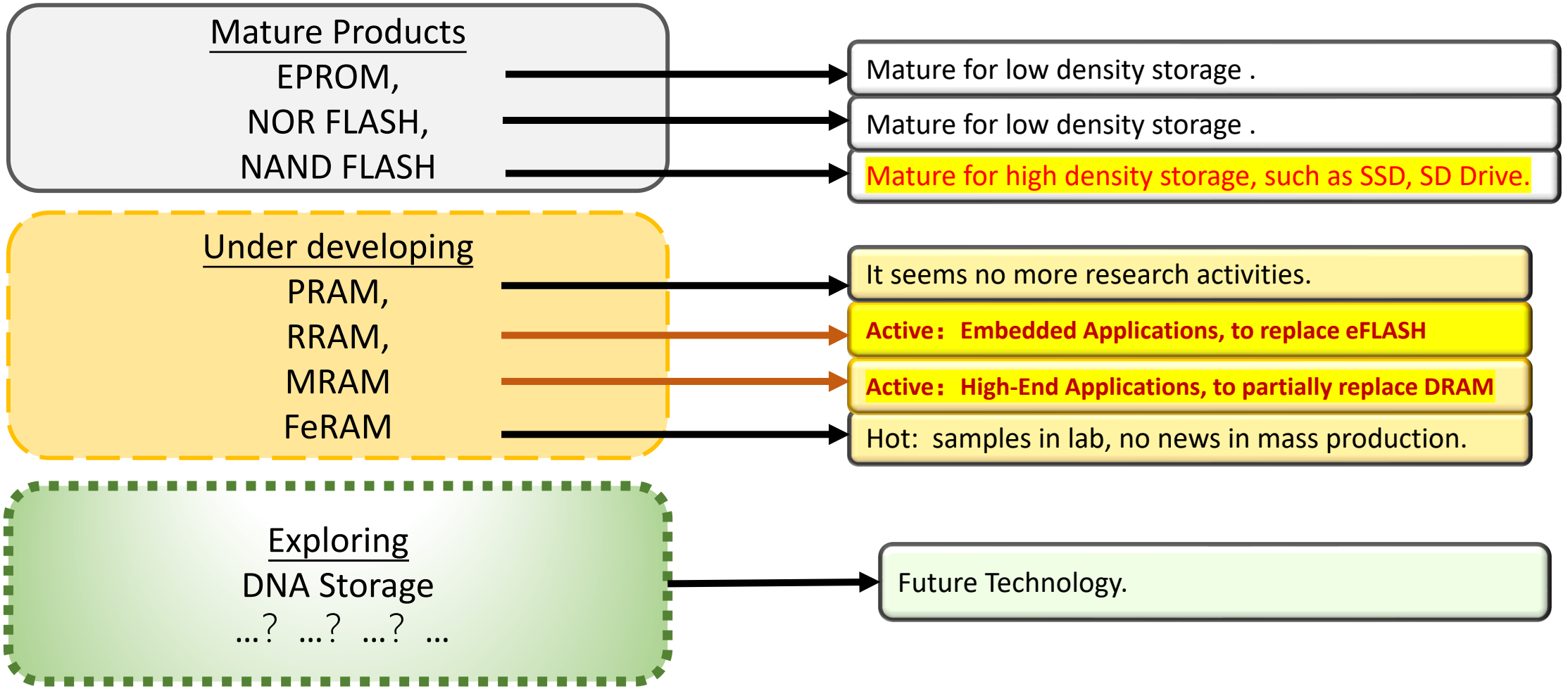
④ Data Encryption/Decryption ➔ Emerging problems

Emerging Memories



	SRAM	eDRAM	eFlash	RRAM	PCM	MRAM	FeRAM
Endurance (cycles)	Unlimited	Unlimited	10^5	10^4~10^6	10^9	10^{10}~10^{14}	10^{14}
Read/write speed(ns)	<1	1-2	10/10^3	10-100	10/100	1-20	30
Density	Low	Medium	Medium	High	High	Medium	Low
Write power	Medium	High	High	Medium	High	Medium	Medium
Standby Power	High	Medium	Low	Low	Low	Low	Low

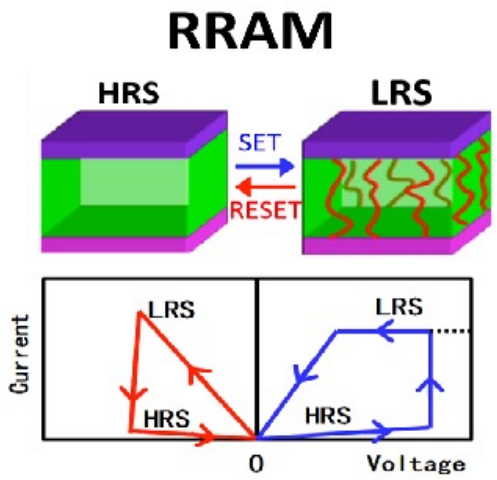
Investigation Summary

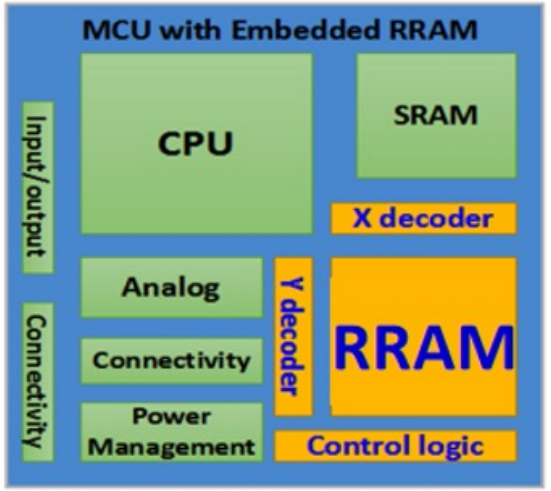


Practicing in RRAM projects

- After 28nm nodes, RRAM is one of the main embedded memory solutions in next-gen SOC.
- Many manufacturers have announced mass production.

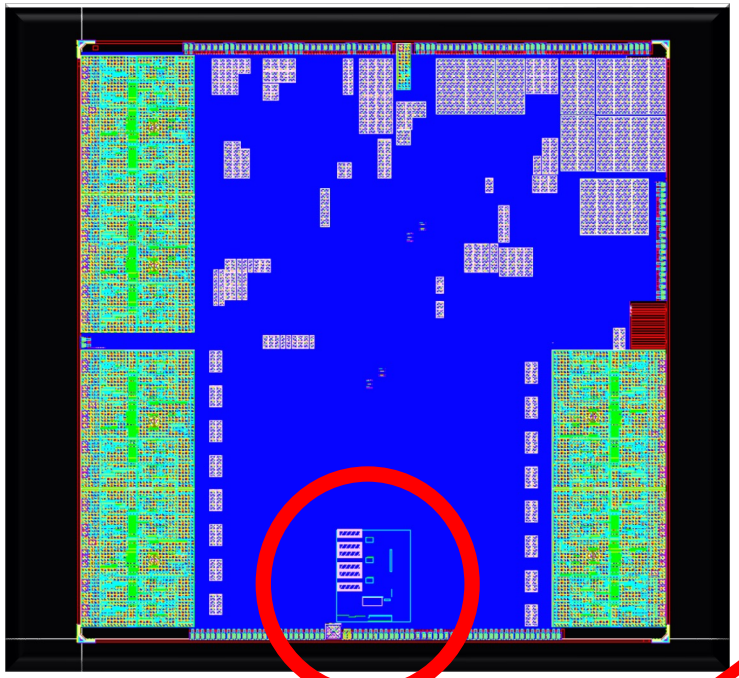
Outstanding advantages in embedded memory and neuromorphic computing

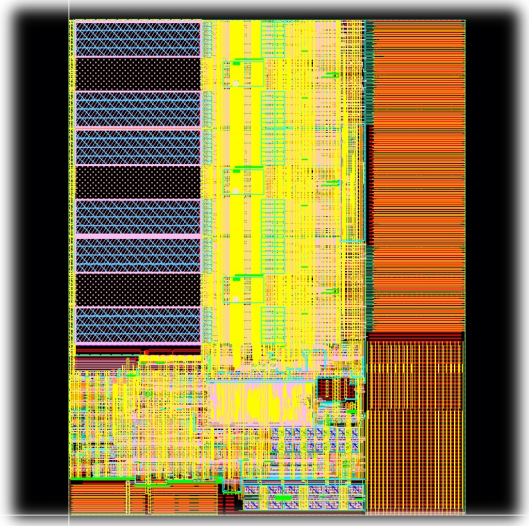




Tech nodes	55nm / 40nm / 28nm / 22nm
Intel	e-Flash → RRAM, MRAM
TSMC	e-Flash → RRAM, MRAM
Samsung	e-Flash → MRAM
Global Foundary	e-Flash → MRAM
UMC	e-Flash → RRAM

Practicing in RRAM projects





SOC with Embedded RRAM
(PCIE-SAS/SATA HBA Controller)

- **1Mbit embedded RRAM By 28nm Process**

Only 2 additional mask layers based on Generic Logic Process

Practicing in RRAM projects

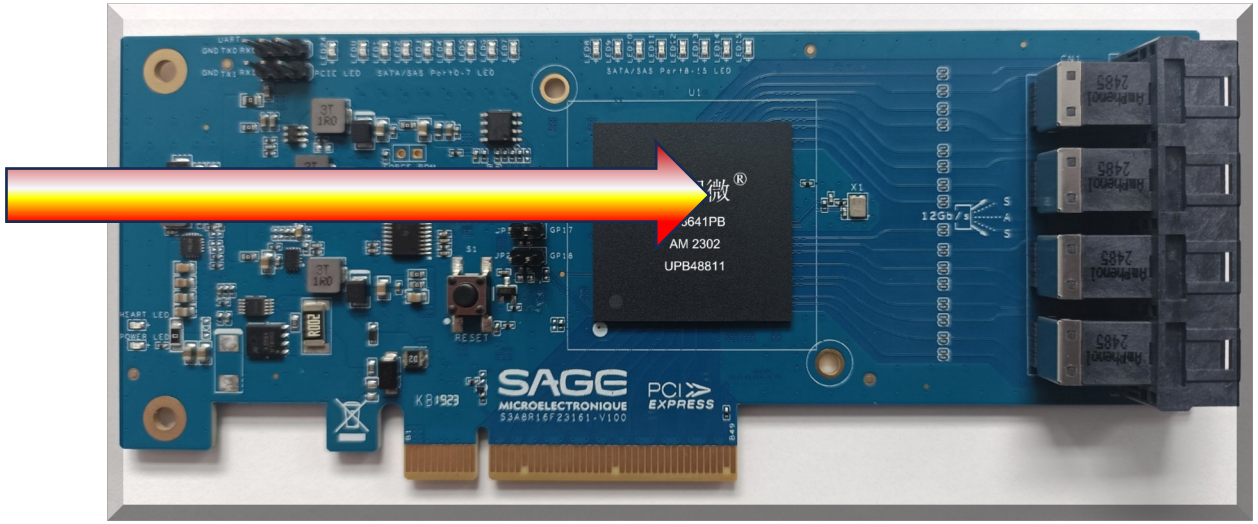
PCIE-SAS/SATA HBA Card in Mass Production

RRAM in Mass Production

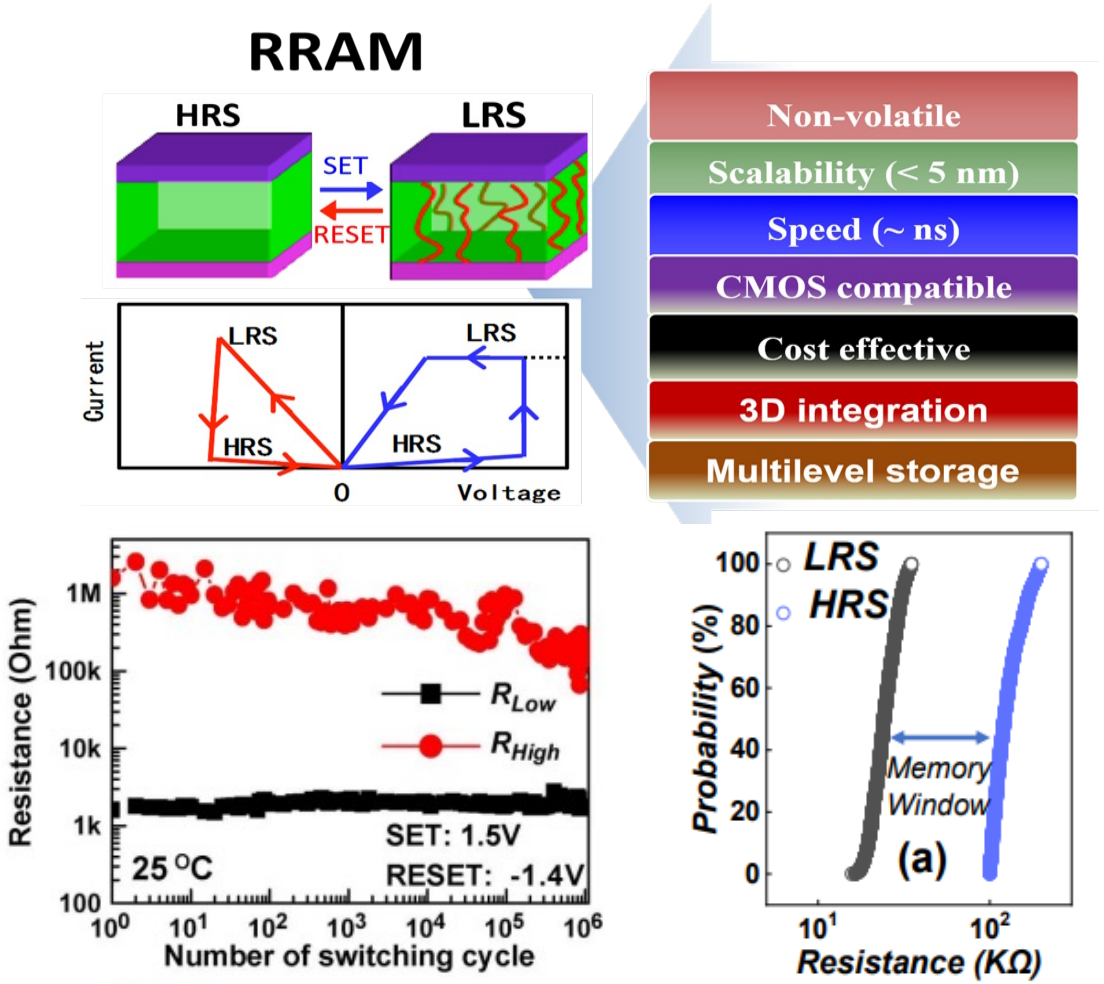
Interface: PCIe Gen3.0 x 8Lane
SATA 3.0 x 16 Port
performance: 800K IOPS (4K RR) ; 6500MB/s (1MB SR)
Host protocol : AHCI 1.3.1
Embedded Encryption: AES/SM4
OS: Win10, UBUNTU Linux,
CentOS, KylinOS, UOS
Connector: 4x4 SFF-8643
Formfactor: 167.65 mm x 68.90 mm
Power Consumption: 3.5W

RRAM 1Mbit

- Fireware code
- Configuration parameters
- Encryption/Decryption Keys

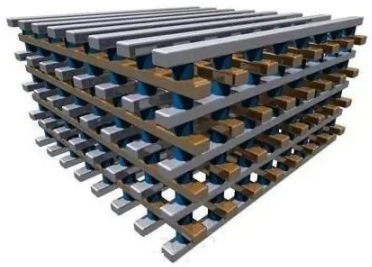


RRAM Challenges



Challenges：

- Current on/off ratio is still small
- The effect of IR drop needed to be reduced
- Switch voltage is pretty high
- Uniformity and Reliability needed to be improved
- Optimizing power consumption and retention simultaneously.
- Universal selector for ultra-high density 3D integration



Practicing in MRAM projects

Enterprise SSD with MRAM

High Reliability for sudden power failure

②

DRAM

①

PCIE/SAS
Dual-Port

Enterprise SSD with MRAM

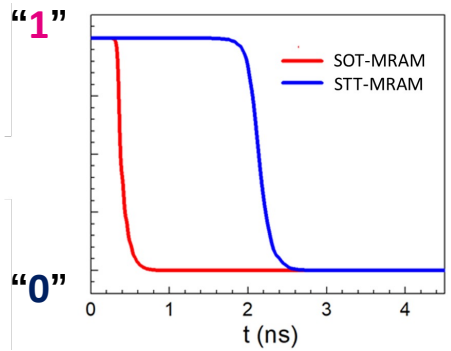
High Reliability for sudden power failure

Flash
Flash
Flash
Flash
Flash
Flash
Flash
Flash

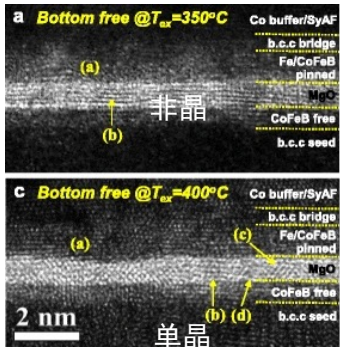
③

MRAM

Challenge of SOT-MRAM

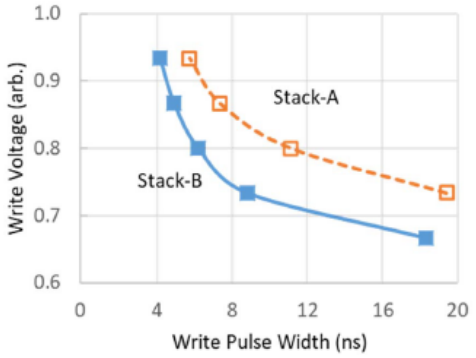


- **Theoretical predicted Fast write speed of SOT-MRAM**

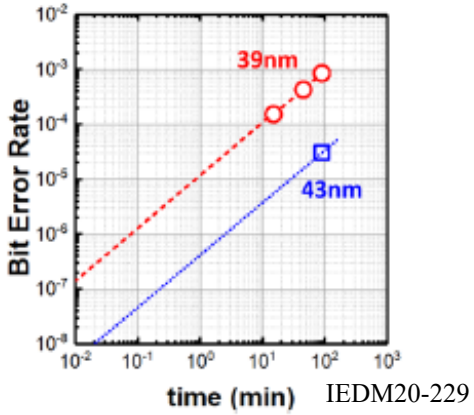


- **Accurate and clear boundary of different Crystal plane and crystal orientation**

Nanoscale Res Lett
11, 433 (2016)



- **Reduced write latency and power consumption** IEDM20-229



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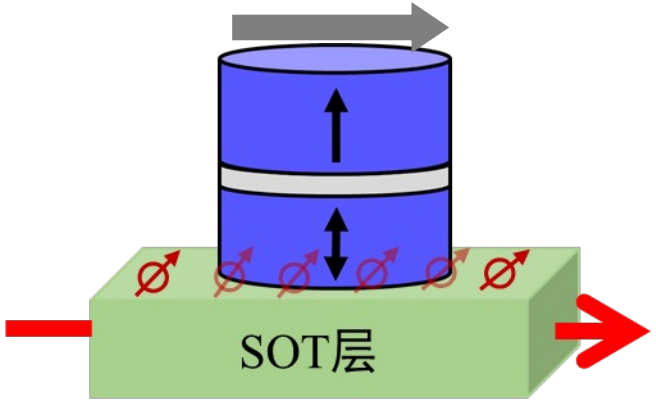
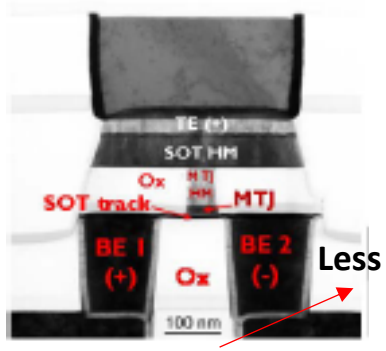
- **Fail rate during write cycle**



- **Field free switching of SOT-MRAM**



Less than 1nm

- **High resolution etch**

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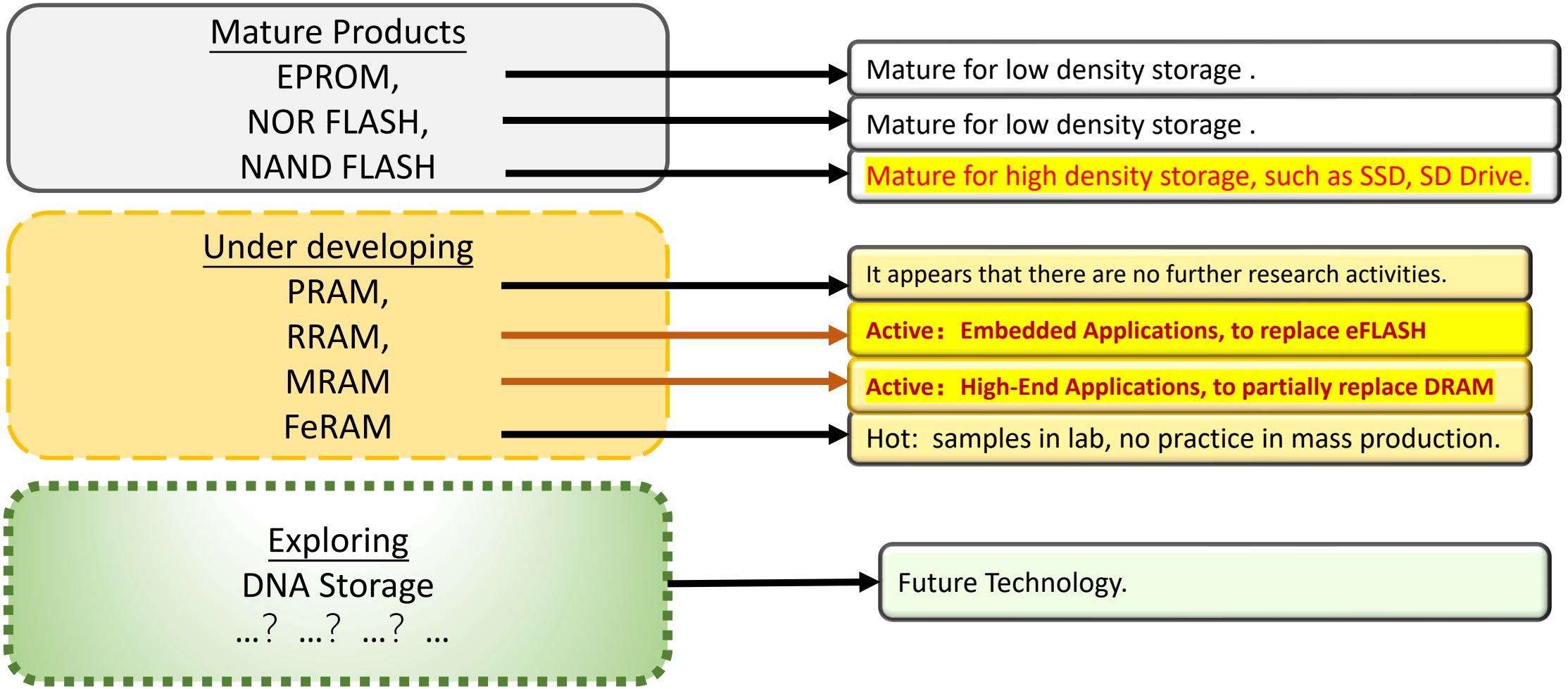
Investigation Summary



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Thanks