the Future of Memory and Storage

How UCIe Reduces the Barrier to Entry in Chiplet Design

UCIC-102-1: UCIe Technology Opportunities and Benefits: FMS 2024

Mayank Bhatnagar, Product Marketing Director, Cadence

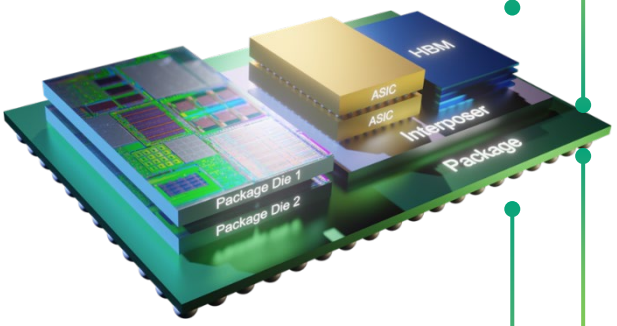
August 6, 2024

cadence

Agenda

- Why chiplet-based designs are the future
- System-in-package designs with and without a standard chiplet interface
- Business case for increasingly expensive custom silicon
- How chiplet ecosystem lowers barrier to entry
- Comparison of various interface standards
- Outlook for adoption of standards

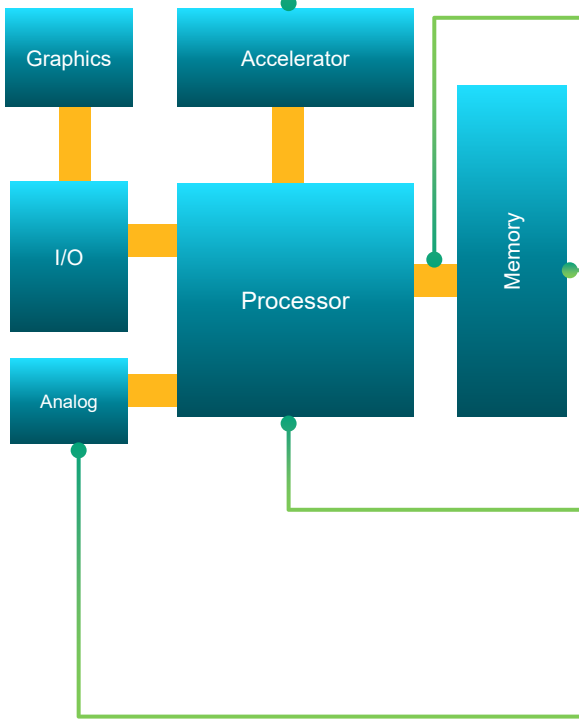
Why Chiplets?



- Reticle size and yield issue
- Pick right combination of nodes (optimize transistor cost)
- Take advantage of package technology improvements
- Modular and scalable design
- Optimize for performance, power, and cost

Pre-Standardization Era

Without standard chiplet interface



All chiplets designed in-house/same project

Need to design custom interface for each process

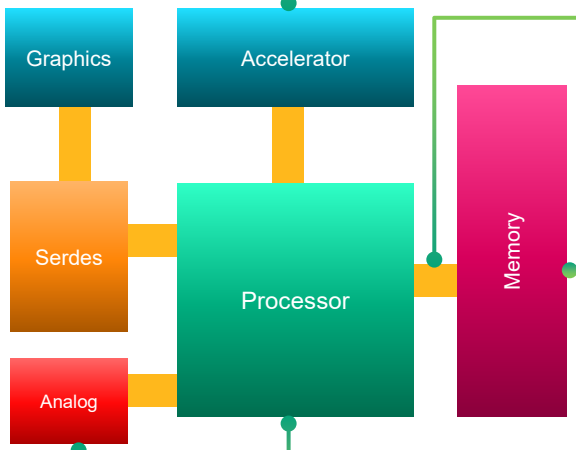
Design of non-differentiating chiplets takes resources

Quality limited by the availability of expertise in-house

Significant investment of design power and time

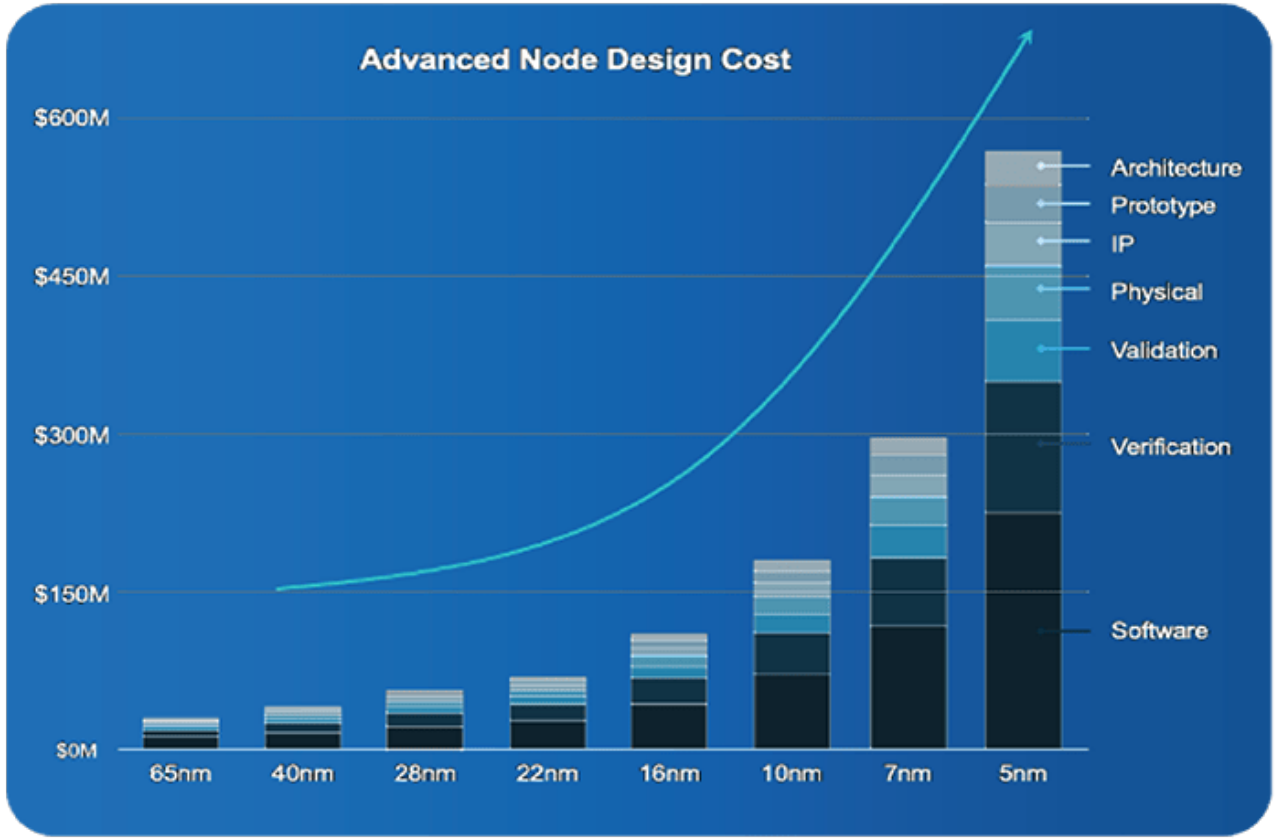
Post-Standardization Paradigm Shift

With a widely adopted standard chiplet interface



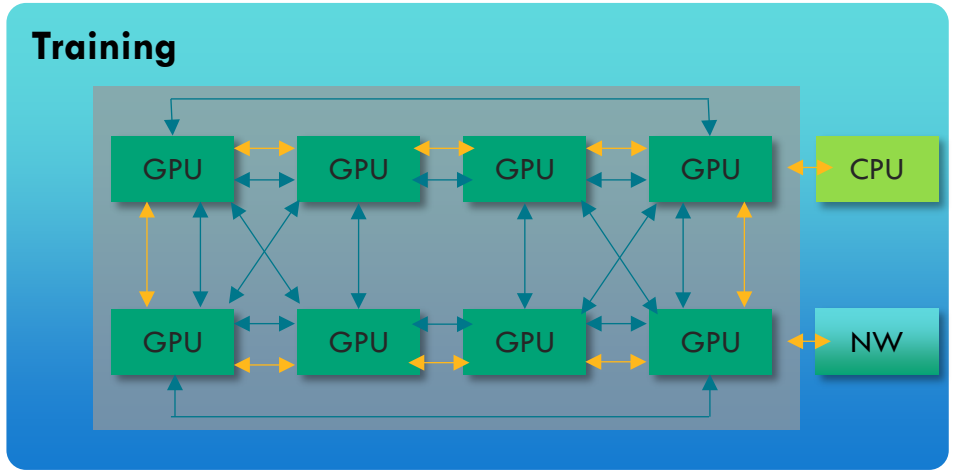
- Only core differentiating chiplets designed
- Standard pre-validated interfaces with a robust standard
- Buy/reuse proven chiplets
- More options for best-quality chiplets
- Minimize resources used, speed up time to market

Rising Cost of Large Designs



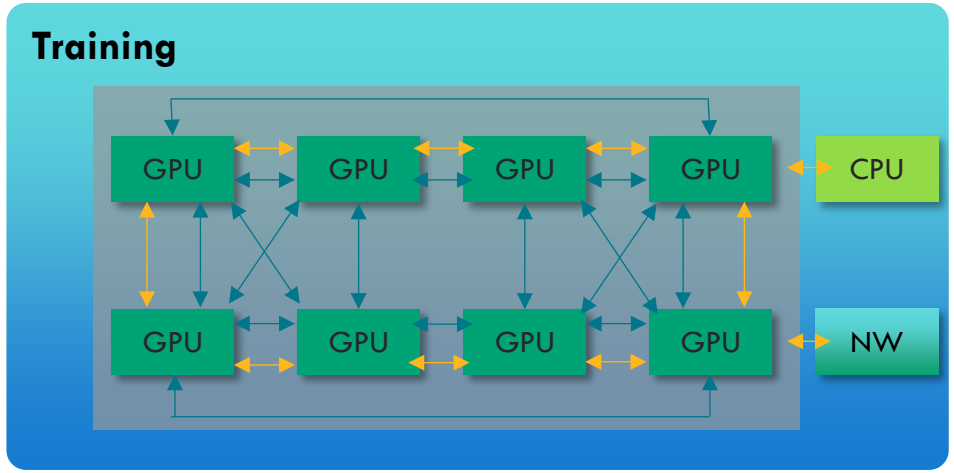
Source: IBS Global Semiconductor Industry Service Report: Design Activities and Strategic Implications, July 2018

Increasingly Custom Silicon to Meet AI Needs



CPU GPU Mem NVM NW

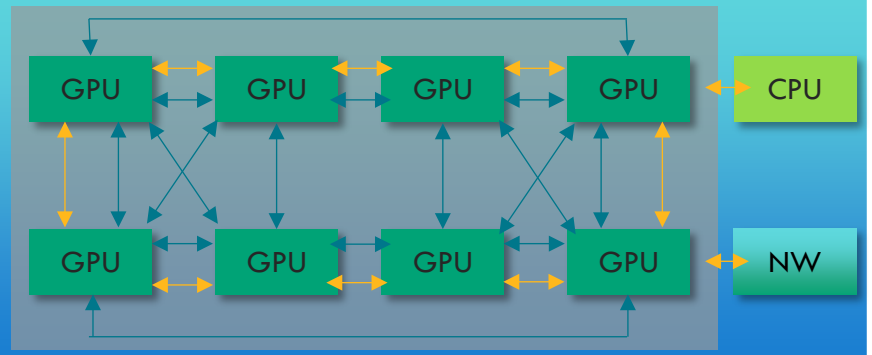
Increasingly Custom Silicon to Meet AI Needs



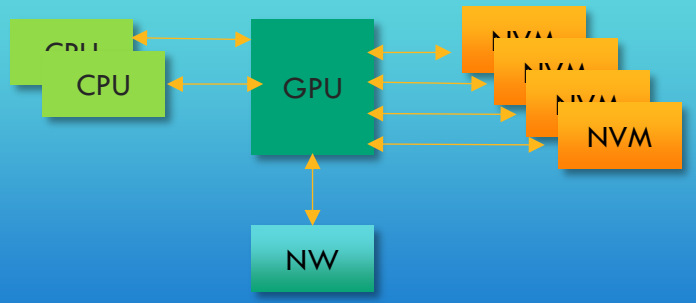
CPU GPU Mem NVM NW

Increasingly Custom Silicon to Meet AI Needs

Training



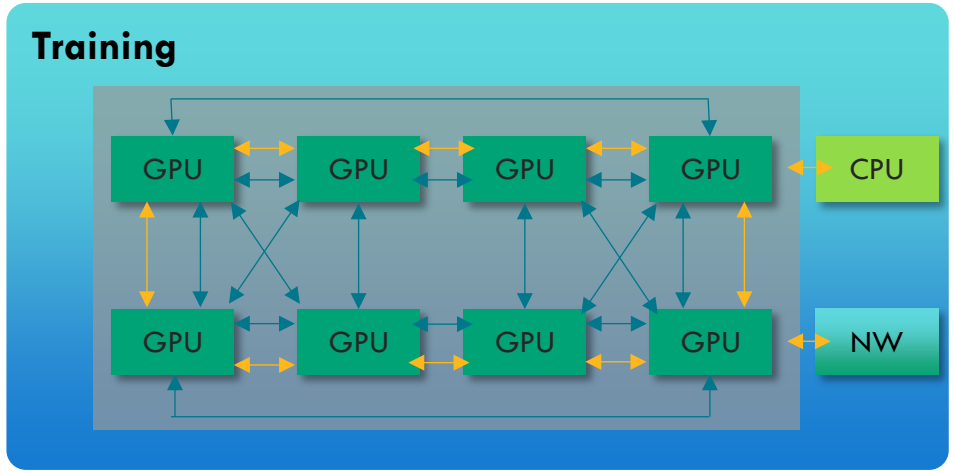
Data Mining

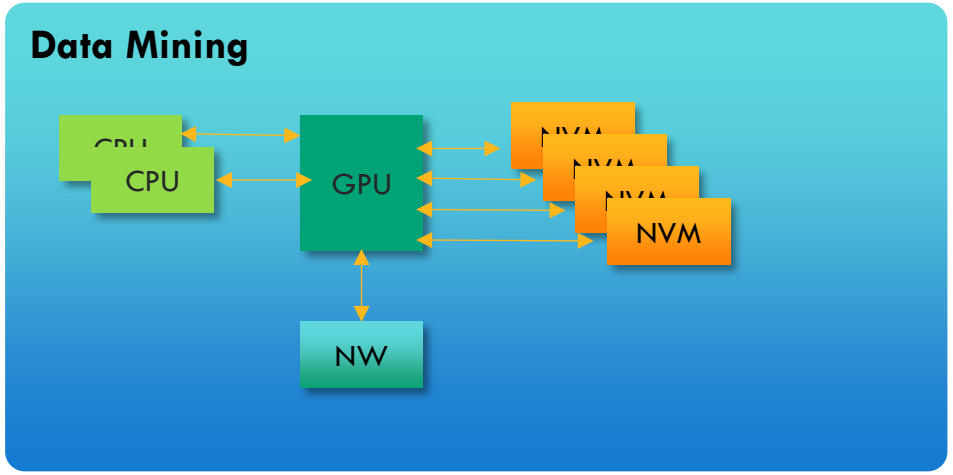


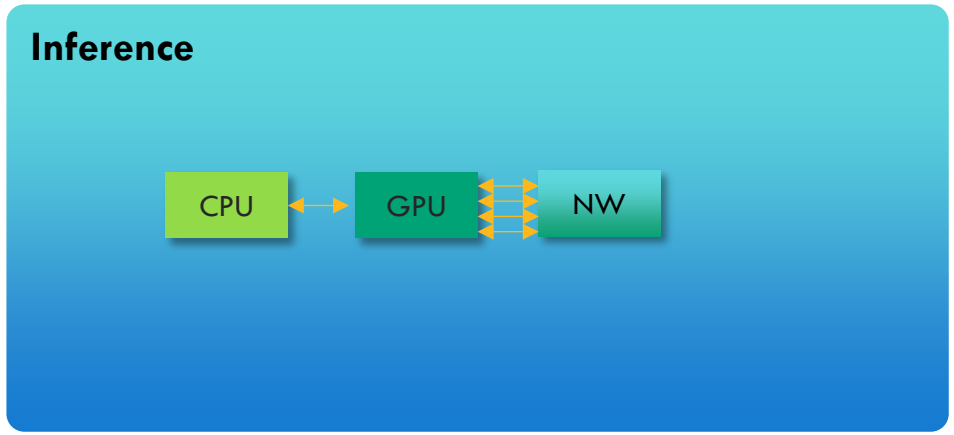
Inference

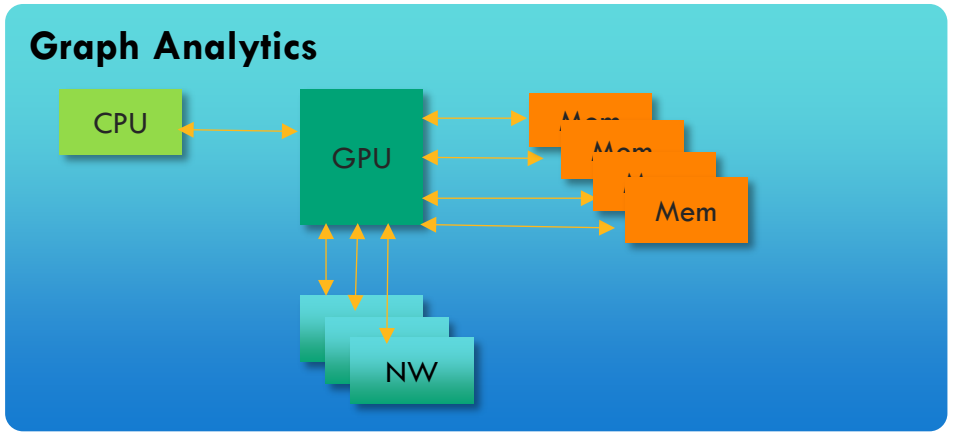
CPU GPU Mem NVM NW

Increasingly Custom Silicon to Meet AI Needs





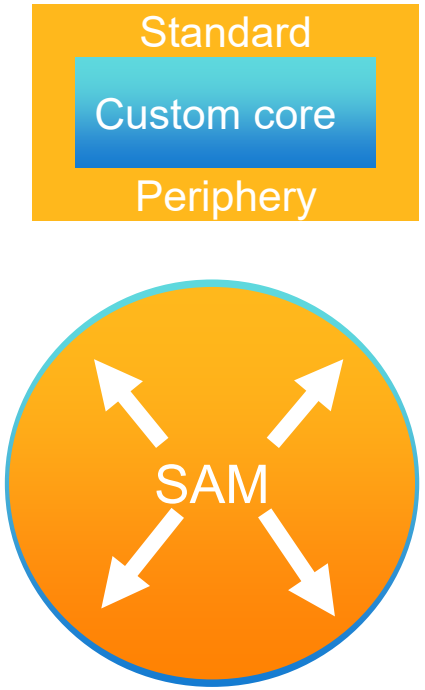




CPU GPU Mem NVM NW

Chiplet Ecosystem for Chiplet Designers: Use of Standard Interfaces

Internal (now) and external (long term) ecosystems



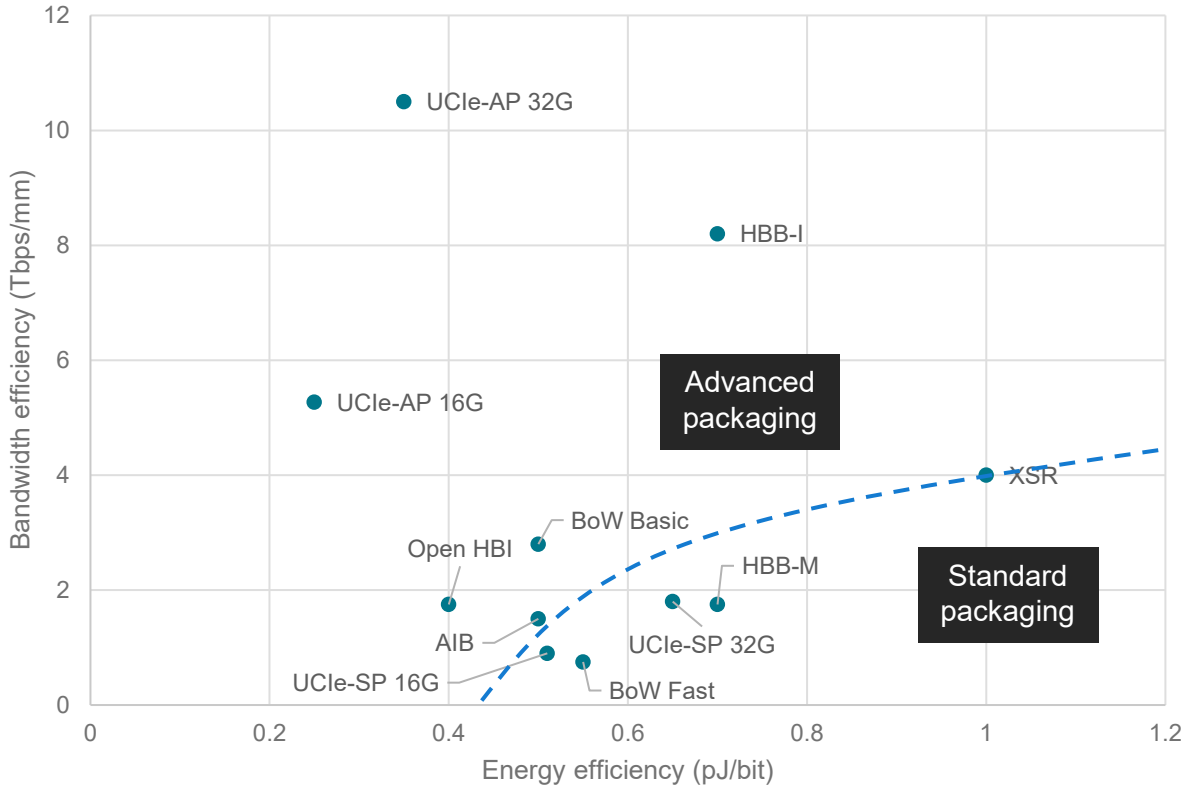
Build chiplet with highly customized core

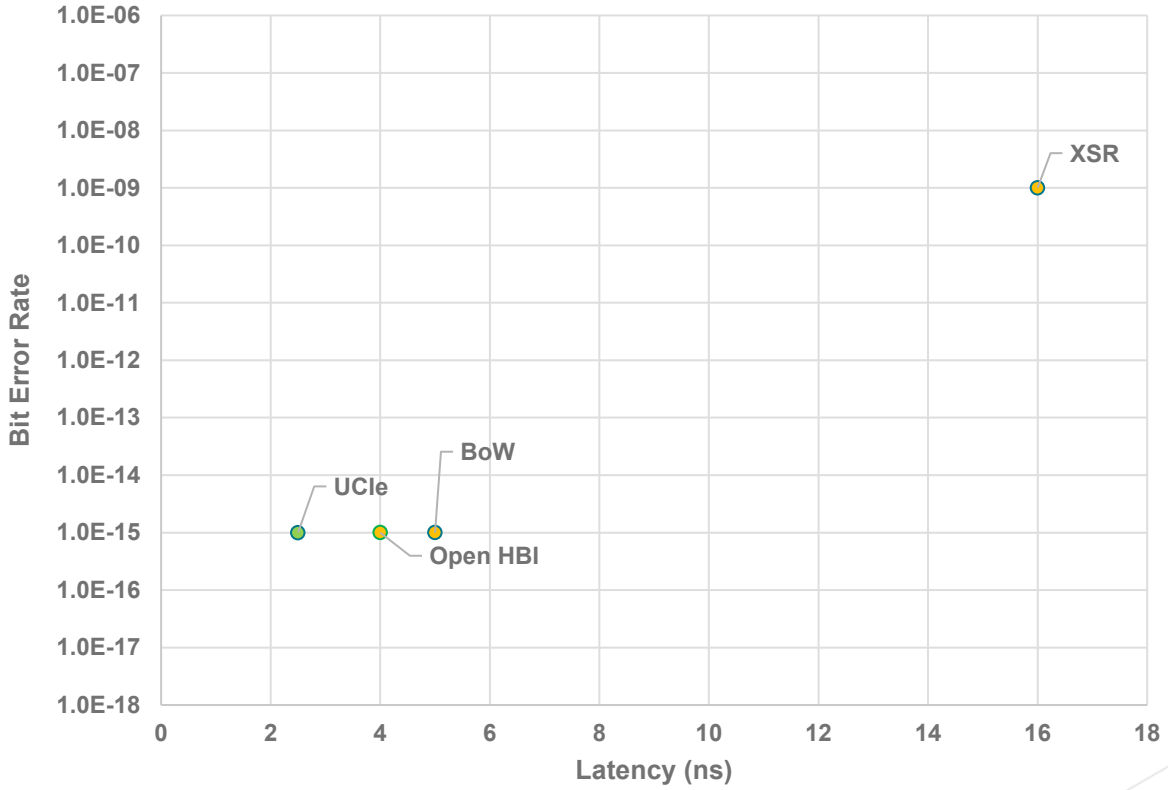
Surround core with standard periphery, maximize serviceable market

Comprehensive standard for interface and to account for boundary effects

Comparative Analysis of Chiplet Interconnect Standards

Physical layer

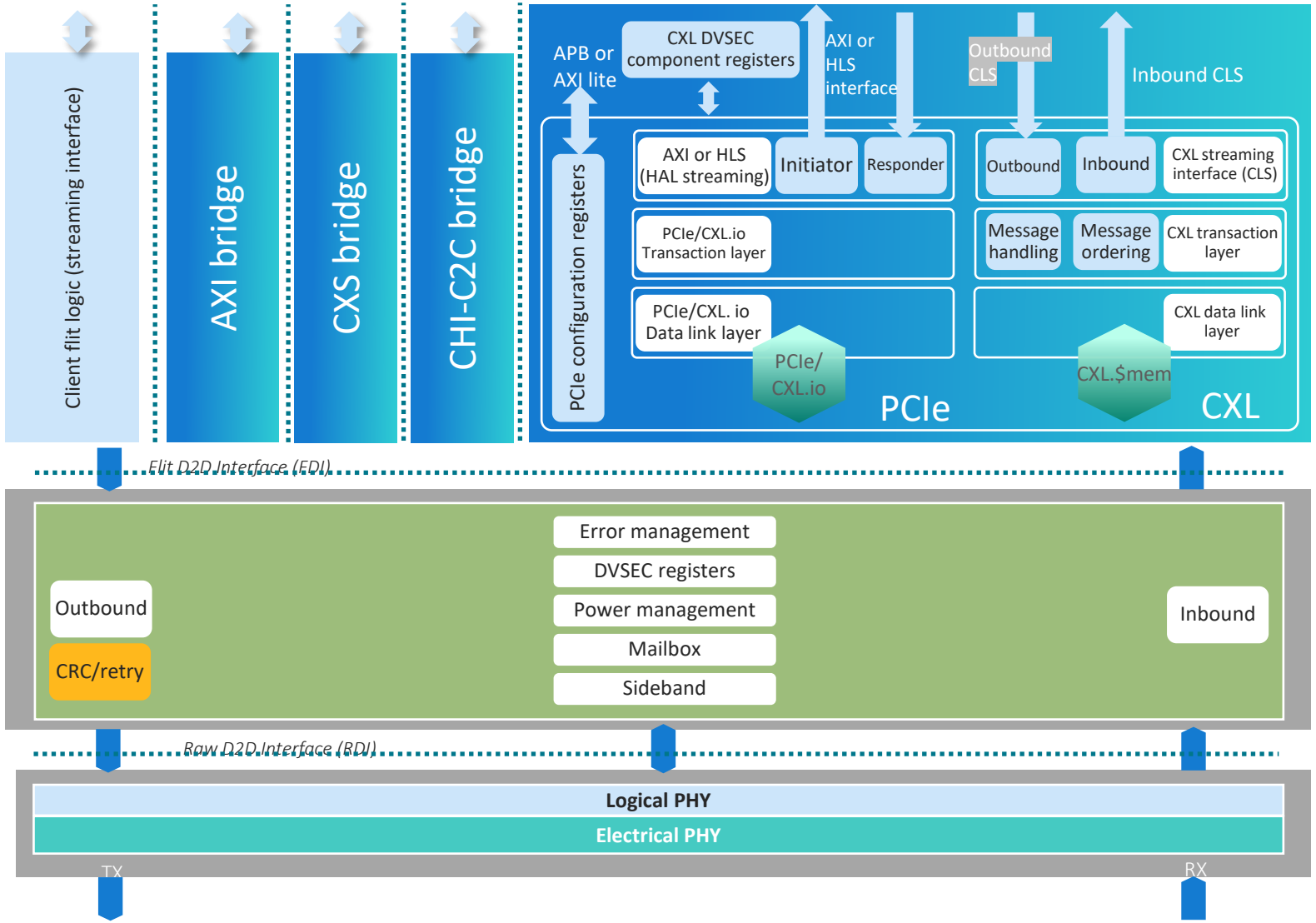




Source: Cheolmin Park, "UCIe evolution and memory integration technology evolution for supercomputers", ISC-HPC 2023
Open Compute Project Open Domain-Specific Architecture comparison

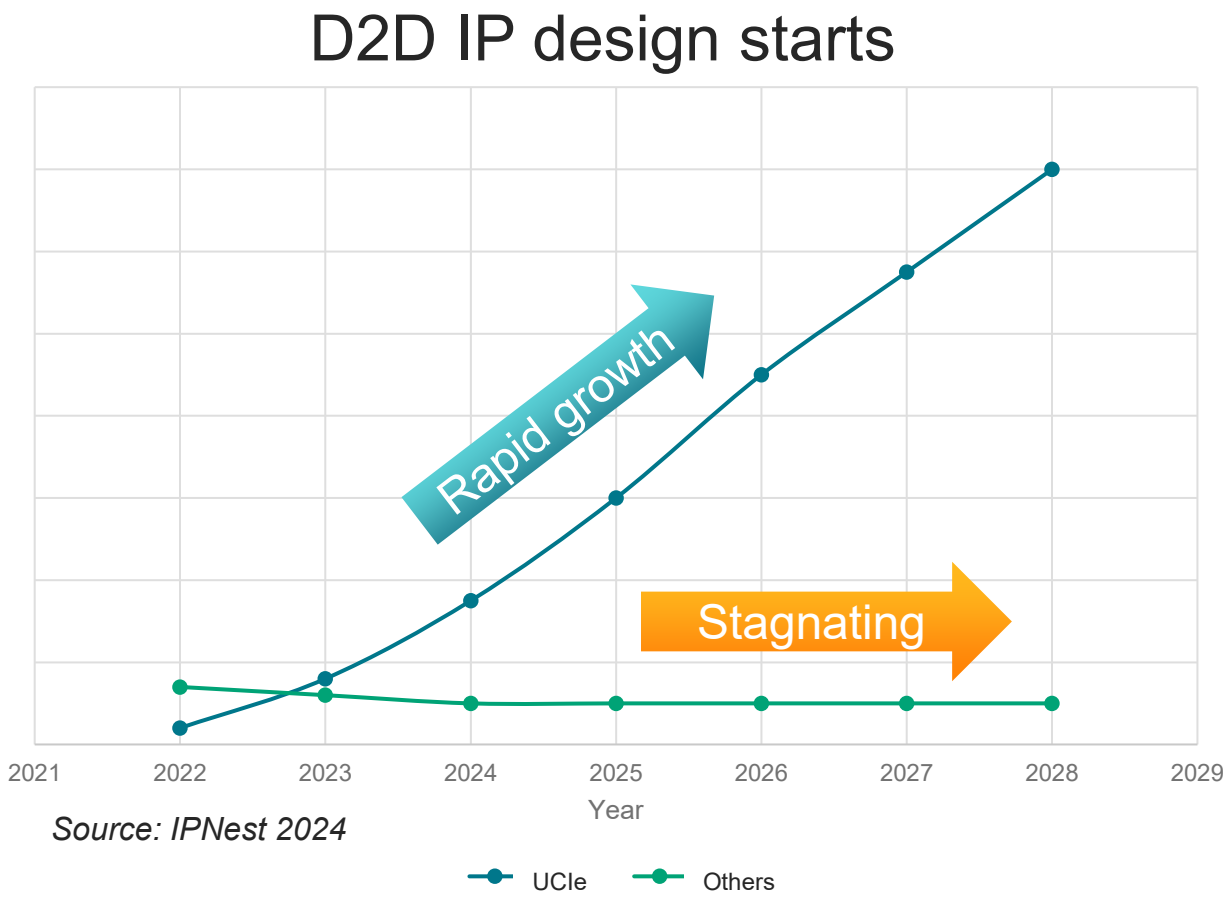
UCIe – A Subsystem Solution

Protocol connectivity



- Well-defined protocol layer
- Streaming/bridges for disaggregation
- PCIe and CXL for aggregation

Outlook on Standard Adoptions



Source: IPNest 2024

D2D interconnects show signs of coalescing around UCIe™

Interoperability will be a key factor in adoption

Rapid adoption of a common standard will unlock chiplet reuse

Summary

- Chiplets key to remaining profitable in semiconductor design
- Standardization can yield significant benefits
- Custom silicon needs chiplet ecosystem: internal and external
- Standardization of periphery will make boutique chiplet design possible
- UCIe™ has the best technical metrics of all open standards
- UCIe is gaining traction due to metrics and wide industry support