High Performance Disaggregated Systems through UCIe Interconnects and Chiplets

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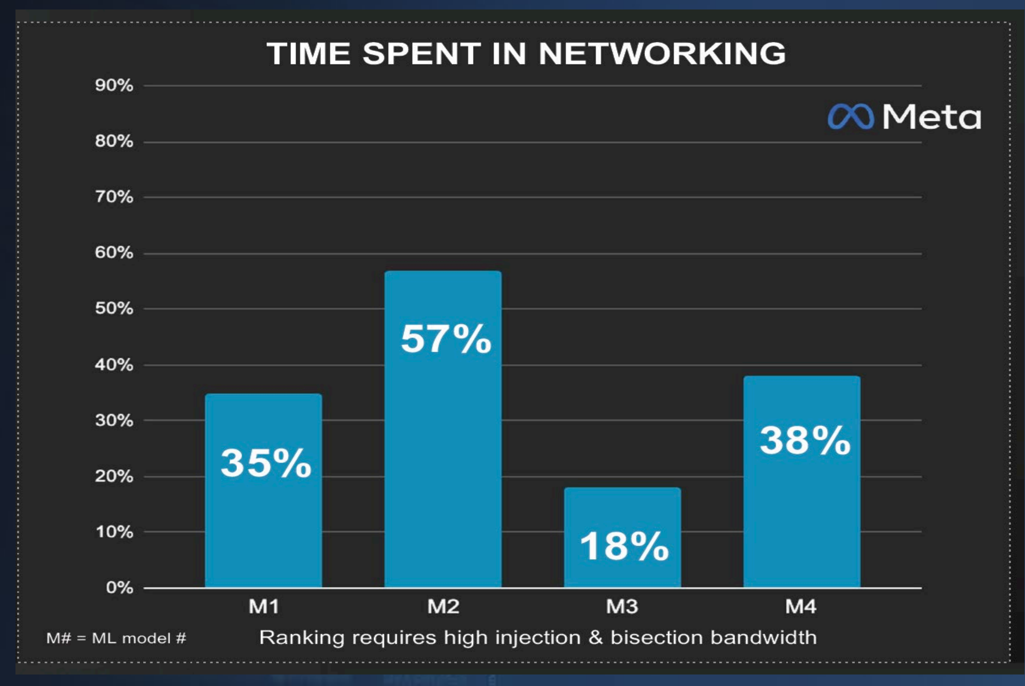
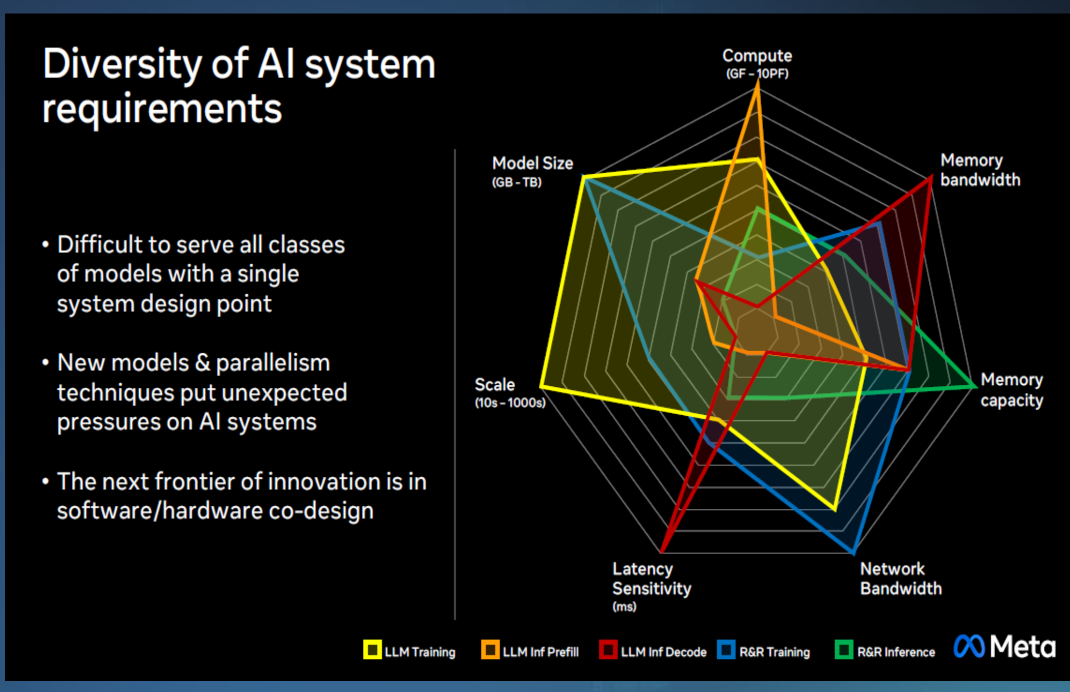
the Future of Memory and Storage

Deploying AI at Scale - Data Centre Challenges

Connectivity



Custom Compute



Source AI Summit : "Leading with Open" Meta

AI requires dedicated hardware with maximum communication bandwidth

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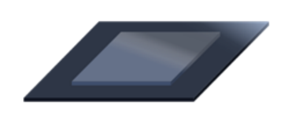
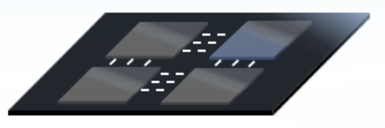
Chiplets - Ushering a New Era of Semiconductors

The New Chiplet Design Paradigm

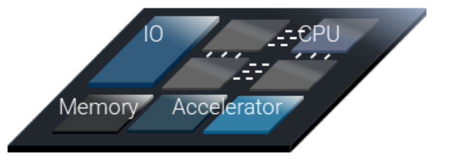
Chiplets rely on a fabric of dense high-speed die-to-die interconnect

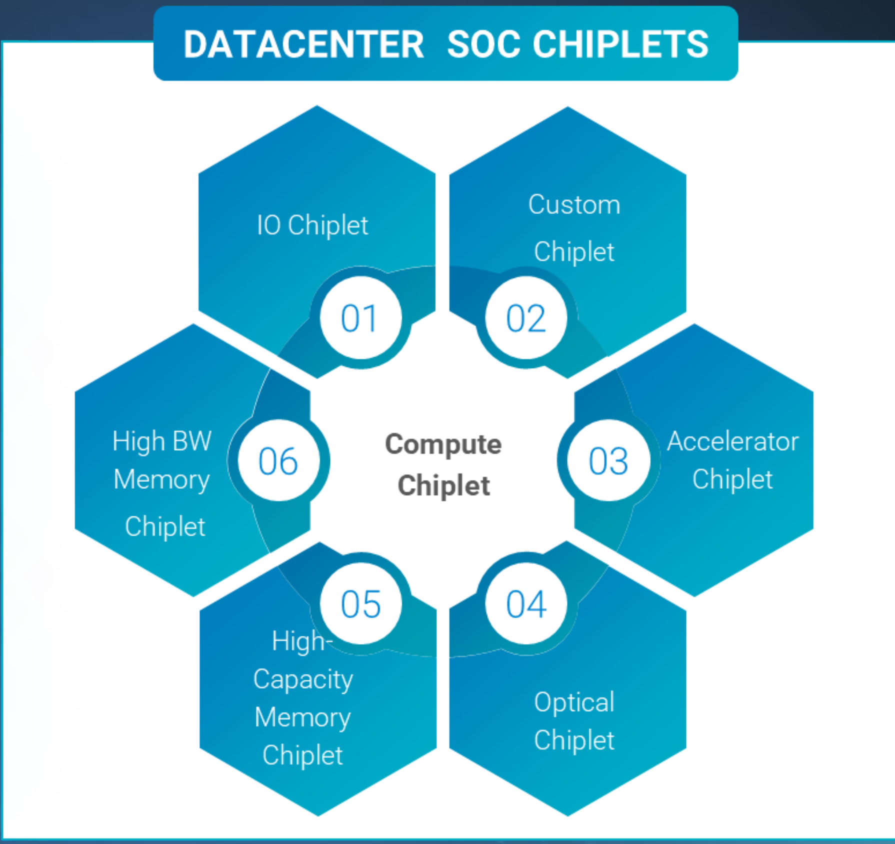


Wide acceptance of the Universal Chiplet Interconnect Express[1] (UCIe™) standard in 2022 to accelerate and democratize the chiplet ecosystem



IC design and package optimizations are the future for advanced compute semiconductors





[1] https://www.uciexpress.org/

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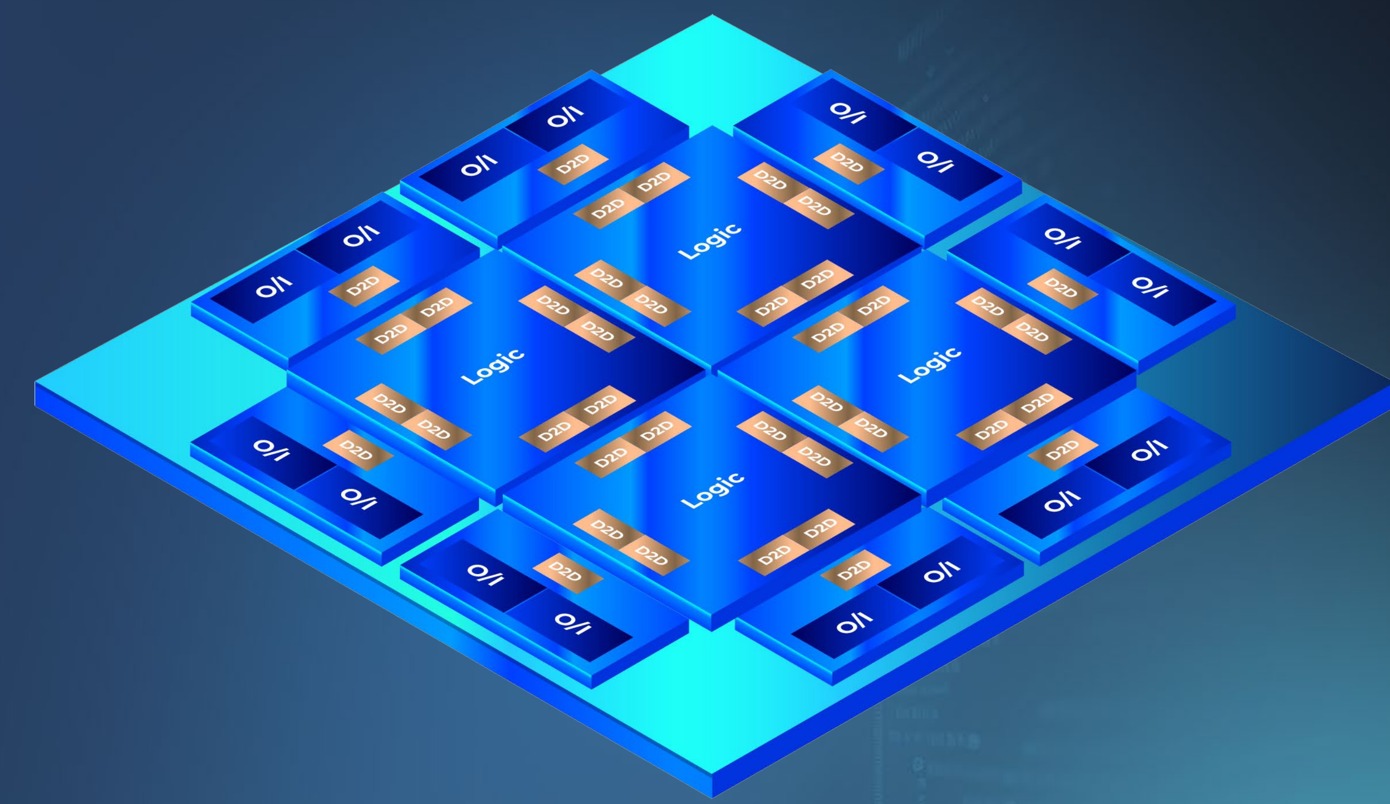
Chiplets: Accelerating the Adoption of Hardware Upgrades

- Reduced design time
- Reduced risk
- Composability



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Full AI Connectivity Suite Needed for Designing at Scale

Front End: Ethernet

Peripheral interconnects PCIe/CXL

CPU

Internal Links Custom

xPU

xPU

HBM

Back End: Ethernet or PCIe based

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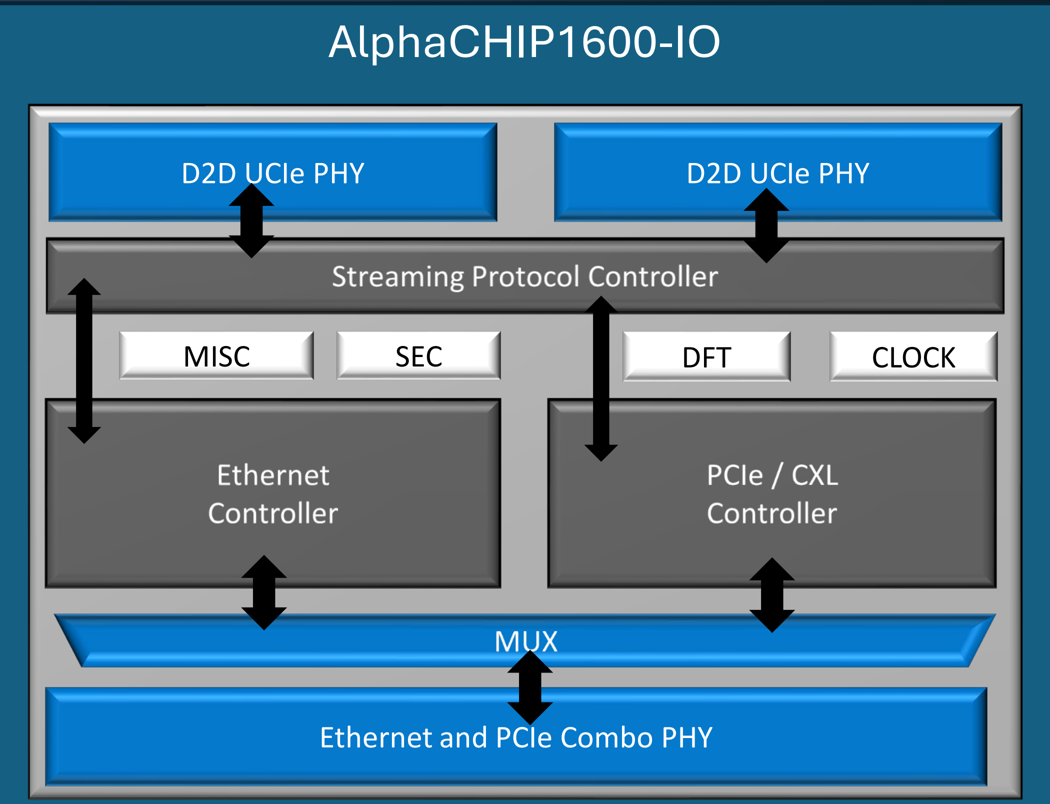
Industry First, Multi-Protocol I/O Connectivity Chiplet

- AlphaCHIP1600-IO
  - Reconfigurable Multi-Standard 112G SerDes I/O
  - UCIe Compliant ver1.1 D2D interconnect
  - Integrated protocol controllers, security IP and UCIe PHY, and Controller IP that enables up to 1.6T of throughput at MR, XLR, and PCIe/CXL reach.



Application

- Medium Reach Optical Driver Chiplet
- Extra Long Reach Ethernet Chiplet
- Combo PCIe/CXL/Ethernet Chiplet
- 1.6T high-speed I/O Chiplet

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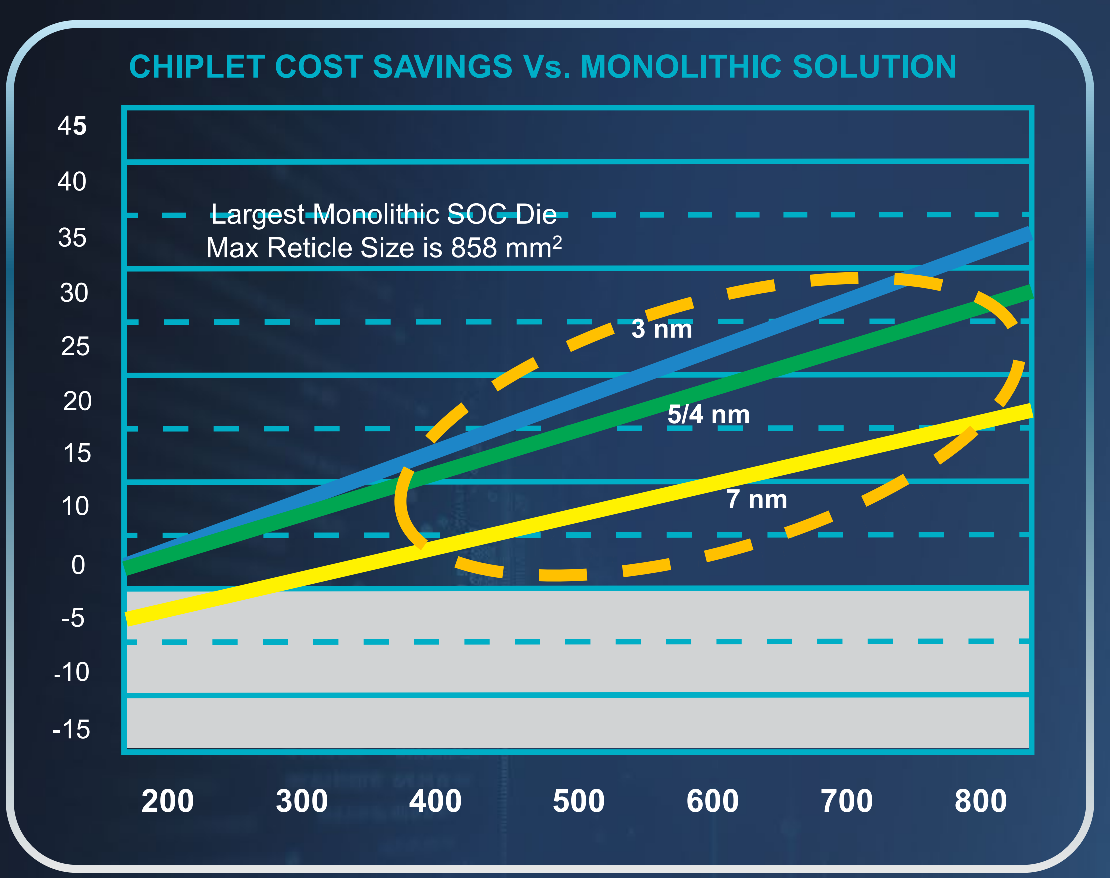
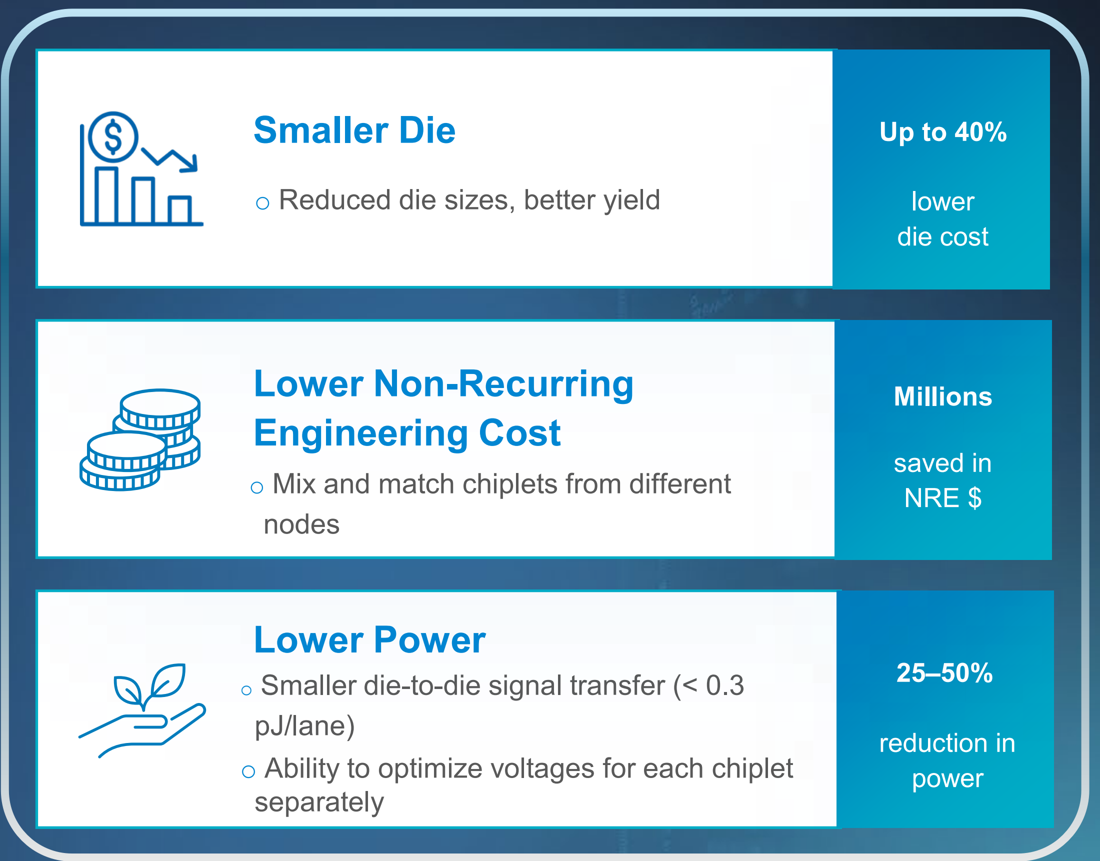
Scaling Networking and Computing Barriers





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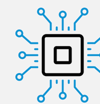
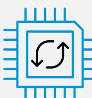
the **Future** *of* **Memory** *and* **Storage**



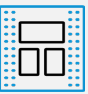
Custom Silicon

Spec-to-Silicon Capabilities
Advanced 2.5D/3D Packaging
Application Optimized IP
Subsystems



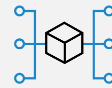
Silicon IP

High Performance
Connectivity IP
- PCIe/CXL
- Ethernet
- HBM/DDR



Chiplets

UCIe ™ Enable
- I/O Chiplet
- Memory Chiplet
- Compute Chiplet



Connectivity Products

Industry Leading
Electrical and Optical
PAM4 and Coherent DSPs

Thank You

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