Verification Challenges and Solutions for Multi-Die Systems

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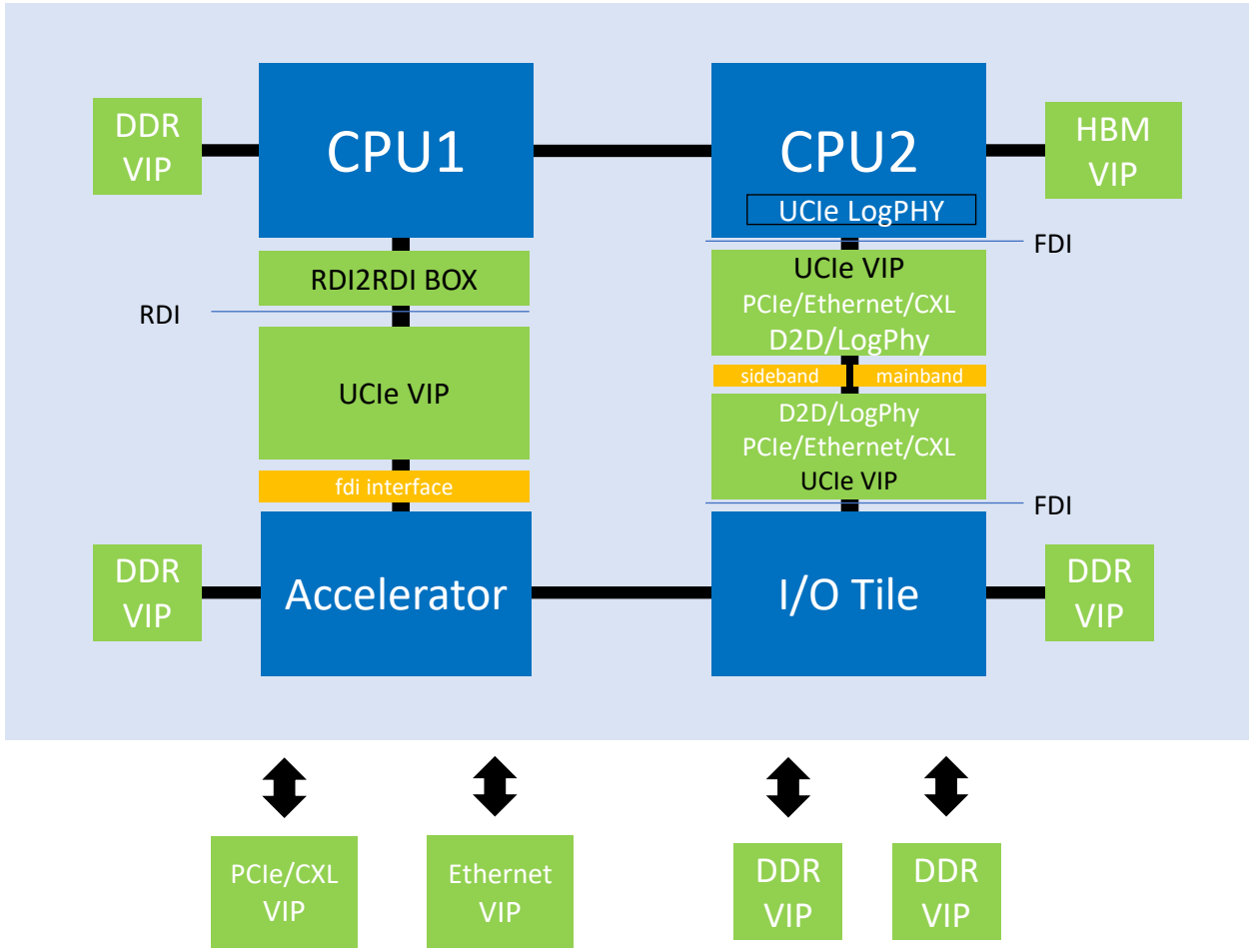
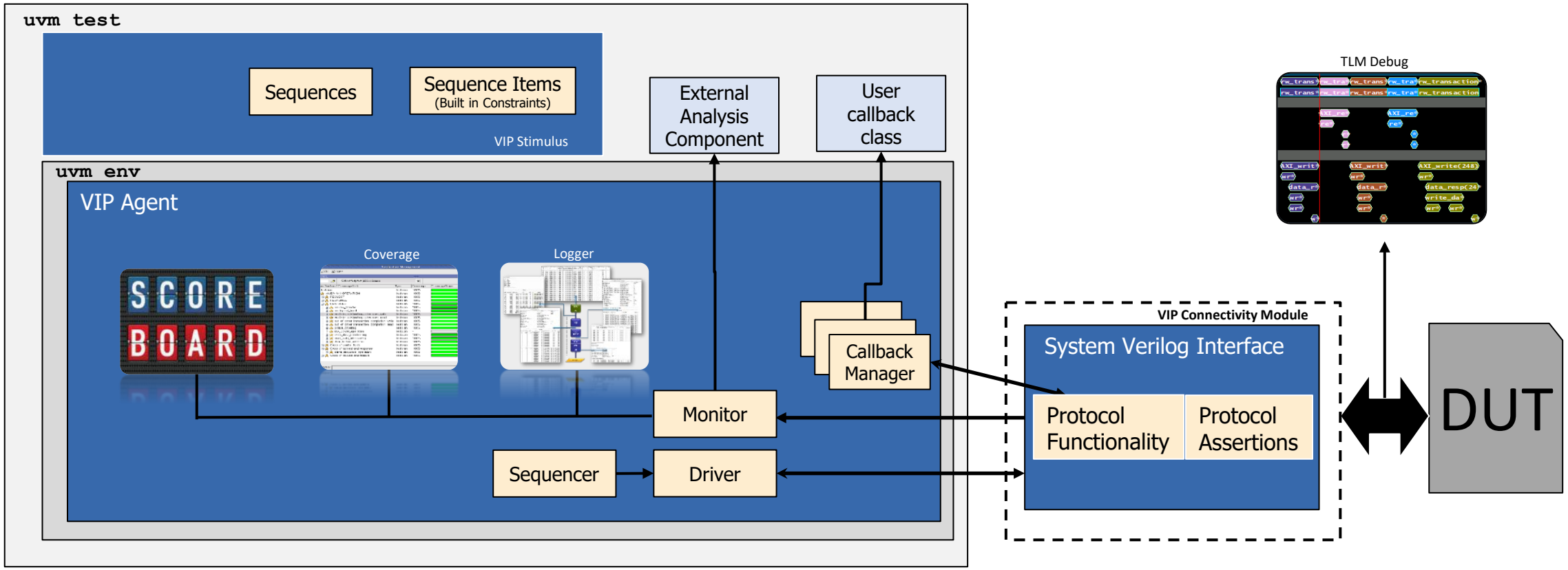
Agenda

- Typical Functional Verification Solution
- Challenges
- Verification IP
- Verification Workflow
- Automatic testbench generation
- Verification Plan and Stimuli
  - Compliance Test Suite
  - SIG compliance
- Verification IQ : Regression and coverage analysis
- Protocol Checks
- Debug : Trackers and Protocol Aware Debug
- Summary

Multi-die SoC



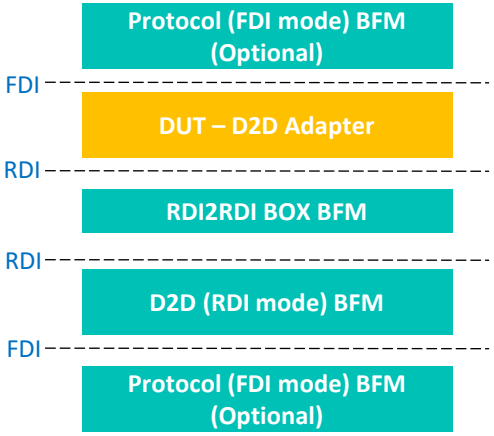
Typical Functional Verification Solution

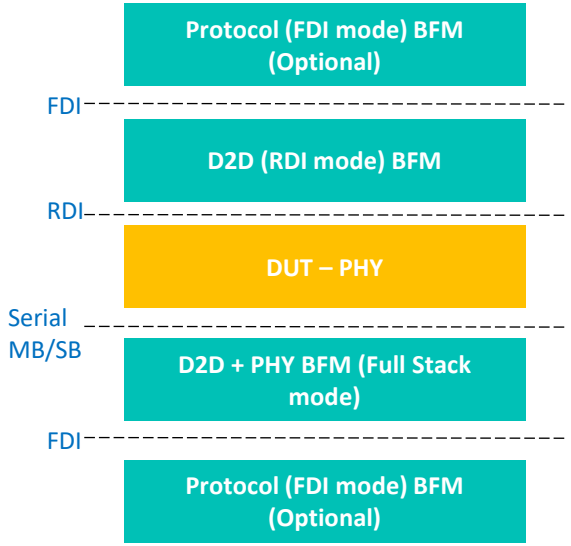


Challenges

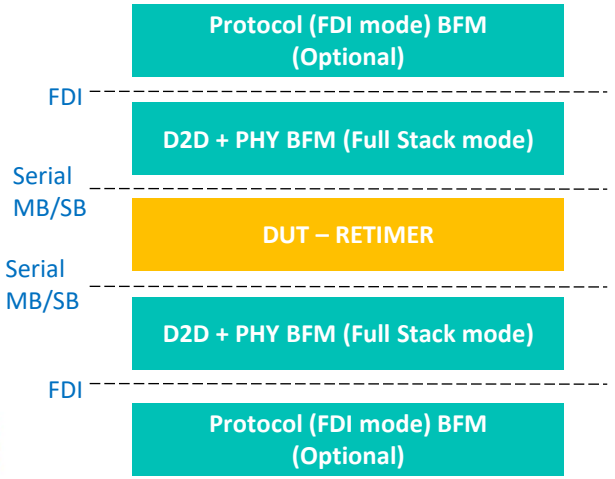
- Transition from block-level to system-level verification
- Update in the functionality, newer versions of products – changing the protocol layer
- Usability
  - useful APIs to achieve the desired scenarios
  - common use cases to corner cases
- Controllability
  - traffic flowing from top layer to pin interface
  - error injection testing
  - Bypass initialization at each layer and each state of LTSM
  - Blocking and non-blocking mode of txn
  - Txn monitoring and scoreboarding
- System-level analysis like bandwidth, throughput measurement, benchmarking
- UVM Register Adapter Layer with model
- Simulation to emulation and even prototyping scope

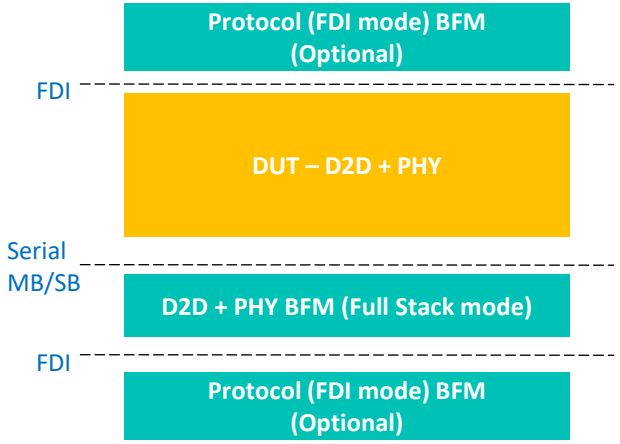
Block to subsystem to multi-die



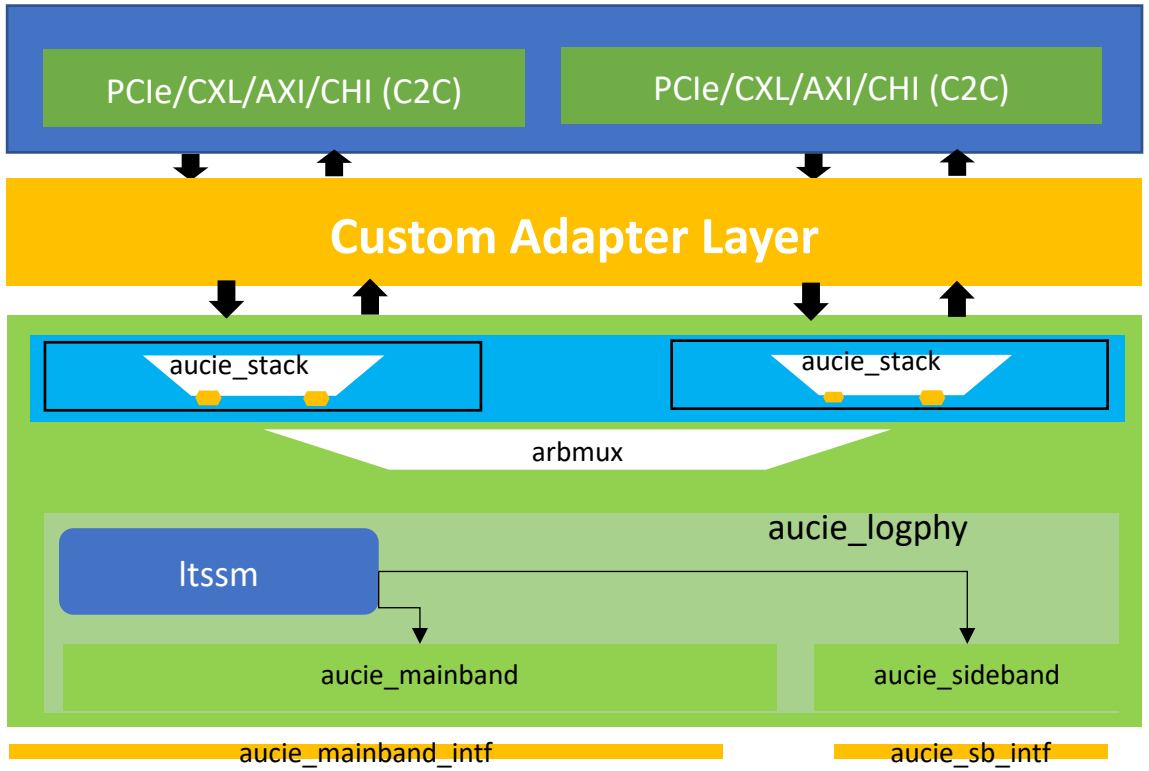


- Various use model to support block level verification like D2D adapter, Logphy
- Easy reuse of existing testbench when moving from block-level to subsystem and multi-die environments
- Utilizing the existing infrastructure of block level in subsystem and multi-die level verification environment





Common custom adapter layer



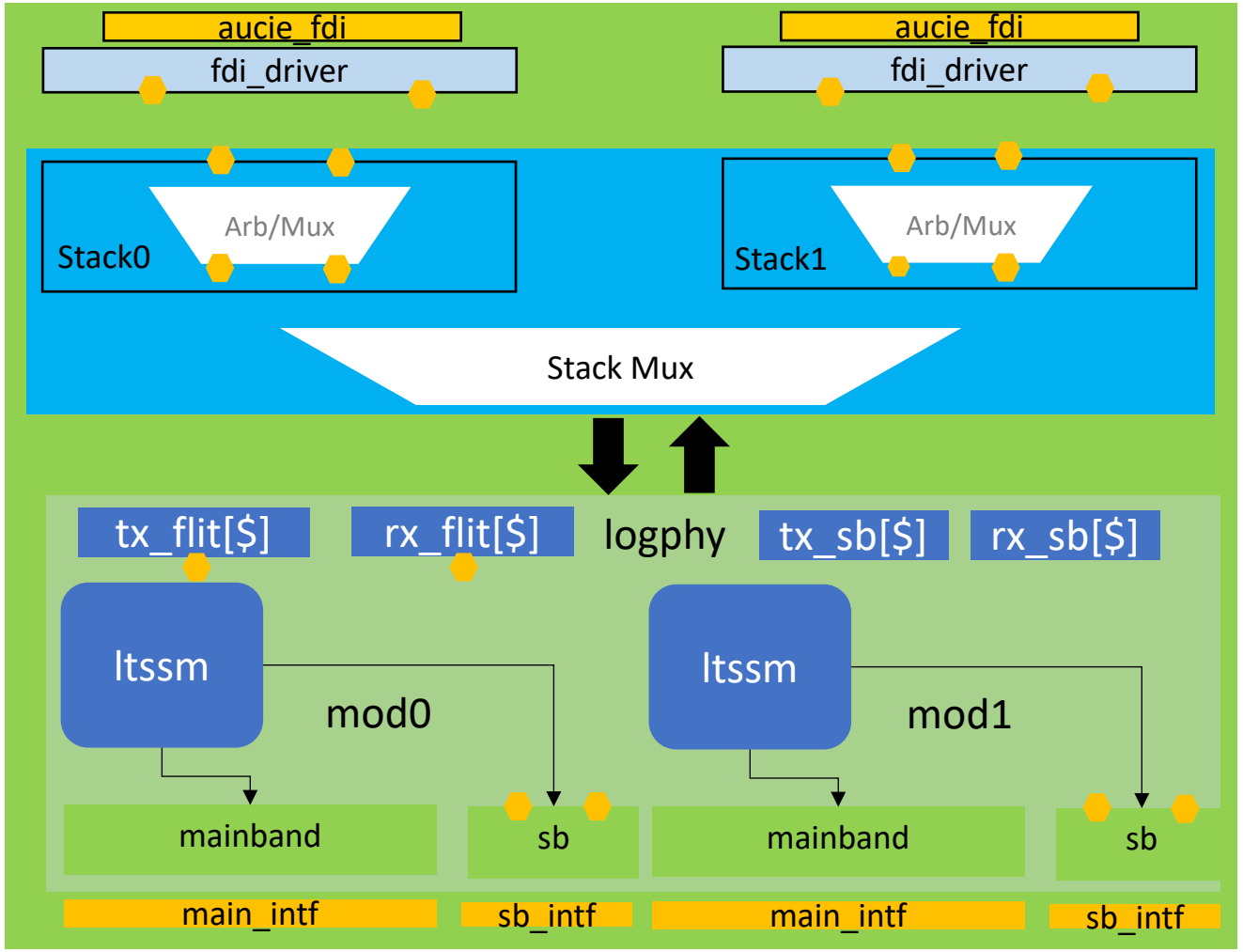
- Seamless integration of various protocol layer like PCIe, CXL or streaming protocols like AXI, CHI etc. with or without CXS/C2C
  - PCIe/CXL-UCIe
  - CHI-CXL-CXS-UCIe
  - CHI-C2C-UCIe
  - AXI-C2C-UCIe
- Easy migration of one to other using common adapter and adaptable higher layer stimulus using common APIs with no changes.
- Enables the reuse of various test related infrastructures (like regression suite, compliance test suites) of respective protocol layers over the UCIe using the set of common APIs.

Usability : Ease of Use

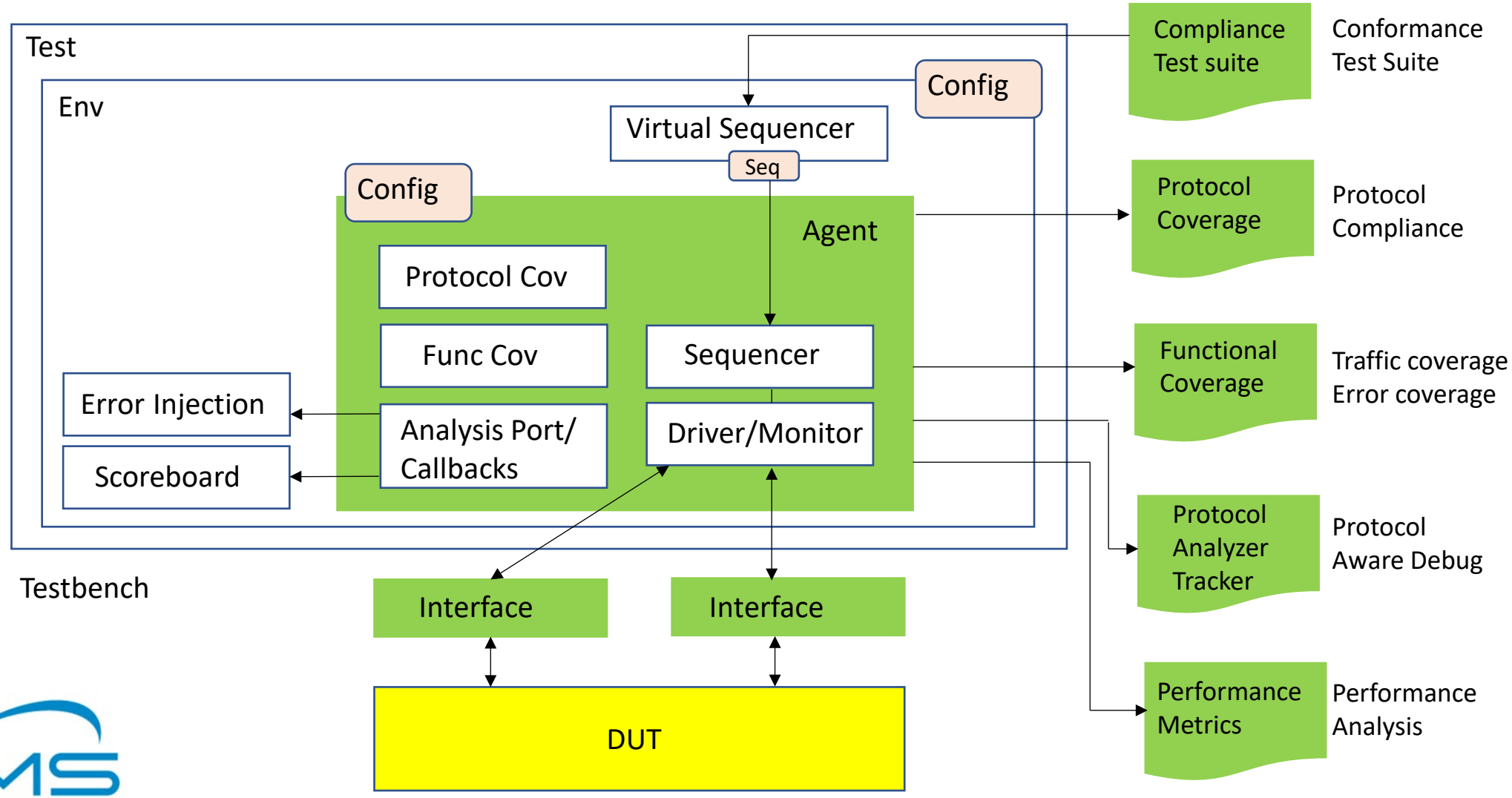
- ❑ Only two data classes : Flit and Sideband packet
- ❑ Randomize flits, sideband packet with built in constraints
- ❑ Total and direct control on each field
- ❑ BFMs D2D handles sequence and CRC generation
- ❑ Built-in APIs for various operations
  - ❑ Dynamic BFM behaviour variations
  - ❑ Sending desired flits and sideband packets
  - ❑ Entry/Exit APIs for cold reset
  - ❑ Entry/Exit APIs for all LSM states

Controllability : Full Control

- Comprehensive callbacks to control the traffic flowing through various layers and components which enables
  - scoreboarding
  - performance monitoring
  - error injection
- User traffic injection
- Built-in APIs for various operations
  - LTSM transition
  - pause/stall LTSM
  - timeout scenarios



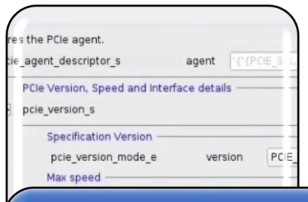
Verification IP



Verification Workflow

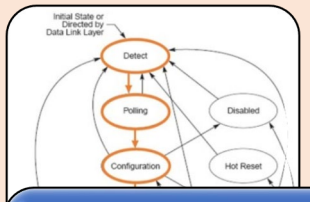
DUT – TB Connections

- Connect DUT pins to VIP signals
- Connect Clock & Reset
- Configure parameters



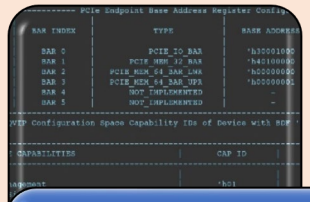
VIP Configuration

- VIP configured according to design's characteristics



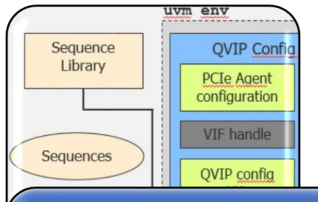
UCIe Initialization

- VIP runs sideband and mainband training based on configuration
- Link trained to desired configuration



Enumeration

- Run bus enumeration sequence for Device discovery and setting Device capabilities

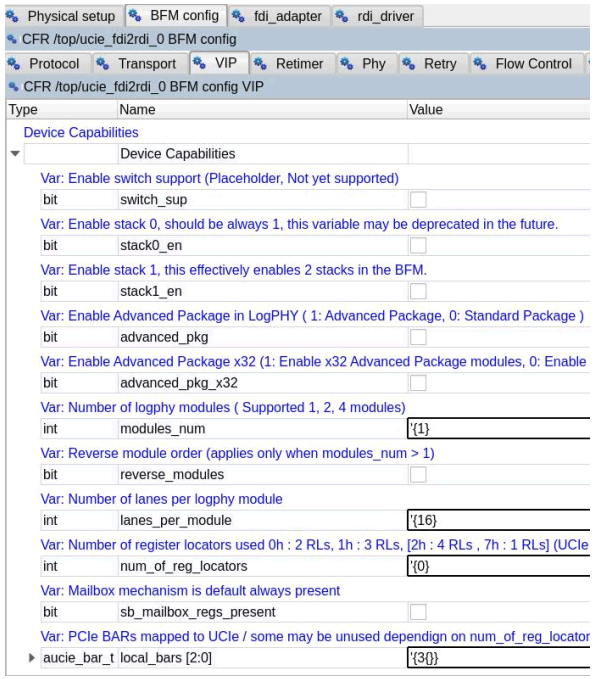


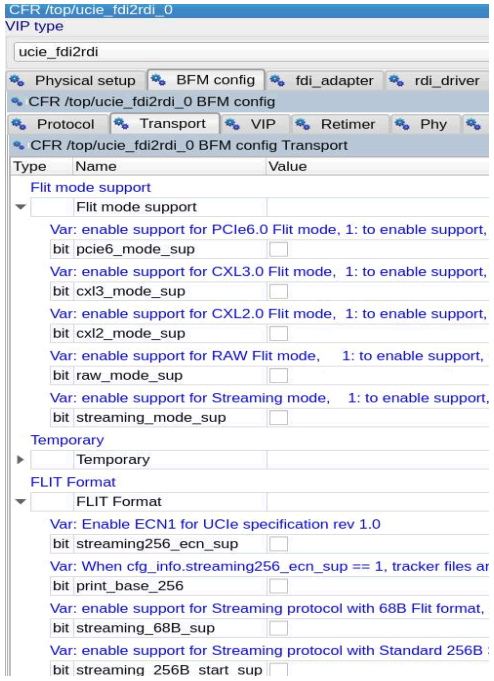
Application Verification

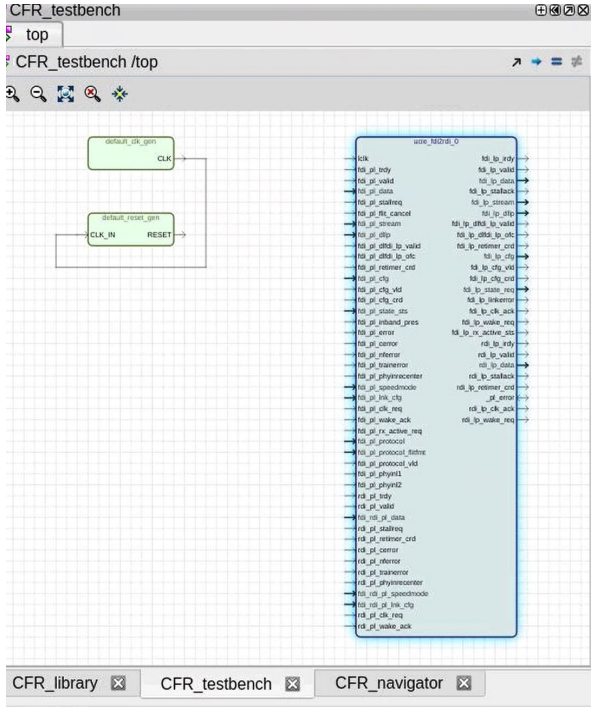
- Users run built-in ready to use stimulus - CTS
- or write device specific stimulus

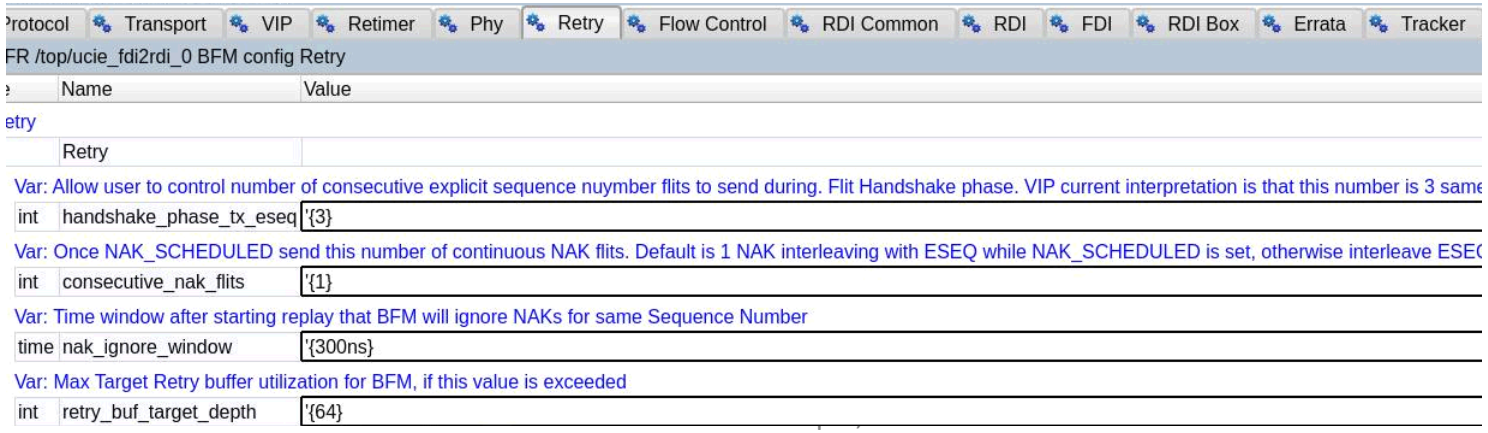
Getting Started possible in hours

Automatic UVM testbench generation









Verification Plan with Stimuli

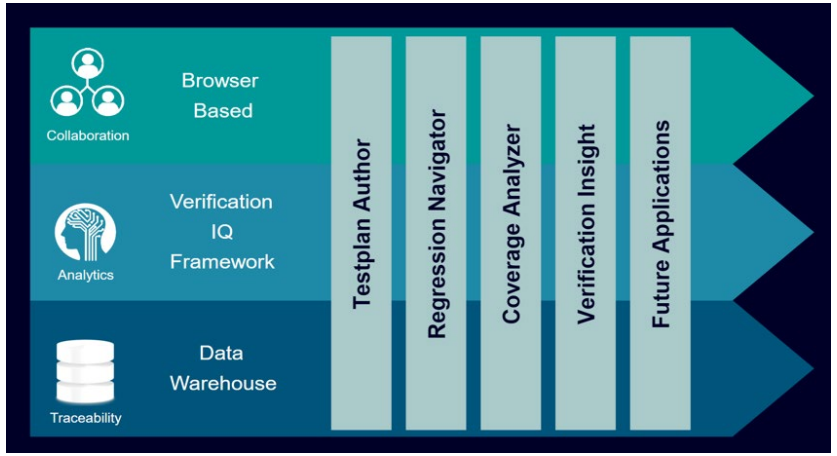
- Compliance Test Suite
  - Exhaustive and ready to use test suite
  - Covers all layers : Protocol, D2D adapter, logphy
  - Covers all interfaces : FDI, RDI, mainband, sideband
  - Config Space, LTSSM, sideband packets, retry, parity, parameter exchange
  - Multi-module, multi-protocol
  - Power Management
  - Error injection scenarios for various errors
  - Various resets
  - Started on Security – IDE, TDISP, SPDM/CMA, DOE, KM
  - GUI based tool (VIQ) to enable feature/layer wise selection and run stimuli

Stimuli

- SIG compliance suite
  - As per UCIe specs
  - PCIe compliance
  - CXL compliance

Verification IQ (VIQ)

One tool to rule them all !!



- ❑ Your verification co-pilot is here
  - ❑ Unified support of multiple tools
  - ❑ Collaborative tool with Analytical Navigation and Smart Visualization
  - ❑ Test selection as per DUT feature support
  - ❑ AI/ML based debug
    - ❑ Smart Regressions
      - ❑ Failure Predictors
      - ❑ Smoke test predictors
    - ❑ Accelerate Coverage Hole Debug

VIQ – Test Selection & analysis

#	Section	Coverage %
1	Parity	100.00%
1.1	aucie_uvm_err_inject_parity_seq	100.00%
1.2	aucie_uvm_enable_parity_seq	100.00%
2	Sideband	95.00%
3	Parameter Exchange	83.33%
4	Retry	100.00%
4.1	aucie_uvm_rand_flit_replay_seq	100.00%
4.2	aucie_uvm_ack_nak_ignore_seq	100.00%
4.3	aucie_uvm_nak_rule0_seq	100.00%
4.4	aucie_uvm_nak_rule2_seq	100.00%
4.5	aucie_uvm_seq_num0_acknak_seq	100.00%
4.6	aucie_uvm_nop_nak_timing_seq	100.00%
4.7	aucie_uvm_retimer_stall_seq	100.00%
5	LTSSM	98.00%
5.1	SBINIT	100.00%
5.2	MBINIT	100.00%
5.3	MBTRAIN	100.00%
5.4	PHYRETRAIN	88.00%
5.4.1	aucie_uvm_adapter_init_phy_retrain_seq	80.00%
5.4.2	aucie_uvm_config_retrain_seq	100.00%
5.4.3	aucie_uvm_multi_config_speed_change_seq	100.00%
5.4.4	aucie_uvm_phy_init_phy_retrain_seq	80.00%
5.4.5	aucie_uvm_phy_die_init_phy_retrain_seq	80.00%
5.5	PM Flow	100.00%
5.6	Miscellaneous	100.00%
6	Config Space	100.00%
6.1	UCIe Link DVSEC	100.00%
6.1.1	aucie_uvm_check_ro_reg_dvsec_seq	100.00%
6.1.2	aucie_uvm_dvsec_default_reg_values_seq	100.00%
6.1.3	aucie_uvm_dvsec_rsvd_chk_seq	100.00%
6.1.4	aucie_uvm_dvsec_cap_desc_chk_seq	100.00%
6.1.5	aucie_uvm_dvsec_link_cap_chk_seq	100.00%
6.1.6	aucie_uvm_dvsec_random_wr_rd_seq	100.00%
6.1.7	aucie_uvm_cfg_sp_raw_mode_and_adv_pkt_enable_seq	100.00%
6.1.8	aucie_uvm_link_status_change_seq	100.00%
6.2	D2D/PHY Register Block	100.00%

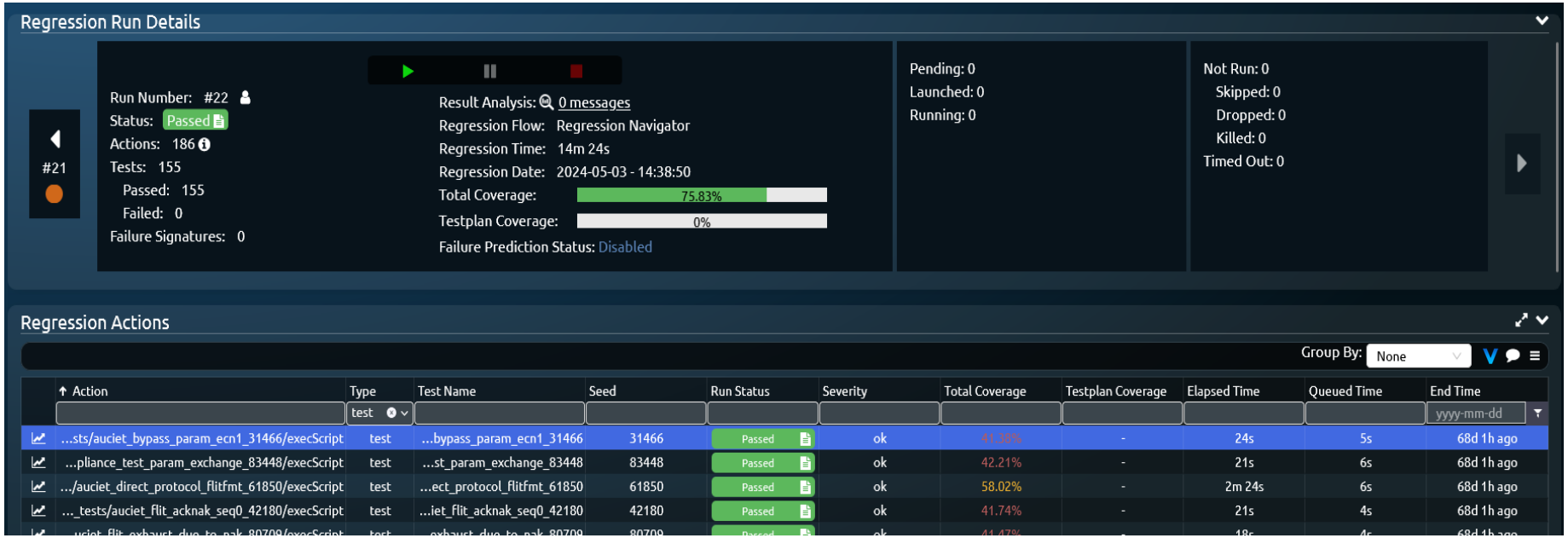
CXL2_DEVICE_DUT 98.29%

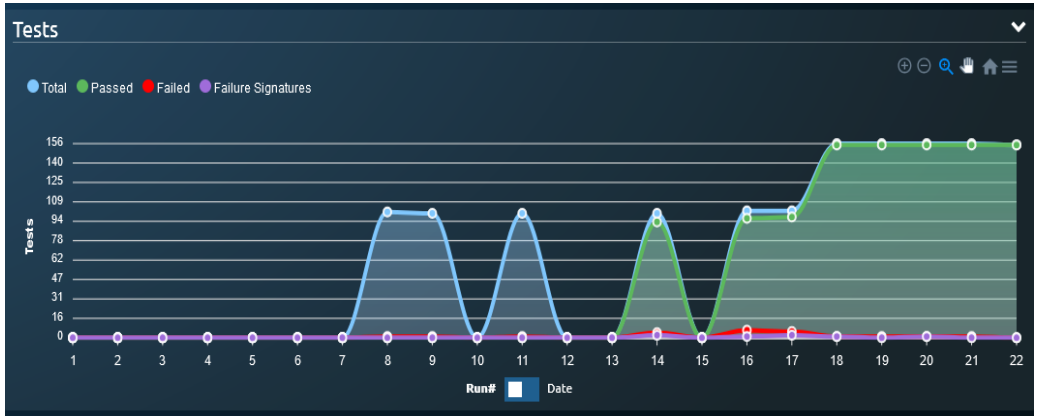
Created By saurabhs, Jun 5.

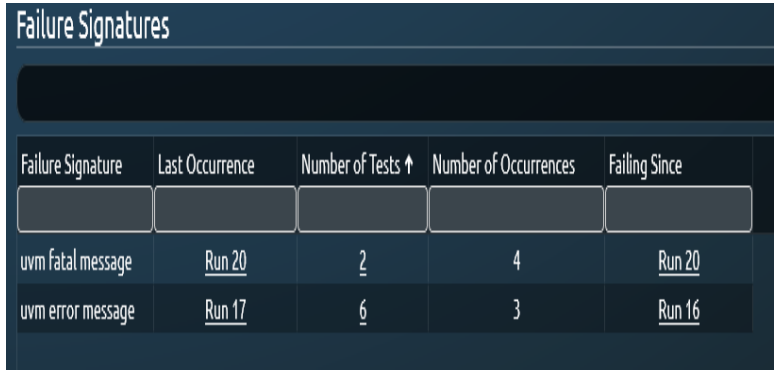
#	Section	Coverage %
3	CXL TL	96.06%
3.2	CXL_CACHE_TRAFFIC	95.66%
3.3	CXL_TL_CM_BASIC	94.31%
3.4	CXL_IO_TRAFFIC	100.00%
4	CXL Reset Compliance	100.00%
5	CXL Flexbus	99.54%
6	CXL LL	95.83%
6.1	CXL_LL_BASIC	100.00%
6.2	CXL_LL_FLIT	91.66%
7	CXL Config	97.49%
8	CXL Security	97.24%
8.1	CXL_IDE	92.49%
8.2	IDE	100.00%
8.2.1	acxlt_14_11_2_1_io_link_ide_streams	100.00%
8.2.2	acxlt_14_11_2_2_io_link_ide_streams_aggregation	100.00%
8.2.3	acxlt_14_11_2_3_io_link_ide_streams_pcrc	100.00%
8.2.4	acxlt_14_11_2_4_io_sel_ide_streams	100.00%
8.2.5	acxlt_14_11_2_5_io_sel_ide_streams_aggregation	100.00%
8.2.6	acxlt_14_11_2_6_io_sel_ide_streams_pcrc	100.00%
8.3	SPDM	99.24%
8.3.1	acxlt_14_11_3_10_ide_early_mac	100.00%
8.3.2	acxlt_14_11_3_11_1_ide_invalid_key	100.00%
8.3.3	acxlt_14_11_3_11_2_ide_inject_mac_delay	90.90%
8.3.4	acxlt_14_11_3_11_3_ide_insert_unexpected_mac	100.00%
8.3.5	acxlt_14_11_3_11_4_invalid_cxl_query_req	100.00%
8.3.6	acxlt_14_11_3_1_ide_cap	100.00%
8.3.7	acxlt_14_11_3_4_ide_latency_opt_256B_flit_mode	100.00%
8.3.8	acxlt_14_11_3_5_ide_f68	100.00%
8.3.9	acxlt_14_11_3_6_ide_local_gen_iv	100.00%
8.3.10	acxlt_14_11_3_7_ide_contain_mode	100.00%
8.3.11	acxlt_14_11_3_8_ide_skid_mode	100.00%
8.3.12	acxlt_14_11_3_9_ide_key_refresh	100.00%
9	CXL RAS	97.25%
9.1	CXL_RAS	91.77%
9.2	CXL_POISON	100.00%
9.3	CXL_VIRAL	100.00%
10	CXL MISC	100.00%
11	CXL DOE Compliance	97.82%
12	CXL Test Spec Compliance	99.52%

VIQ – Regression Analysis

- Quick summary for regression run
- Result analysis and incremental run
- Failure signature detection

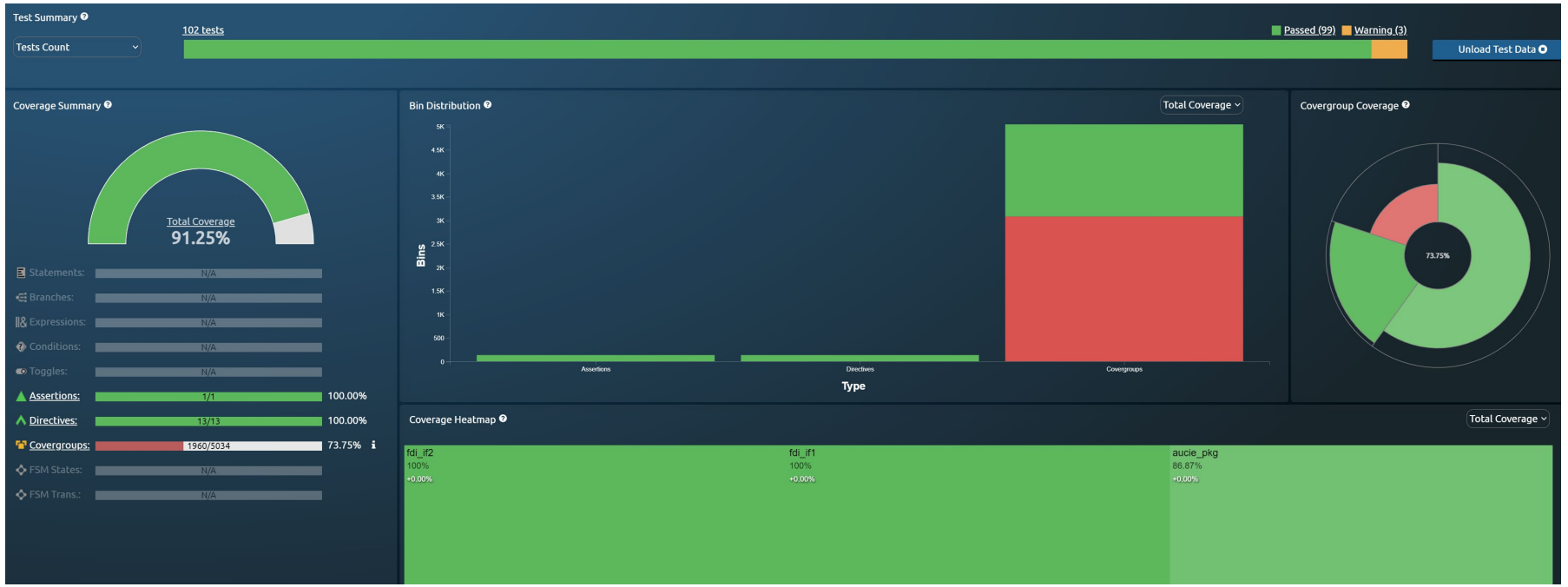






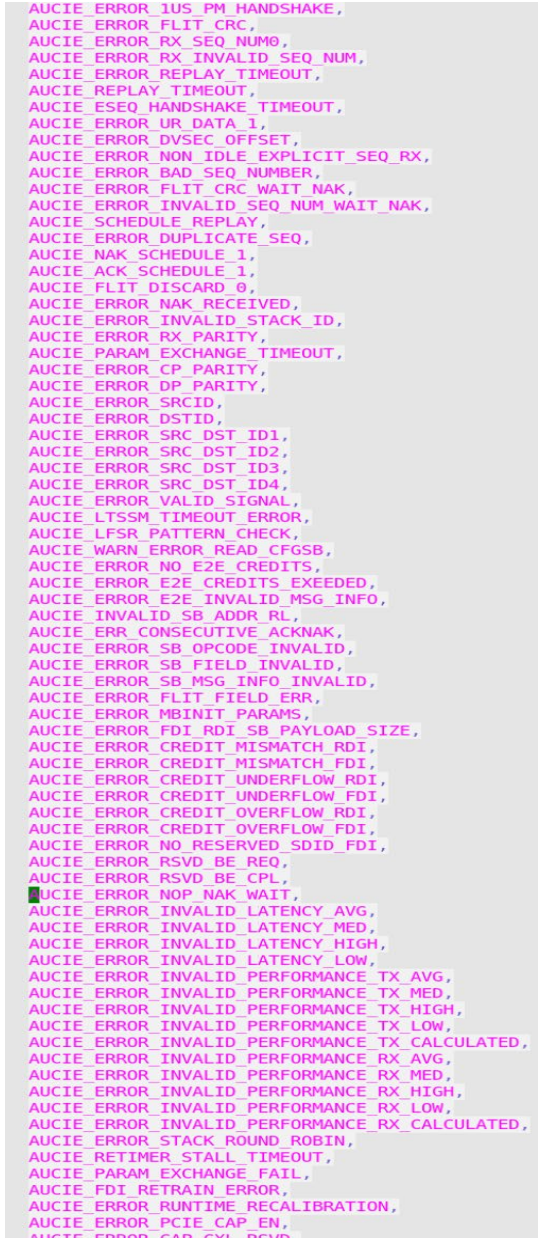
VIQ – Coverage Analysis

- ❑ Hole analysis
- ❑ Heatmaps
- ❑ Bin distribution



Protocol Checks

- Exhaustive set of protocol checks (~500)
  - FDI, RDI, Logphy, Config Space
  - Parameter Negotiation
  - PCIe, CXL and AXI checks (~3000)
- Coverage of protocol checks
  - make sures that all the protocol scenarios has been exercised without violation



```
AUCIE_ERROR_1US_PM_HANDSHAKE,
AUCIE_ERROR_FLIT_CRC,
AUCIE_ERROR_RX_SEQ_NUM0,
AUCIE_ERROR_RX_INVALID_SEQ_NUM,
AUCIE_ERROR_REPLAY_TIMEOUT,
AUCIE_REPLAY_TIMEOUT,
AUCIE_ESEQ_HANDSHAKE_TIMEOUT,
AUCIE_ERROR_UR_DATA_1,
AUCIE_ERROR_DVSEC_OFFSET,
AUCIE_ERROR_NON_IDLE_EXPLICIT_SEQ_RX,
AUCIE_ERROR_BAD_SEQ_NUMBER,
AUCIE_ERROR_FLIT_CRC_WAIT_NAK,
AUCIE_ERROR_INVALID_SEQ_NUM_WAIT_NAK,
AUCIE_SCHEDULE_REPLAY,
AUCIE_ERROR_DUPLICATE_SEQ,
AUCIE_NAK_SCHEDULE_1,
AUCIE_ACK_SCHEDULE_1,
AUCIE_FLIT_DISCARD_0,
AUCIE_ERROR_NAK_RECEIVED,
AUCIE_ERROR_INVALID_STACK_ID,
AUCIE_ERROR_RX_PARITY,
AUCIE_PARAM_EXCHANGE_TIMEOUT,
AUCIE_ERROR_CP_PARITY,
AUCIE_ERROR_DP_PARITY,
AUCIE_ERROR_SRCID,
AUCIE_ERROR_DSTID,
AUCIE_ERROR_SRC_DST_ID1,
AUCIE_ERROR_SRC_DST_ID2,
AUCIE_ERROR_SRC_DST_ID3,
AUCIE_ERROR_SRC_DST_ID4,
AUCIE_ERROR_VALID_SIGNAL,
AUCIE_LTSSM_TIMEOUT_ERROR,
AUCIE_LFSR_PATTERN_CHECK,
AUCIE_WARN_ERROR_READ_CFGSB,
AUCIE_ERROR_NO_E2E_CREDITS,
AUCIE_ERROR_E2E_CREDITS_EXEEDED,
AUCIE_ERROR_E2E_INVALID_MSG_INFO,
AUCIE_INVALID_SB_ADDR_RL,
AUCIE_ERR_CONSECUTIVE_ACKNAK,
AUCIE_ERROR_SB_OPCODE_INVALID,
AUCIE_ERROR_SB_FIELD_INVALID,
AUCIE_ERROR_SB_MSG_INFO_INVALID,
AUCIE_ERROR_FLIT_FIELD_ERR,
AUCIE_ERROR_MBINIT_PARAMS,
AUCIE_ERROR_FDI_RDI_SB_PAYLOAD_SIZE,
AUCIE_ERROR_CREDIT_MISMATCH_RDI,
AUCIE_ERROR_CREDIT_MISMATCH_FDI,
AUCIE_ERROR_CREDIT_UNDERFLOW_RDI,
AUCIE_ERROR_CREDIT_UNDERFLOW_FDI,
AUCIE_ERROR_CREDIT_OVERFLOW_RDI,
AUCIE_ERROR_CREDIT_OVERFLOW_FDI,
AUCIE_ERROR_NO_RESERVED_SDID_FDI,
AUCIE_ERROR_RSVD_BE_REQ,
AUCIE_ERROR_RSVD_BE_CPL,
AUCIE_ERROR_NOP_NAK_WAIT,
AUCIE_ERROR_INVALID_LATENCY_AVG,
AUCIE_ERROR_INVALID_LATENCY_MED,
AUCIE_ERROR_INVALID_LATENCY_HIGH,
AUCIE_ERROR_INVALID_LATENCY_LOW,
AUCIE_ERROR_INVALID_PERFORMANCE_TX_AVG,
AUCIE_ERROR_INVALID_PERFORMANCE_TX_MED,
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AUCIE_ERROR_INVALID_PERFORMANCE_TX_LOW,
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AUCIE_ERROR_INVALID_PERFORMANCE_RX_HIGH,
AUCIE_ERROR_INVALID_PERFORMANCE_RX_LOW,
AUCIE_ERROR_INVALID_PERFORMANCE_RX_CALCULATED,
AUCIE_ERROR_STACK_ROUND_ROBIN,
AUCIE_RETIMER_STALL_TIMEOUT,
AUCIE_PARAM_EXCHANGE_FAIL,
AUCIE_FDI_RETRAIN_ERROR,
AUCIE_ERROR_RUNTIME_RECALIBRATION,
AUCIE_ERROR_PCIE_CAP_EN,
```

Debug Tools

- ❑ Debug Messages
- ❑ Trackers and transcript
- ❑ Protocol Aware Debug

Debug messages

```
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] aucie_module::exit_cold_reset()
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting logphy
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting module : 3
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] mode = AUCIE_MODULE_tx_rx
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] aucie_module
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting sb_deserializer
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting module : 2
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] mode = AUCIE_MODULE_tx_rx
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] aucie_module
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting sb_deserializer
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting module : 1
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] mode = AUCIE_MODULE_tx_rx
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] aucie_module
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting sb_deserializer
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting module : 0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] mode = AUCIE_MODULE_tx_rx
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] aucie_module
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Starting sb_deserializer
```

```
uvm_test_top.env0.bfm2.bfm2_log [AUCIE_INF] AVERY: ECN1: Advertising additional bits in {FinCap.Adapter}
uvm_test_top.env0.bfm2.bfm2_log [AUCIE_INF]                 cfg_info.streaming_68B_sup:              0
uvm_test_top.env0.bfm2.bfm2_log [AUCIE_INF]                 cfg_info.streaming_256B_end_sup:         1
uvm_test_top.env0.bfm2.bfm2_log [AUCIE_INF]                 cfg_info.streaming_256B_start_sup:       0
uvm_test_top.env0.bfm2.bfm2_log [AUCIE_INF]                 cfg_info.streaming_256B_lom_w_ob_sup:    0
uvm_test_top.env0.bfm2.bfm2_log [AUCIE_INF]                 cfg_info.streaming_256B_lom_no_ob_sup:   1
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] AVERY: ECN1: Advertising additional bits in {FinCap.Adapter}
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                 cfg_info.streaming_68B_sup:              0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                 cfg_info.streaming_256B_end_sup:         1
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                 cfg_info.streaming_256B_start_sup:       0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                 cfg_info.streaming_256B_lom_w_ob_sup:    0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                 cfg_info.streaming_256B_lom_no_ob_sup:   1
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Received {AUCIE_SIDE_MSG_AdvCap_Adapter}        :
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] Received {AUCIE_SIDE_MSG_AdvCap_Adapter}
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.retimer_en:              0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.cxl_lat_opt_fmt6_sup:    0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.cxl_lat_opt_fmt5_sup:    0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.stack0_en:               1
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.stack1_en:               0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.multi_protocol_en:       0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.retry_sup:               1
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.streaming_mode_sup:      1
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.pcie6_mode_sup:          0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.cxl3_mode_sup:           0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.cxl2_mode_sup:           0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.raw_mode_sup:            1
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.UP:                      0
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF]                  advCap.DP:                      1
```

```
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] FDI BRINGUP PROCESS ENDS
uvm_test_top.env0.bfm1.bfm1_log [AUCIE_INF] STARTING FDI BRINGUP PROCESS
'bfm2"(mod0): LTSSM go to AUCIE_LTSSM_RESET
uvm_test_top.env0.bfm2.bfm2_log [AUCIE_INF] FDI BRINGUP PROCESS ENDS
uvm_test_top.env0.bfm2.bfm2_log [AUCIE_INF] STARTING FDI BRINGUP PROCESS
```

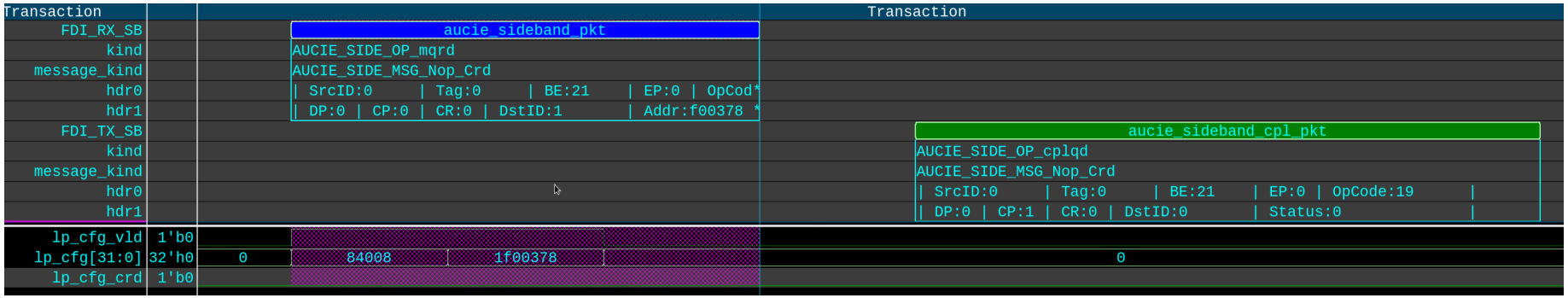
Debug using trackers

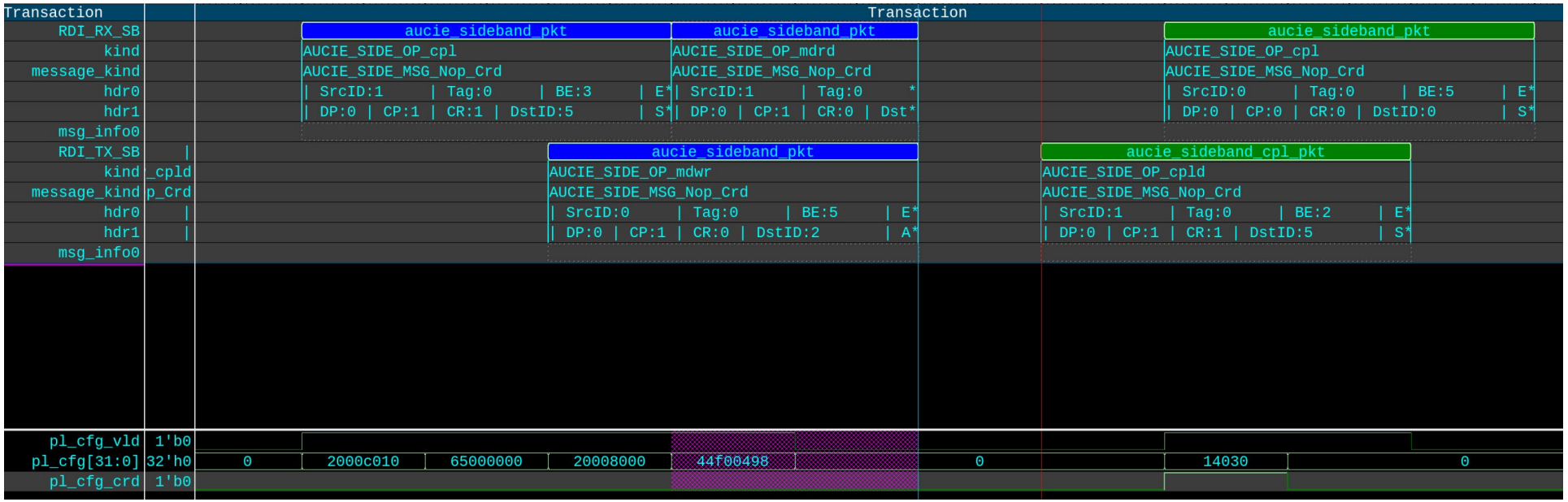
- Visualize transactions in “spec” formats
  - Sideband Packets
  - FLITs, etc.
- Multiple trackers for each layer
  - FDI, RDI, D2D
  - Logphy
  - Correlated between layers and multi-protocol stacks (PCIe-UCIe), (CXL-UCIe), (AXI-UCIe) etc.
- conditional user annotations to pin-point transactions and bugs quickly

```
==> Time:346.459ns  MSGD #4cd5(AUCIE_SIDE_MSG_AdvCap_Adapter)
+-------------------------------------------------------------+
| SrcID:1     | MsgCode:1                    | OpCode:1b      |
| DP:1 | CP:0 | DstID:5   | MsgInfo:0      | MsgSubCode:0   |
+----- MsgInfo ------------------------------------------------+
| - Regular Message                                           |
+----- Data --------------------------------------------------+
| Data [31: 0]: 014000b0                                      |
| Data [63:32]: 00000000                                      |
| - [0] Raw Format: 0                                         |
| - [1] 68B Flit Mode: 0                                      |
| - [2] CXL 256B Flit Mode: 0                                 |
| - [3] PCIe Flit Mode: 0                                     |
| - [4] Streaming: 1                                          |
| - [5] Retry: 1                                              |
| - [6] Multi_Protocol_Enable: 0                              |
| - [7] Stack0_Enable: 1                                      |
| - [8] Stack1_Enable: 0                                      |
| - [9] CXL_LatOpt_Fmt5: 0                                    |
| - [10] CXL_LatOpt_Fmt6: 0                                   |
| - [11] Retimer: 0                                           |
| - [20:12] Retimer Credits: 'd1024                           |
| - [21] DP: 0                                                |
| - [22] UP: 1                                                |
| - [23] 68B Flit Format: 0                                   |
| - [24] Standard 256B End Header Flit Format: 1              |
| - [25] Standard 256B Start Header Flit Format: 0            |
| - [26] Latency-Optimized 256B without Optional Bytes        |
|        Flit Format: 0                                       |
| - [27] Latency-Optimized 256B with Optional Bytes           |
|        Flit Format: 0                                       |
| - [28] Enhanced_Multi_Protocol_Enable: 0                    |
| - [29] Stack 0 Maximum Bandwidth_Limit: 0                   |
| - [30] Stack 1 Maximum Bandwidth_Limit: 0                   |
+-------------------------------------------------------------+
```

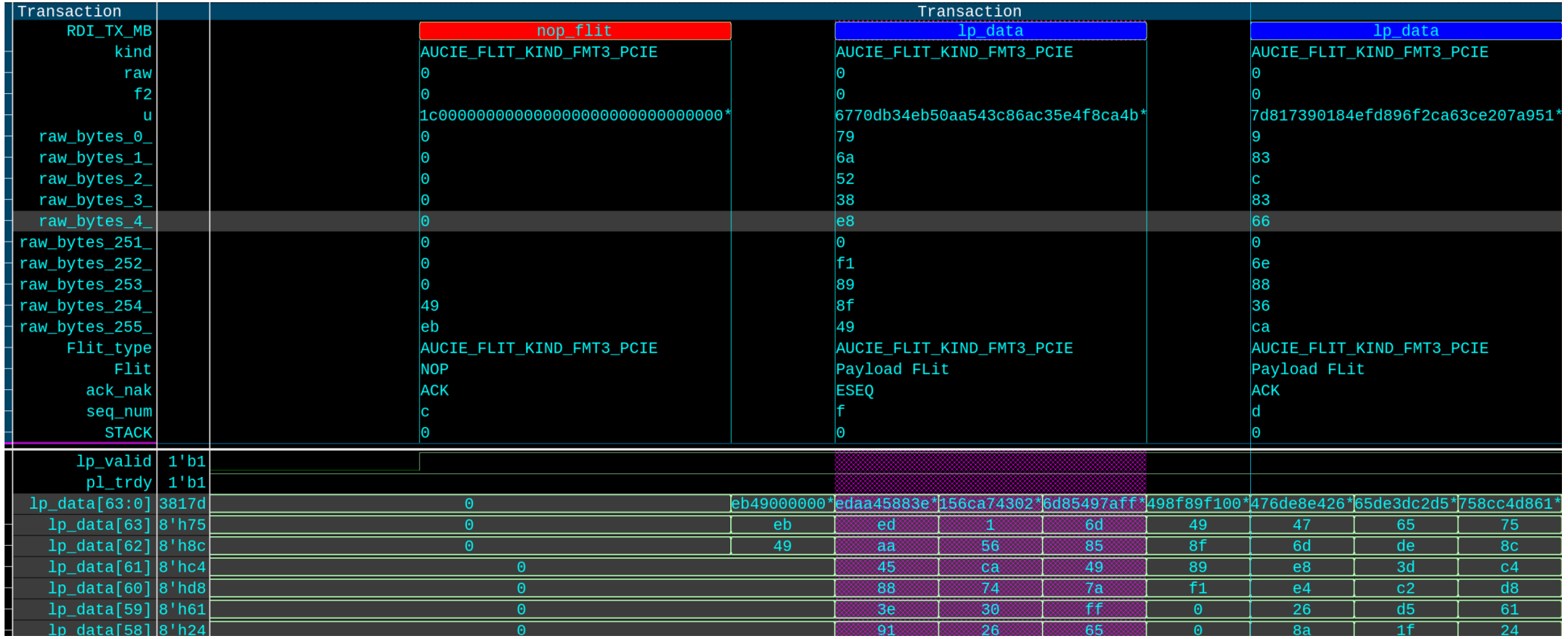
```
==> Time:1629.000ns  AUCIE_FLIT_KIND_FMT4_CXLIO_PCIE#4dc1 (Seq 02 )
Prot_id: 1 | Stack_id: 0 | dlp: 0 | S_upper: 0 | rsvd0: 0 | Ack_Nak: 0 | S_lower: 2
Chunk0: e4a638b6 1315d5df e836052c 43b87bf7 93c29e6e d359a22b ea41f3ed 9bbc2b1a e74ff53b 4e302f41 1b2cf39e 5b6b0ca2 8a857caf 3903529a c399b6c3 a4e0
Chunk1: 29dd7782 f299596c bad52dc7 207fe14f 4d6c55e9 1cae6e31 5cbd3f44 1e5eec4d 8183bd1d 99dcc5a2 a89d888c ddb20667 d1ab3935 13315d8d cc1d02c1 68e70539
Chunk2: 5b0e5646 ea908e9b 1b501ee6 42f635b8 46707880 e5064e97 720a4adf 0f67946b d9d25dc9 69d9bd97 37ce245f 61928d69 c7e0e643 adb26e1a fe91496a 66a9baff
Chunk3: 2746a3ba aa7f0b92 542256b4 2b0fed58 191e3e06 cf801940 d935dfb5 1af30bbe b6a8bb91 130788ed 68430982 04ba
DLP: 00000000 | 10B_RSVD: 00000000000000000000 | CRC0: 4278 | CRC1: 1a1d
tx_seq: 02
```

Protocol Aware Debug





Protocol Aware Debug (contd..)



Transaction			Transaction		
RDI_TX_MB		nop_flit	lp_data		lp_data
kind		AUCIE_FLIT_KIND_FMT3_PCIE	AUCIE_FLIT_KIND_FMT3_PCIE		AUCIE_FLIT_KIND_FMT3_PCIE
raw		0	0		0
f2		0	0		0
u		1c000000000000000000000000000000*	6770db34eb50aa543c86ac35e4f8ca4b*		7d817390184efd896f2ca63ce207a951*
raw_bytes_0_		0	79		9
raw_bytes_1_		0	6a		83
raw_bytes_2_		0	52		c
raw_bytes_3_		0	38		83
raw_bytes_4_		0	e8		66
raw_bytes_251_		0	0		0
raw_bytes_252_		0	f1		6e
raw_bytes_253_		0	89		88
raw_bytes_254_		49	8f		36
raw_bytes_255_		eb	49		ca
Flit_type		AUCIE_FLIT_KIND_FMT3_PCIE	AUCIE_FLIT_KIND_FMT3_PCIE		AUCIE_FLIT_KIND_FMT3_PCIE
Flit		NOP	Payload FLit		Payload FLit
ack_nak		ACK	ESEQ		ACK
seq_num		c	f		d
STACK		0	0		0
lp_valid	1'b1				
pl_trdy	1'b1				
lp_data[63:0]	3817d	0	eb49000000*	edaa45883e*	156ca74302*	6d85497aff*	498f89f100*	476de8e426*	65de3dc2d5*	758cc4d861*
lp_data[63]	8'h75	0	eb	ed	1	6d	49	47	65	75
lp_data[62]	8'h8c	0	49	aa	56	85	8f	6d	de	8c
lp_data[61]	8'hc4	0		45	ca	49	89	e8	3d	c4
lp_data[60]	8'hd8	0		88	74	7a	f1	e4	c2	d8
lp_data[59]	8'h61	0		3e	30	ff	0	26	d5	61
lp_data[58]	8'h24	0		91	26	65	0	8a	1f	24

Performance Measurement

- Performance summary log on Tx and Rx bus
- Configurable for a particular simulation window

```
TX PERFORMANCE SUMMARY
Performance TX AVG:  64032.080201 MB/s
Performance TX MED:  59733.333333 MB/s
Performance TX HIGH: 68266.666667 MB/s
Performance TX LOW:  59733.333333 MB/s

RX PERFORMANCE SUMMARY
Performance RX AVG:  63903.759398 MB/s
Performance RX MED:  68266.666667 MB/s
Performance RX HIGH: 68266.666667 MB/s
Performance RX LOW:  51200.000000 MB/s
```

Summary

- ❑ Automatic UVM-TB generation
- ❑ Compliance test suites (ready to use exhaustive stimulus)
- ❑ VIP controllability to hit corner case scenarios
- ❑ Usability for ease of use
- ❑ Debug tools
- ❑ Discussed features enabled our customers to verify the designs faster and achieve lesser time to market

Questions ??

Please visit booth # 1051 (Siemens) for more information