Software Controlled Physical Layer

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Abstract

The physical layer requirements for NAND flash are rapidly evolving. It is difficult to create an ASIC in advance of the new technologies that will match specifications that have not yet been developed. This can result in inefficiency, as well as a reduced longevity of an ASIC development. We will present a software controlled physical layer, that allows us to specify every cycle to match any arbitrary interface waveform. This allows us to be perfectly efficient and provides some future-proofing ability as well.

Agenda

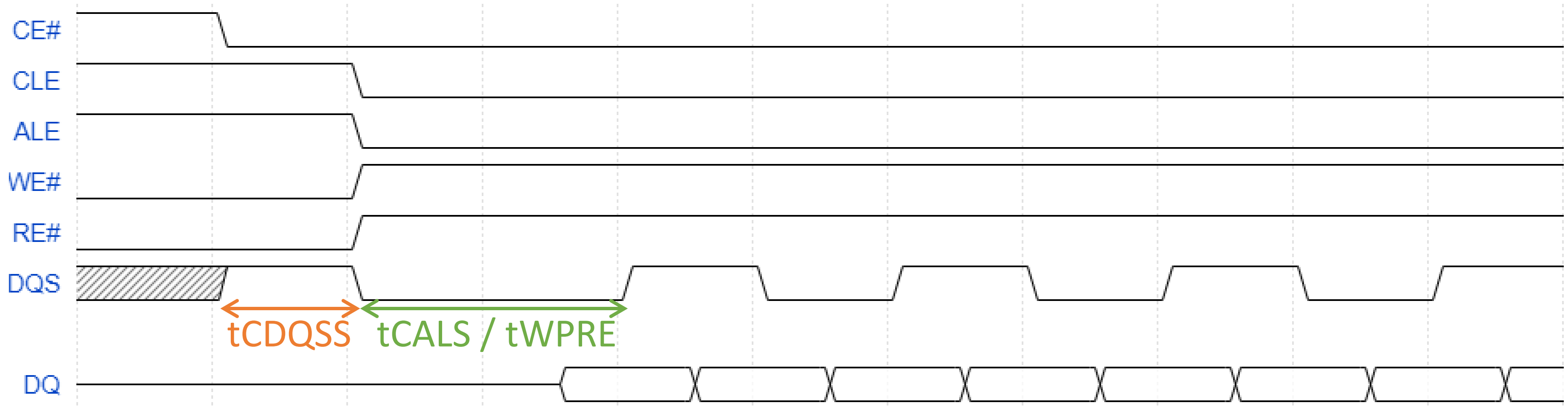
- Standardization and evolving physical interface needs
- Example issues
- Control over the interface pins
- Macro encapsulation of operations
- Conclusions

Standardization Challenges

In order to be efficient in power and area an ASIC design should be optimized for a target technology. Unlike other standards like PCIe® , NAND Flash technology presents several challenges to optimization:

- ONFI and Toggle competing standards for NAND interfacing
- An ASIC development has to take place before a NAND is available to hit the market window
- An ASIC needs to be flexible enough to anticipate specifications not yet created
- The need to buffer the physical interface for high density drives creates custom challenges:
  - Reduce the loading required
  - Expand targets supported
  - Many companies implement a custom solution, which effects the physical protocol beyond the public specifications

Example 1: TCDQSS Ambiguity (Data Input)

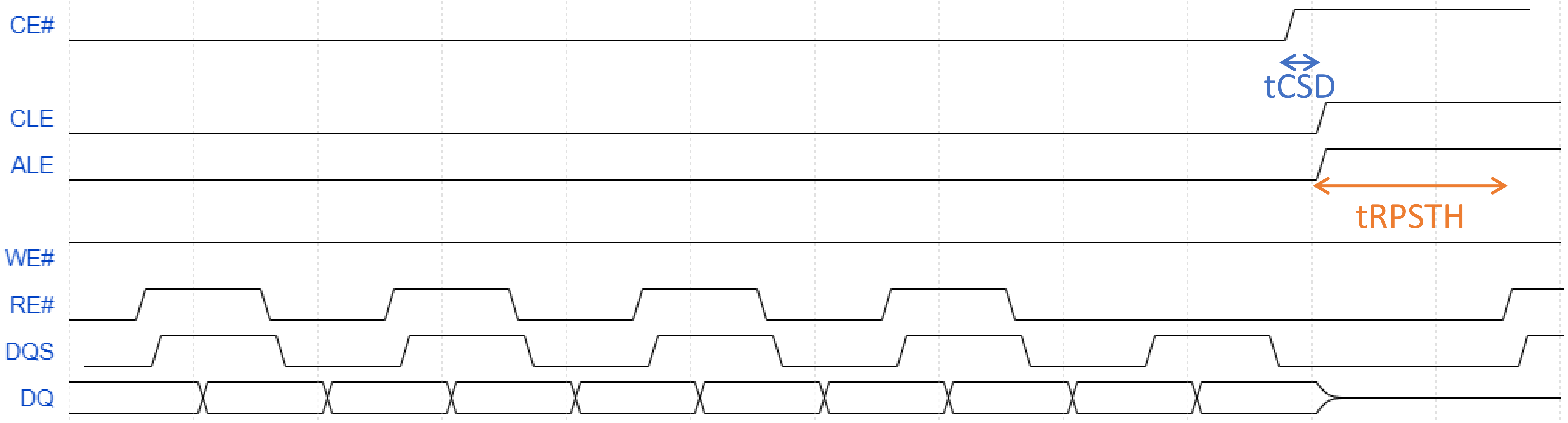


(Internal Termination)

Specification states: “DQS may be high or low during tCDQSS”

But a new part comes out that specifies a “low” value, but your hardware chose a “high” value….

Example 2: Closing a Transaction



Spec states:

“To exit the data burst, either CE#, ALE, or CLE is set to one by the host”

But then a buffer chip comes out that must exit with CE#, and the controller uses CLE…

Software Controlled Physical Layer

- To manage unique opening and closing transactions we can have software send the state of the bus in VCD (Value Change Dump) format
- This will specify the exact state of the bus, and for how many cycles it will remain.
- In this way we can have transactions fit any defined waveform
- Using IE (Input Enable) and TE (Termination Enable) we can receive data as well

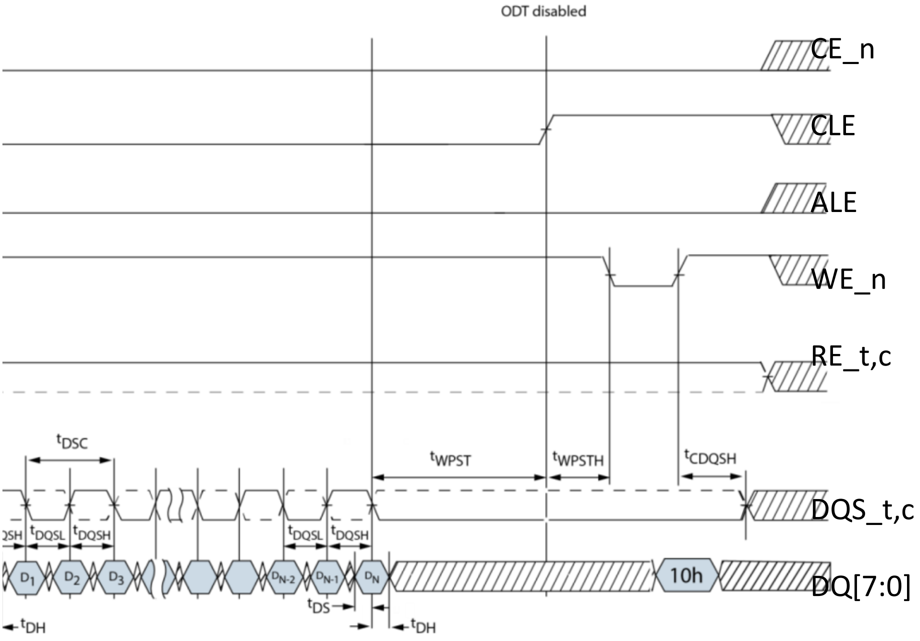
Cycles	CE#	ALE	CLE	WE#	RE#	DQ OE	DQ IE	DQ TE	DQ	DQS
5	0	0	0	1	1	1	0	0	0x70	0
1	1	0	0	1	1	0	0	0	0	0
…										

But Software Can’t Keep Up with That!?!

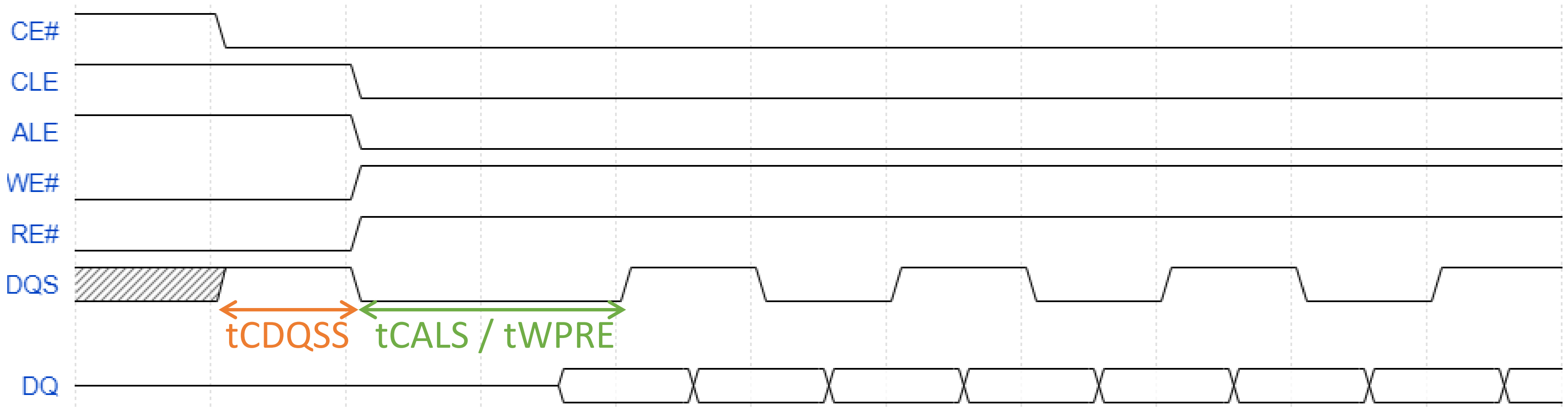
- We only need this for **features, status**, **data-preamble**, and **data-postamble**
- Macros can be created in RAM and software can simply point to the macro to run.

DIN Postamble Macro

Cycles	CE#	ALE	CLE	WE#	RE#	DQ OE	DQ IE	DQ TE	DQ	DQS
tWPST	0	0	0	1	1	1	0	0	Dn	0
tWPSTH	0	0	1	1	1	1	0	0	Dn	0
tCAS	0	0	1	0	1	1	0	0	0x10	0
tCAH	0	0	1	1	1	1	0	0	0x10	0
1	1	0	0	1	1	0	0	0	0	0



Example 1: Solution



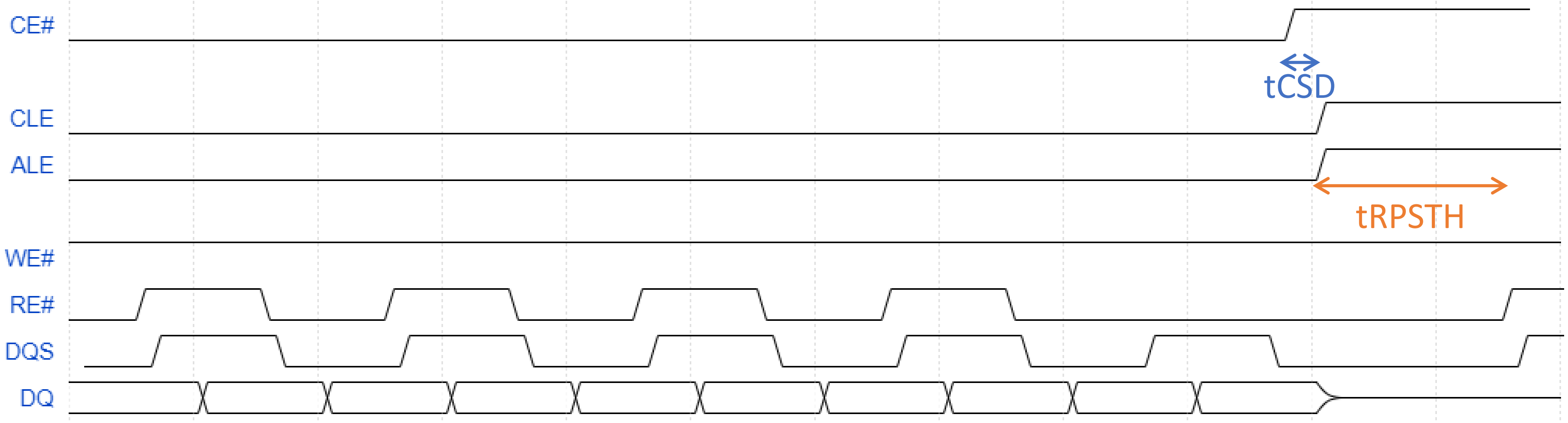
(Internal Termination)

Specification states: “DQS may be high or low during tCDQSS”

But a new part comes out that specifies a “low” value, but your hardware chose a “high” value….

Cycles	CE#	ALE	CLE	WE#	RE#	DQ OE	DQ IE	DQ TE	DQ	DQS
tCDQSS	0	1	1	0	0	1	0	0	0	0
tWPRE	0	0	0	1	1	1	0	0	0	0
…										

Example 2: Solution

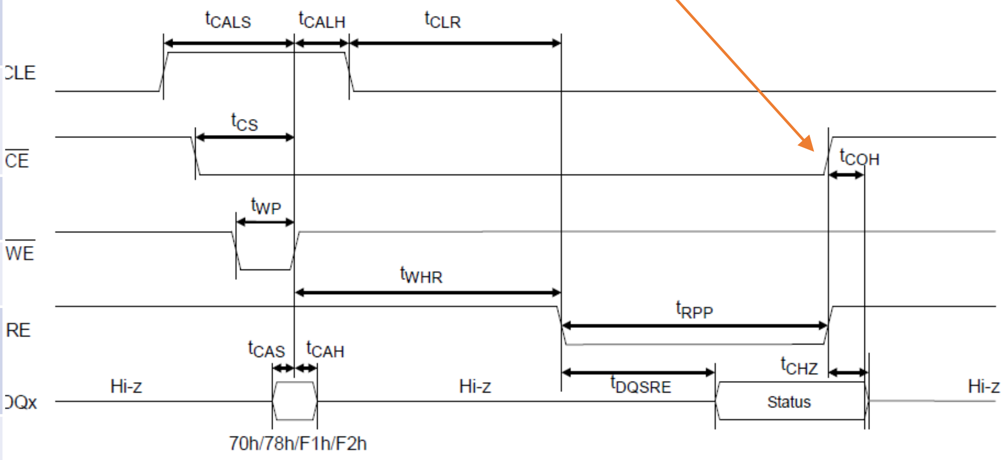


Cycles	CE#	ALE	CLE	WE#	RE#	DQ OE	DQ IE	DQ TE	DQ	DQS
tCSD	1	0	0	1	0	0	0	0	0	0
tRPSTH	1	1	1	1	0	0	0	0	0	0
…										

Unusual Read Status Example

Cycles	CE#	ALE	CLE	WE#	RE#	DQ OE	DQ IE	DQ TE	DQ	DQS
tCALS-tCS	1	0	1	1	1	0	0	0	0	0
tCS-tWP	0	0	1	1	1	0	0	0	0	0
tCAS	0	0	1	0	1	1	0	0	0x70	0
tCAH	0	0	1	1	1	1	0	0	0x70	0
tWHR-tCAH	0	0	0	1	1	0	0	0	0	0
tRPP	0	0	0	1	0	0	1	1	0	0
tCOH	1	0	0	1	1	0	0	0	0	0

CE Raised?
No Problem....



Conclusions

- Using VCD Format we can use software to control the NAND Protocol
  - Future proof
  - Fix errors in software
  - Optimize every cycle for specific RAM types
  - Adjust to vendor specific requests
- Implemented in Microchip Flashtec® NVMe® 5016 (Performance 16-Channel Gen 5 PCIe® Flash Controller)

Thank you!

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