

### CXL 2.0 Use Case Using Both DDR4 & DDR5 on the Same Server to Allow Memory & Bandwidth Scaling

Presented by: Geof Findley, WW VP Sales & Business Development

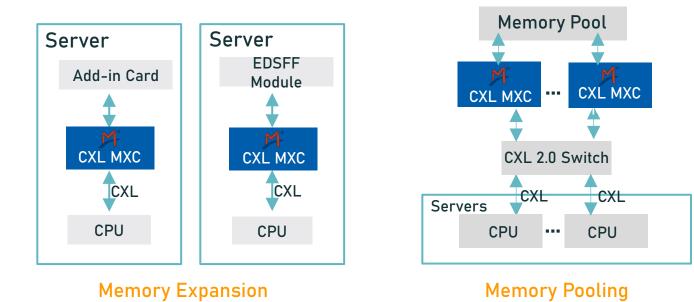
# About Montage Technology



- More than 20 years in memory products leading the industry on DDR4 and DDR5 memory interface products
- PCIe Gen 4 and 5 Retimer portfolio with design wins around the world
- Leading in shipments and mass production of CXL controllers.
- Ecosystem enabling in cloud computing & data center markets

### CXL technology-based solutions available today and future products in the pipeline!

# **CXL Adoption in the Datacenter**





- Industry's leading Type 3 CXL Memory eXpander Controller (MXC)
- Providing high-bandwidth and low-latency interconnect between CPU and CXL-based devices to enable memory expansion and pooling for data centers
- Compliant with DDR4/DDR5 JEDEC and CXL 2.0 specifications, supporting PCIe 5.0 speeds
- Designed for use in Add-In Card (AIC), EDSFF Memory Module and CXL pooled memory

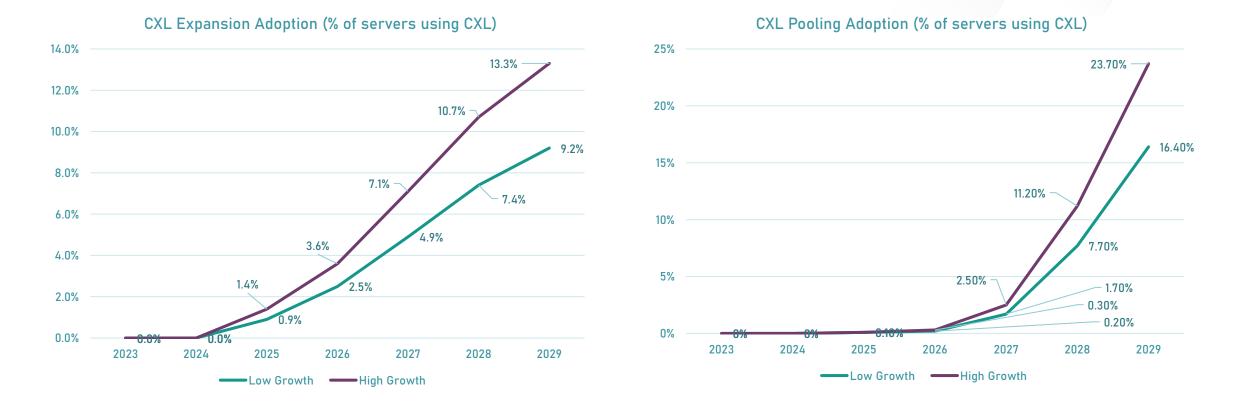
Compute

Express

## **CXL Adoption in the Datacenter**

Compute Express Link®

Expansion usage is being challenged by 32Gb monolithic die (and corresponding 128GB RDIMM) & the emergence of MRDIMM (with higher bandwidth).

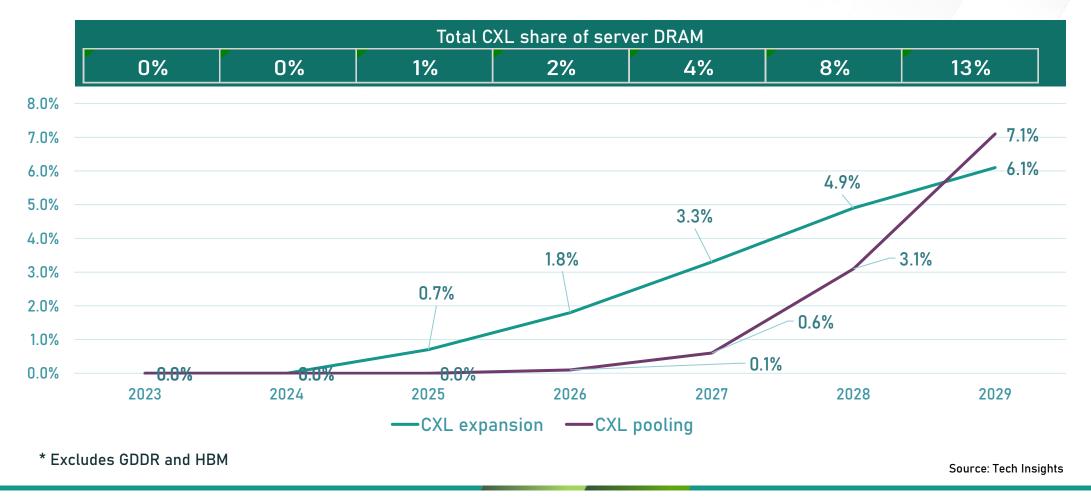


Source: Tech Insights

## CXL Share of Server Bit Demand

#### DRAM behind CXL will grow to ~10% of server DRAM by 2029.

#### Share of server bit demand\*



Compute

Express

Compute Express Link® and CXL® are trademarks of the Compute Express Link Consortium.

Compute

Express

### CXL Memory eXpander Controller: MXC

#### Industry's Leading Memory Expander Controller

- CXL Type 3 Memory Expander
- CXL 1.1/2.0 compliant
- PCIe Add-In Cards
- Backplane
- EDSFF memory modules
- DIMMS or soldered down Memory
- DDR4-3200 and DDR5-6400
- Rich RAS features supported
- High BW utilization & efficiency
- Ultra Low power optimized for Modules

#### Module Partners TODAY...

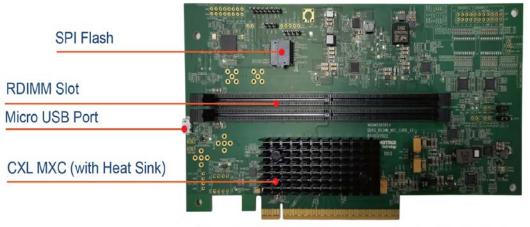
- Samsung
- SK hynix



### MXC Features



The MXC provides *high-bandwidth and low-latency interconnect* between the CPU and the CXL-based devices, allowing them to share memory for higher performance, reduced software stack complexity, and lower data center TCO.

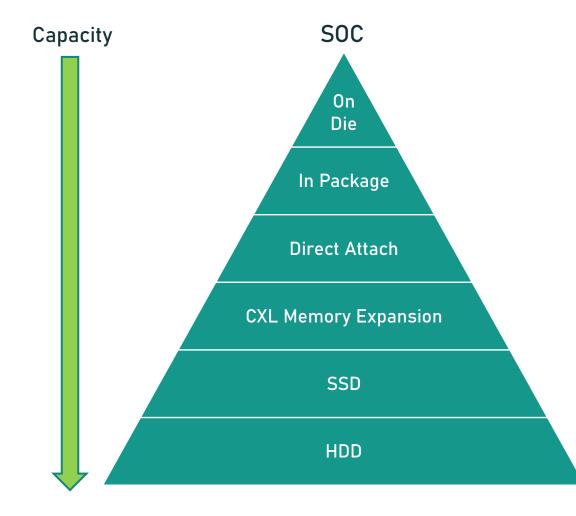


CXL MXC Evaluation Board (DDR5 RDIMM)

- CXL Type 3 Memory eXpander Controller
  - Integrated CXL Controller
  - DDR 4/5 Controller
  - RISC-V micro-processor
  - On-Chip PVT Sensor
  - SMBus, I3C, I2C, SPI Interfaces
  - 767 ball FCCSP package
- CXL Controller
  - Compliant with CXL 1.1 and CXL 2.0 RAS specifications
  - Supports CXL.mem and CXL.io protocols
  - X8 PCIe 5.0 interface up to 32GT/s
  - Rich RAS features
- DDR Controller
  - Compliant with JEDEC DDR4/5 standards
  - Supports DDR4/5 UDIMM, RDIMM, soldered down DRAM
  - Supports DDR4-3200 and DDR5-6400
  - Low-power consumption
  - Optimized DDR I/O equalization
  - Programmable I/O impedance

### MXC Performance





Direct Attach Memory is not able to keep up with the capacity requirements per core.

#### CXL Memory Expansion addresses this issue!

- 4 ranks DDR5 per sub channel
- Two 40bit DDR5 Sub Channels
- One 72-bit DDR4 channel
- 2 DIMMs per channel
- Accommodate up to 80 DRAM placements
- Low Power
- 1.28TByte Capacity with 3DS DRAM
- Latency Optimized to 1 NUMA hop

### MXC Readiness – Components Available Now



#### **Status**



🛹 All major memory suppliers

Contact your module provider for solution availability.





8/28/2024

Technology



### Now is the time to invest in CXL!

- The MXC CXL controller is available from Montage today, both as raw silicon and on a reference board.
- Add-in card, such as those offered by Samsung & SK Hynix, are available today.
- Servers with CXL slots are being offered by all major OEMs.
- Demonstrations are available showcasing CXL's increases in performance for memory-bound applications.
- View our demo featuring multiple suppliers with multiple technologies & speeds – all working on Intel's latest platform – in the Exhibitor Area!



Thank You

Compute Express Link® and CXL® are trademarks of the Compute Express Link Consortium.