



the Future of Memory and Storage

SFF: Connecting Everything Together

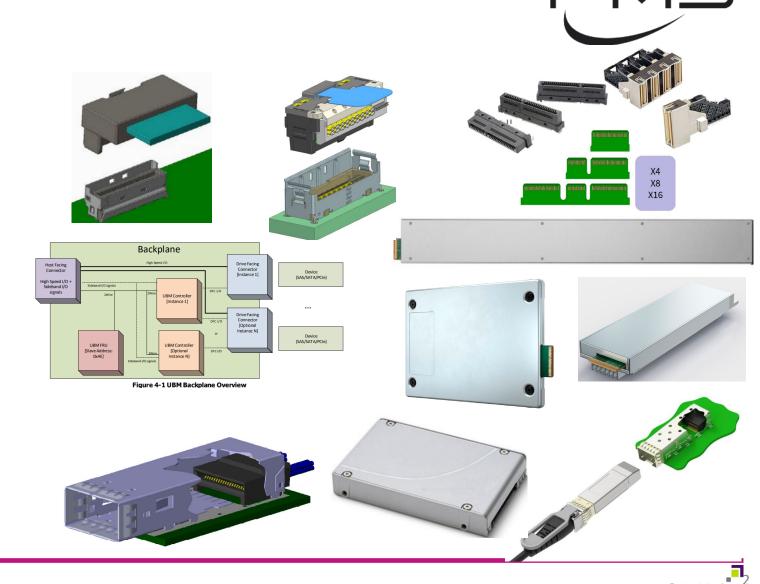
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Co-chair of SNIA SFF TA



You may not know SFF, but you know our work

- SFF TA TWG develops technical specifications covering:
 - Cables
 - Connectors and cages
 - Form factors
 - Management interfaces
 - Copper transceiver modules
 - Optical transceiver modules
 - Electrical interfaces



Who Are We?



76 member companies



150+ published specs



Specifications used everywhere



In the last <u>year</u>, we:

<u>Published</u> 5 new specifications

<u>Revised</u> 7 existing specifications



Example: Server Storage and CXL Memory



- Problem: Existing storage form factors did not meet needs of future usages
 - **Result:** EDSFF (E1.S, E1.L, E3)
- New problem: Scale for higher speeds?
 - Result: Added PCle 5.0, 6.0 support, Thermal characterization spec, E1.S expanded skus
- New Problem: Need for new usages
 - Result: E3 NICs, JEDEC CXL Module support



Challenges to Address











Need More NVM Sites

less packages/SSD = more dies/package = lower yield/package

Support SSDs and MORE

Legacy connectors have been SSD only.

Optimize for NVM

Legacy form factors in Enterprise and Datacenter based on HDDs or client SSDs.

Thermals and TCO Matter

Legacy SSDs not thermally optimized. Airflow to CPU restricted.





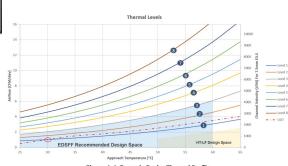


Figure 4-4: Example Device Thermal Profile

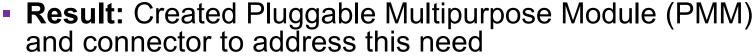


Example: Al Form Factor

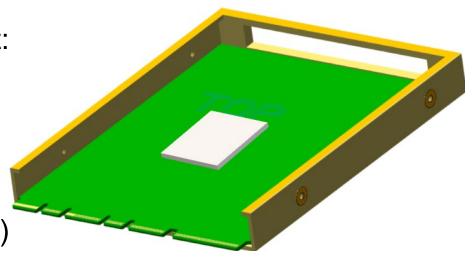


• Problem: Form Factors for AI are missing a sweet spot:

- Serviceability
- Power
- Lane count
- Stranded lanes



- Support for NICs, XPUs, CXL
- Front/rear loadable
- 600W support
- 32 lanes
- Lane subdivision and directional configurability
- Compatibility to OCP NIC 3.0 and EDSFF (via interposer).

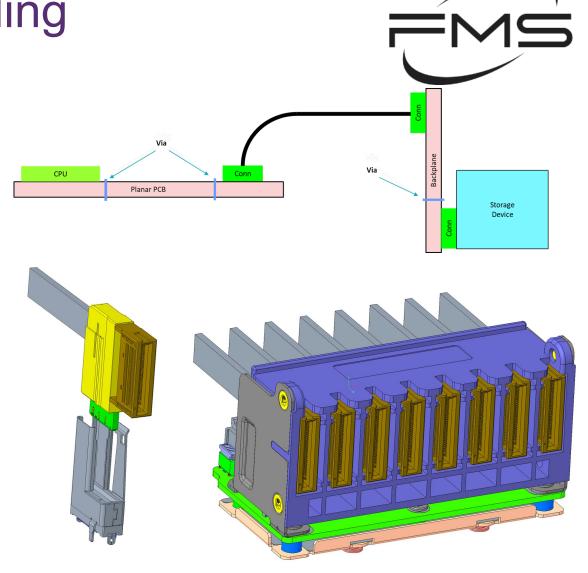


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Example: PCIe Storage Signaling

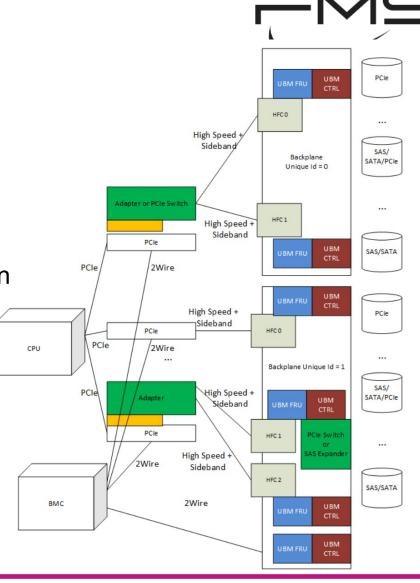
- Problem: Current SI budget forces system vendors to very expensive low loss PCB materials or the addition of PCIe retimers
- Result: Ortho-Hybrid Connector (found in SFF-TA-1016)
 - Eliminates the backplane SI component
 - Backplane under connector provides power/sidebands
 - Supports different thicknesses through connector removal
 - Backplane can support x8 by swapping out the connector cage and cables





Example: Backplane Management

- Problem: Traditional backplane management could not scale beyond 8 devices and did not support PCIe needs.
 - Result: SFF-TA-1005 (UBM) was created to offload the host
 - Uses I2C to inform the Host of the backplane configuration
 - Take over former SGIO needs
 - Handles LED pattern generation.
- New problem: New usages and evolving needs
 - Result: Updated to support EDSFF for SSDs, NICs, and CXL Memory devices





Example: Protocol Agnostic Cables

MS

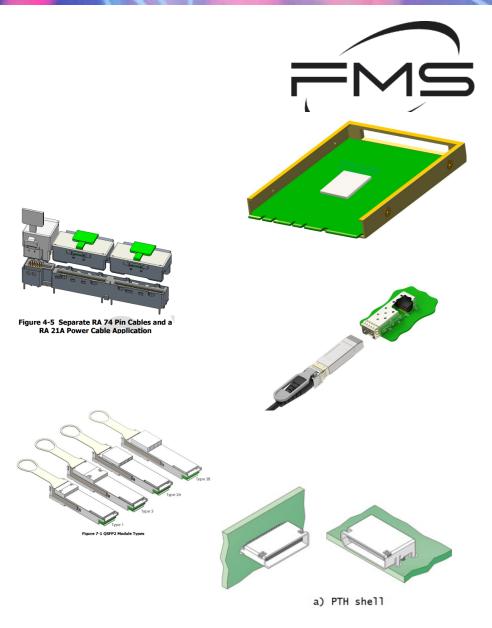
- Problem: How do use same cable for different protocols (e.g., SAS, PCIe)?
 - Solution: Created SFF-9402 for Common naming/direction convention

Control of the second s													
	Root / Controller					Endpoint/ Backplane				Devices on Backplane			
SFF-9400	SFF-8654 (38-circuit) <i>Q/P</i> SAS-4	SFF-8621 (42-circuit) OCuLink / SAS-4	9402 Multi-Protocol (OCuLink, Other Protocol (Q/P), SAS-4)) x4 Cab le Interface OCuLink and SAS-4/ SFF-8448 Sign al Names		CABLE	(OCuLink, Other Protocol (O/P), SAS-4)) x4 Cable Interface OCuLink and SAS-4/ SFF-8448 OCu		SFF-8621 (42-circuit)	SFF-8654 (38-circuit) <i>Q/P</i> SAS-4	SF F-8639 Connector			
Type1 4X								OCutink/ SAS-4		Quad PCI Express® (x4)	SFF-TA-1001 (x4)	MultiLini SAS™	
	PIN	PIN	ROOT	Controller	DIR	Endpoint	Backplane	PIN	PIN	PIN	PIN	PRI	
RSV	9	AI	POWER 3.3 Vact RX	RESERVED	NO WIRE	POWER 5 V#1	RESERVED	81					
GND	A1	A2	GROUND	GROUND	_	GROUND	GROUND	B2	B1			·	
HS	A2	A3	PER p0	RXO+	+	PETp0	TXO+	B3	B2	E14 (PERp0)	S6 (PERp0)	56 (TXD+	
HS	A3	A4	PERMO	RXO-	+	PETriO	TXO-	B4	B3	E13 (PERnO)	SS (PERnO)	55 (TXO-	
GND	A4	A5	GROUND	GROUND	-	GROUND	GROUND	85	B4				
HS	A5	A6	PERp1	RX1+	+	PETp1	TX1+	B6	B5	521 (PERp1)	S13 (PERp1)	\$13 (TX1	
HS	A6	A7	PERn1	RX1-	+	PETri1	TX1-	B7	B6	S20 (PERn1)	S12 (PERn1)	\$12 (TX1	
GND	A7	A8	GROUND	GROUND	-	GROUND	GROUND	B8	B7				
SB	A8	A9	BP_TYPE(VSP)	BP_TYPE (S87)	++	BP_TYPE(VSP)	BP_TYPE (S87)	89	B8				
SB	A9	A10	CWAKEN,OBFF (VSP)	RESET, SDataOut (SB4)	++	CWAKE#,OBFF/(VSP)	RESET, SDataOut (SB4)	B10	B9	P1 (WAKE#)	P1 (WAKE#)		
SB	A10	A11	GND	GND (S83)	-	GND	GND (SB3)	B11	810			è	
SB	A11	A12	REFCLK+(VSP+)	(S8+)	→	REPCLK+(VSP+)	(S8+)	812	811	E7 (REFCLK+)	E7 (REFCLK+)		
SB	A12	A13	REFCLK-(VSP-)	(58-)	→	REFCLK-(VSP-)	(S8-)	813	812	E8 (REFCLK-)	E8 (REFCLK-)	9	
GND	A13	A14	GROUND	GROUND	1	GROUND	GROUND	B14	B13				
HS	A14	A15	PERp2	RX2+	+	PETp2	TX2+	815	814	S27 (PERp2)	521(PERp2)	S21 (TX2	
HS	A15	A16	PERn2	RX2-	+	PETn2	TX2-	B16	B15	\$26 (PERn2)	S20 (PERn2)	S20 (TX2	
GND	A16	A17	GROUND	GROUND	-	GROUND	GROUND	B17	B16				
HS	A17	A18	PERp3	RX3+	+	PET p3	TX3+	B18	817	E21 (PERp3)	S27 (PERp3)	S27 (TX3	
HS	A18	A19	PERn3	RX3-	+	PETn3	TX3-	B19	818	E20 (PERn3)	526 (PERn3)	526 (TX3	
GND	A19	A20	GROUND	GROUND	_	GROUND	GROUND	820	B19				
RSV		A21	POWER 5 V #2	RESERVED	NOWRE	POWER 3.3 Vact TX	RESERVED	821					
RSV		81	POWER 5 V #1	RESERVED	NO WIRE	POWER 3.3 Vact RX	RESERVED	A1					
GND	81	82	GROUND	GROUND	THU WHILE	GROUND	GROUND	A2	A1				
HS	B2	83	PETIDO	TXD+	->	PERDO	RXO+	A3	A2	E10 (PETp0)	S2 (PETp0)	52 (RXD+	
HS	B3	84	PETINO	TXD-	<i>→</i>	PERINO	RXO-	AA	A3	E11 (PETnO)	S3 (PETnO)	53 (RXO-	
GND	B4	85	GROUND	GROUND	-	GROUND	GROUND	A5	A4	Cas (FEIIN)	30 (FEITO)	30 (1010	
HS	B5	B6	PETp1	TXI+	→	PERp1	RX1+	A6	A5	S17 (PETp1)	S9 (PETp1)	59 (RX1+	
HS	B6	B7	PETn1	TXI-	<i>→</i>	PERn1	RXI-	A7	A6	S18 (PETn1)	S10 (PETn1)	S10 (RX1	
GND	87	B8	GROUND	GROUND		GROUND	GROUND	A8	AZ				
SB	88	89	2W-CLK	2W-CLK, Sclock (580)	↔	2W-CLK	2W-CLK, SClock (SB0)	A9	AB				
SB	B9	810	2W-DATA	2W-DATA, Sload (S81)	↔	2W-DATA	2W-DATA, SLoad(S81)	A10	A9				
SB	B10	811	GND	GND (582)	_	GND	GND(S82)	A11	A10				
58	B11	812	PERST# (VSP)	ADD, SDatain (SBS)	↔	PERSTW (VSP)	ADD, SDatain (S85)	A12	A11	E5 (PERST#)	E5 (PERST#)	8	
SB	812	813	CPRSNT# (VSP)	CNTRLR_TYPE (SB6)	++	CPRSNT#(VSP)	CNTRLR_TYPE (SB6)	A13	A12				
GND	B13	B14	GROUND	GROUND	_	GROUND	GROUND	A14	A13			13	
HS	814	B15	PETp2	TX2+	->	PERp2	RX2+	A15	A14	523 (PETp2)	517 (PETp2)	517 (RX2	
HS	815	B16	PETin2	TX2-	->	PERn2	RX2-	A16	A15	S24 (PETn2)	S18 (PETn2)	518 (RX2	
GND	B16	B17	GROUND	GROUND	-	GROUND	GROUND	A17	A16				
HS	B17	818	PETp3	TX3+	→	PERp3	RX3+	A18	A17	E17 (PETp3)	523 (PETp3)	S23 (RX3	
HS	818	819	PETri3/	TX3-	→	PERn3	RX3-	A19	A18	E18 (PETn3)	S24 (PETn3)	\$24 (RX3	
GND	B19	B20	GROUND	GROUND		GROUND	GROUND	A20	A19				



5 New Projects Completed

- Pluggable Multi-Purpose Module (SFF-TA-1034)
 - Front or rear loadable form factor for general purpose device
- Internal High-Speed Cable / Modular Connector System (SFF-TA-1033)
 - Internal cable/connector solution supporting high-speed and power transmission
- SFP2 Cage, Connector, & Module Specification (SFF-TA-1031)
 - 112Gb/s and beyond Transceiver
- QSFP2 Connector, Cage, & Module Specification (SFF-TA-1027)
 - 112Gb/s and beyond over 4 lanes Transceiver
- MiniLink 4/8X Shielded Connector (SFF-8612)
 - High-speed serial connector for multi-gigabit speeds





7 Projects Recently Revised



- Cables and Connector Variants Based on SFF-TA-1002 (SFF-TA-1020)
- Internal Unshielded High Speed Connector System (SFF-TA-1016)
- Enterprise and Datacenter Standard Form Factor Pin and Signal Specification (EDSFF) (SFF-TA-1009)
- Enterprise and Datacenter Standard Form Factor (E3) (SFF-TA-1008)
- Protocol Agnostic Multi-Lane High Speed Connector (SFF-TA-1002)
- Mini Multilane 4/8X Shielded Cage/Connector (HDsh) (SFF-8614)
- SFF Module Management Reference Code Tables (SFF-8024)



Future SFF Work

EMS

Al Interconnects

CXL Interconnects

Making our specs better

Better Education

The 18 Open Projects

- SFF-TA-1038: Low Profile High Density Flexible Cable Connector
- SFF-TA-1037: Connectors For Pluggable Multi-Purpose Module
- SFF-TA-1036: Cable Optimized Boot Peripheral Connector
- SFF-TA-1035: Next Gen High Speed Cable Connector System
- SFF-TA-1033: Internal High-Speed Cable / Modular Connector System
- SFF-TA-1032: Multi-lane External High Speed Cable System
- SFF-TA-1029: Cabled QSFP Cage & Connector
- SFF-TA-1027: QSFP2 Connector, Cage, & Module Specification
- SFF-TA-1026: Storage System High Speed Cable Interconnect
- SFF-9402: Multi-Protocol Internal Cables for SAS and/or PCIe
- SFF-8679: QSFP+ 4X Hardware and Electrical Specification
- SFF-8665: QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8614: Mini Multilane 4/8X Shielded Cage/Connector (HDsh)
- SFF-8613: Mini Multilane 4/8X Unshielded Connector (HDun)
- SFF-8472: Management Interface for SFP+
- SFF-8419: SFP+ Power and Low Speed Interface
- SFF-8024: SFF Module Management Reference Code Tables
- REF-TA-1011: Cross Reference to Select SFF Connectors and Modules



Getting Involved in SFF



- Come to SDC and bring us your problems: https://www.sniadeveloper.org/
 - Our opinionated experts want feedback
 - Tell us what problem you need solved
 - Tell us what problem we created

Resources:

- How to Join: https://www.snia.org/sff/join
- Public Site: https://www.snia.org/sff
- Specifications: https://www.snia.org/sff/specifications
- Questions about membership? Please send mail to membership@snia.org
- Additional questions? Please send mail to sff_ta_twgchair@snia.org

