

# Memory Market/ IP Licensing Dynamics

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# IP: Memory/Storage



Nvidia Blackwell : [800GB/s embedded](#)  
Decompression engine



## Sample CXL controller: IP Blocks

Accelerators  
(compression,  
encryption)

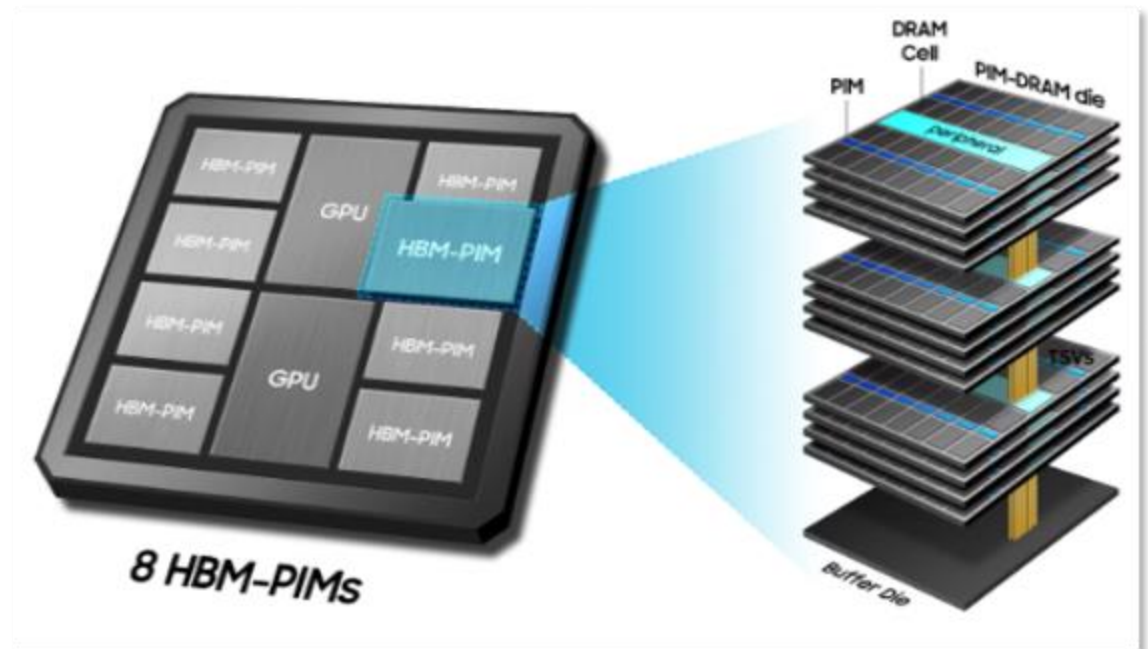
Embedded  
Processors

Block cache

Core(CXL Protocol,  
State Machine, EDC,  
Link)

Other (config, PMU,  
Clk/, RAS, debug)

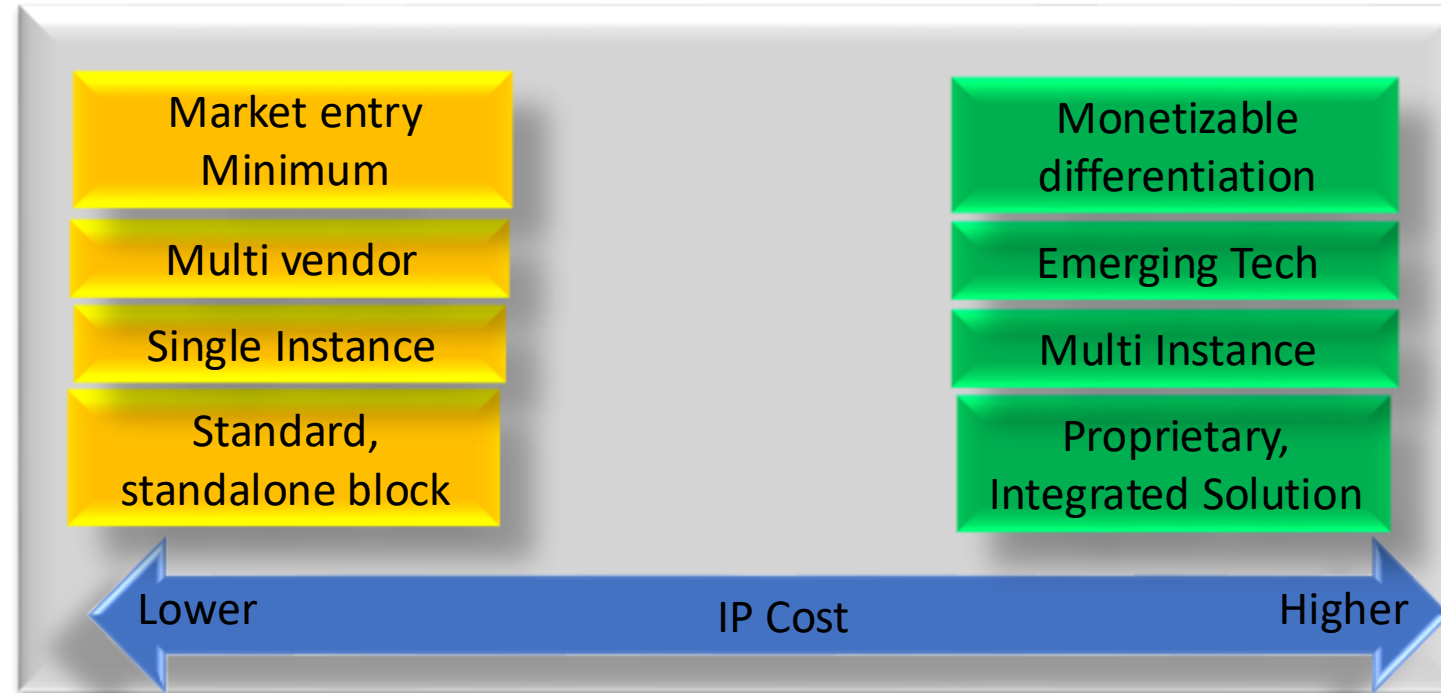
I/F: PCIe, Memory Controller,  
sideband, AXI (internal)



Source: [Samsung](#) HBM PIM (Processing in memory)


# IP: Memory/Storage Dynamics

- TTM (Monetizable Innovation, Reuse, Core competency)
- License fees + tech support v/s Development Headcount
- Ecosystem development, standards, ease of integration
- Shared risk option: NRE + Royalty



# Memory Market Ecosystem

Cloud Provider



Server



Memory



Memory Controller



IP Provider



XPU



Standards



# Memory Market Dynamics

TCO

Cloud Provider

Server

Memory

Memory Controller

IP Provider

Commoditization, multi source, rapid spec evolution

Platform transition  
Node count reduction

XPU  
BW/capacity ratio,  
DRAM + interface pj/bit

Margin, form factor

Spec Stability

Standards

DDR4 retirement timeline,  
recycle transition: BW, Latency,  
capacity \$/GB, form factor

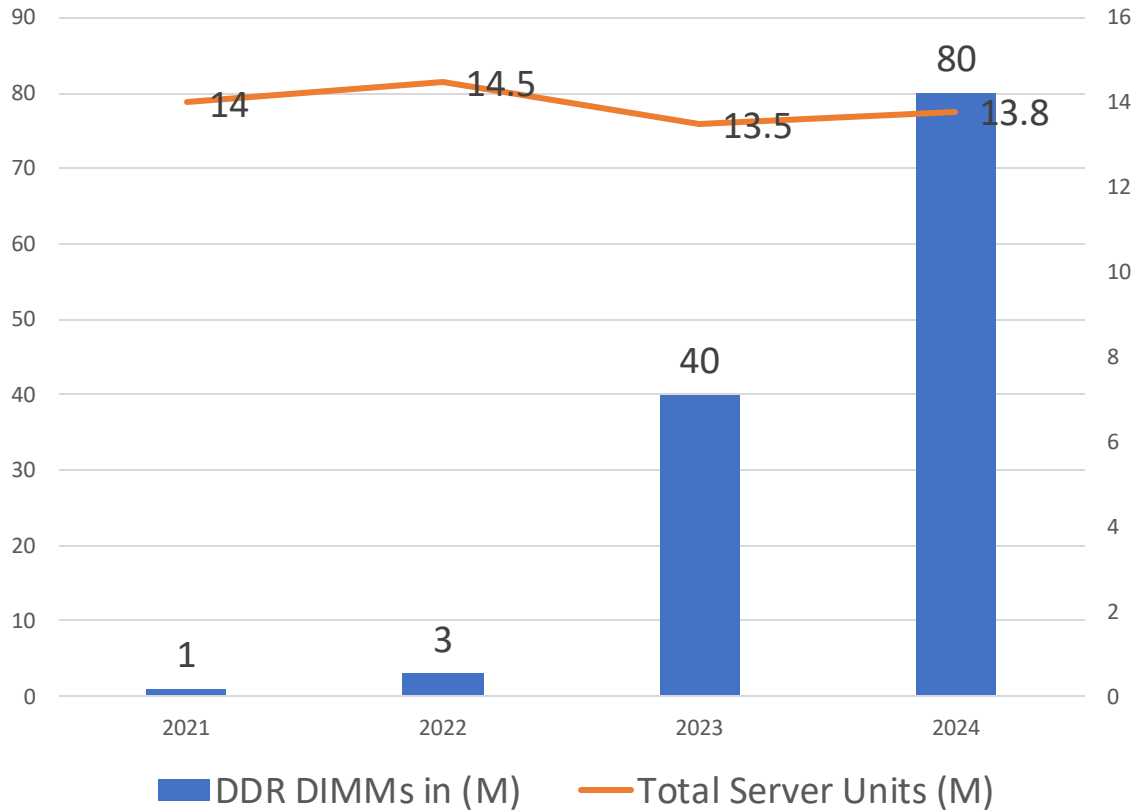
Innovation: caching  
policies, compression,  
3DPC. CSP knobs to own  
their own destiny

Monetizable  
features

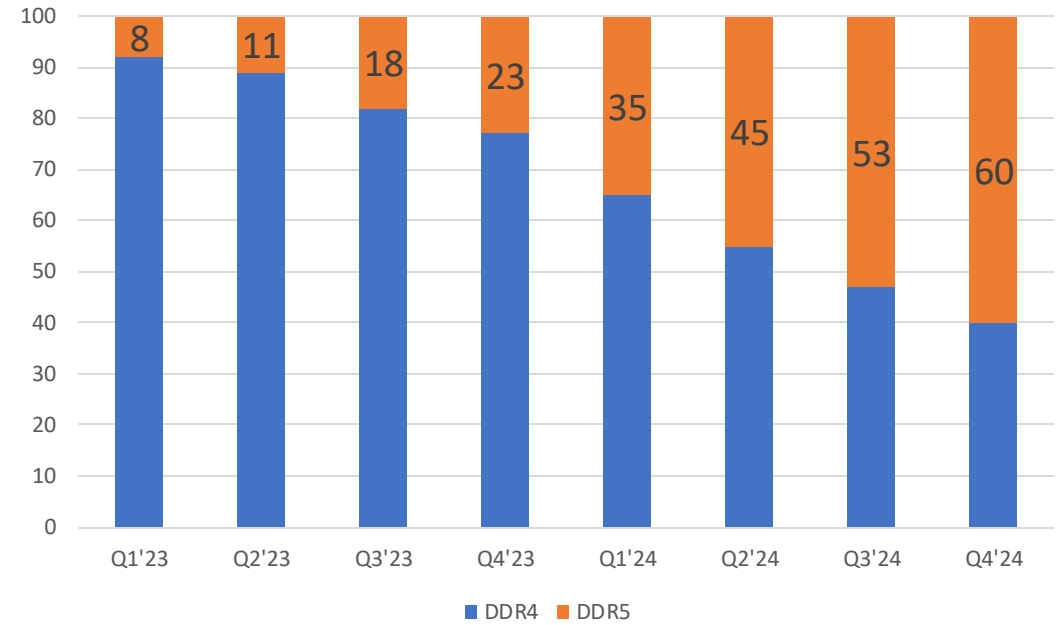


# DDR5 transition

Server DDRM DIMMs (M)



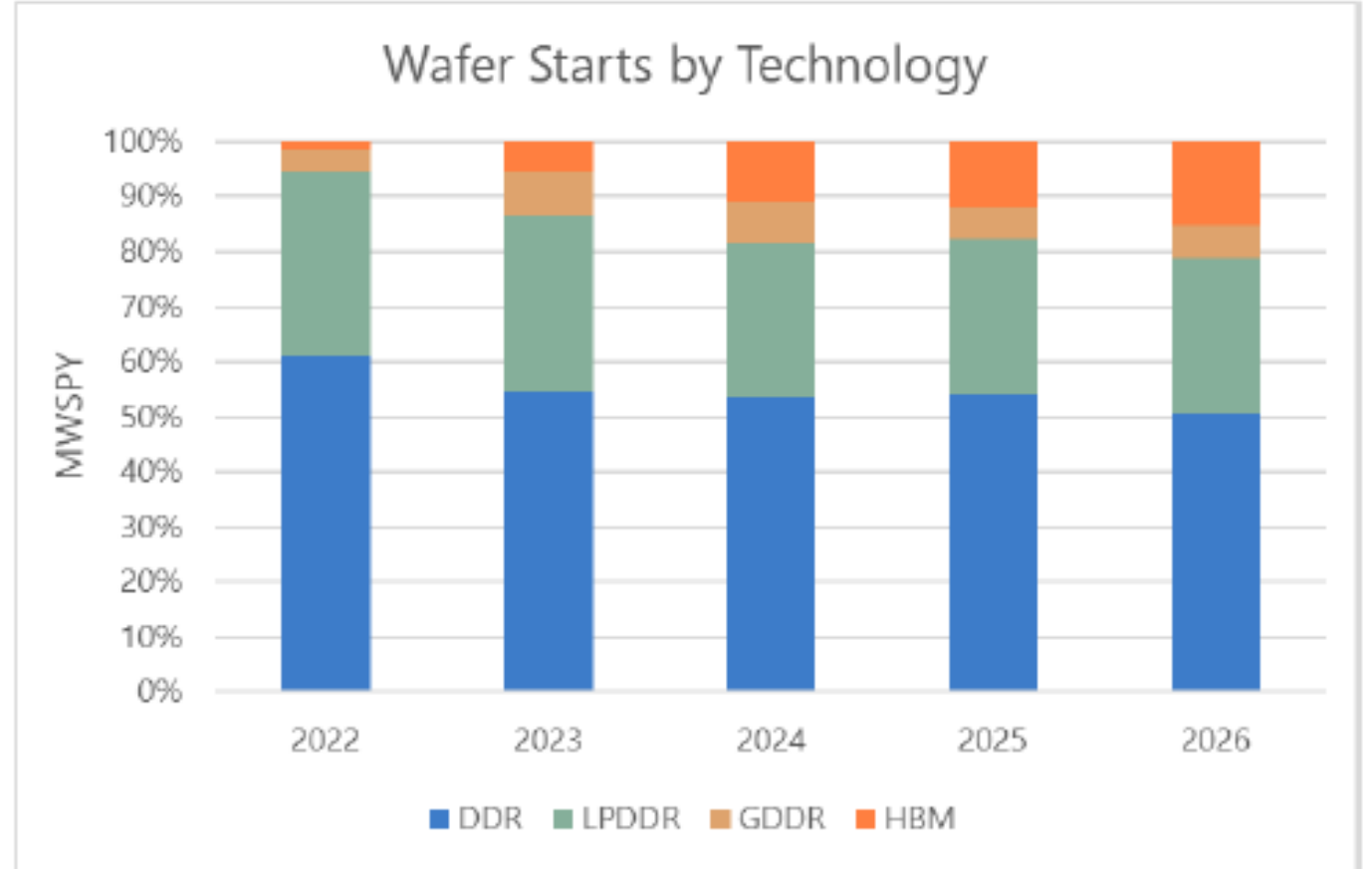
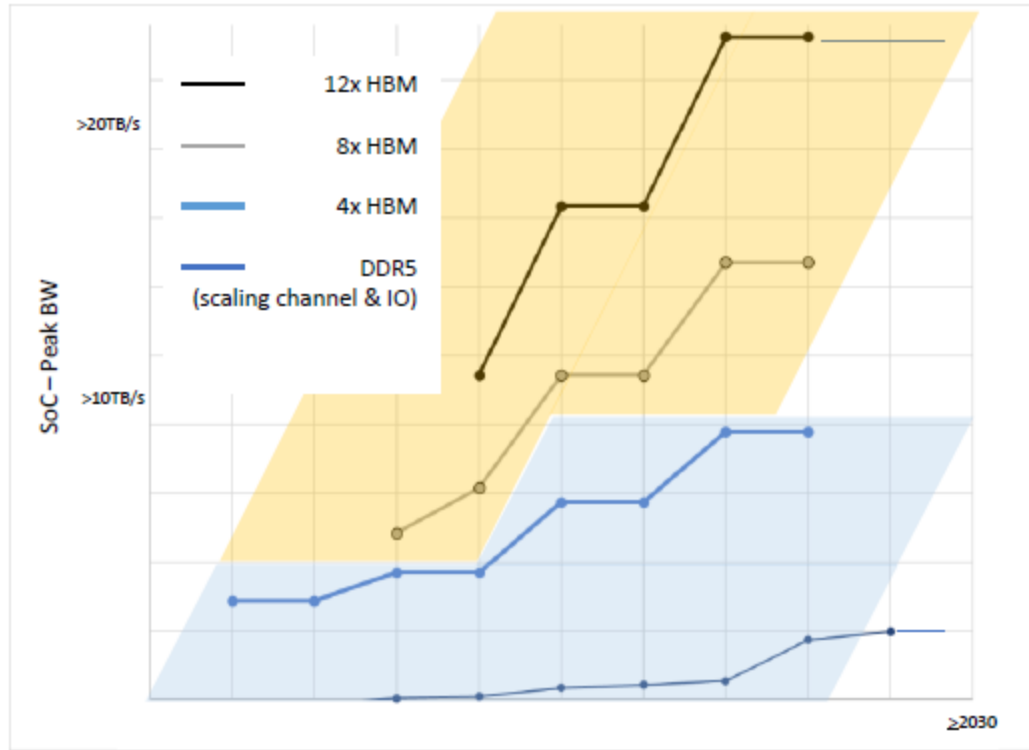
Server DRAM Transition in Percent



Source: Suppliers, Yole, IDC, Montage Technology internal estimates



# DRAM trends: HBM Implications for AI



Source: TechInsights, Intel analysis



# Key Messages/ Call To Action

- Complex dynamics driving Memory, Storage markets
- IP licensing crucial to memory & storage new technology time to market
- Ecosystem Collaboration: Emerging Standards(UAL, UCle, UEC, CXL,etc) + Chiplet technology enable emerging memory types/ new architectures , product innovation opportunities