Flash Memory Summit

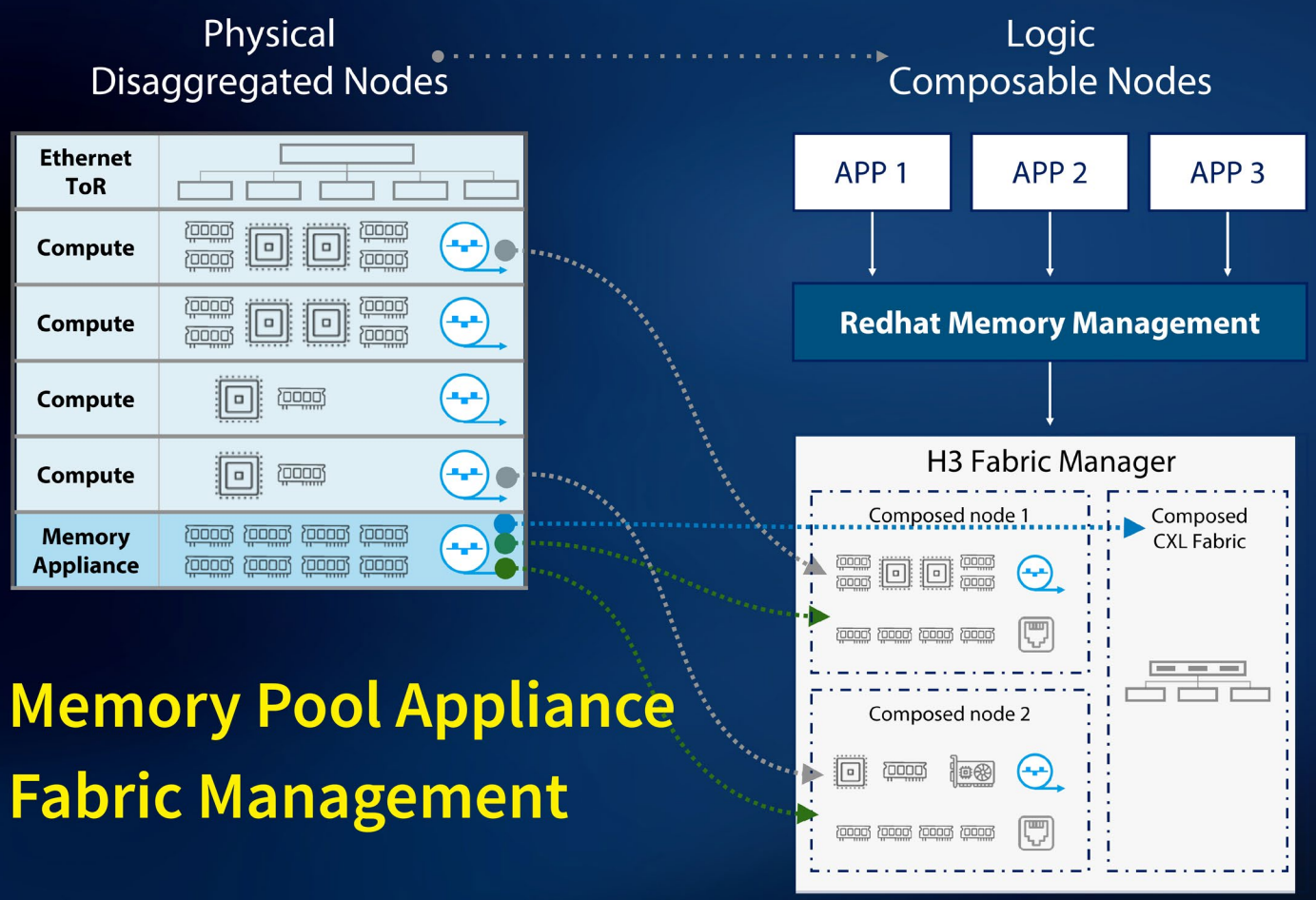
Memory Pooling Solution

H3 Platform
Brian Pan

Agenda

- CXL Solution Architecture
- Key Specification and Features
- Graphic User Interface
- Fabric Management API
- Testing Results

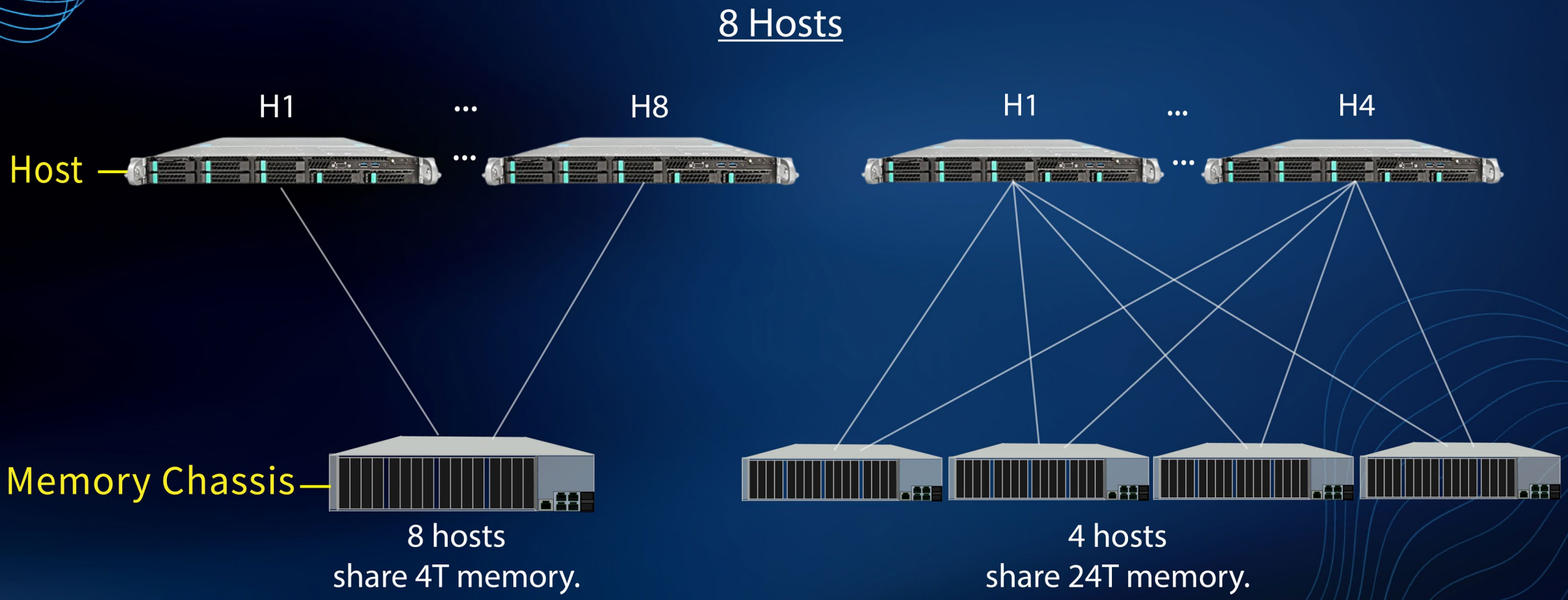
Memory Pooling Solution



Memory Pool Appliance

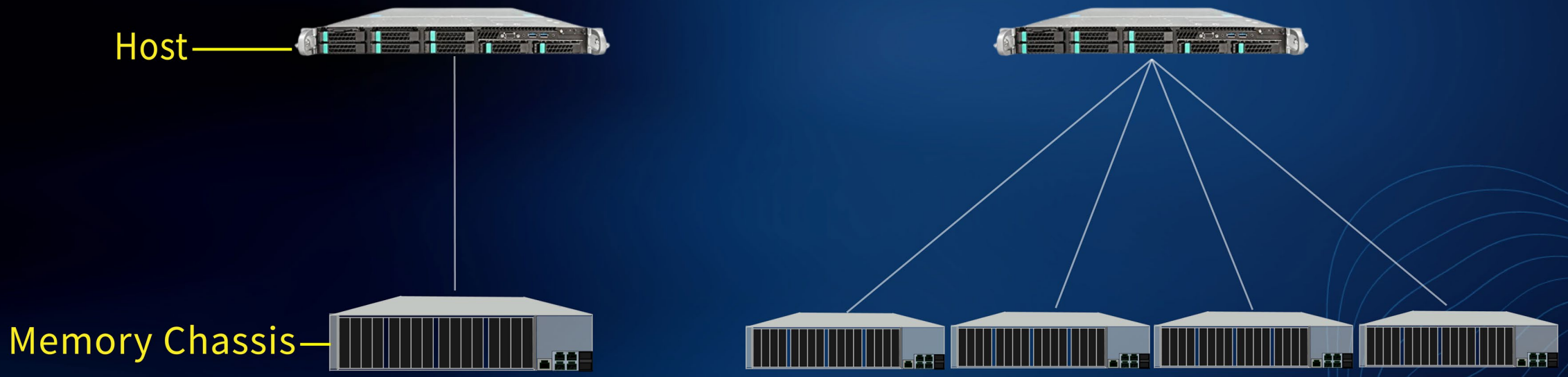
Fabric Management

CXL Memory Pooling/Sharing Usage



CXL Memory Expansion Usage

Single Host



Software Architecture of Fabric Manager

H3 Platform GUI

User Account Management / Enclosure Information / Healthy Status / CXL Memory Resource Management

H3 Platform BMC

Memory Device Information
Enclosure Sensors Information
XCONN Apollo Controller Information
Console Mode Only

H3 Platform RESTful API

GET/POST/PATCH/DEL/CXL/Hosts/xxx
/CXL/Devices/xxx/CXL/MDs/xxx

H3 Platform Daemon 2

Fan Speed / Power / GPIO / LED / Memory Device Information / Enclosure Sensors

H3 Platform Daemon 1

XCONN_CMD_REGISTER / XCONN_CMD_QUERY / XCONN_CMD_ALLOC / XCONN_CMD_ATTACH / XCONN_CMD_FREE / XCONN_CMD_CLEAR / XCONN_CMD_EXIT/ H3_CMD_PORT_INGRESS_QUERY / H3_CMD_PORT_EGRESS_QUERY / H3_CMD_PORT_ERROR_QUERY

Apollo Management over UART

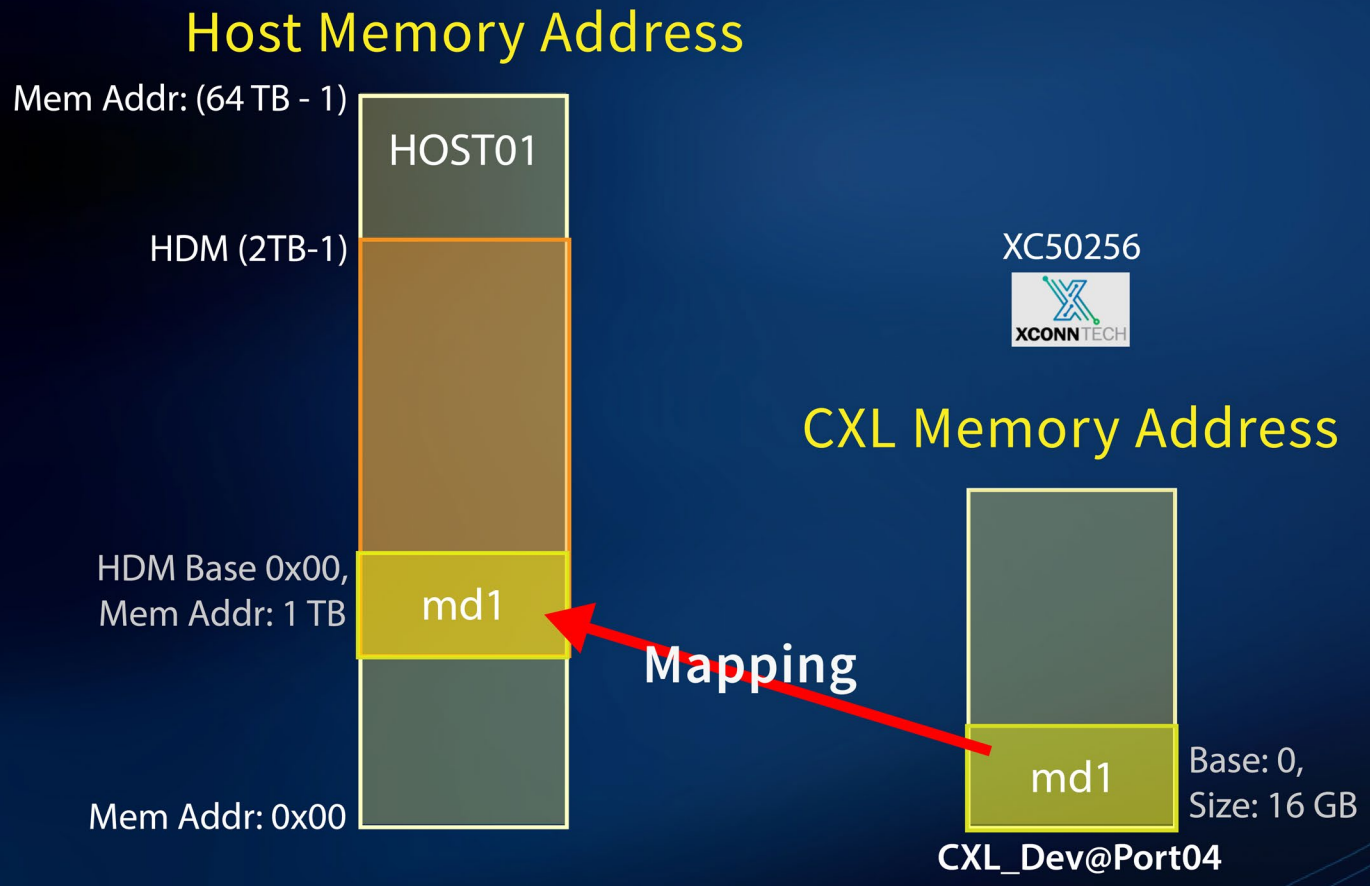
Apollo Management over PCIe
Mgmt. EP PCIe IDs: 1F16-C500 or 144D-A808

Apollo Switch Core

Memory Device
Inband/Outband IF

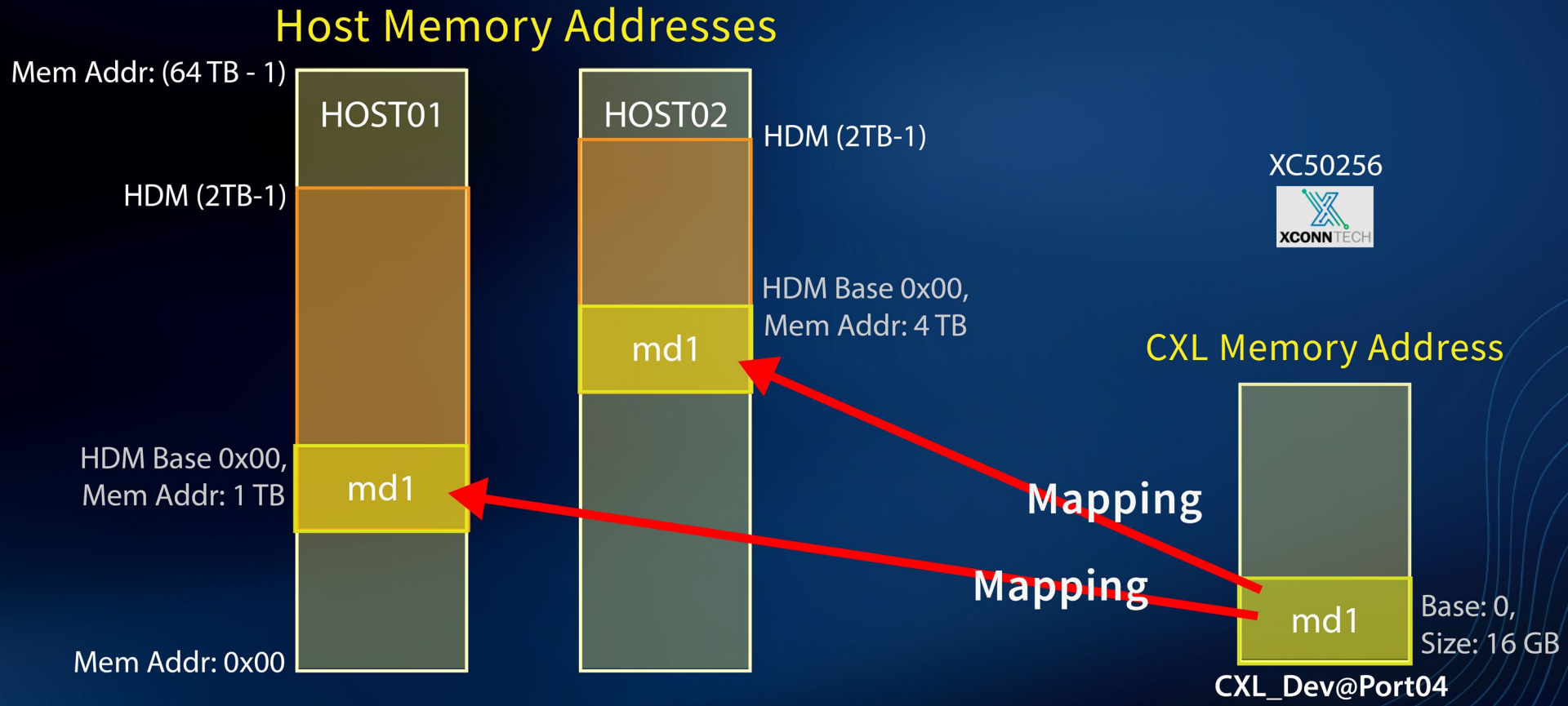
CXL Memory Pooling

Mapping Global to Local Memory Address

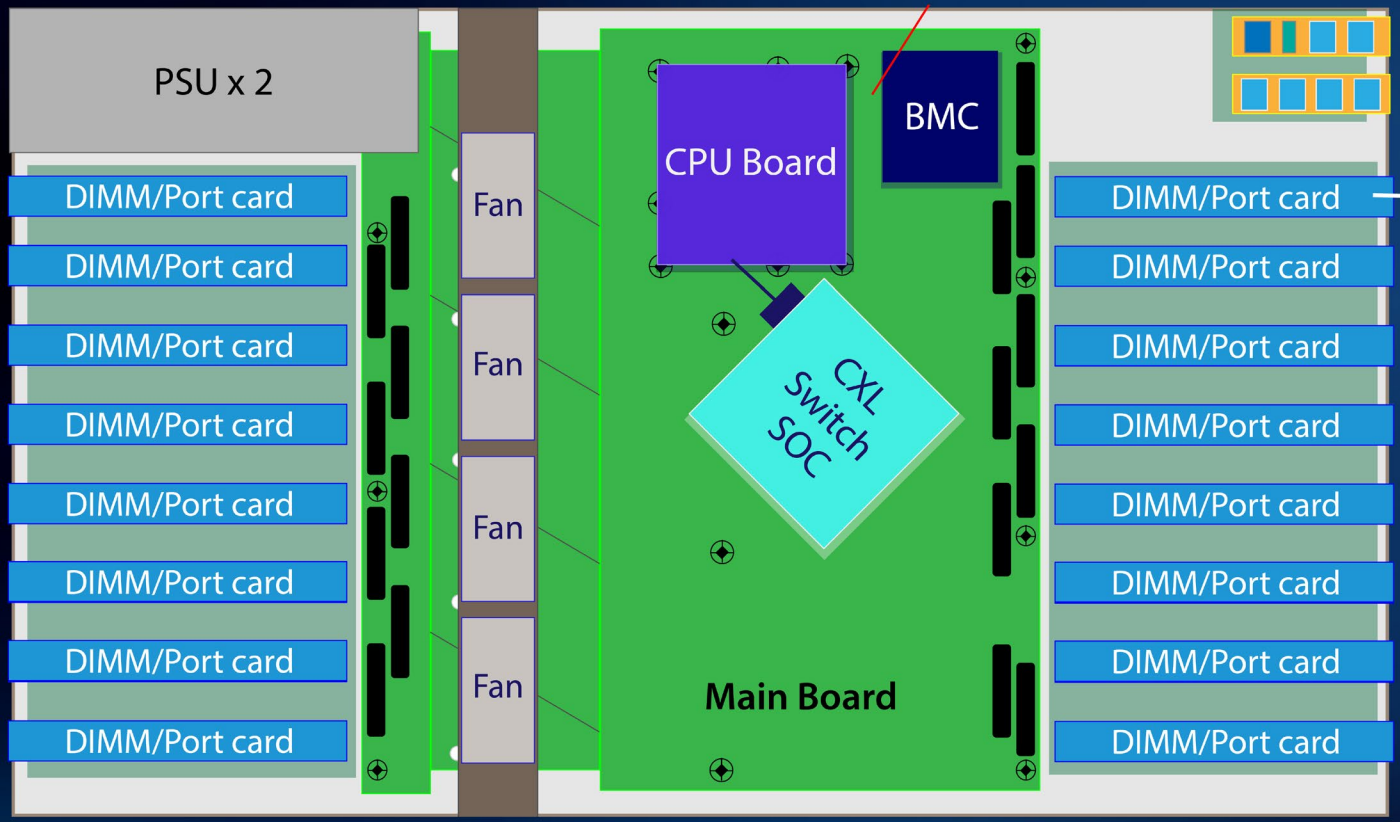


CXL Memory Sharing

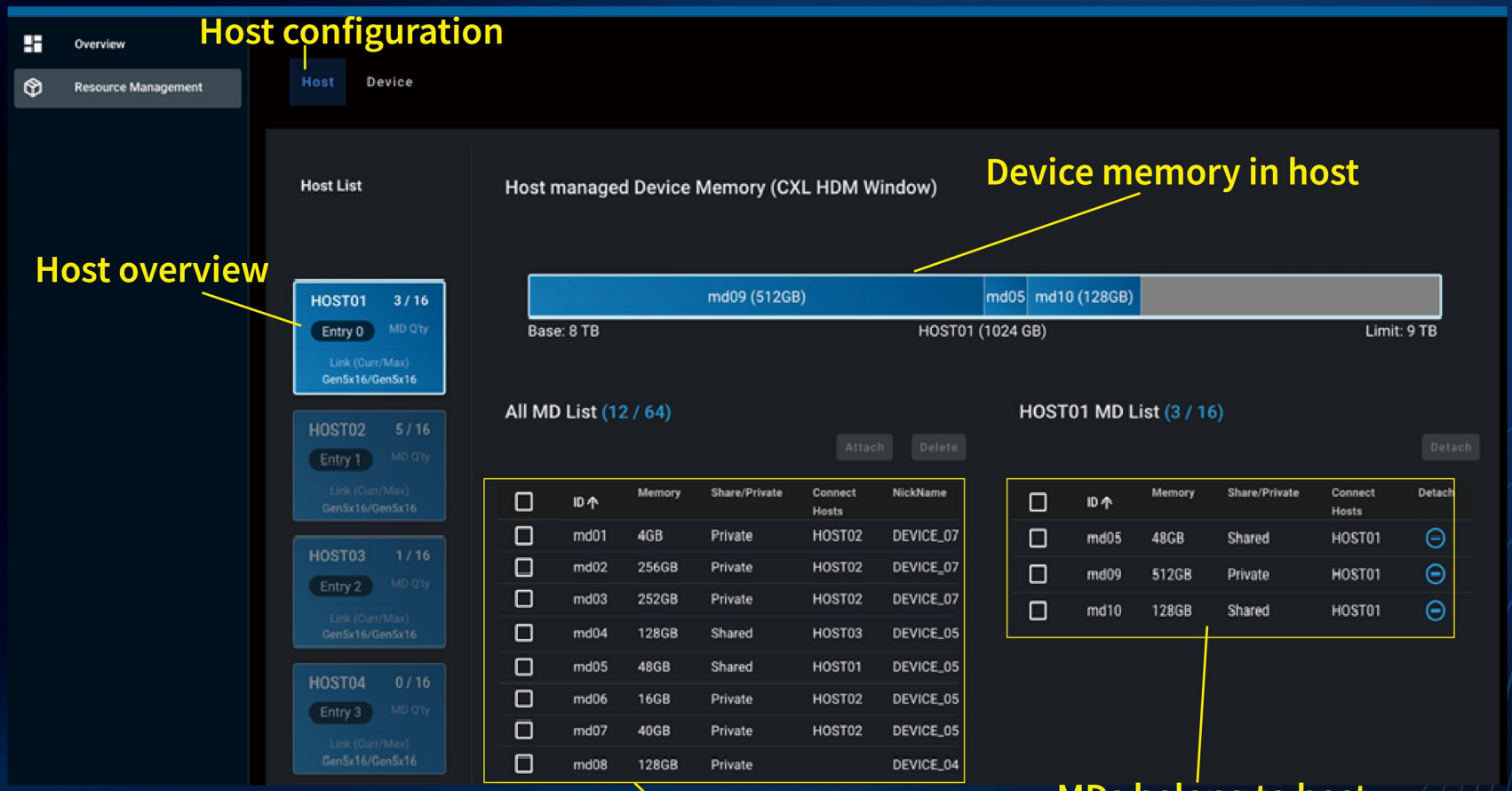
Mapping Global to Multiple Local Memory Address



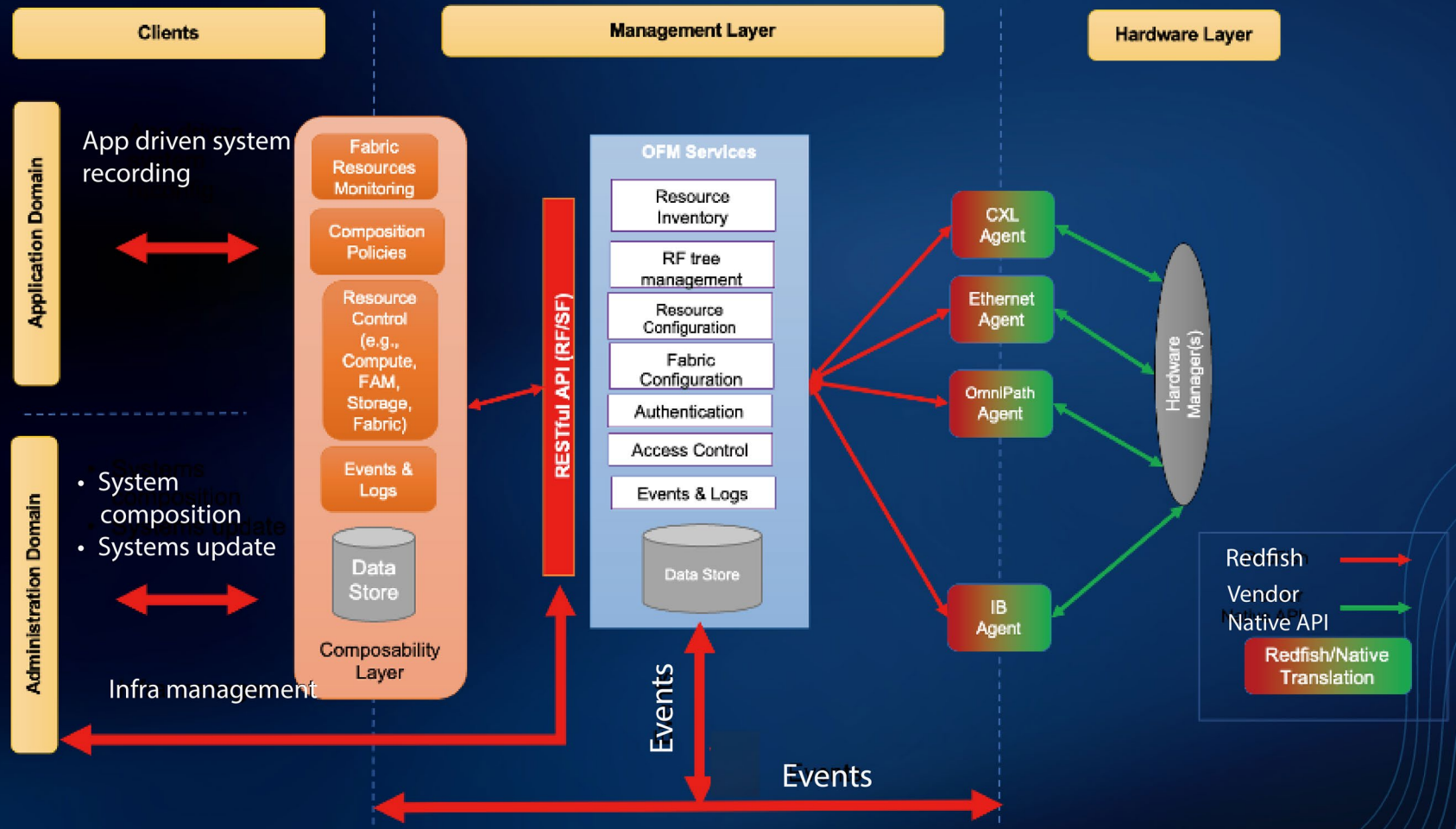
Flexible Port Configuration of CXL Slots



Management User Interface

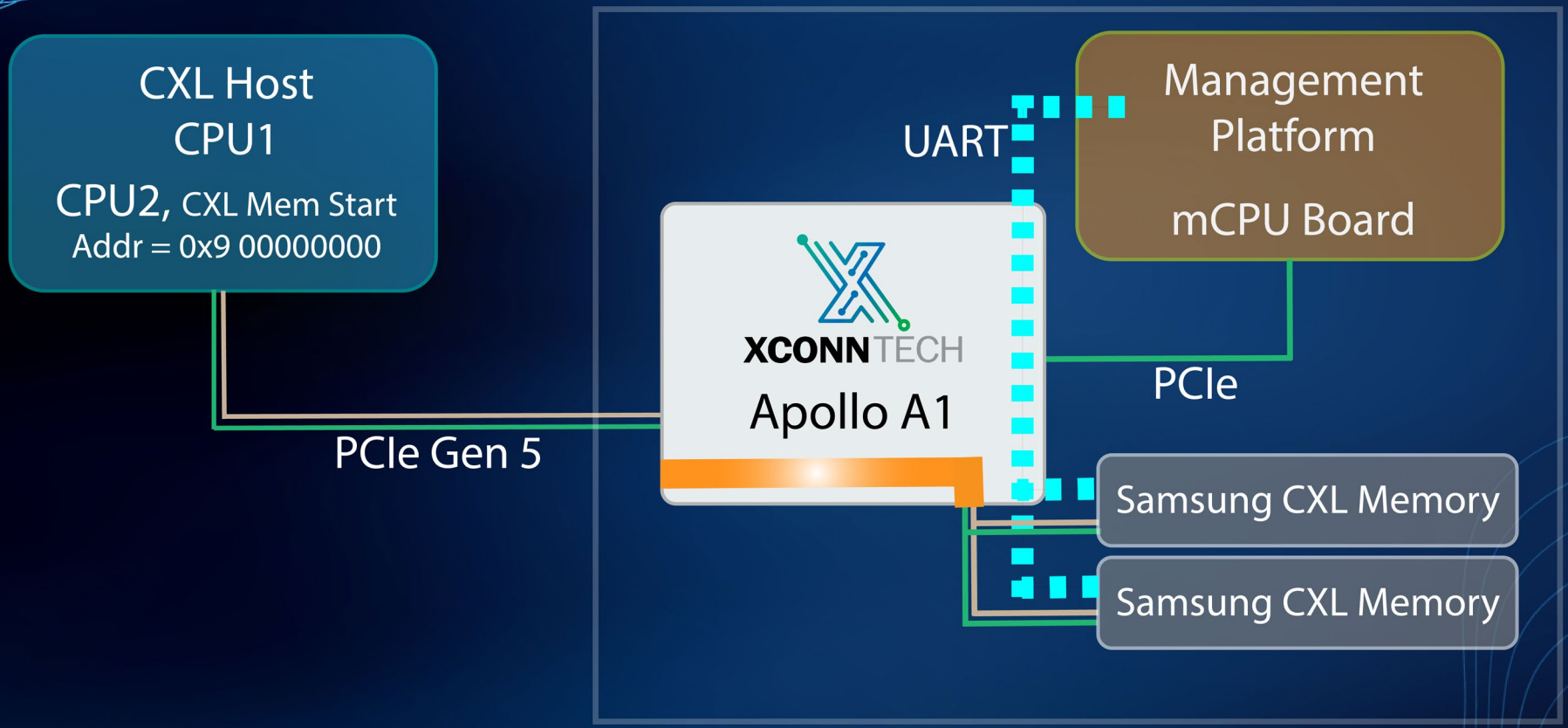


Open Fabric Management Framework



From: Open Fabric Management Framework

Demo System Setup



Memory Pooling Solution

Demo System Specification

Items	Details
Server	• Intel Sapphire Rapids • Dual Xeon 8470 (2000MHz)
CXL Memory	• Samsung 128GB CXL Memory
OS	• Ubuntu 22.04.2 LTE • Linux Kernel 6.2.0-060200-generic • daxctl – version 72.1+ • daxio – version 1.11.1 • mlc – version 3.10

Results of Intel Memory Latency Check

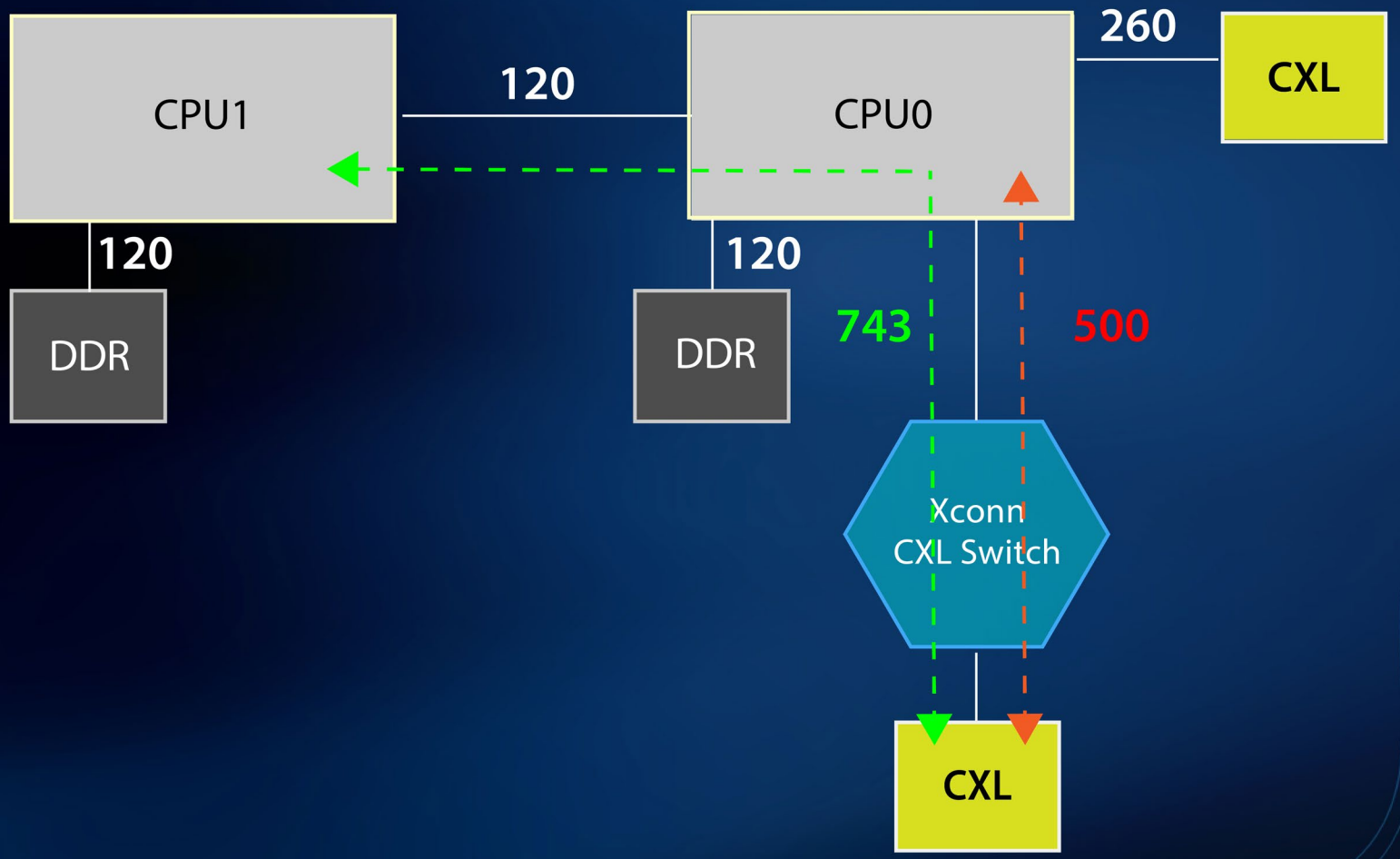
Node	0	1	2
0	10	21	14
1	21	10	24
2	14	24	10

- Node 2 is the Samsung CXL memory module
- The Samsung CXL memory module is connected to the CXL port of Node 0 CPU

Intel MLC Results — Idle Latency (ns)

	DDR	Direct-CXL	Switch-CXL	Note
Node 1	120	260	500	Close Node
Node 2	120	260	743	Far Node
Diff	0	140	240 483	

Intel MLC Results — Idle Latency (ns)



Result Analysis

- Latency optimization
  - CPU
  - **CXL controller**
  - **CXL switch**
  - **Re-timer**
- Latency breakdown
  - Will use the protocol analyzer to break down the latency in each part