

# *DDR5 MR-DIMM Technology*

MR-DIMM: Multiplexed Ranks on DIMM

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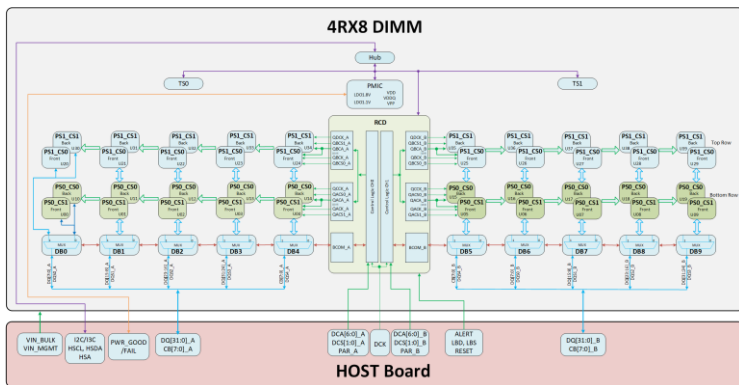
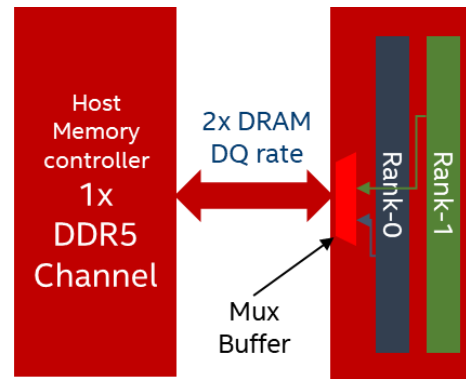


# MR-DIMM Objectives

- Mitigate segment specific BW, capacity gap without burdening mainstream DRAM technology
- Provide seamless BW upgrade for applications looking to exceed DDR5 RDIMM data rates
- Platform compatible with RDIMM for flexible end-user BW configuration.
- Utilize standard DDR5 DIMM ingredients including DRAM, DIMM FF, SPD, PMIC, and TS
- Exploit logic process capability of RCD/DB for efficient I/O scaling
- Leverage LRDIMM ecosystem for design and test infrastructure
- Multi-generational MRDIMM scaling to DDR5-EOL

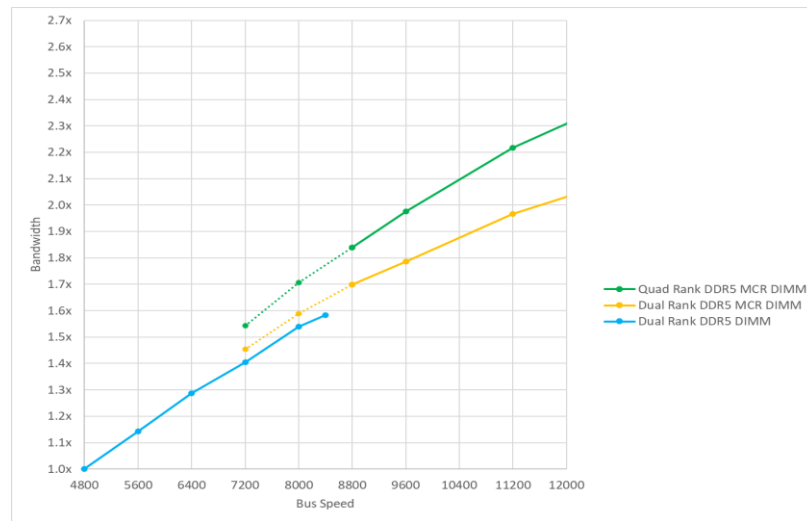
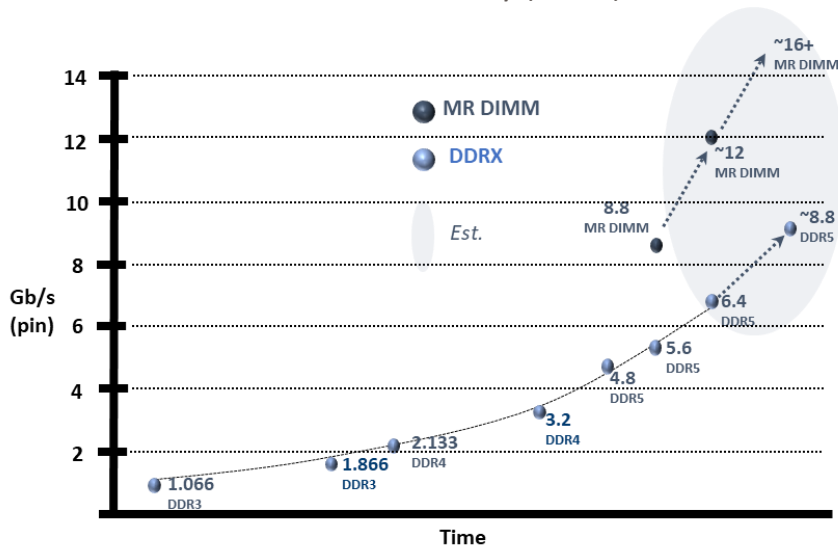
# Technical overview

- Multiplexed Ranks (MR) DIMM doubles host bus BW
- BW doubled by accessing both ranks on a 2-Rank DIMM
- DIMM configured with standard, unmodified, x4 or x8 DDR5 DRAMs
- New RCD maps 2 independent CA access to corresponding ranks (PCH\*)
- New LRDIMM style data buffers with built-in mux/de-mux on Data bus



# MR DIMM Performance and BW scaling

- MR DIMM utilizes BW headroom on point-to-point channel with logic I/O (1DPC)
- BW scaling expected across DDR5 frequencies,
- MR DIMM achieves higher effective BW than RDIMM at iso frequency, by operating DRAM at half the interface speed
- MR DB adds minimal latency (2-3ns) over RDIMM, which is easily offset by the higher MR DIMM speed



# Capacity Scaling: DDP MRDIMM

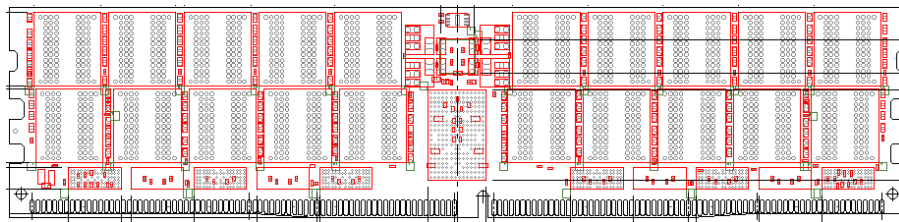
- MR-DIMM supports cost efficient for capacity scaling
  - Wire-bonded DDP (2H stack)
  - No reliance on 3DS technology, which has overhead on mainstream DRAM
  - MR-DIMM doesn't preclude 3DS
- MRDIMM 2:1 Mux divides the DRAM signaling rates on each pseudo-channel by a factor of 2.
  - 8800MT/s MRDIMM -> DRAM DQ bus rate=4400MT/s; DRAM CA bus rate=2200 MT/s
- DDP feasible due to reduced DRAM signaling rate\* on 8800MTs+ MRDIMMs
  - 2 independent Chip select per DDP
- Resulting 4Rx4 configuration fits on standard LP form factor
  - 40 DDP packages (80 DRAM dices)
  - Same MO-329 outline specification as DDR5 RDIMM/LRDIMM
  - Similar PCB structure as 6.4GT/s DDR5 RDIMM

Signals	DDR5-8800	Units
*DRAM Signal rates highlighted		
Host side clock	4400	MHz
DRAM side clock	2200	MHz
BCOM clock	2200	MHz
Host side DQ rate	8800	MT/s
DRAM side DQ rate	4400	MT/s
Host bus CA rate (1N)	8800	MT/s
DRAM side CA rate (1N)	2200	MT/s
Host side CS rate	4400	MT/s
DRAM side CS rate	2200	MT/s
BCOM bus CS rate	2200	MT/s
BCOM bus rate	2200	MT/s

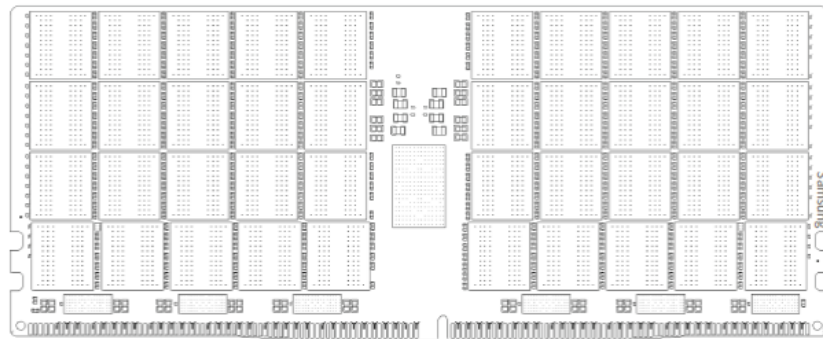
# MRDIMM DIMM configurations

- Multiple capacity and form factor options based on cost, platform volumetric, and power efficiency requirements
  - Supported DRAM types: x4, x8, 3DS and DDP

MRDIMM Capacity/DRAM density			DRAM Package	DIMM Configuration	Ranks/PCH	Raw Card
16Gb	24Gb	32Gb				
32GB	48GB	64GB	SDP	2Rx8	1	2Rx8
64GB	96GB	128GB	SDP	4Rx8	2	4Rx8
64GB	96GB	128GB	SDP	2Rx4	1	2Rx4
128GB	192GB	256GB	3DS-2H	4Rx4	2	SDP, 3DS
128GB	192GB	256GB	DDP-2H	4Rx4	2	4Rx4, DDP
128GB	192GB	256GB	SDP	4Rx4	2	4Rx4, 2U



1U-4Rx4, using DDP



2U-4Rx4, using SDP

# Power and thermal assessment

- 2Rx4 MR DIMM @8.8GT/s consumes ~ 16.5W
- DRAM remains the thermal limiter
- No thermal solution (FDHS) required

Power Contributor	64GB RDIMM (4400MT/s, x4DRAMs)	64GB MR DIMM (4400MT/s, x4DRAMs)
Activate	1.5W	3.0W
Refresh	3.0W	3.0W
Read/Write	1.5W	3.0W
Background	1.0W	1.0W
<b>Total</b>	<b>7.0W</b>	<b>10.0W</b>
<b>+RCD &amp; DQ Buffers</b>	<b>8.0W</b>	<b>15.0W</b>
<b>+ PMIC, 90% eff.</b>	<b>9.0W</b>	<b>16.5W</b>

MR DIMM provides 2x BW with <2x power

# Summary

- MRDIMM is JEDEC standard technology with healthy industry support
- JEDEC specifications for Gen 1 & Gen 2 MR DIMMs are currently underway, targeting 8.8GT/s and 12.8GT/s, respectively
- MRDIMM mux mode scales BW and capacity efficiently over the life of DDR5
  - BW: ~16GT/s, Capacity: 256GB w/ DDP, Tall DIMM; 1TB with 3DS-4H+Tall DIMM
- At iso frequency, MR DIMM achieves higher effective BW than RDIMM
- Future MRDIMMs are backwards compatible to previous generation
- 1U and 2U form factor to support flexible and efficient capacity scalability