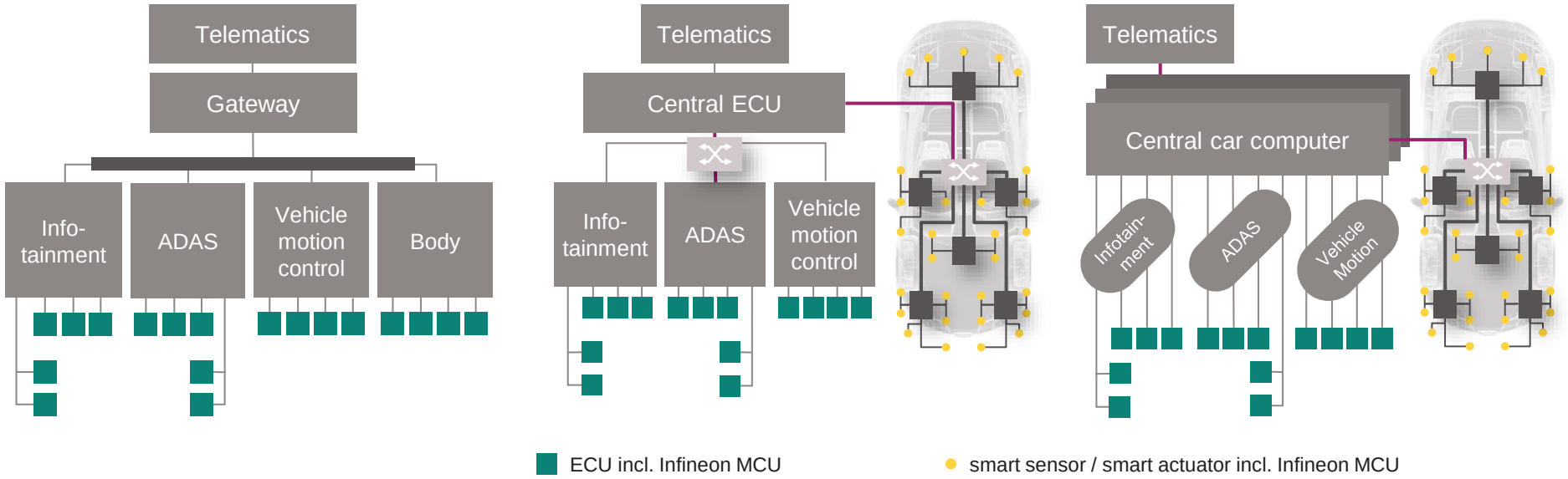
LPDDR Flash:
Enabling automotive E/E architectures

Sandeep Krishnegowda
VP of Marketing
Infineon Technologies

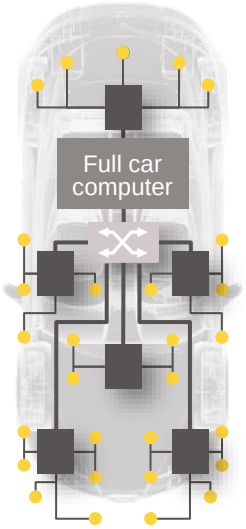
Software-defined cars will become a reality through architectural transformation

Flash Memory Summit

Domain architecture



Full car computer



New E/E architectures offer benefits of:

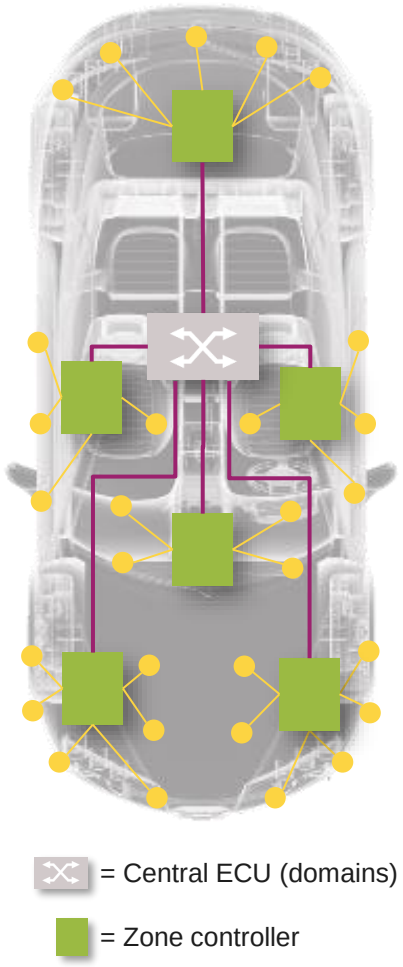
- Hierarchical software
- Fail-operational power distribution
- Optimized power management
- Reduced wiring harnesses

... leading to:

- More smart actuators
- More smart sensors
- Higher redundancy
- Dependable electronics
- **More memory**

... fueling semiconductor growth

Domain and zone controllers consolidate many safety-critical functions, and must process data in real time

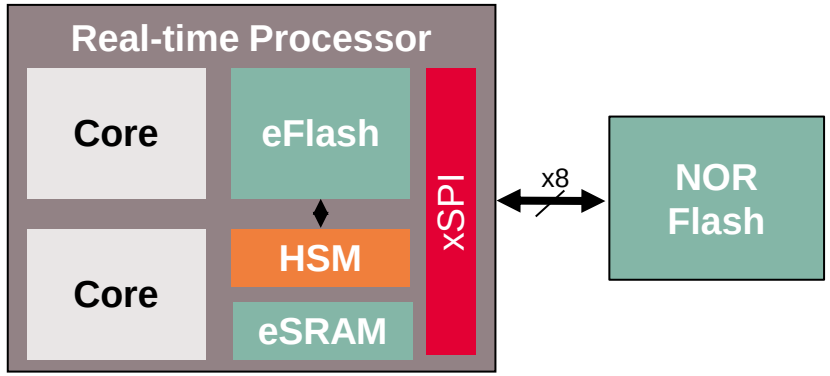


The real-time processors in domain and zone controllers need the performance of advanced process nodes

Real-time processors without embedded Flash need equivalent performance from an external Flash

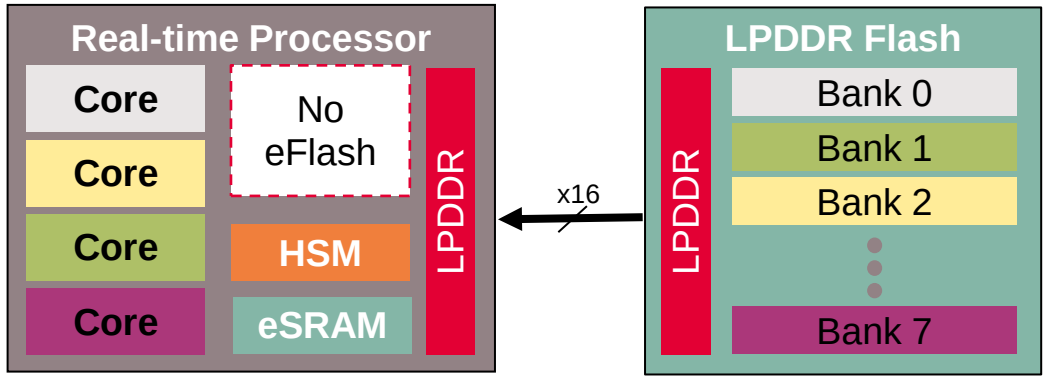
Flash Memory Summit

Traditional: Execute from embedded Flash



Embedded Flash + External Flash
XiP from on-chip eFlash; external NOR Flash used as memory expansion

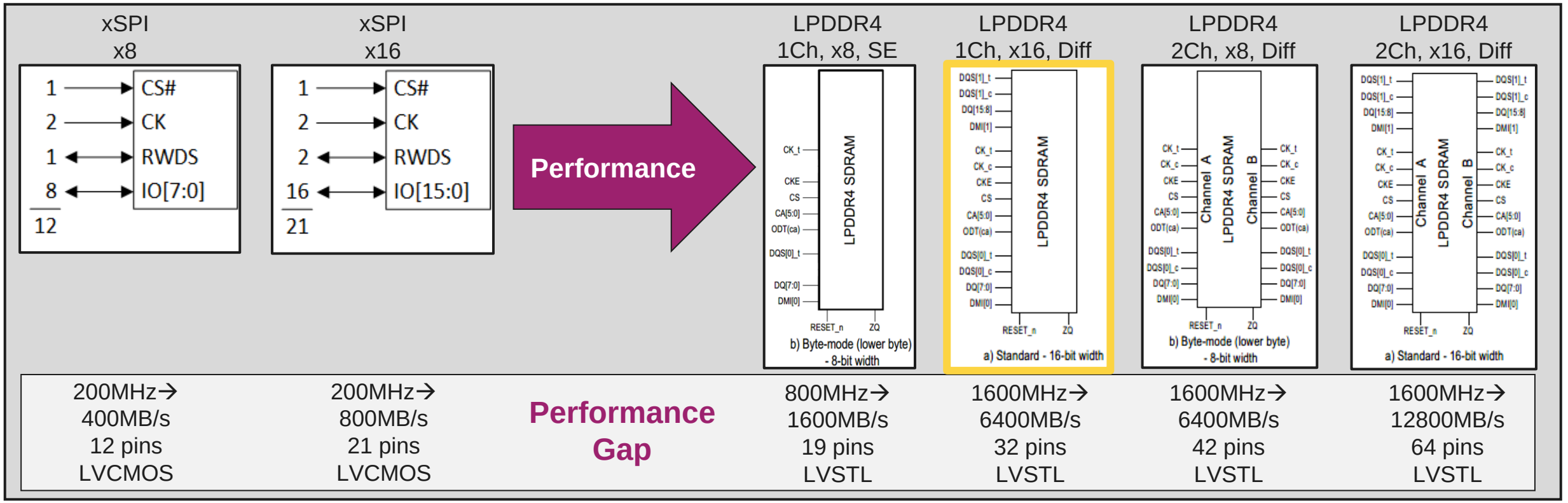
Next Gen: Execute from external LPDDR Flash



Real-time LPDDR Flash
High-performance LPDDR interface enables XiP from external Flash

- At advanced process nodes (e.g. 12nm FF), automotive-qualified eNVM technologies are challenged by high cost (die area, process layers) and lack of scalability
- More memory is needed to support growing code size and complexity
- Standard xSPI NOR flash does not meet real-time execute-in-place (XiP) performance requirements

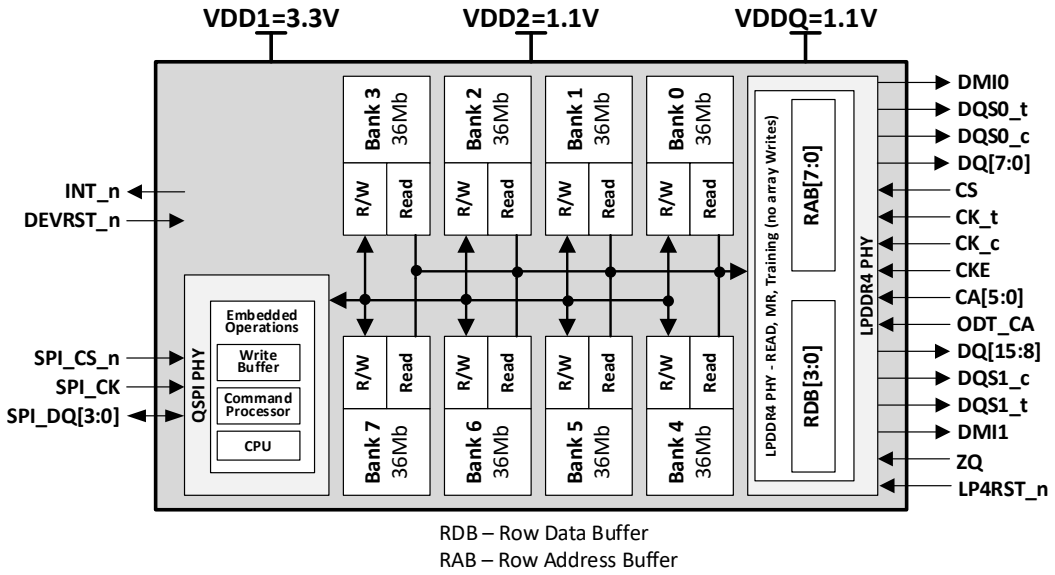
LPDDR4/4X interface offers the scalability and performance required for direct code execution from external NVM device



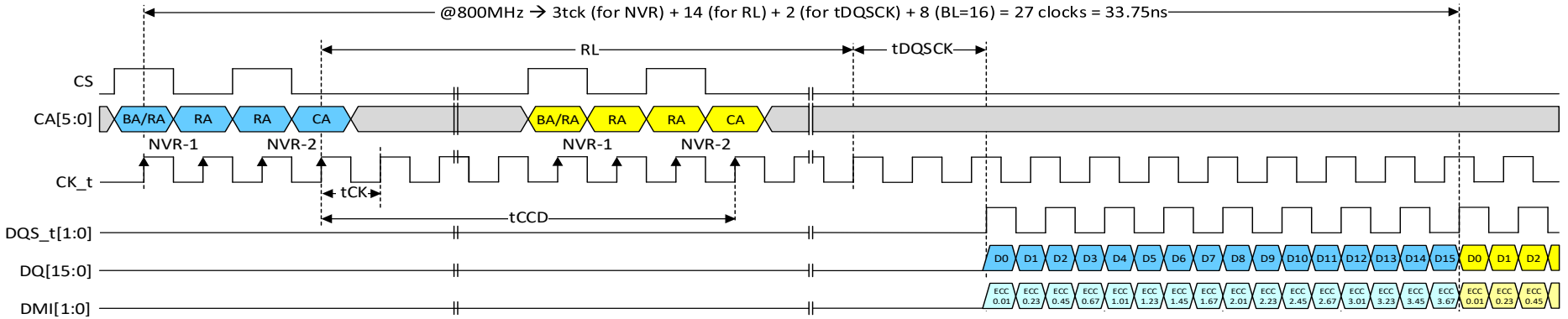
- LVCMOS has little room for advancement (limit ~200MHz)
- SPI uses a multiplexed cmd/add/data bus (no pipelining)
- LVSTL has significant advantages (Freq >2133MHz, low power, ..)
- LPDDR has split cmd/add and data busses (allows pipelining)
- LPDDR4 is a scalable interface (bus widths, # of channels, …)

LPDDR Flash offers ultra low-latency with unconstrainted read performance and enhanced safety mechanism

- **Unconstrainted read access between banks**
  - No banking violation
- **Execute in Place (XiP)**
  - Random access every 10 ns within a bank (36B, BL = 16)
  - No pre-charge required
- **All eight banks available**
  - No bank activate window (tFAW) limitation
- **Latency: 33.75 ns (800 MHz, BL = 16)**
- **100% DQ bus utilization** with BL=16
- **E2E ECC** over DMI pins



RDB – Row Data Buffer
RAB – Row Address Buffer



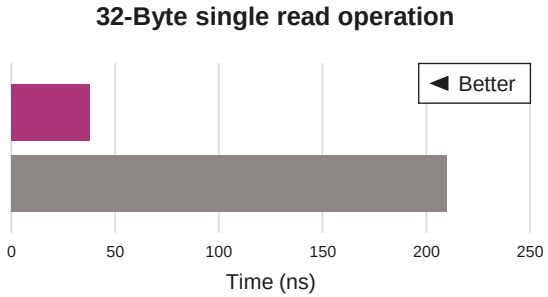
LPDDR Flash offers significant performance gains compared to standard xSPI NOR Flash

Flash Memory Summit

5x FASTER

32-Byte single read operation

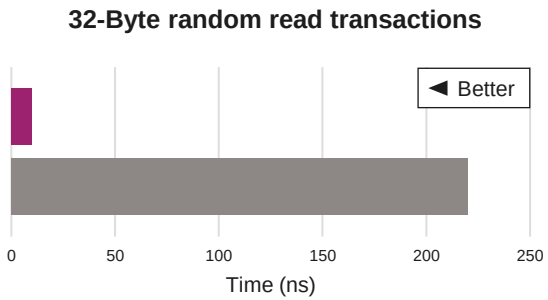
SEMPER™ X1 is 5x faster from command request to read data with low initial access time enabled by Infineon's eCT Flash technology



20x BETTER

32-Byte random read transactions

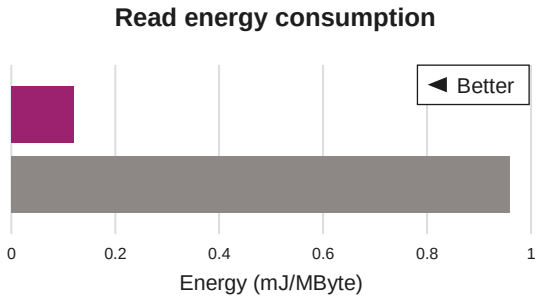
SEMPER™ X1 is 20x better for pipelined random read transactions with split cmd/address and data bus



8x LOWER

Read energy consumption

SEMPER™ X1 consumes 8x lower read energy per MByte with 8x higher throughput performance



LPDDR4 Flash

xSPI NOR Flash

Comparison assumes xSPI NOR Flash supporting 400 MBytes/s across Octal interface and SEMPER™ X1 supporting 3.2 GBytes/s across LPDDR4 interface

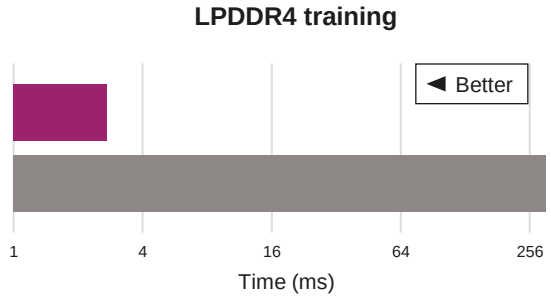
LPDDR Flash offers significant performance gains compared to standard DRAM

Flash Memory Summit

100x FASTER

Training time

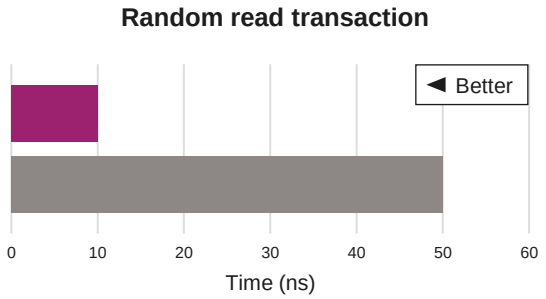
SEMPER™ X1 is optimized for read training only (no writes) compared to SDRAM



5x FASTER

Random read transaction

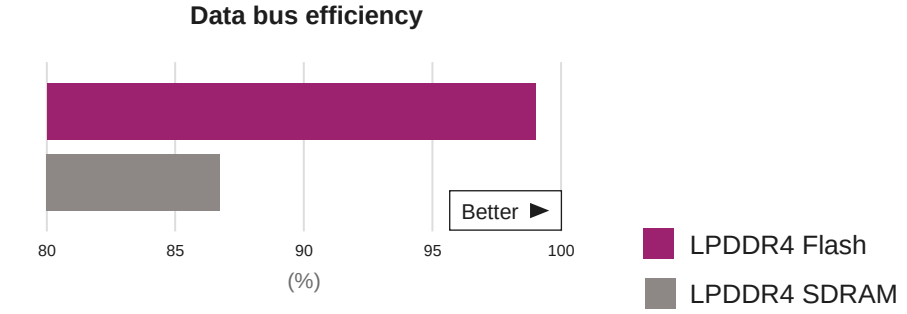
SEMPER™ X1 is 5x faster in random memory access with no banking restriction, row activation and refresh



14% HIGHER

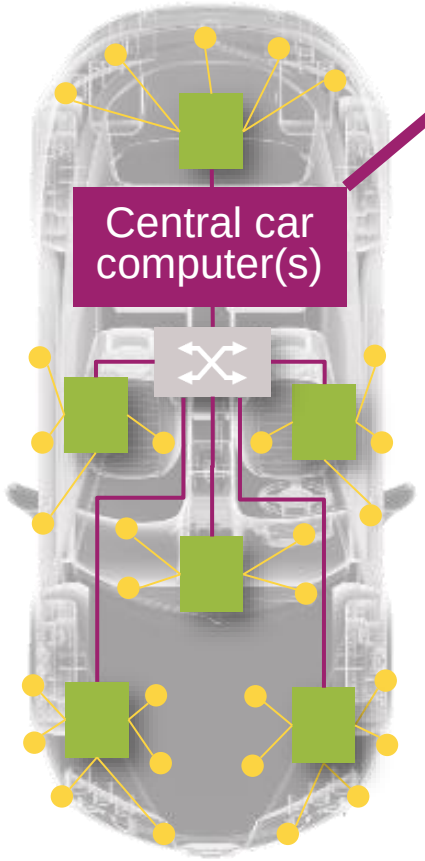
Data bus efficiency

SEMPER™ X1 supports 99% bus efficiency, at 125ºC and does not need periodic refresh



Comparison assumes SEMPER™ X1 and LPDDR4 DRAM supporting 3.2 GBytes/s bandwidth with LPDDR4 interface

Introducing SEMPER™ X1: World's first LPDDR Flash enables real-time code execution from external NOR Flash



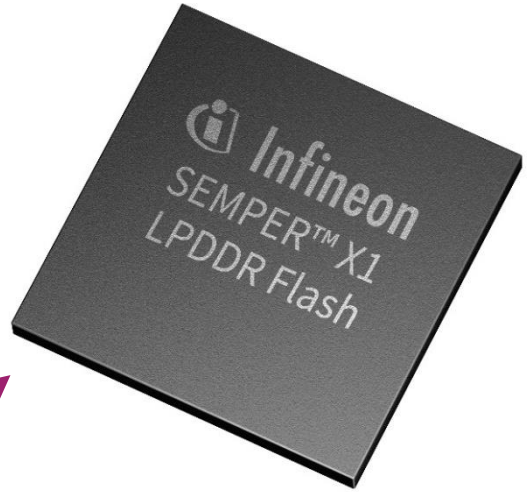
Evolution from domain architecture to central car computer(s)

- Software-defined vehicle
- Cloud-connected
- Autonomy with centralized processing
- Service oriented
- Higher safety and security

Memory requirements for automotive real-time processors

- 8x higher bandwidth[1]
- 20x faster random access[1]
- ISO 26262 ASIL-B compliant (ASIL-D Ready)
- AEC-Q100 qualified up to 125°C
- Multi-bank architecture
- OTA updates with zero downtime

SEMPER™ X1 LPDDR Flash



[1] Compared to xSPI Octal NOR Flash

User experience meets new E/E architecture

A car becomes a smarter car