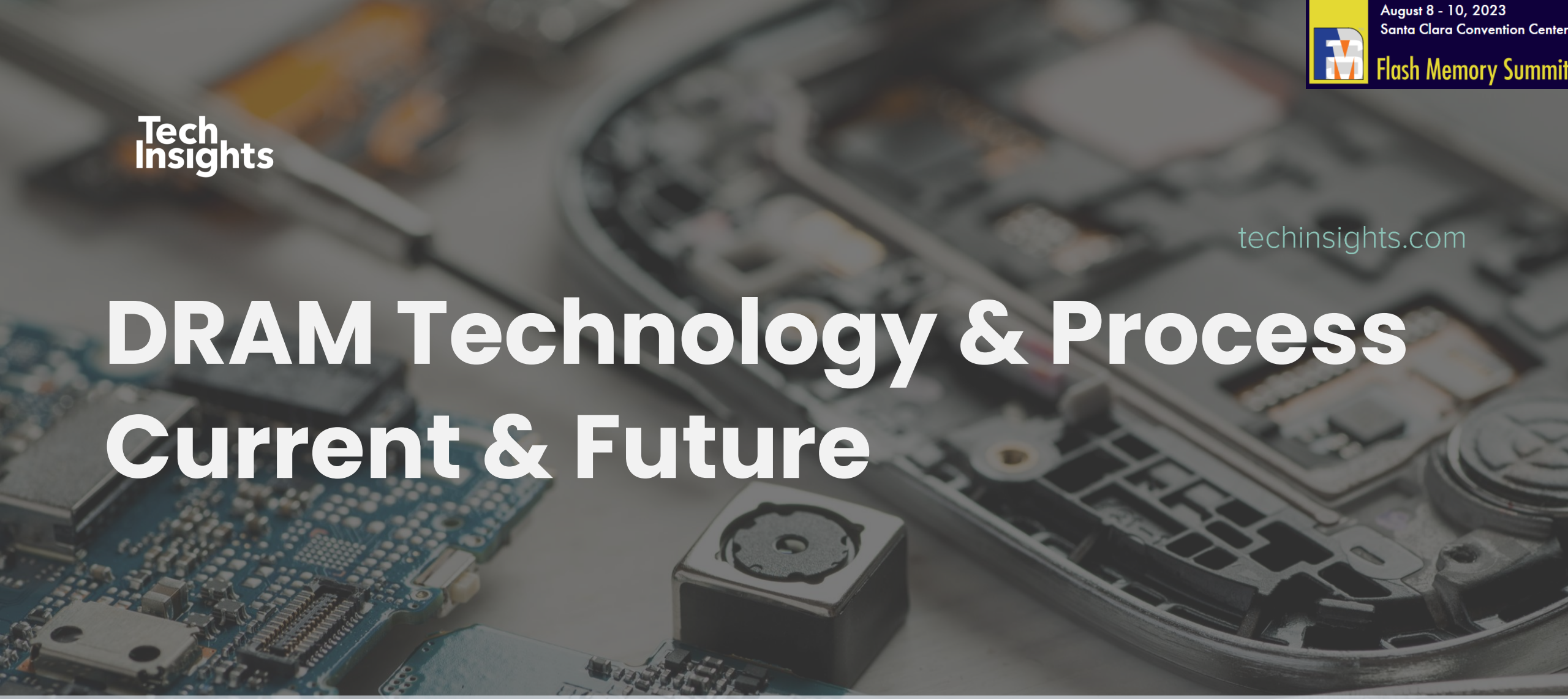

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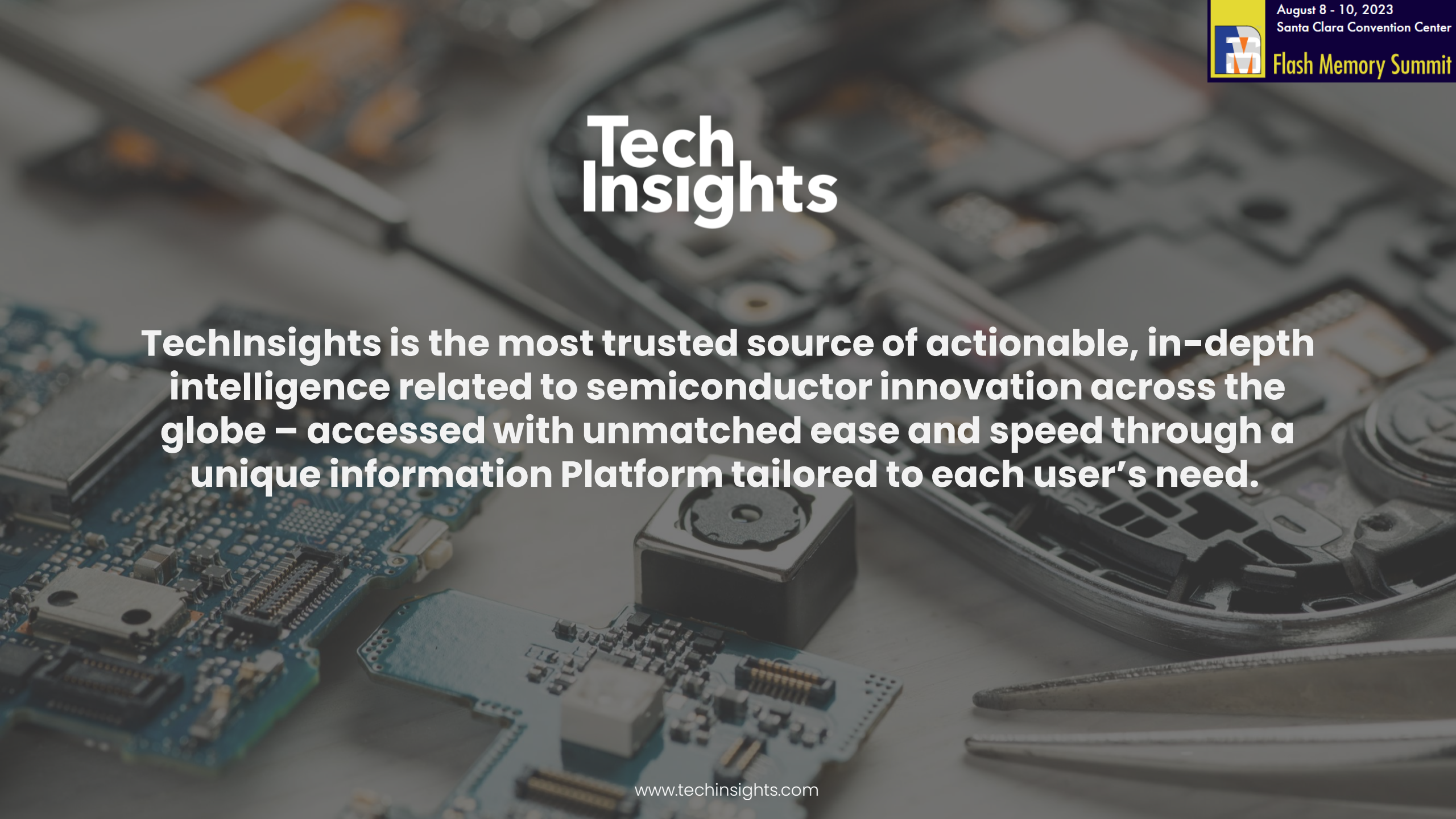
# DRAM Technology & Process Current & Future

Aug. 9, 2023

Dr. Jeongdong Choe
Senior Technical Fellow, SVP
www.techinsights.com



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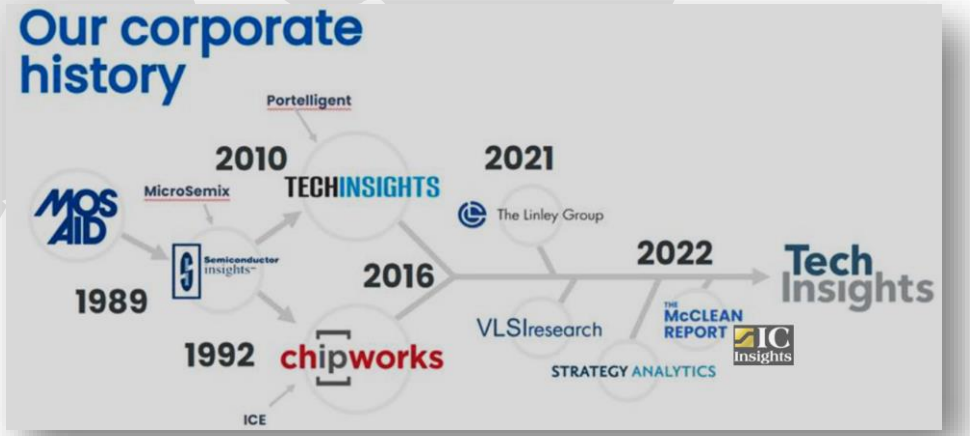


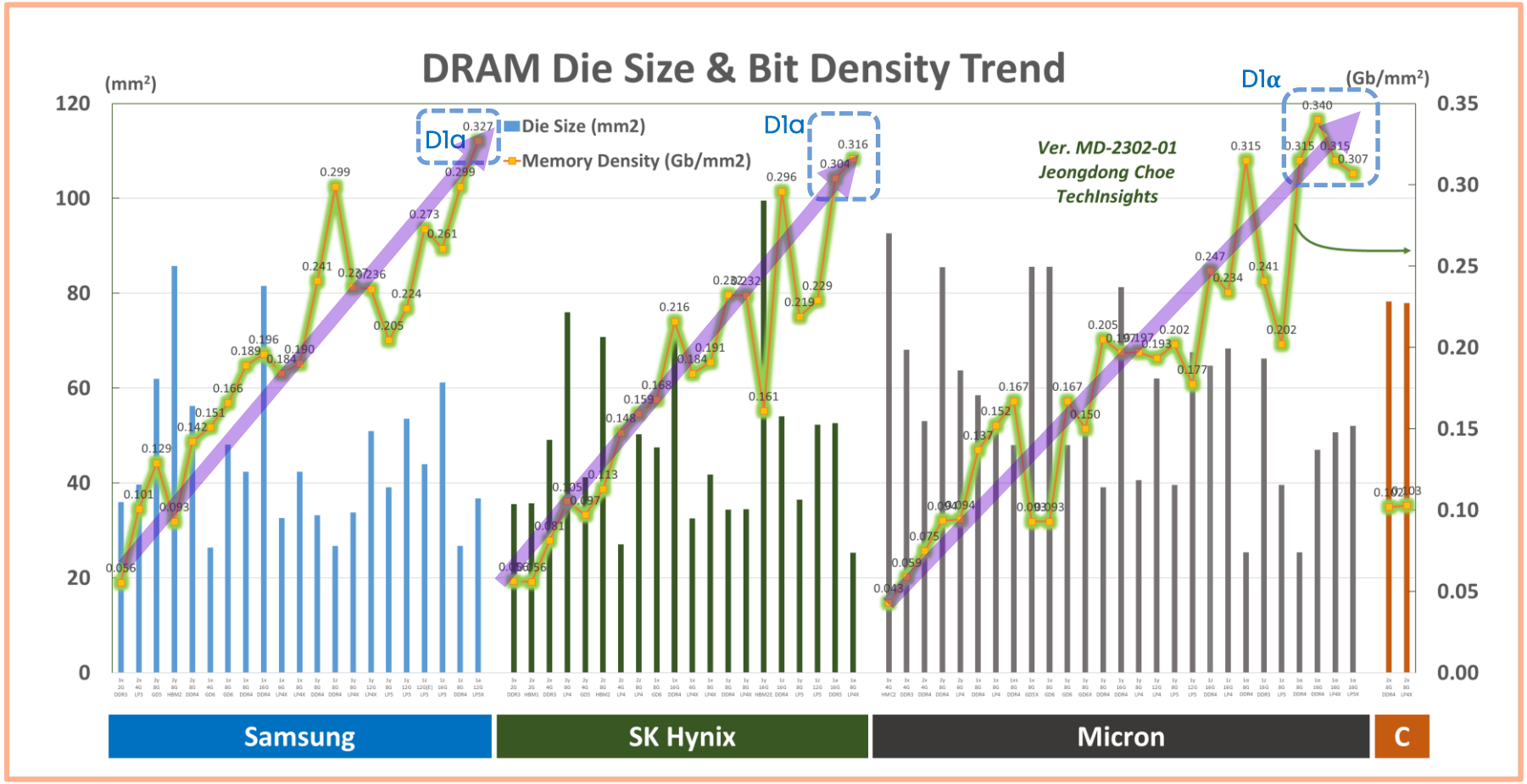
# 3D NAND Process Technology : 2023 & Beyond




## Presentation Agenda

# DRAM Bit Density Trend

## ■ Samsung, SK Hynix, Micron Technology, CXMT (including LPDDR5, LPDDR5X)




*Ref.*
- YMTC 232L TLC NAND → 15.02 Gb/mm2
- Intel XPoint Gen2 → 1.3 Gb/mm2
- Everspin 1Gb STT-MRAM → 0.01 Gb/mm2

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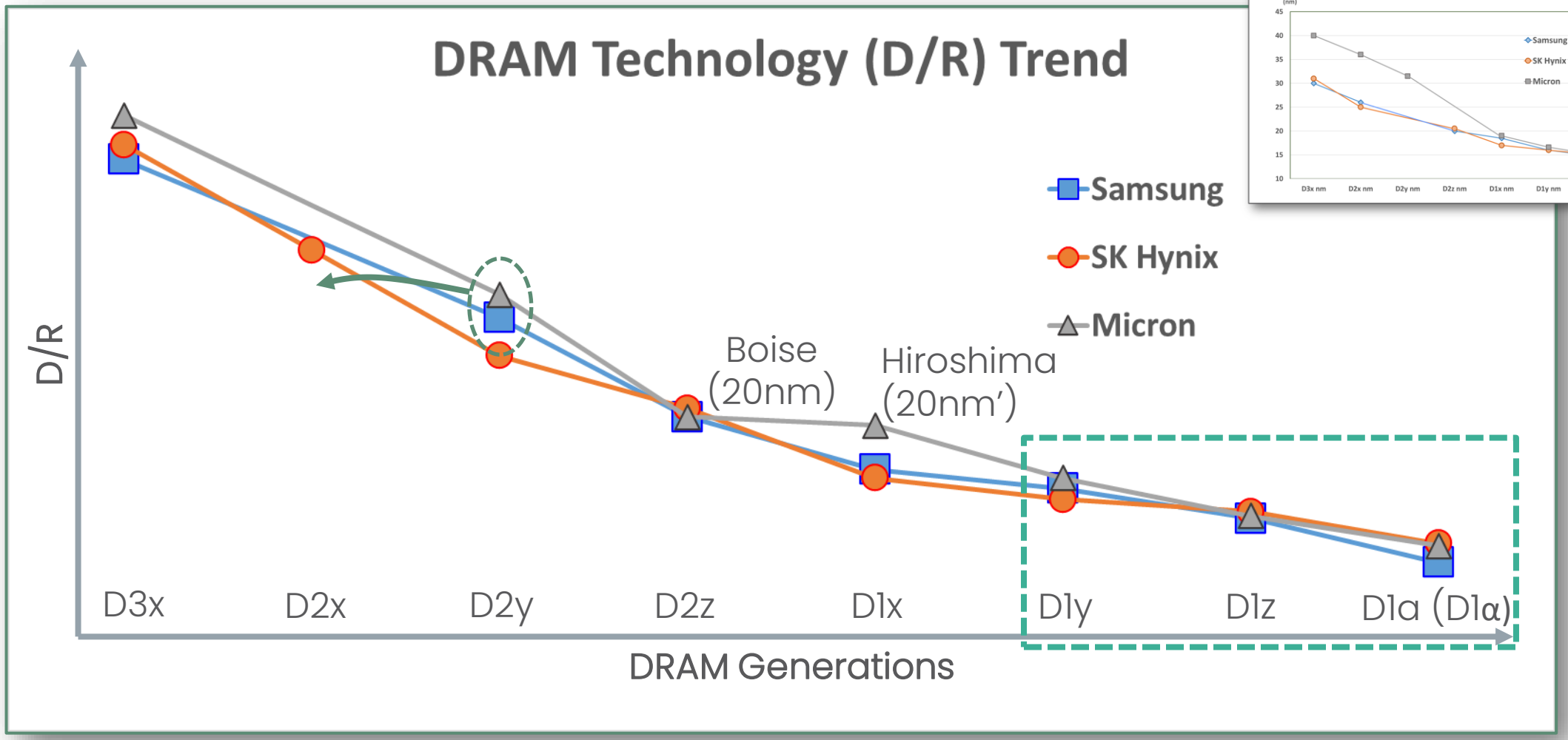
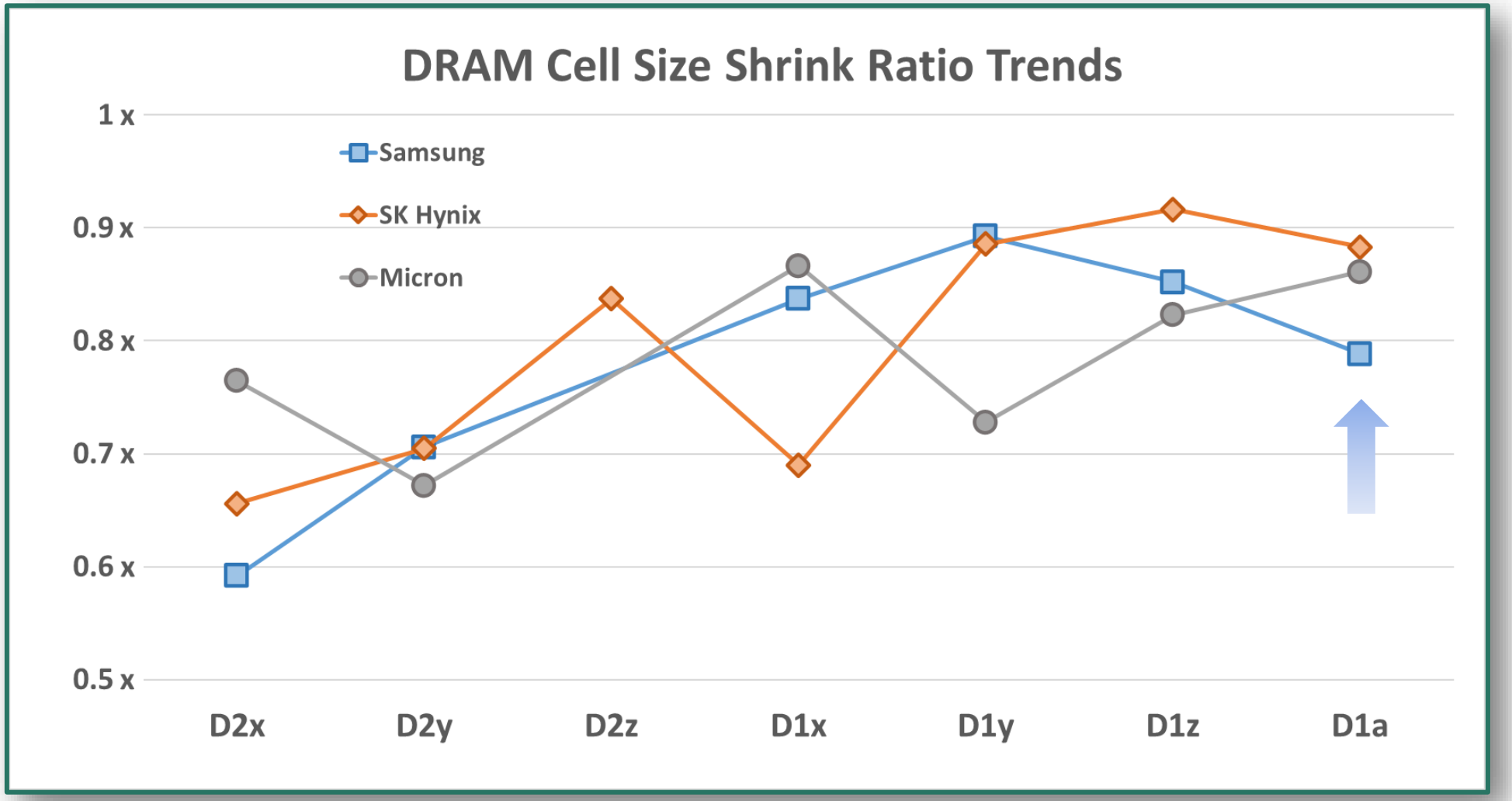
# DRAM Comparison: Cell Size & D/R

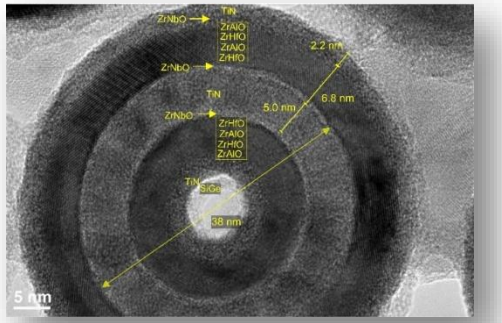


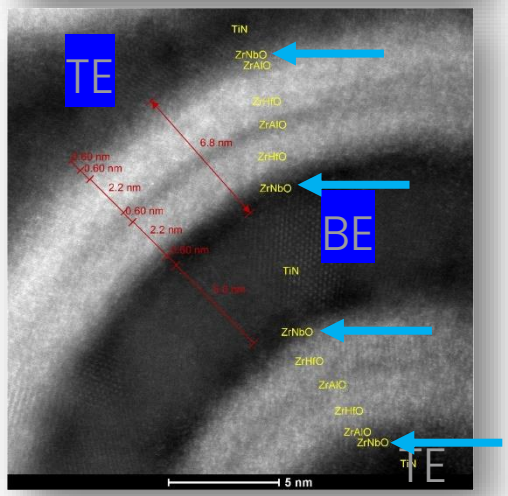
# DRAM Comparison: Cell Shrink Ratio



# NbO Dielectrics: Micron D1y, D1z, D1α

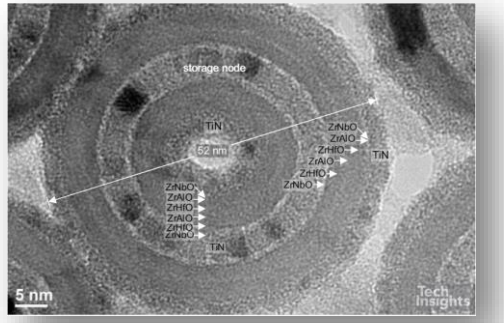
2-Sided ZrNbO

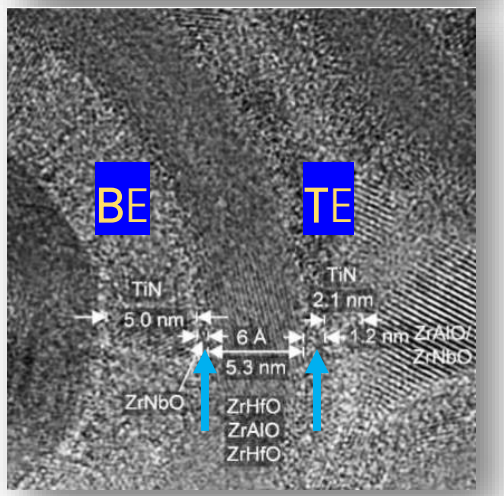



D1x

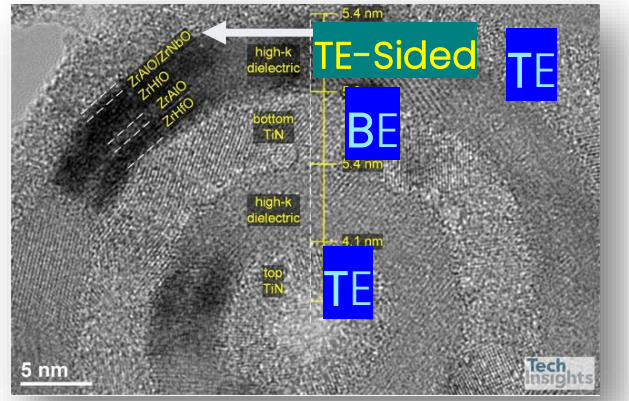
2-Sided ZrNbO



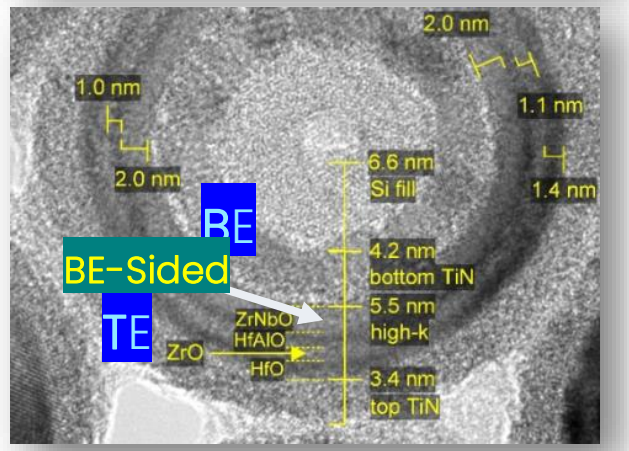




D1y

1-Sided ZrNbO




D1z

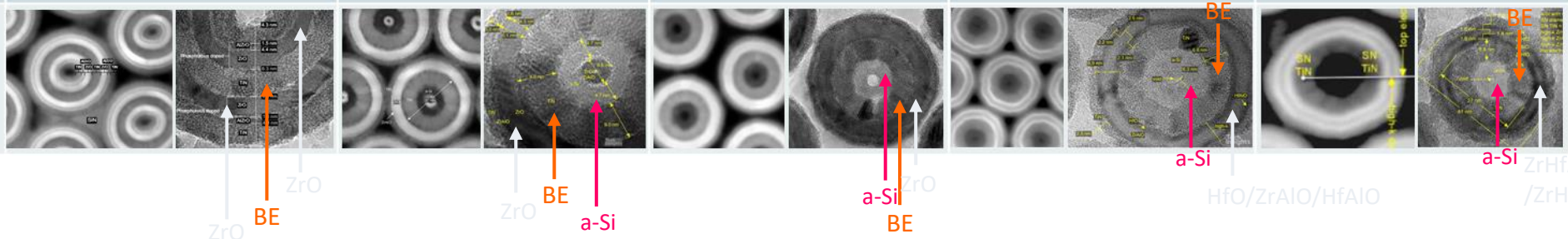



D1α

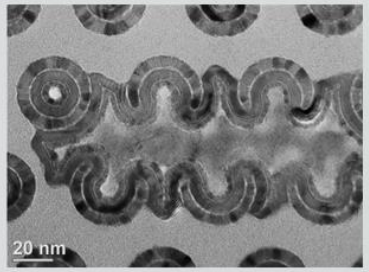
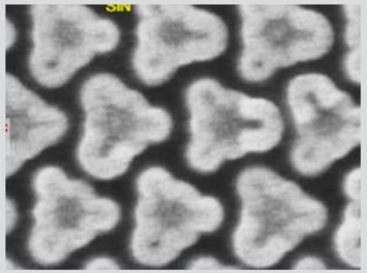
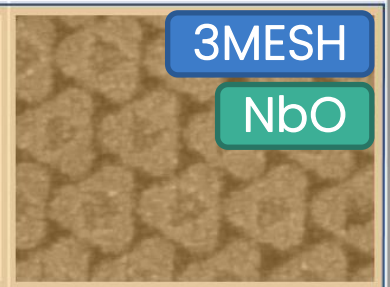
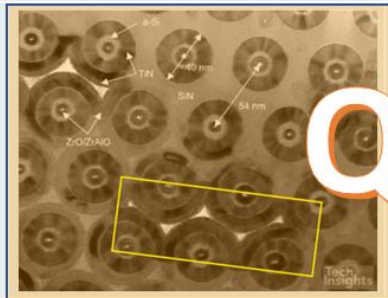
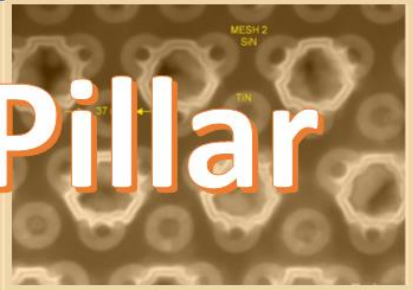
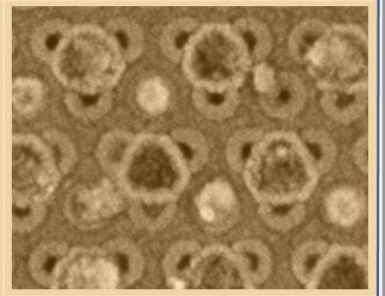
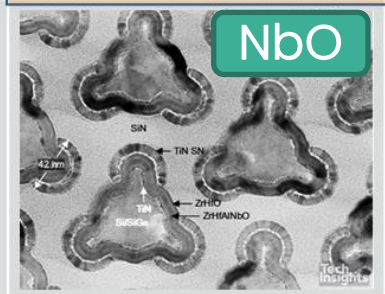
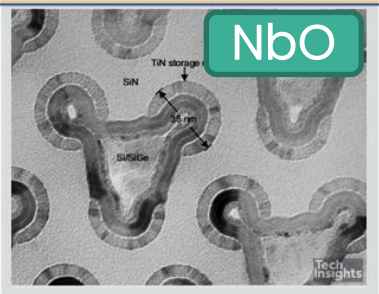
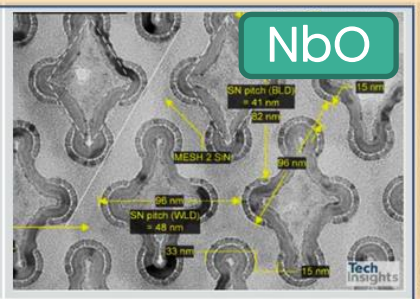
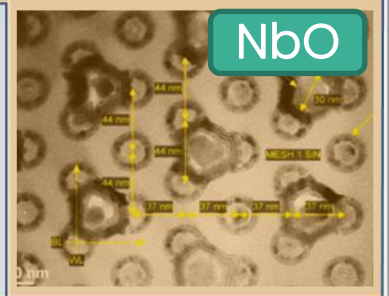
# Trend: Cylinder *vs.* One-sided Capacitor (SK Hynix)

*(2-sided Cap.)*

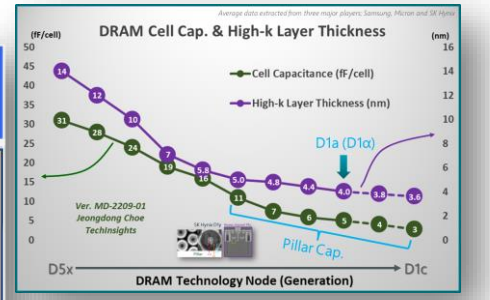
*Quasi-Pillar (1-sided Cap.)*

| Items | D2z | D1x | D1y | D1z | D1a |
|---|---|---|---|---|---|
| Cell Cap. Height | 1.22 μm | 1.22 μm | 1.22 μm | 1.10 μm | 1.10 μm |
| Capacitor Type | Cylinder | Cylinder (a-Si filled) | Cylinder (a-Si filled) | Cylinder (a-Si filled) | Cylinder (a-Si filled) |
| Bot. Node | TiN | TiN / (a-Si) | TiN / (a-Si) | TiN / (a-Si) | TiN / (a-Si) |
| High-k Dielectrics | TE/ZrAlO/ZrO/BE | TE/ZrAlO/ZrO/BE | TE/ZrAlO/ZrO/BE | TE/HfAlO/ZrAlO/ HfO/BE | TE/ZrHfO/ZrAlO/ ZrHfAlO/BE |
| Plate (Top Electrode) | W/SiGe/TiN | W/SiGe/TiN | W/SiGe/TiN | W/SiGe/TiN | W/SiGe/TiN |
| # MESH | 2 | 2 | 2 | 2 | 2 |
| 1st / 2nd MESH Thickness | 32 nm / 109 nm | 40 nm / 92 nm | 18 nm / 110 nm | 20 nm / 80 nm | 18 nm / 60 nm |
| Top Viewed Cap. & MESH TEM/SEM Images |  | | | | |

# DRAM Comparison: Capacitor

| Player | D1x | D1y | D1z | D1a (D1α) |
|---|---|---|---|---|
| SAMSUNG |  |  |  |  |
| SK hynix |  |  |  |  |
| Micron |  |  |  |  |





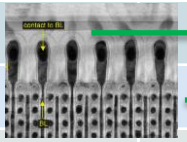

H=1.10 μm

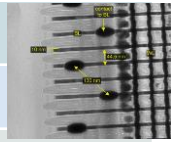
H=1.08 μm

H=0.89 μm

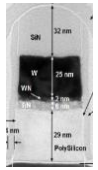
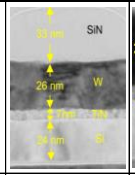
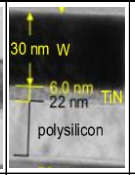
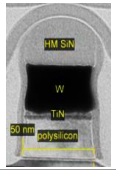
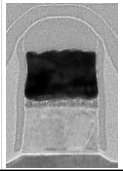
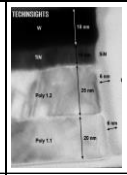
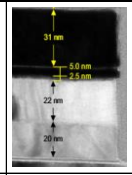
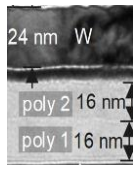
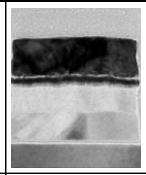
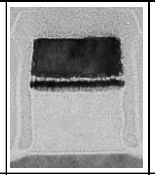
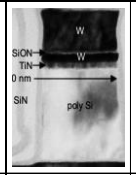
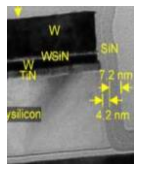
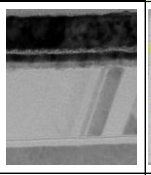
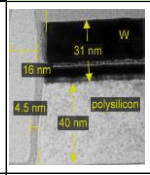
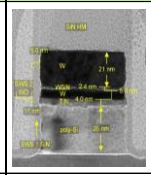
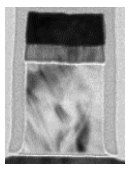
# DRAM Development Example: SK Hynix

| Items | SK Hynix D1z 16 Gb | SK Hynix D1a 16 Gb |
|---|---|---|
| Die Size / Ex. Device | 54.02 $mm^2$ / DDR4 16 Gb (7.40 mm x 7.30 mm) | 52.61 $mm^2$ / DDR5 16 Gb (7.40 mm x 7.11 mm) |
| Bit Density, Cell Size | 0.296 Gb/$mm^2$, 0.00197 $\mu m^2$ | 0.304 Gb/$mm^2$, 0.00169 $\mu m^2$ |
| WL (Cell Gate) Materials | Poly-Si(32nm)/W(62nm)/TiN | Poly-Si(20nm)/W(56nm)/TiN |
| Active Island Pattern Length | 105 nm | 97 nm |
| Pitch (Act/WL/BL) | 30 nm / 41 nm / 48 nm | 28 nm / 38 nm / 44.5 nm |
| BL Spacer, BL Top CD, M1-BL CONT | NO (low-k), 8.5 nm, linear | NO (low-k), 8.5 nm, zigzag |
| MESH Thickness 1, 2 | 20 nm, 80 nm | 10 nm, 60 nm |
| SNC Etch | SAC | SAC |
| Top Plate Materials | W 28 nm / SiGe 175 nm on TiN | W 28 nm / SiGe 165 nm on TiN |
| Cap., Dielectrics, Height | 1-sided Pillar, HfAlO/ZrAlO/HfO on BE, 1.10 µm | 1-sided Pillar, ZrHfO/ZrAlO/ZrHfAlO on BE, 1.10 µm |
| Cap. MESH Pattern | Triangle | Triangle |
| M2 & M3 Top Layer | Cu | Cu |

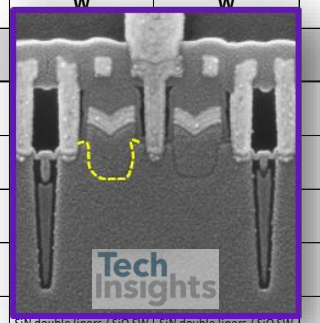




# DRAM Comparison: Peri TRs

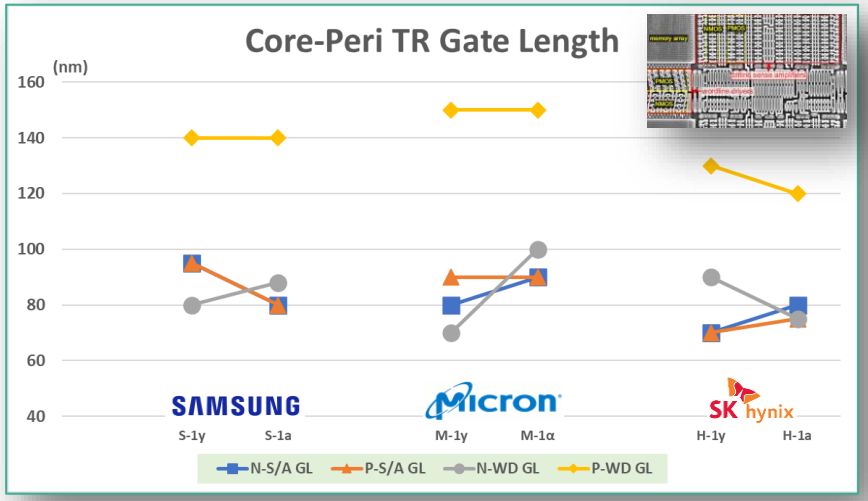
| Manufacturer | Samsung | | | | | Micron | | | | | SK Hynix | | | | | CXMT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Tech Node | D2y | D1x | D1y | D1z | D1a | D2y | D1x | D1y | D1z | D1α | D2z | D1x | D1y | D1z | D1a | D2x (22nm) |
| Gate Image (x-section TEM) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Gate Layer 1 | Poly-Si | Poly-Si | Poly-Si | Poly-Si | Poly-Si | Poly-Si 1 | Poly-Si 1 | Poly-Si 1 | Poly-Si 1 | Poly-Si 1 | Poly-Si | Poly-Si | Poly-Si | Poly-Si | Poly-Si | Poly-Si |
| Gate Layer 2 | TiN | TiN | TiN | TiN | TiN | Poly-Si 2 | Poly-Si 2 | Poly-Si 2 | Poly-Si 2 | Poly-Si 2 | TiN | TiN | TiN | TiN | TiN | TiN |
| Gate Layer 3 | WN | W | W | W | W | TiN | TiN | TiN | TiN | TiN | W | W | W | W | W | W |
| Gate Layer 4 | W | | | | | W | WN | WN | W | W | SiON | WSiN | WSiN | WSiN | WSiN | |
| Gate Layer 5 | | | | | | | W | WSiN | WSiN | WSiN | W | W | W | W | W | |
| Gate Layer 6 | | | | | | | | W | W | W | | | | | | |
| Gate Height | 62 nm | 57 nm | 58 nm | 55 nm | 52 nm | 73 nm | 80.5 nm | 63 nm | 56 nm | 50 nm | 98 nm | | | 71 nm | 58.4 nm | 78 nm |
| Gox Structure | SiO/SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | | | SiON/SiO | SiON/SiO | SiON/SiO |
| LV Gox Thickness | 2.3 nm | 3.0 nm | 2.5 nm | 1.9 nm | 1.9 nm | 2.7 nm | 2.3 nm | 2.0 nm | 2.0 nm | 2.0 nm | 2.2 nm | | | 1.8 nm | 2.6 nm | 2.8 nm |
| HV Gox Thickness | 6.0 nm | 5.8 nm | 5.0 nm | 4.6 nm | 4.6 nm | 6.4 nm | 5.6 nm | 5.0 nm | 5.2 nm | 5.3 nm | 5.2 nm | | | 4.2 nm | 4.6 nm | 5.2 nm |
| Gate Spacer | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO Buffer / SiN | SiN liner / SiO Buffer / SiN | SiN liner / SiO Buffer / SiN | SiN liner / SiO SW | SiN double liners / SiO SW | SiN double liners / SiO SW | SiN/SiO/SiN | SiN/SiO/SiN | SiN liner / SiO SW |
| CONT Materials | CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi |
| Report ID | 0315-39040-O-5DM-100 | AME-1701-805 | AME-1902-802 | AME-2102-801 | AME-2303-801 | 0716-43012-O-5DM-100 | AME-1804-803 | AME-1905-801 | AME-2007-801 | AME-2106-801 | AME-1703-801 | AME-1811-801 | AME-1911-801 | AME-2104-801 | AME-2208-801 | AME-2006-802 |

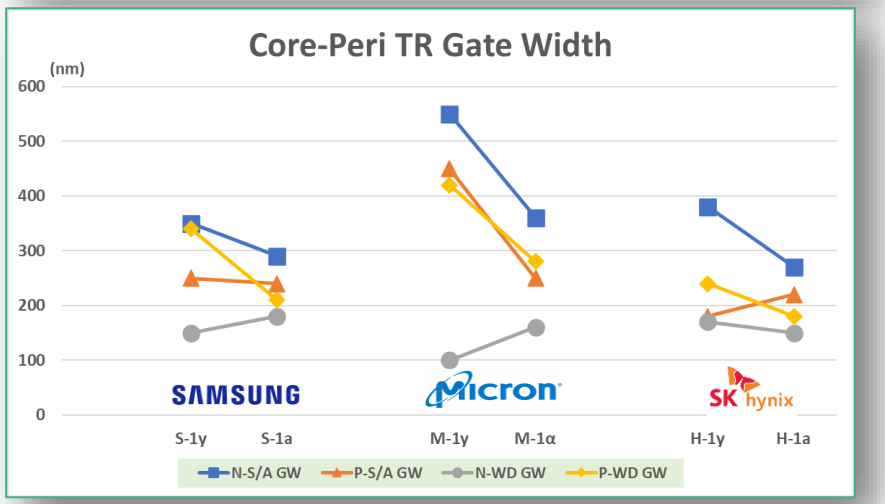
Recess channel TRs

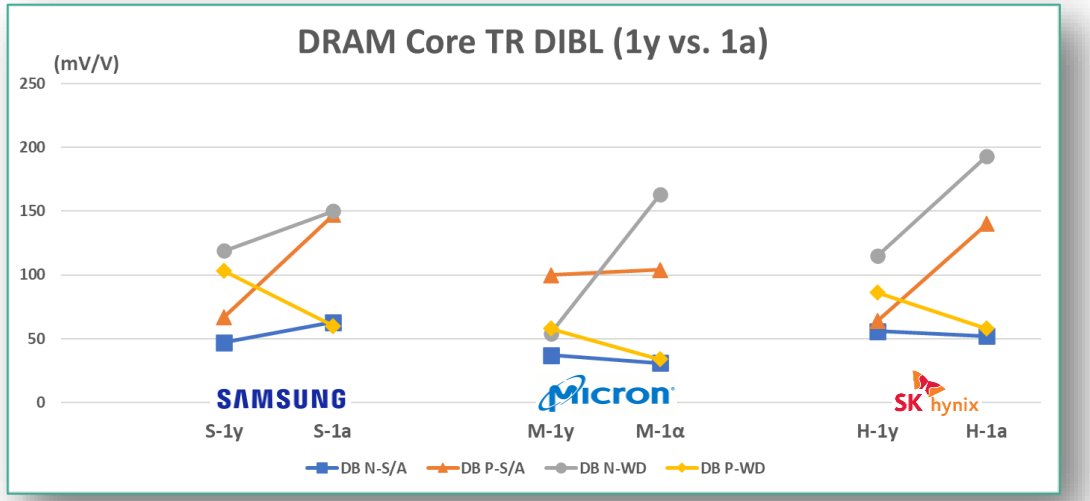


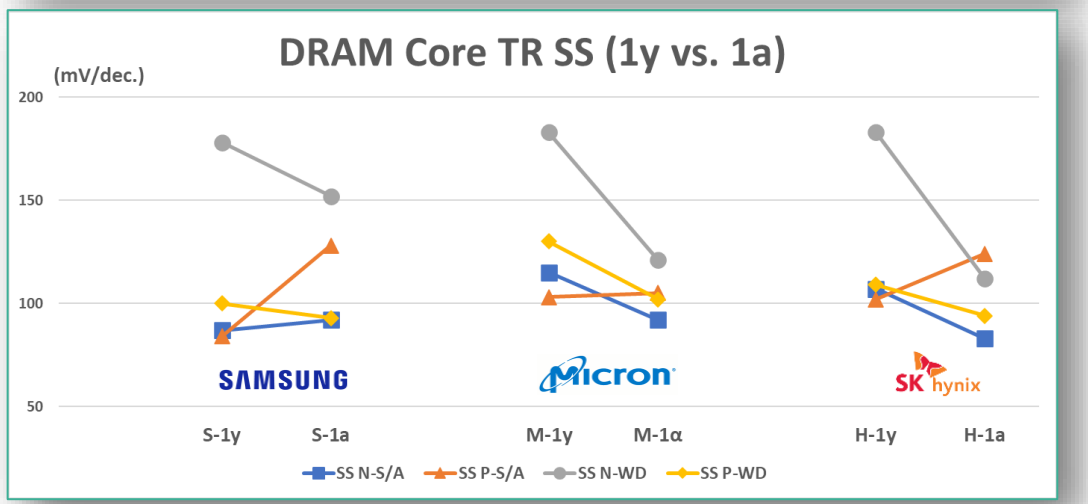

HKMG GDDR6 | HKMG DDR5 | HKMG GDDR6 | ~1β HKMG | HKMG GDDR6 | HKMG LPDDR5X

# DRAM Comparison: Core Transistors



# HBM Battle: SK Hynix, Samsung

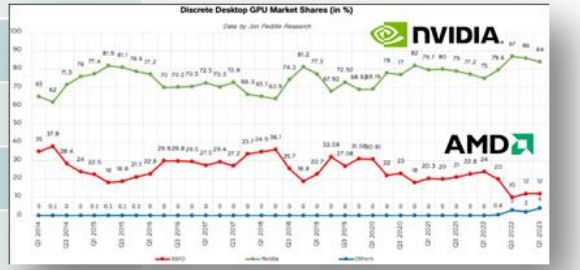
| SK Hynix HBM | HBM | HBM2 | HBM2E |
|---|---|---|---|
| Product Year | 2014 - 2016 | 2017 - 2019 | 2020-2022 |
| Product Example | AMD Radeon R9 Fury X | AMD Vega 10 XT | NVIDIA A100 (80GB) GPU |
| Package Components | 1 GPU + 4 HBM Device<br>4 HBM Dies,<br>1 Basic Logic Die,<br>1 Si-Interposer | 1 GPU + 2 HBM Device<br>4 HBM Dies,<br>1 Basic Logic (Controller) Die,<br>1 Si-Interposer | 1 GPU + 5 HBM Device<br>8 HBM Dies,<br>1 Buffer (Controller) Die,<br>1 Si-Interposer |
| Package Size | 55.0 x 55.0 x 2.7 $mm^3$ | 47.5 x 47.5 x 2.8 $mm^3$ | 55.0 x 55.0 x 3.1 $mm^3$ |
| #Metal Layers in PWB | 10 | 10 | 12 |
| HBM DRAM Die Size | 35.24 $mm^2$ | 71.90 $mm^2$ | 106.05 $mm^2$ |
| HBM DRAM Die Cap. | 2 Gb | 8 Gb | 16 Gb |
| Die Density | 0.056 Gb/$mm^2$ | 0.113 Gb/$mm^2$ | 0.151 Gb/$mm^2$ |
| DRAM Tech. Node | H-D2x (26 nm) | H-D2y (20 nm) | H-D1y |
| # HBM Die | 4 | 4 | 8 |
| HBM Die thickness | 51 µm, 200 µm | 57 µm, 340 µm | 55 µm, 120 µm |
| Active TSV Diameter (max.) | 5.0 µm | 4.0 µm | 4.0 µm |

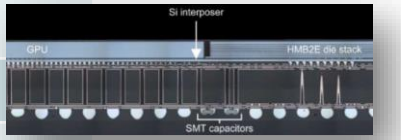
16CH/24Gb
> 800 GB/s
HBM3
2023~

32CH/32Gb
> 1.5 TB/s
HBM4
2024/2025~

- ✓ TSV
- ✓ Power Distribution
- ✓ Thermal Issues
- ✓ Microbump (interface)
- ✓ I/O increase

NVIDIA H100




Where is Samsung?

Aquabolt → Flashbolt → Icebolt
AMD MI300X





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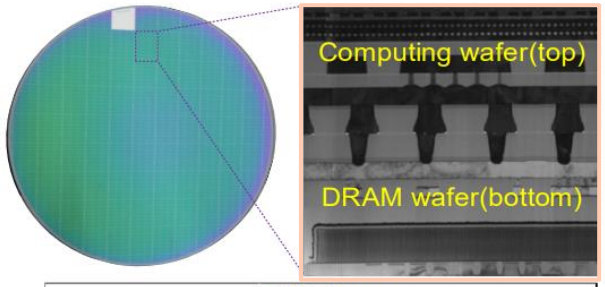
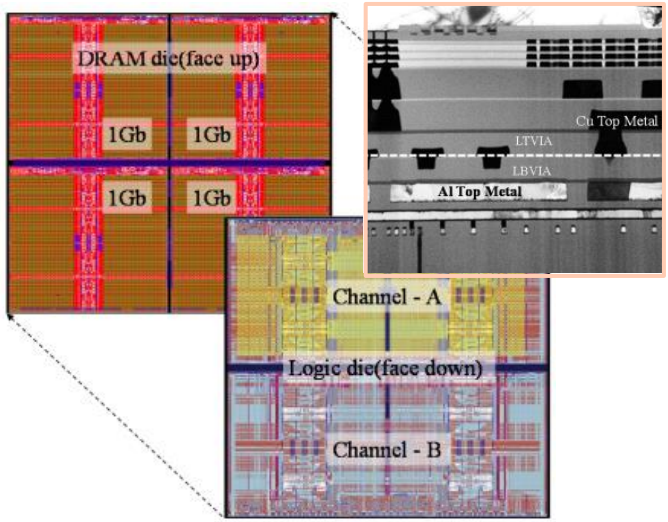
# Hybrid Bonding on DRAM/HBM Application

- **3D DRAM-to-Logic Hybrid Bonding Chip with High-BW, High Capacity, and High Energy Efficiency**
  - ✓ Driven by increasing demand for DRAM scaling and higher BW (Energy < 1pJ/bit)
  - ✓ No commercial products yet (Low temp. HB process is needed for DRAM)
  - ✓ DRAM array wafer and logic wafer were fabricated separately
  - ✓ Issue: HB process/post-annealing affects

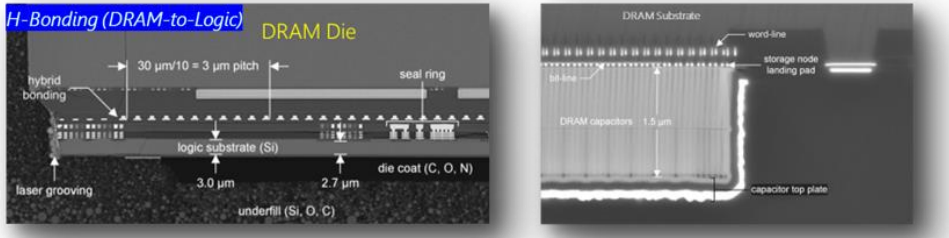



| SoC Chip Summary | |
|---|---|
| Technology node | 25nm for DRAM die, 55nm for computing die |
| Chip package size | 50.0mm x 50.0mm |
| DRAM density | 48Gbits on chip |
| Power | 1.1V for DRAM, 1.2V for Computing |
| Bandwidth | 1596GB/s |
| Energy efficiency | 0.88pJ/b |
| System power consumption | 55W |

*Source: IEEE ASSCC2021*




*Source: IEEE IEDM2020*




*SEDRAM: Stacked Embedded DRAM*
*PNM: Process-Near-Memory (DDR4/5, HBM2/2E/3 or LPDDR4/5)*
*TSV: Through-Silicon Via*
*CIM: Compute In Memory (SRAM)*
*HB: Hybrid Bonding*

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