Flash Memory Summit

UCIe™ Usage Models

Presenter:

Manuel Mota – Senior Product Manger, Synopsys

Moving Beyond Moore's Law With Multi-Die Systems

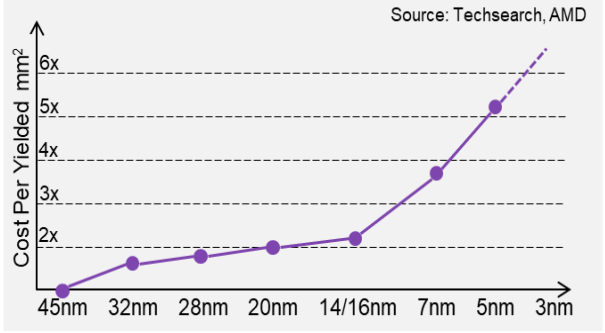
Flash Memory Summit

Addressing the Complexity Gap for the SysMoore Era

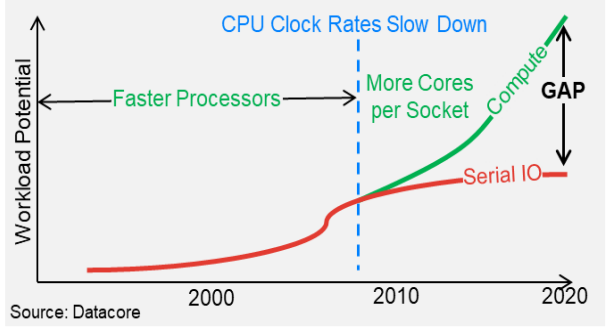
Laws of Semiconductor are Faltering

- Moore's Law (1965) – Cost/mm2 is increasing with process node
- Dennard Scaling (1974) – Clock speed increase with process node constrained by power density increase
- Amdahl's Law (1967) – IO speed bottleneck limits benefits of CPU parallelization and multi-threading

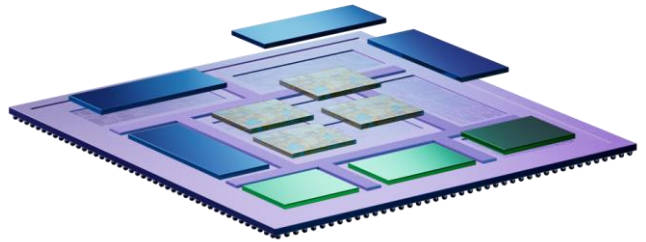
Silicon Cost / mm2 is Increasing

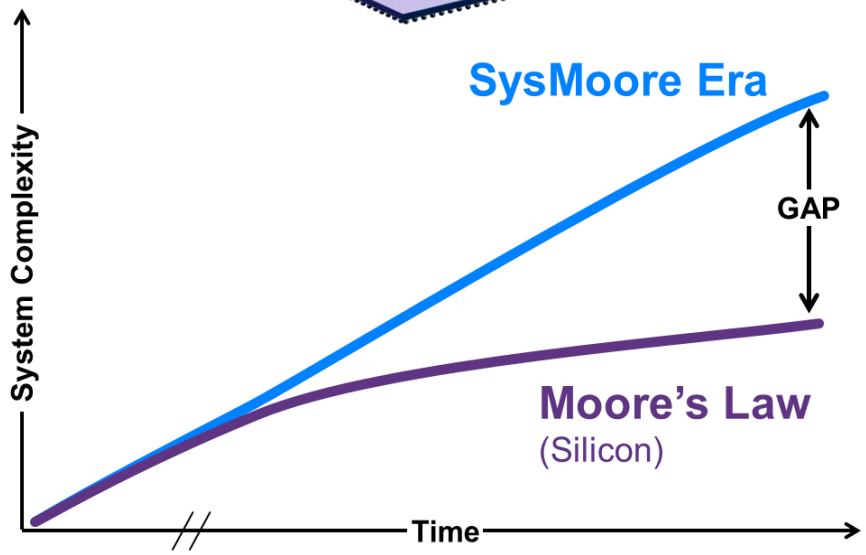


Compute Power & IO Bandwidth Gap is Widening



Multi-Die Systems Address Systemic Complexity & Extend Moore

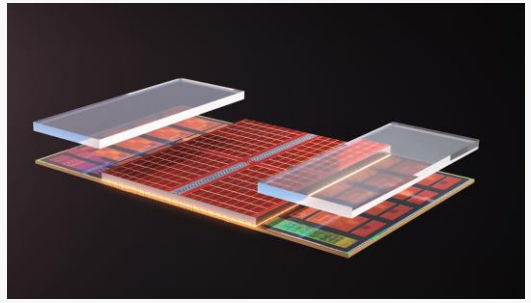




Enabling Truly Transformative Products

Examples of commercial high-performance, high-density multi-die systems

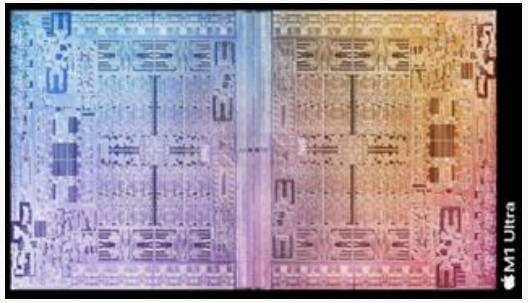
AMD



3D V-Cache: Hybrid Bonded

3x Energy Efficiency, 15x Interconnect Density (v. µbumps)

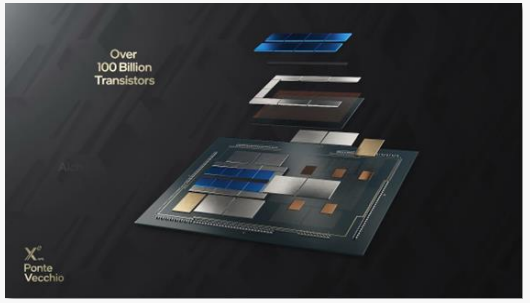
APPLE



Personal Computing

2x Dies, 114B Transistors, 2.5TB D2D BW, Silicon Connected

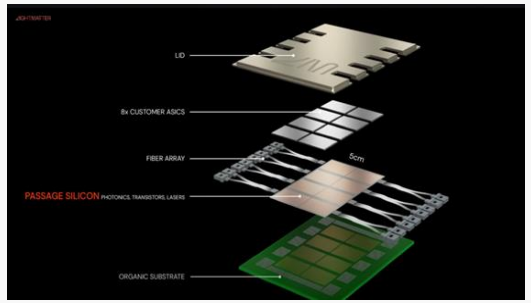
INTEL



Exascale Computing / AI

100B+ Tr's, 47 Active Tiles, 5 Process Nodes, EMIB/Foveros

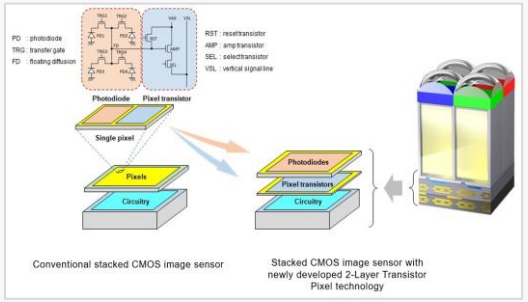
LIGHTMATTER



Photonics, Silicon, Lasers

8x Customer ASICs, Fiber Array

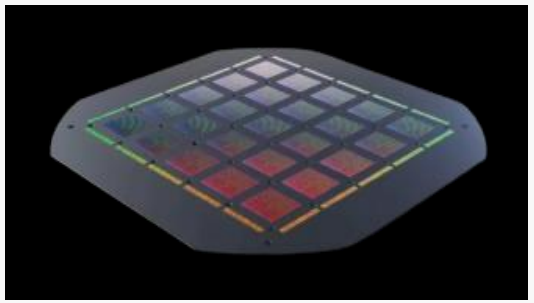
SONY



CIS with 2-layer Transistor Pixel Tech.

2x Electron Storage Capacity (Pix), Less noise, wide dynamic range

TESLA



9 Peta FLOPs AI-Training Tile

25x 50B Transistors, Reconstructed fanout wafer

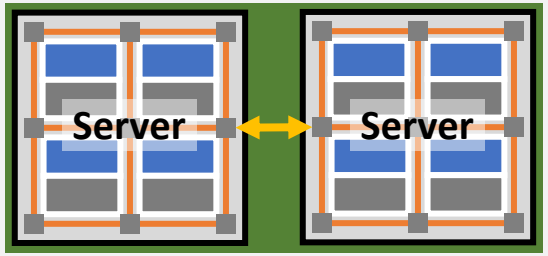
UCIe™ Enables Common and New Use Models

Flash Memory Summit

Compute Scaling and Die Splitting Are Majority of Use Models

Server or AI Scaling (Homogeneous)

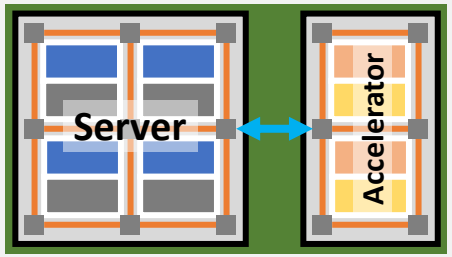
(NoC-to-NoC with low latency & coherency)



UCIe™ Streaming
- CXS or AXI bridge
- User Defined / Proprietary

Heterogeneous Computing (Accelerator)

(Interoperability with low latency & coherency)

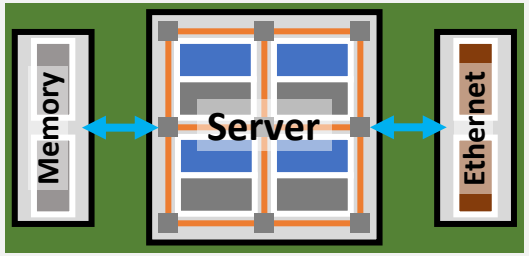


UCIe™ CXL™ or PCIe®
- For interoperability

UCIe™ Streaming
- CXS or AXI bridge

IO or Memory Split

(Interoperability with low latency)

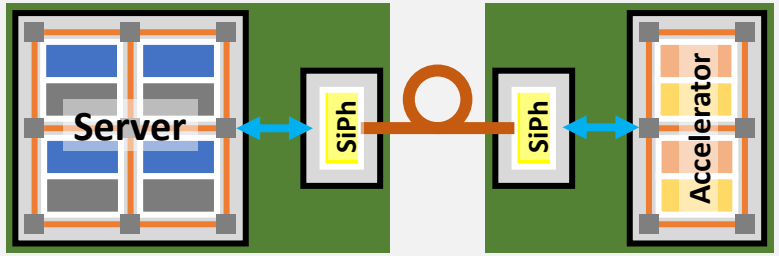


UCIe™ CXL™ or PCIe® 6.0
- Coherency for Memory

UCIe™ Streaming
- AXI bridge for Ethernet

Resource Aggregation (Pooling) w/Retimer

(Rack-to-Rack with low latency)

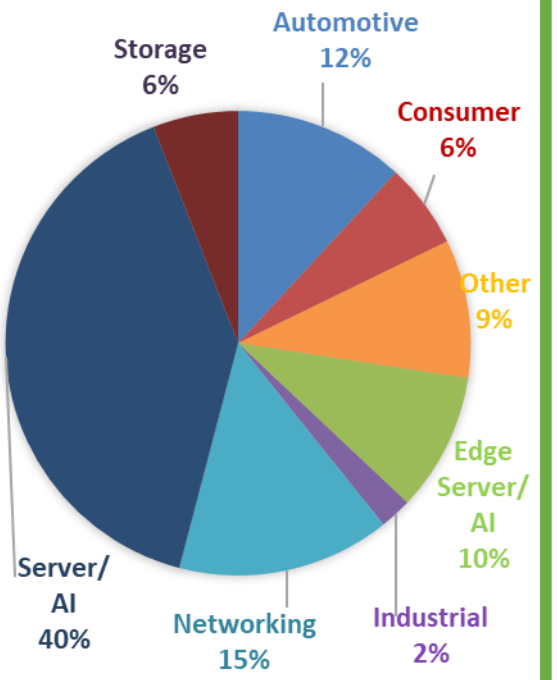
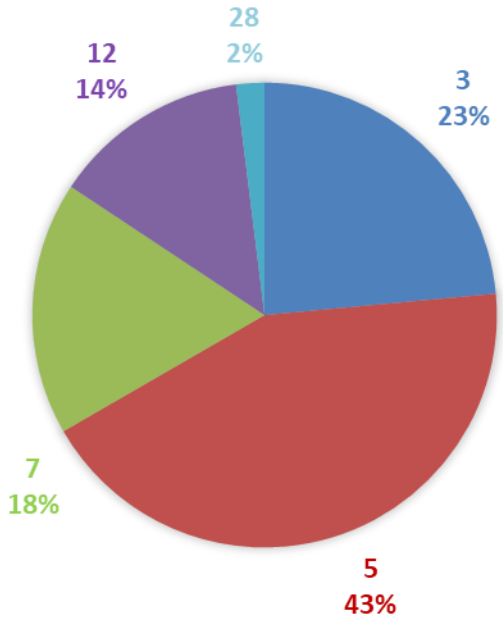
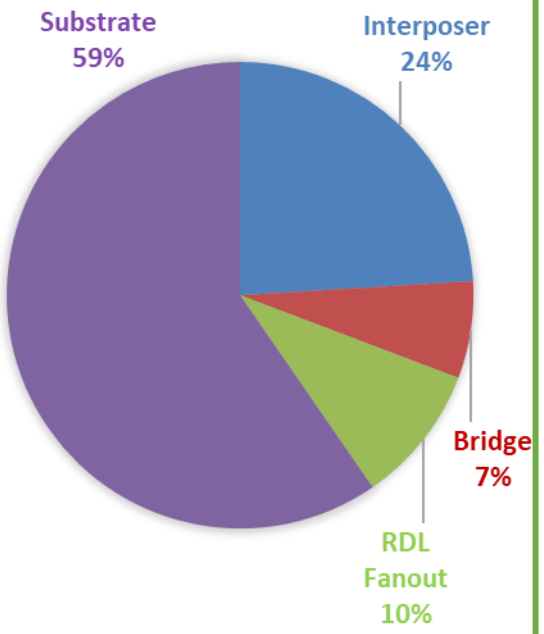


UCIe™ CXL™ or PCIe®6.0
- For Aggregation

UCIe™ Streaming
- For CPO / Eth.

Rapid Adoption of Multi-Die Systems

Tracking 100+ Companies

Application	Node	Package
		
Data Center / Auto	Large Compute Systems	Cost, Availability

Source: Synopsys

Multi-Die vs. Monolithic

Economics

- Re-use for TTM & Low Risk
- Rapidly create SKUs
- Lower system cost

Physics

- Create >2X reticle products (more functionality)
- Lower system power while increasing throughput
- Optimize system form factor
- Increase system performance through speed binning

~90% of Use Cases Today are Captive

Protocol Bridges is Optimized Solution for Captive (Eco)Systems

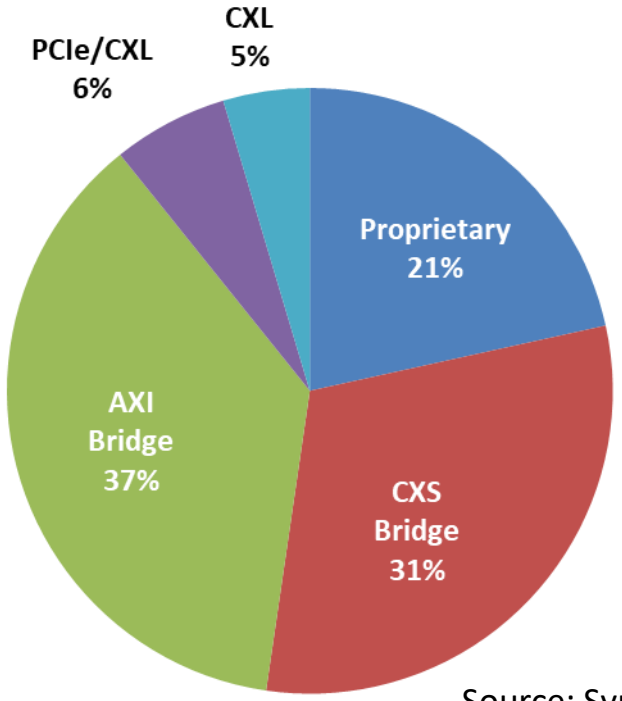
Key Benefits (vs CXL™/PCIe®)

- Virtual multi-die SoC fabric/NoC
- Reduced D2D link latency
- Application specific optimization
- Reduce protocol complexity

Common Use Cases

- Homogeneous Compute / Scaling
- Heterogeneous Compute (w/ same fabric)
- Specialized Functional Attachment

Protocol Bridges w/ UCIe Streaming address Captive Market Requirements



Source: Synopsys

Market Evolution: Captive to Open Ecosystem

Flash Memory Summit

UCIe™ Adoption is Major Step Forward, but Challenges Must be Overcome by Industry

Captive Systems (NOW)

- Both dies/chiplets “owned” by same vendor
- Driven by PPA optimization (e.g: latency)
- Application specific protocols (streaming)
- Proprietary form factor & configuration
- Homogeneous Compute:
  - Large HPC Server, AI Training
  - Tier 1 / Data Center / Mobile

Open Ecosystem

- Aggregation of OTS Chiplets from market
- Driven by interoperation / compliance
- Widely used common protocols (CXL™/PCIe®)
- Restricted form factor & configurations
- Heterogenous Compute, Aggregation
  - IO Chiplet, Memory extension, Accelerator
  - Next wave / Consumer / Automotive

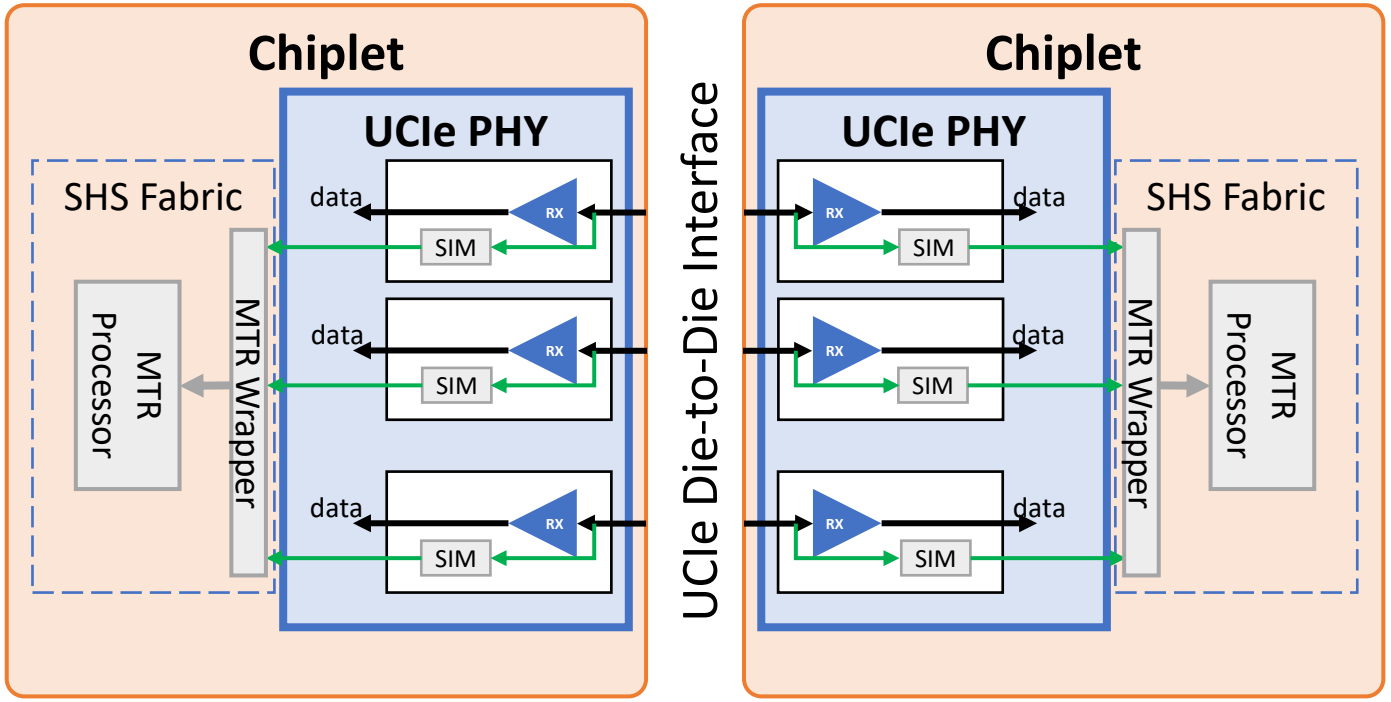
Challenges

- D2D standard / protocols
- Interoperability / “Plug Fest”
- Common form factors
- Security
- Design & Integration Flows / models
- Multi-die functional partition
- Low-cost Adv. Pkg
- Business models

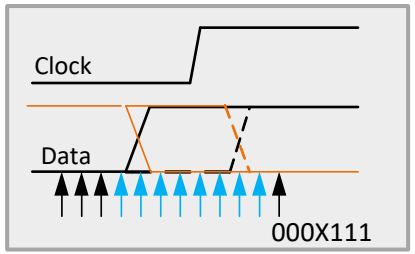
Improving D2D Link Reliability for Automotive Applications

Flash Memory Summit

With Mission Mode Health Monitoring Enabled by UCIe™ 1.1



Signal Integrity Monitor
Operation Concept



Avoids System Outage w/

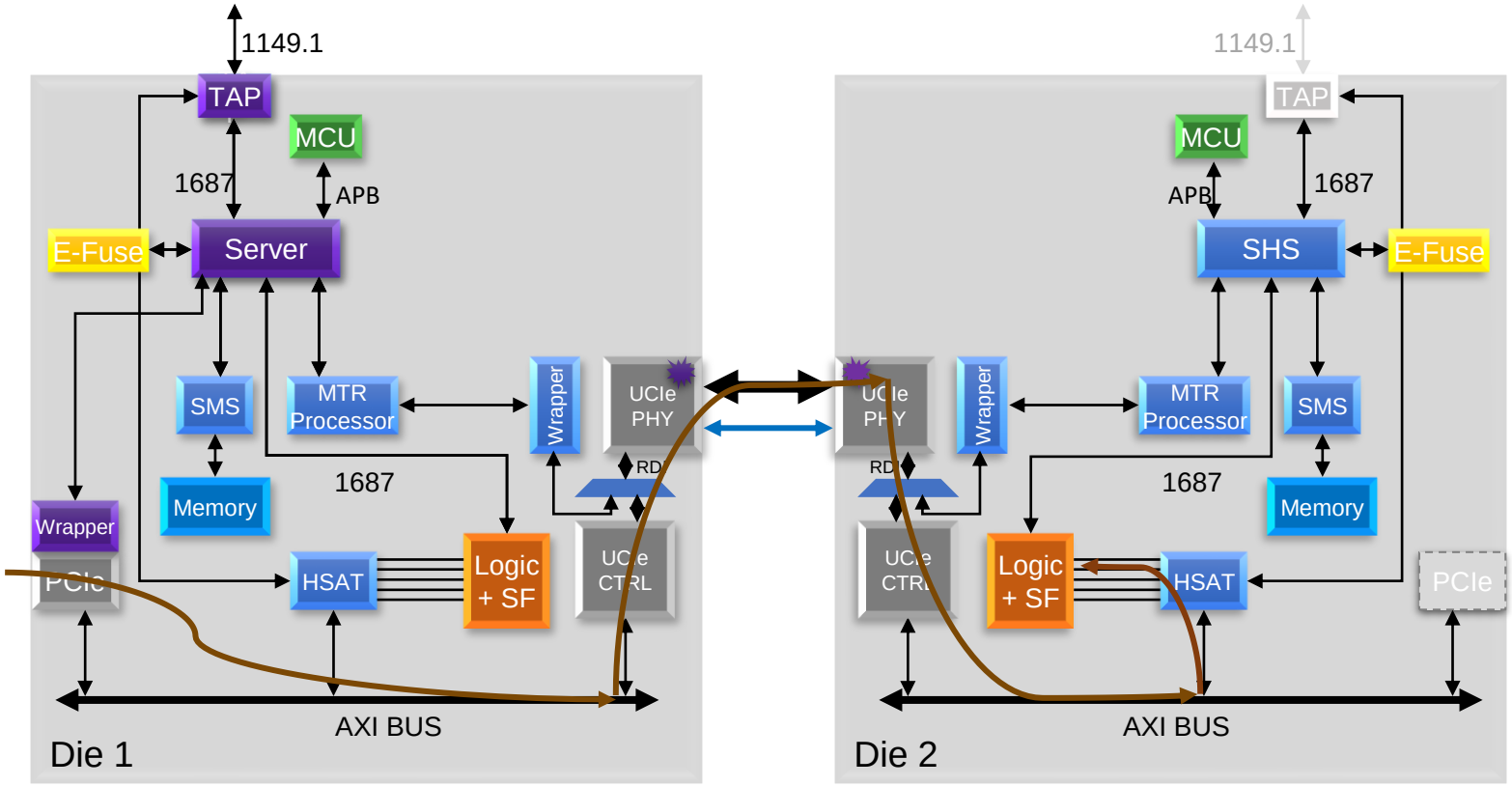
- Per-lane health monitoring
- Lane Testing (algorithmic)
- Lane Repair (cumulative)

Reliability Architecture w/

- Built-in SIM in UCIe PHY
- Mission mode eye-diagram monitoring & repair
- Power-on Self-Test & Repair
- Embedded and cloud analytics for real time control & fleet statistic

Accelerating Multi Die Testing with UCIe™

UCIe I/F as High-Speed Test Access Path for All Chiplets



Test Architecture Enables

- High speed load of test vectors across dies with UCIe™ die to die I/F
- All dies accessible through single point of access for test vector loading with PCIe® I/F (or other)

Flash Memory Summit

UCIe™
Universal Chiplet Interconnect Express

THANK YOU

www.UCIexpress.org