



# Stacked Dynamic Flash Memory (DFM) for a High Density Memory

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# Stacked Dynamic Flash Memory

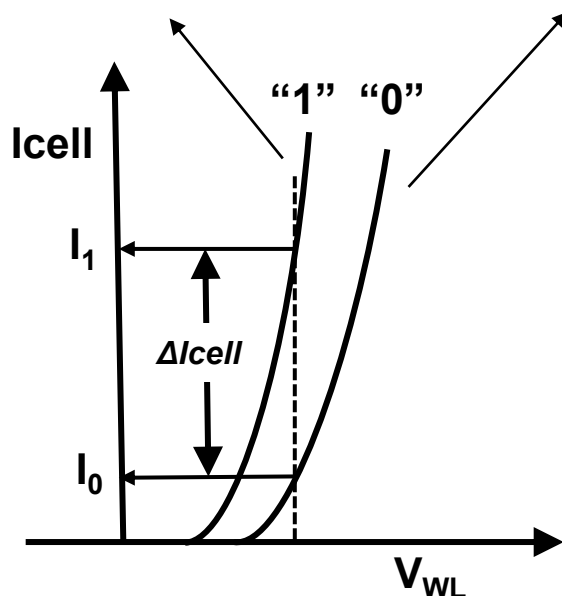
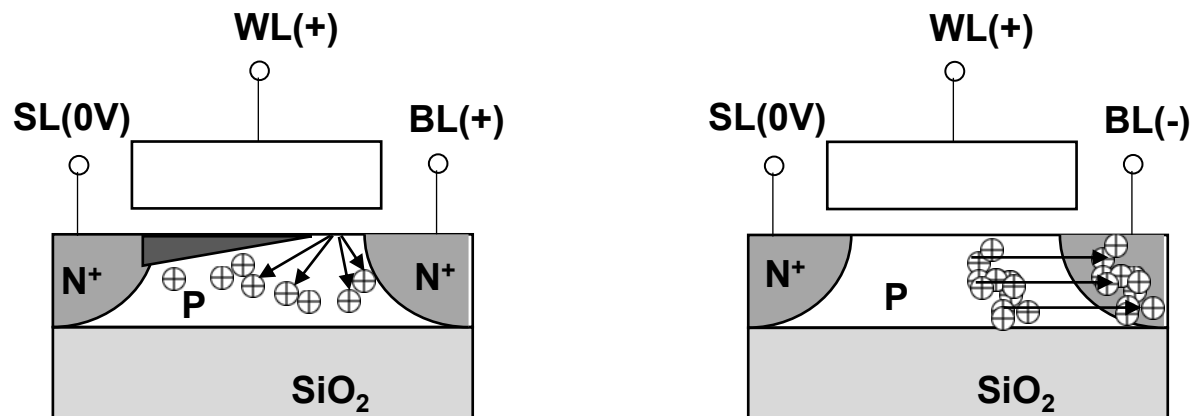
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- 1. 3G\_DFM Introduction**
- 2. Stacked DFM Structure**
- 3. Stacked DFM Prospects and Potential**
- 4. Conclusion**

# 1T-DRAM “1” Program and “0” Erase Mechanism

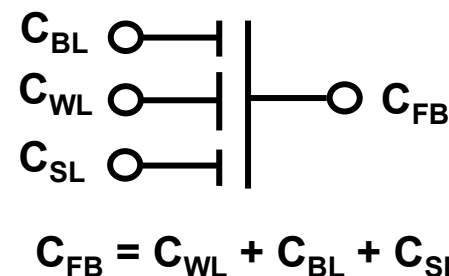


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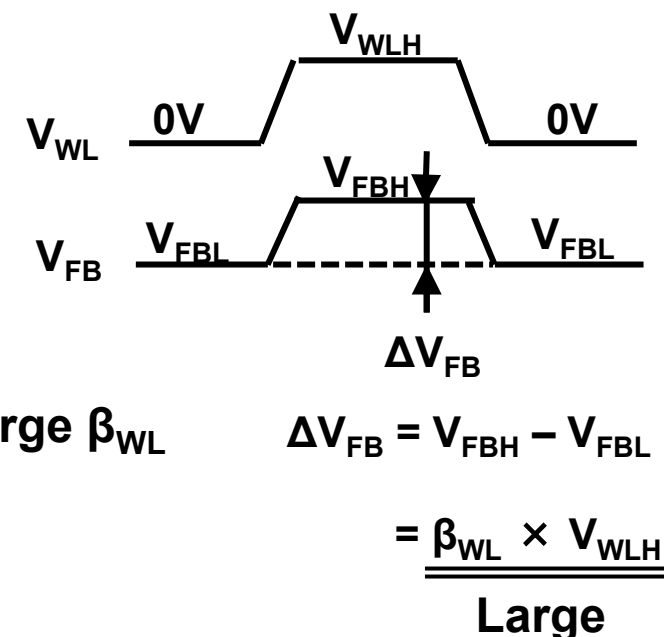


Concerning

1. Large WL capacitive coupling to FB
2. Small “1” and “0” margin
  1. Cell Vth is defined by WL
  2. Negative WL is required for maintaining “1”



$$\beta_{WL} = \frac{C_{WL}}{C_{WL} + C_{BL} + C_{SL}} \Rightarrow \text{Large } \beta_{WL}$$



1. K. Sakui, “Semiconductor Storage Device,” *Japanese Patent Application* Number: 01-311386, Publication Number: 03-171768, Filed on Nov. 30, 1989.  
<https://www.j-platpat.inpit.go.jp/c1800/PU/JP-H03-171768/FB67F895FBFE2F6E87B65C8C6F657C4AF31A01A65ED0C2F6EC8D0EF1473CECCA/11/en>

# “1” Program and “0” Erase Mechanism

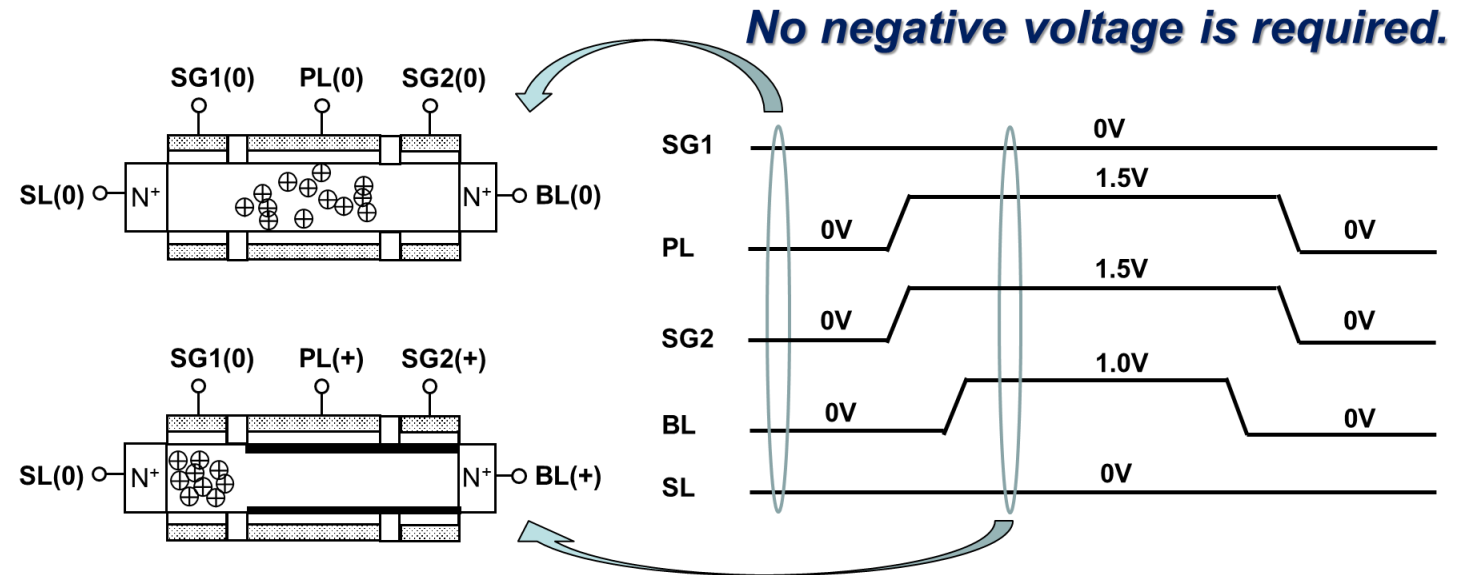
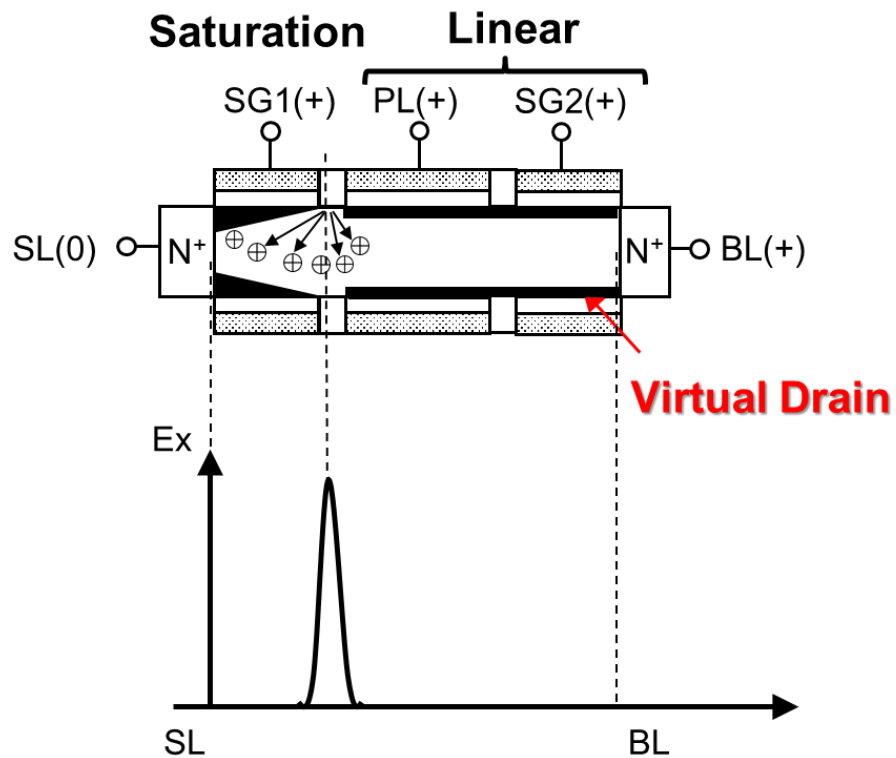


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“1” Program

“0” Erase

~Source-side Impact Ionization~

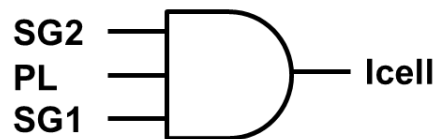


# Wide “1”-“0” Margin



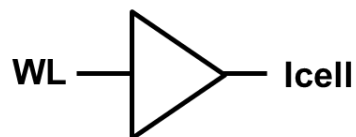
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## Logical Expression



SG1	PL	SG2	Icell
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

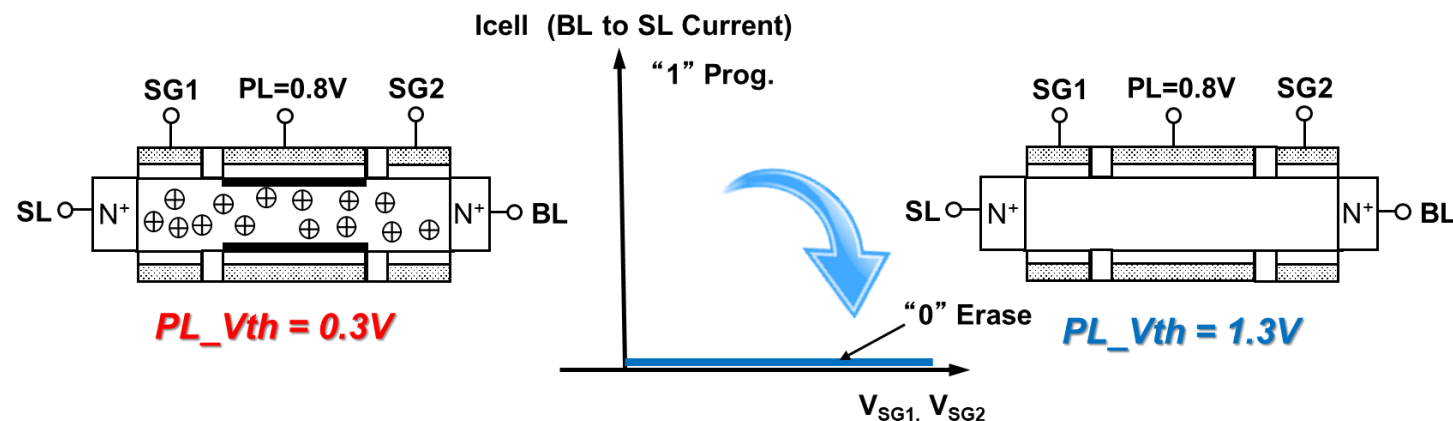
(b) 3G\_DFM



WL	Icell
1	1
0	0

(a) 1T-DRAM

PL plays a storage, while SG1/SG2 plays a switch !



**A fixed voltage of 0.8V is applied to PL on reading.**

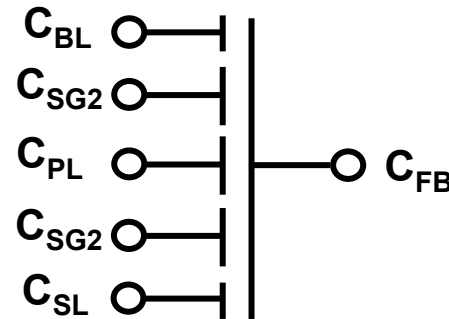
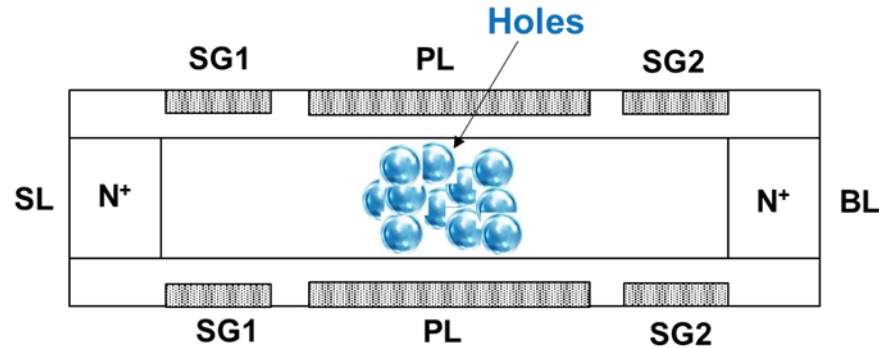
K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, “Design Impact on Three Gate Dynamic Flash Memory (3G\_DFM) for Long Hole Retention Time and Robust Disturbance Shield,” in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

# The FB Stabilization by the Three Gates

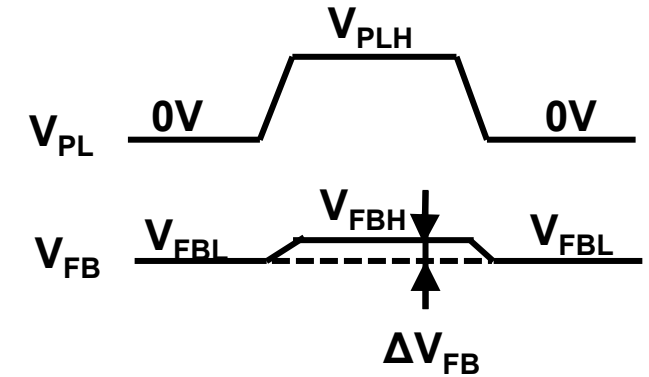


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*Small gate capacitive coupling to FB !*



$$C_{FB} = C_{SG1} + C_{PL} + C_{SG2} + C_{BL} + C_{SL}$$



$$\Delta V_{FB} = V_{FBH} - V_{FBL}$$

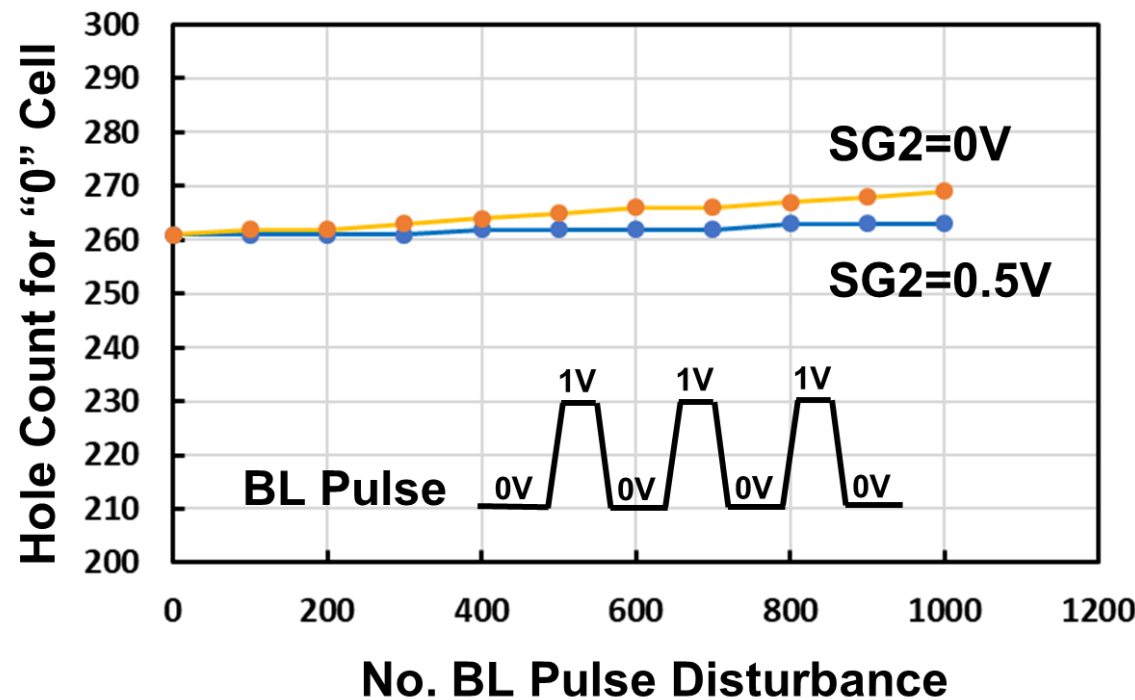
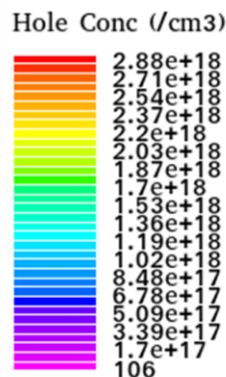
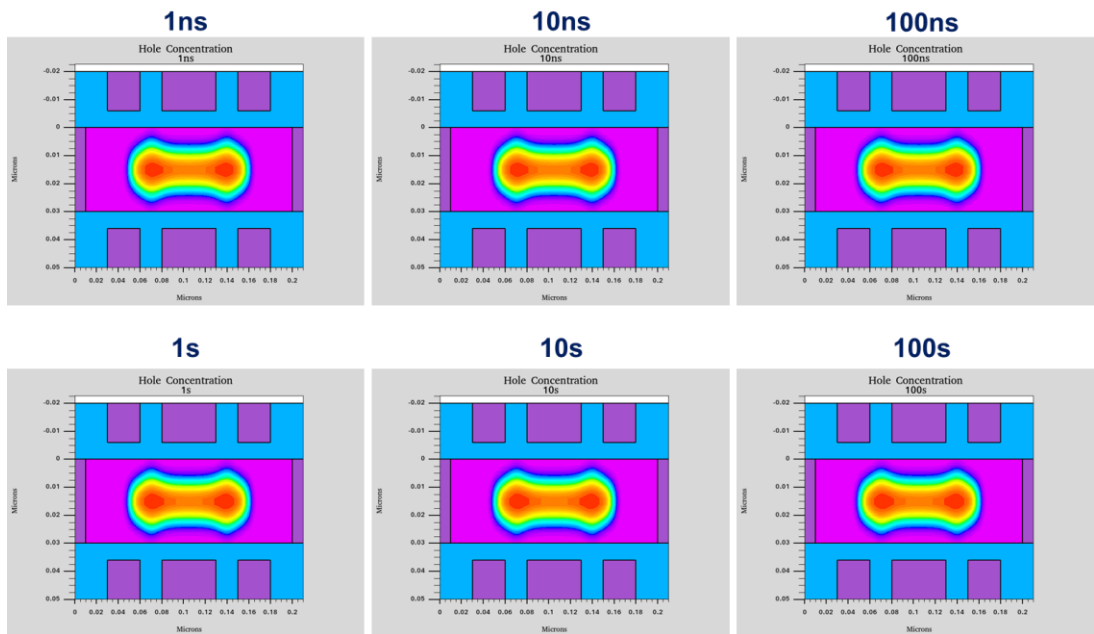
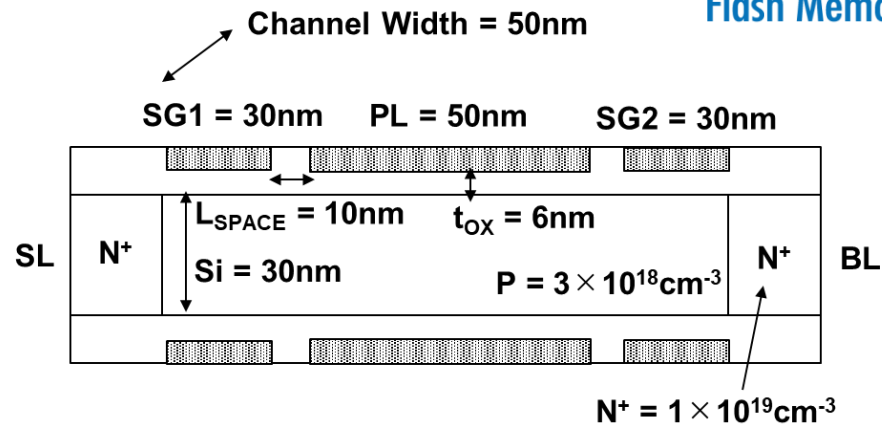
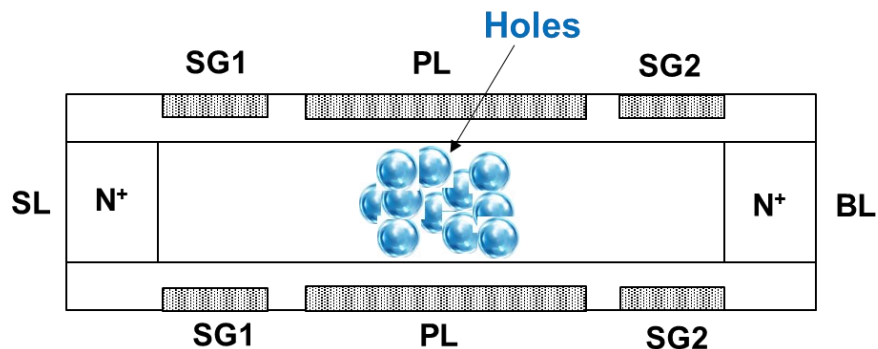
$$\beta_{PL} = \frac{C_{PL}}{C_{SG1} + C_{PL} + C_{SG2} + C_{BL} + C_{SL}} \Rightarrow \text{Small } \beta_{PL} = \frac{\beta_{PL} \times V_{LPH}}{\text{Small}}$$

K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G\_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

# 3G\_DFM Robustness Against Disturbance



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Hole Concentration After "1" Write (PL=0V, 85°C)

# Stacked Dynamic Flash Memory

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## 2. Stacked DFM Structure

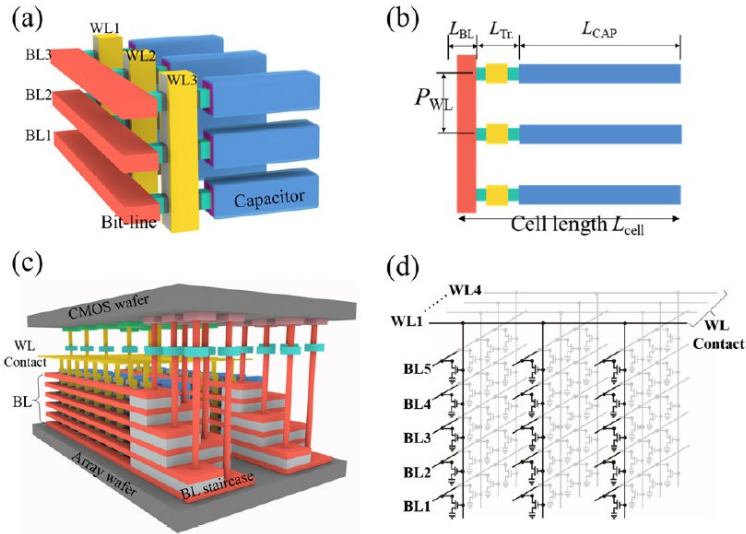


# 3D DRAM Papers



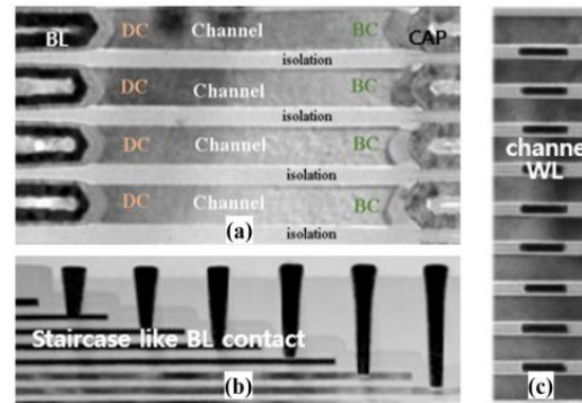
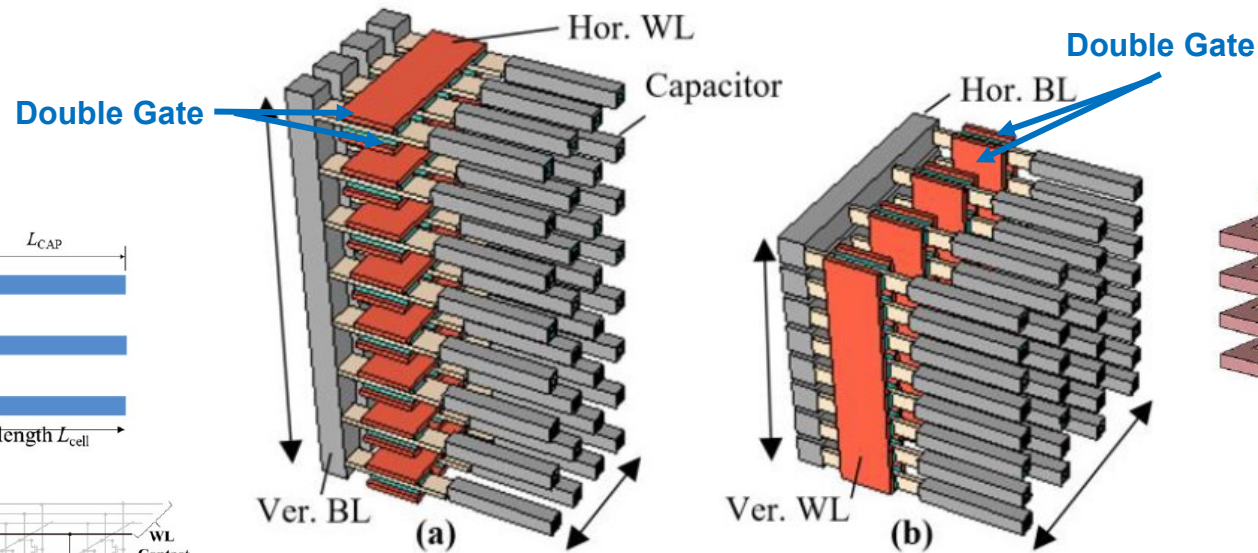
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## CXMT: Stacked 1T1C IMW 2023



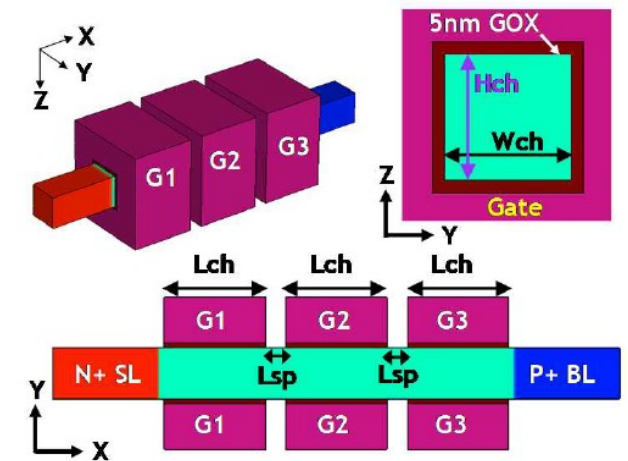
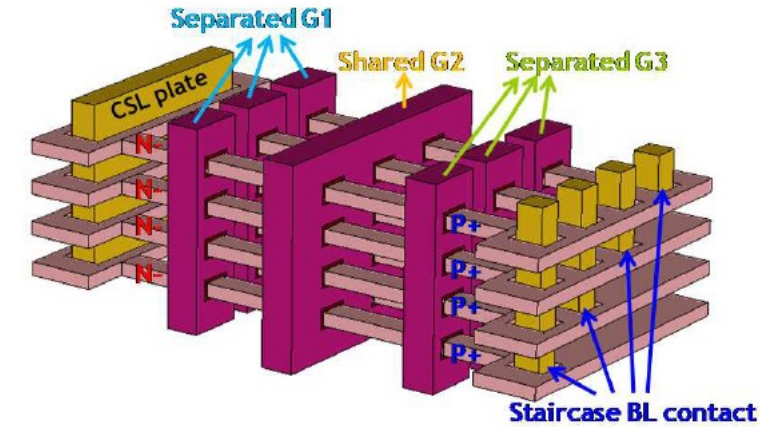
M. Huang et al., "A 3D Stackable 1T1C DRAM: Architecture, Process Integration and Circuit Simulation," in *Proc. IEEE IMW*, pp.29-32, May 2023.

## Samsung: Stacked 1T1C VLSI 2023



J.W. Han et al., "Ongoing Evolution of DRAM Scaling via Third Dimension - Vertically Stacked DRAM -," in *2023 Symposium on VLSI Technology and Circuits Digest of Technical Papers, TFS1-1*, pp.1-2, Jun. 2023.

## Macronix: Stacked Thyristor IEDM 2022, IMW 2023

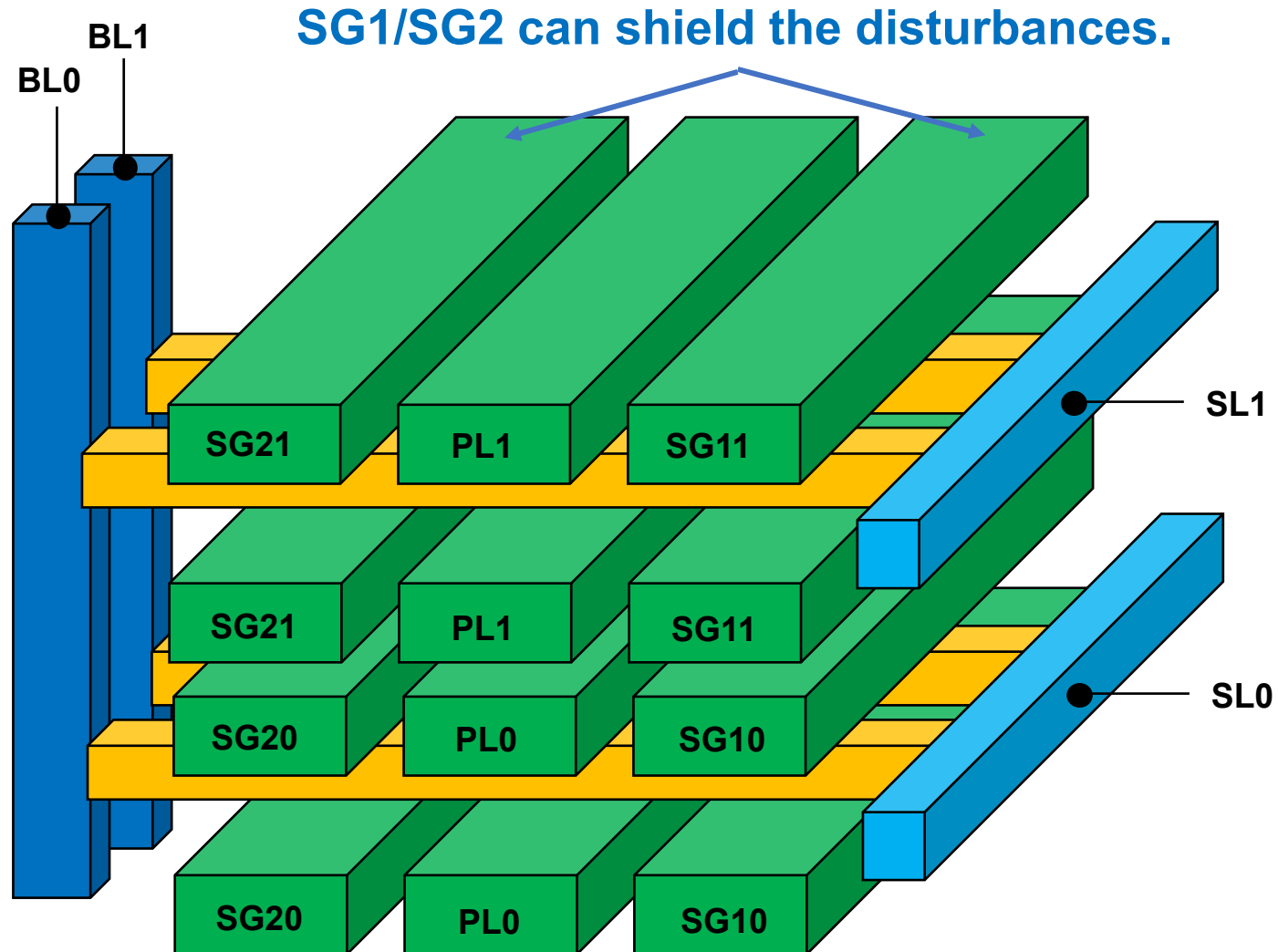


W. C. Chen et al., "A Simulation Study of Scaling Capability toward 10nm for the 3D Stackable Gate-Controlled Thyristor (GCT) DRAM Device," in *Proc. IEEE IMW*, pp.25-28, May 2023.

# Double Stacked DFM (Horizontal Gates)



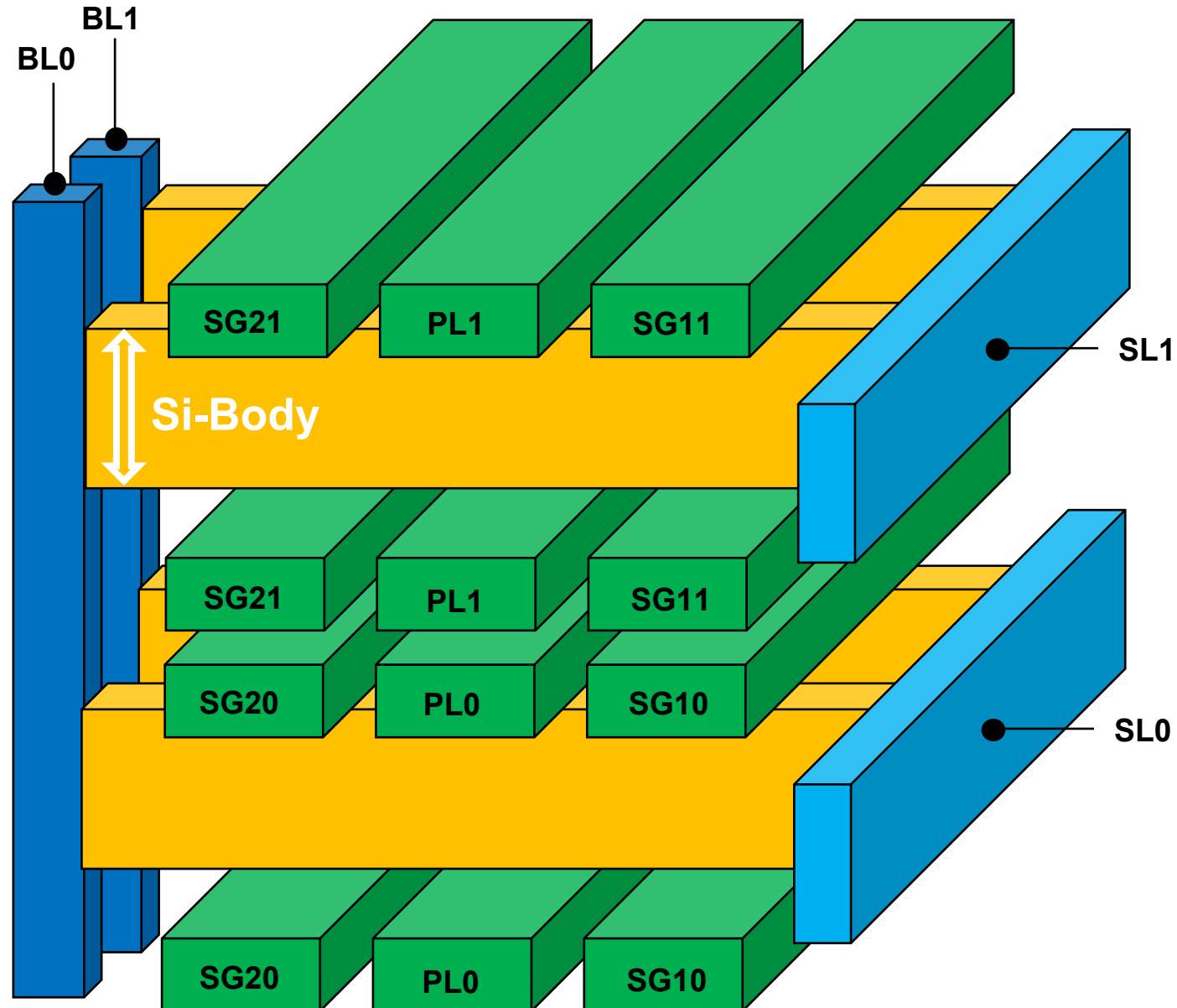
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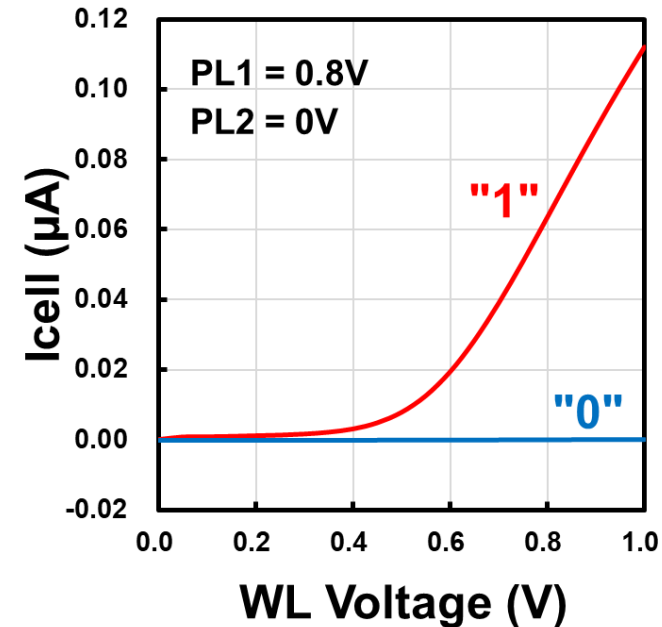
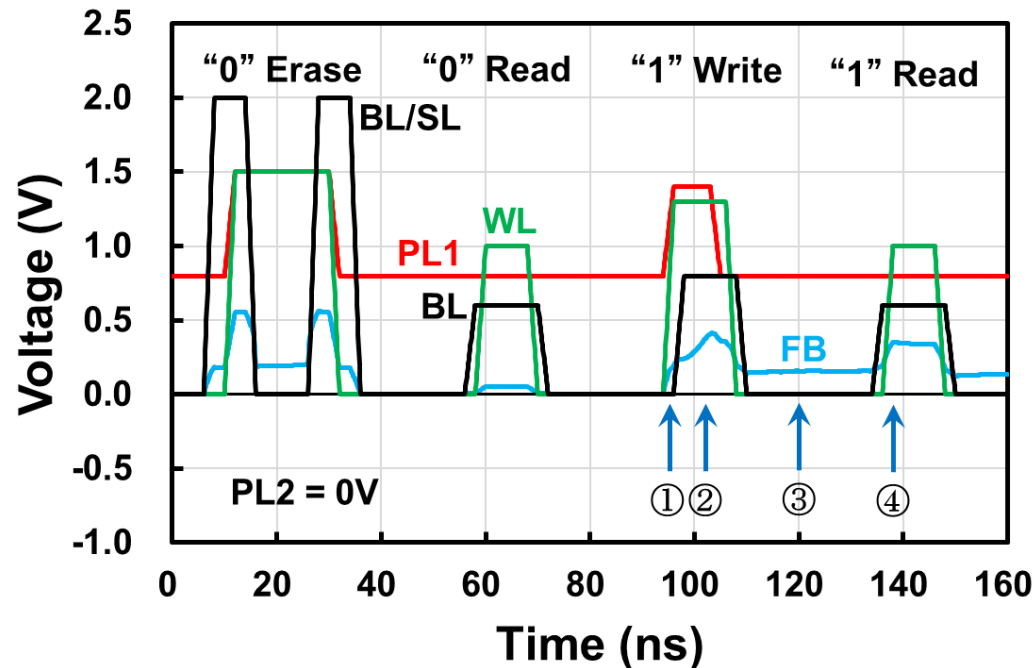
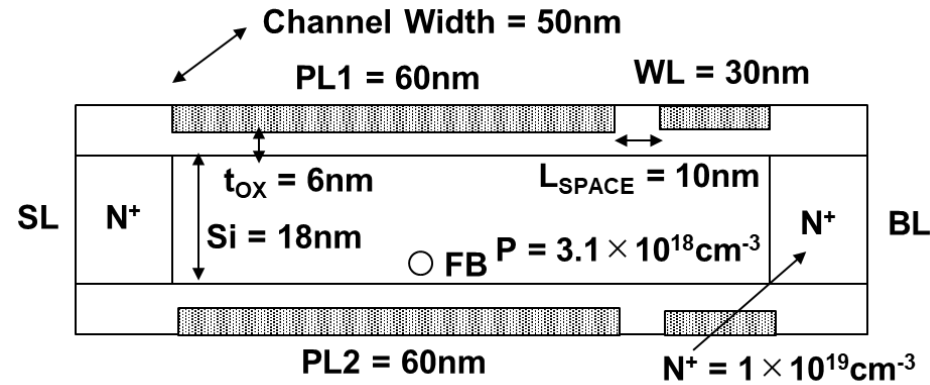
# Si-Body Thickness Control without Cell Size Increase



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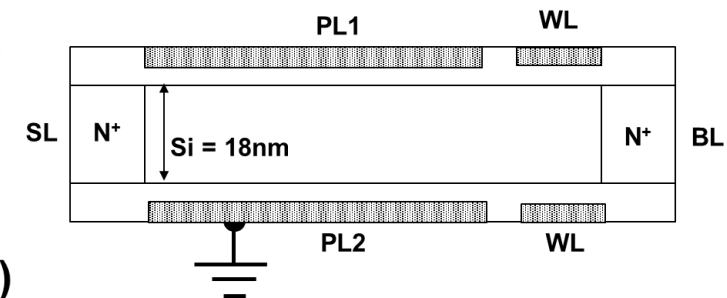
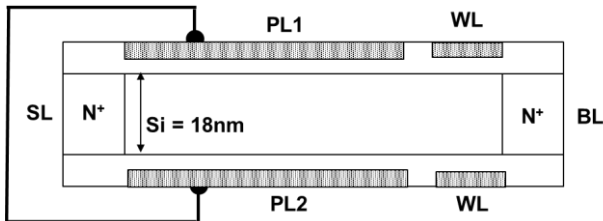
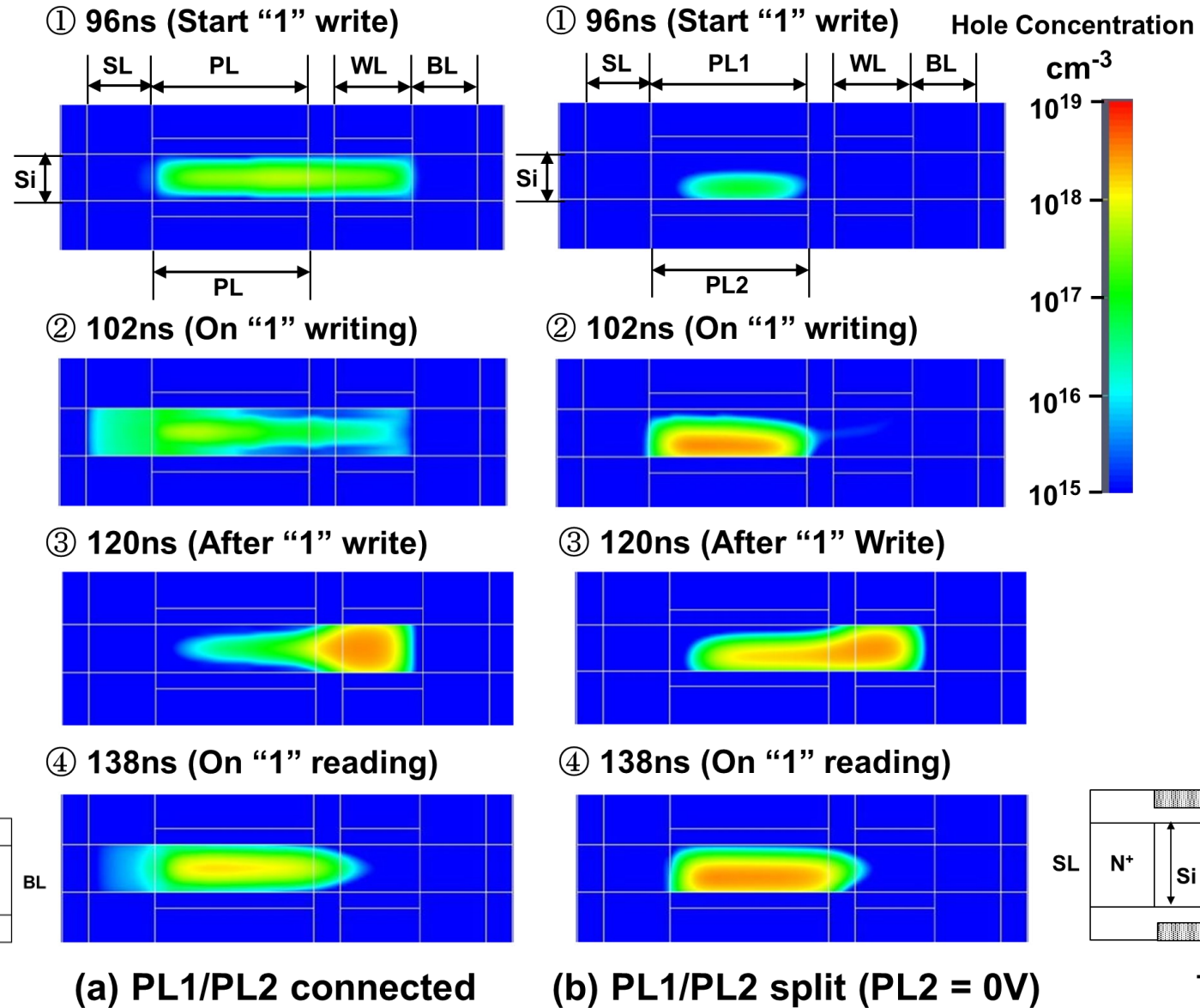
# 2G\_DFM (Double Gate)



# Hole concentration: (a) PL1 = PL2, (b) PL2 = 0V



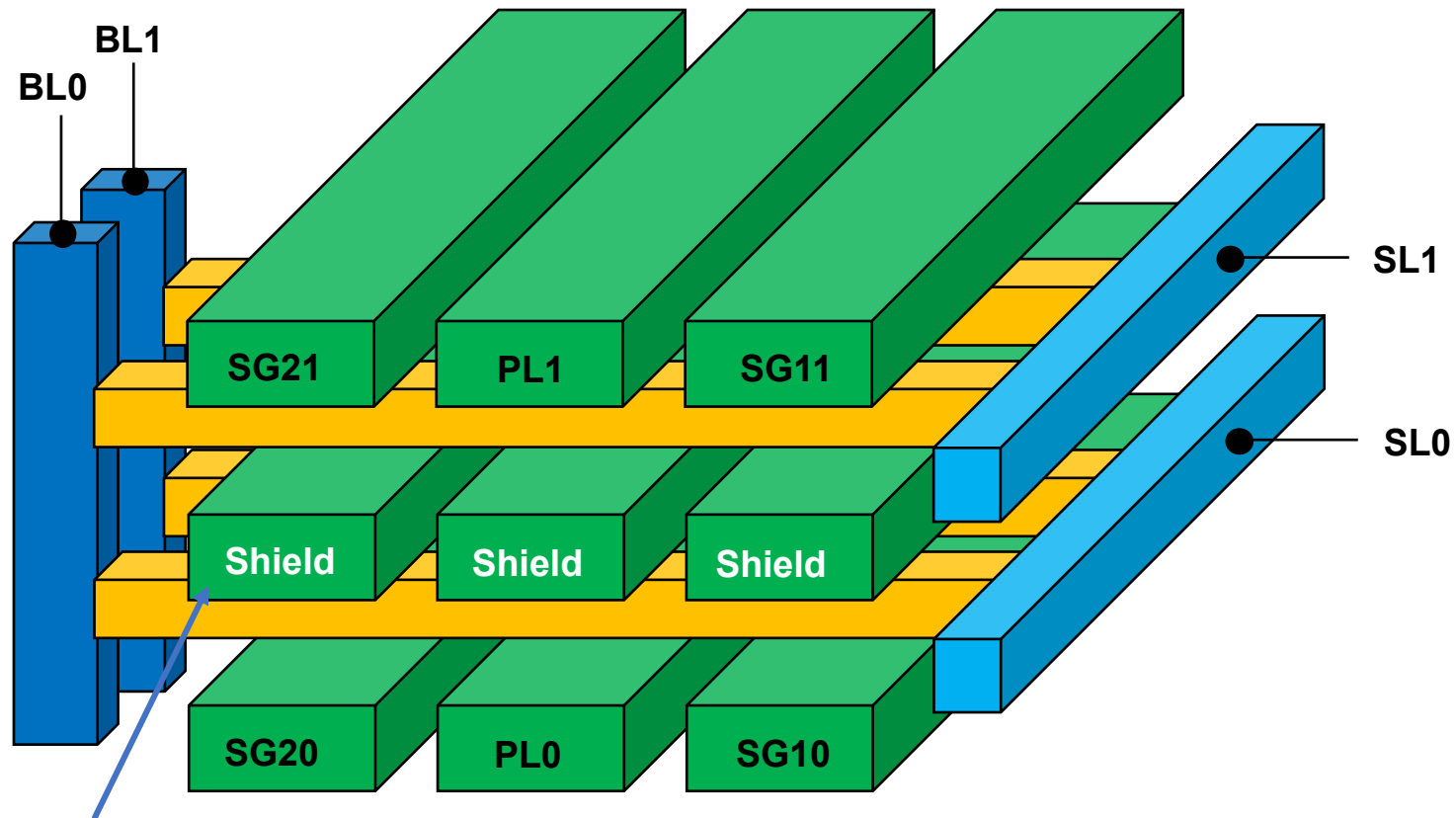
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# Two Stack DFM (Horizontal Gate)

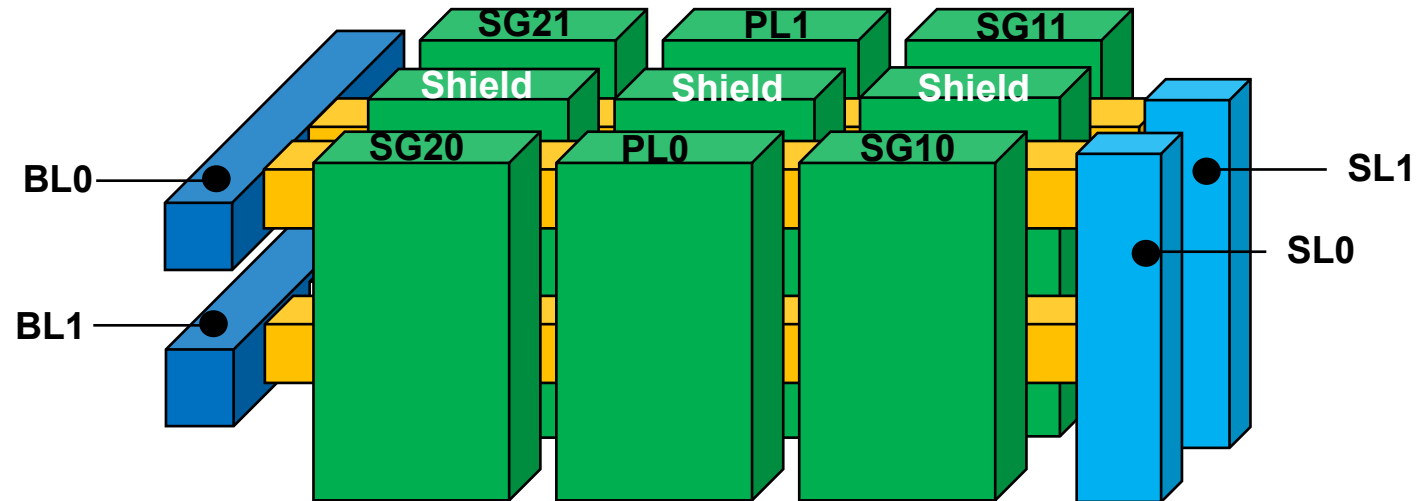


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One of double gates is grounded.

# Two Stack DFM (Vertical Gate)



# Stacked Dynamic Flash Memory

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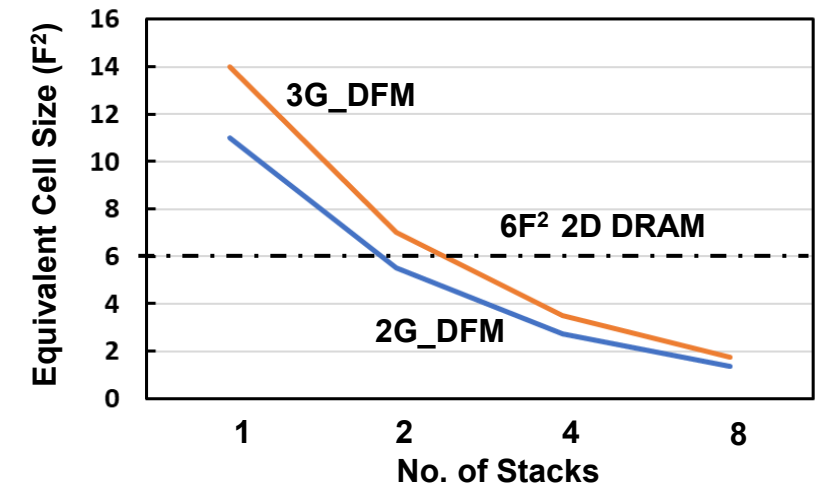
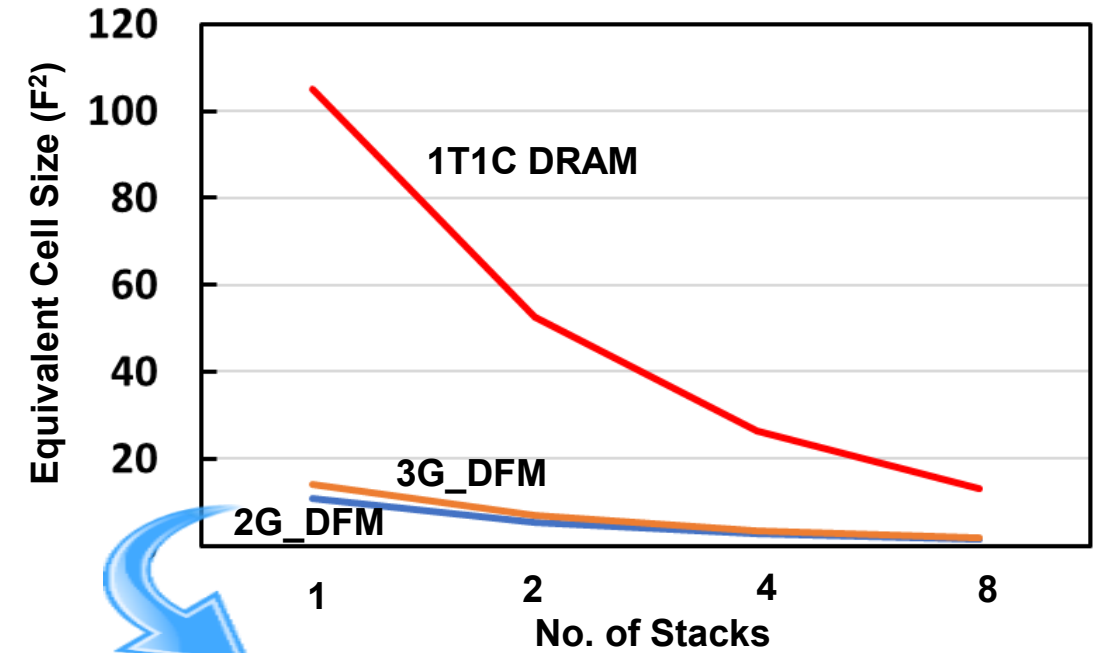
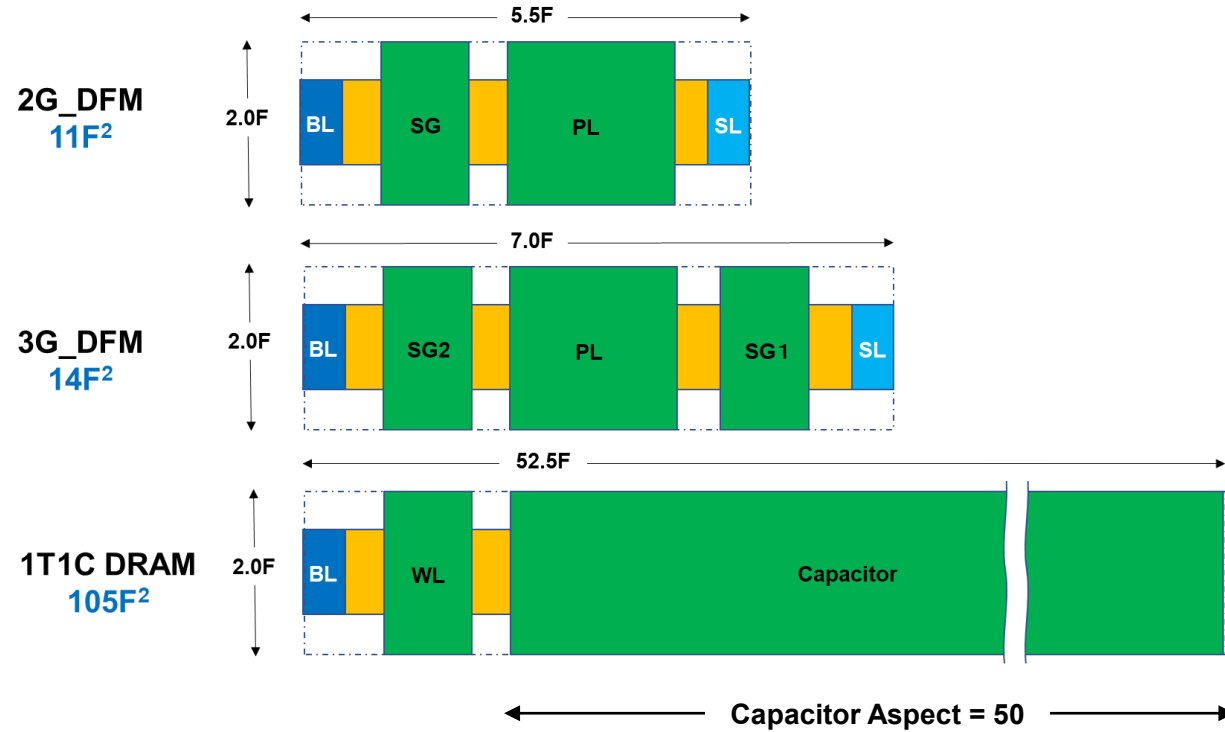
## 3. Stacked DFM Prospects and Potential



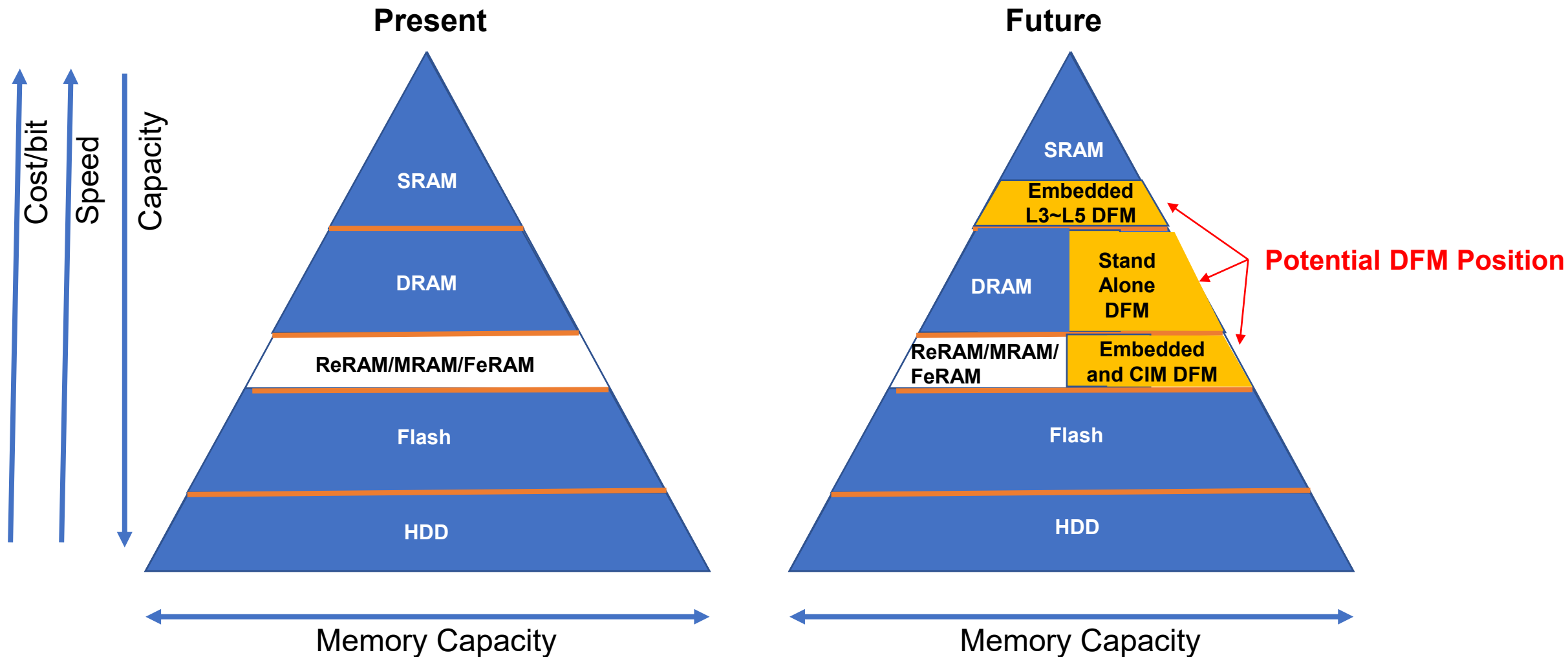
# Equivalent Cell Size



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# Potential DFM Position



# Stacked Dynamic Flash Memory

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## 4. Conclusion

# Conclusion

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1. The stacked 3G\_DFM has a substantial potential to realize a much smaller equivalent cell than  $6F^2$  with 3~4 tiers.
- ➔ 2. Unlike emerging memories, such as ReRAM and MRAM, neither variable resistors nor special materials are needed. It should be noted that DFM can be fabricated with the conventional Si process.
- ➔ 3. A low cost stackable DFM is a promising device positioned next to DRAM and NAND in the memory hierarchy.