QuInAs Technology

Flash Memory Summit

Introducing ULTRA**RAM**: A high-performance, ultra-efficient, non-volatile memory

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9th August, Flash Memory Summit 2023

Physics | Lancaster University

Universal Memory

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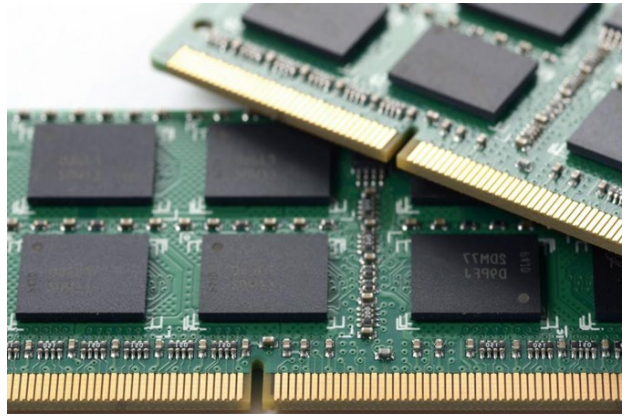
Flash		DRAM
High voltage switching (<20 V)	✗ ✓	Low voltage/energy switching (<2V)
Intrinsically slow P/E (10 μs)	✗ ✓	Fast operation (10 ns)
Low endurance (10^5)	✗ ✓	High endurance (10^{16})
Non-volatile	✓ ✗	Volatile
Non-destructive read	✓ ✗	Destructive read
Highly scalable	✓ ✗	Scaling challenges



A universal memory should combine only the best features of both!

ULTRARAM™
ULTRA-EFFICIENT MEMORY

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Universal Memory:
How to have your cake and eat it?

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The problem with Universal Memory is that we need to fulfil ***contradictory requirements***

- Long storage time (>>10 years at single bit level)
- Ability to quickly (10 ns) and easily program/erase data (low switching energy)

"Now it is generally agreed that the vision of a universal memory is not realistic...

…the need for low energy consumption during writing operations is accomplished by lowering the energy barrier to be overcome when erasing or writing data, which limits the non-volatile retention time of data. "

H.-S. Wong and S. Salahuddin, Nat. Nano. **10**, 191 (2015)

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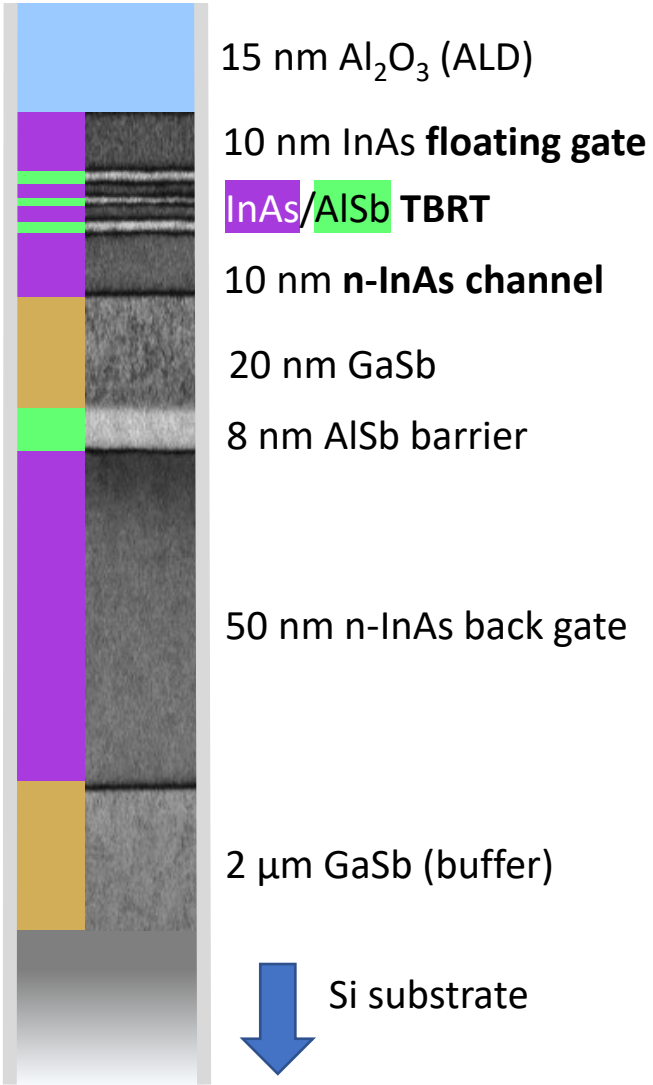
ULTRA**RAM**™ concept

Hayne US10243086B2

- Floating gate memory (like flash)
- Compound semiconductor based
- High-mobility InAs channel
- Grown on silicon substrates
- Oxide tunnelling barrier is replaced by a

Triple barrier resonant tunnelling barrier structure (TBRT)



ULTRA**RAM**™ cell

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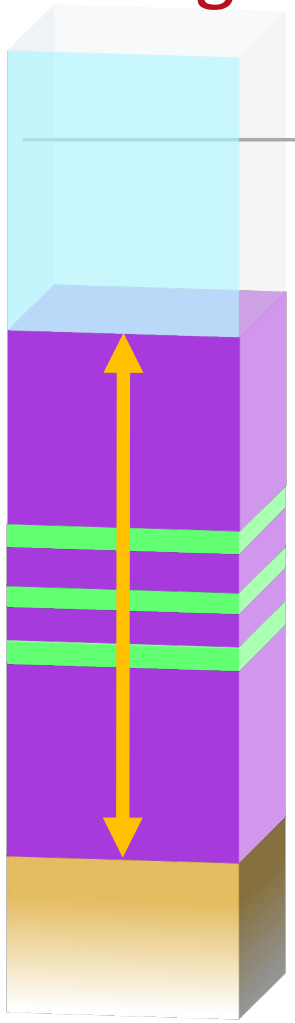
Charge retention (no bias)



blocking barrier oxide

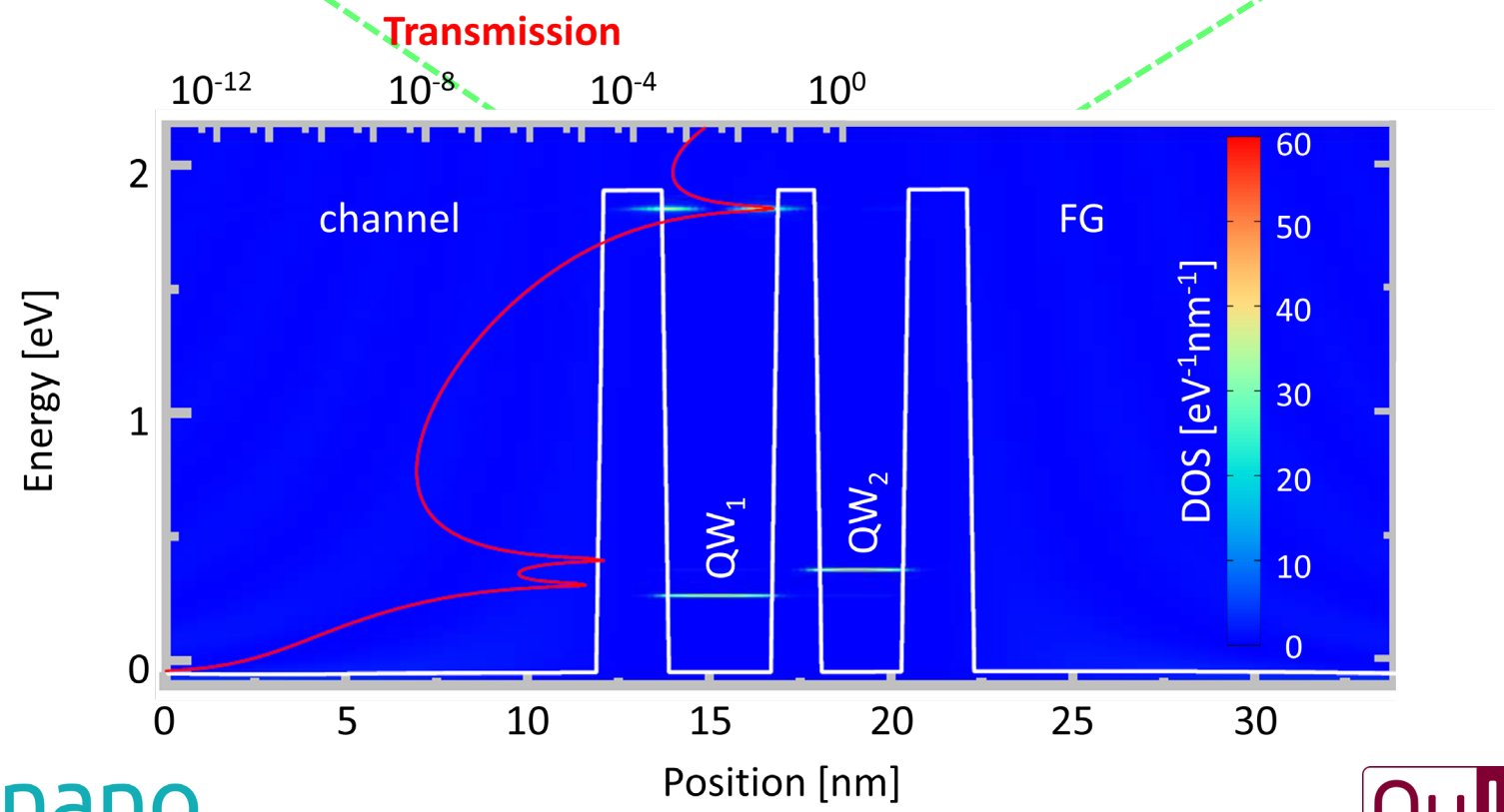
floating gate (**FG**) InAs

TBRT region InAs/AlSb

channel InAs

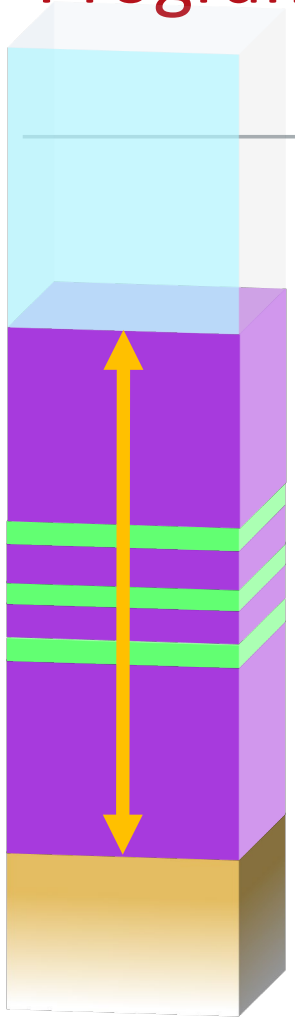
back gate (BG) and substrate layers

1.8 nm AlSb / 3.0 nm InAs / 1.2 nm AlSb / 2.4 nm InAs / 1.8 nm AlSb



Lane and Hayne, J. Phys. D: Appl. Phys. **54**, 35104 (2021)

Program and erase (≤2.5 V)



blocking barrier oxide

floating gate (**FG**) InAs

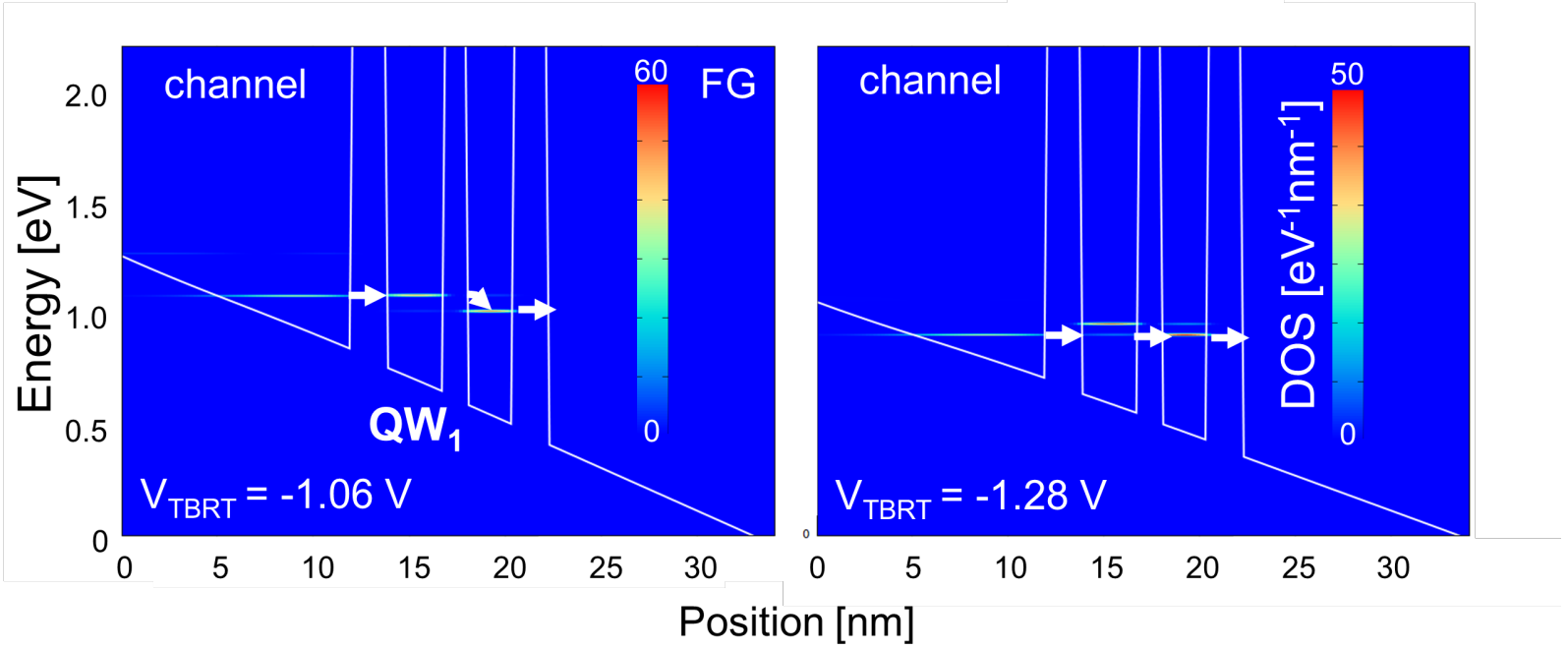
TBRT region InAs/AlSb

channel InAs

back gate (BG) and substrate layers

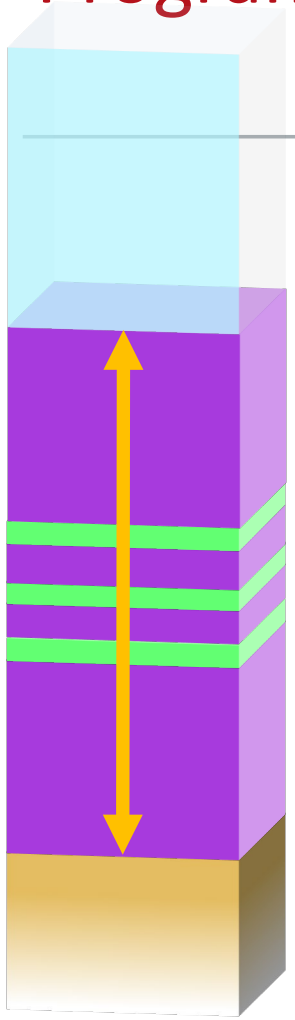
Program (P) cycle: add electrons to the floating gate

V_{CG-S} < +2.5 V



Lane and Hayne, IEEE Trans. Electron Devices **67**, 474 (2020).
Lane and Hayne, J. Phys. D: Appl. Phys. **54**, 35104 (2021).

Program and erase (≤2.5 V)



blocking barrier oxide

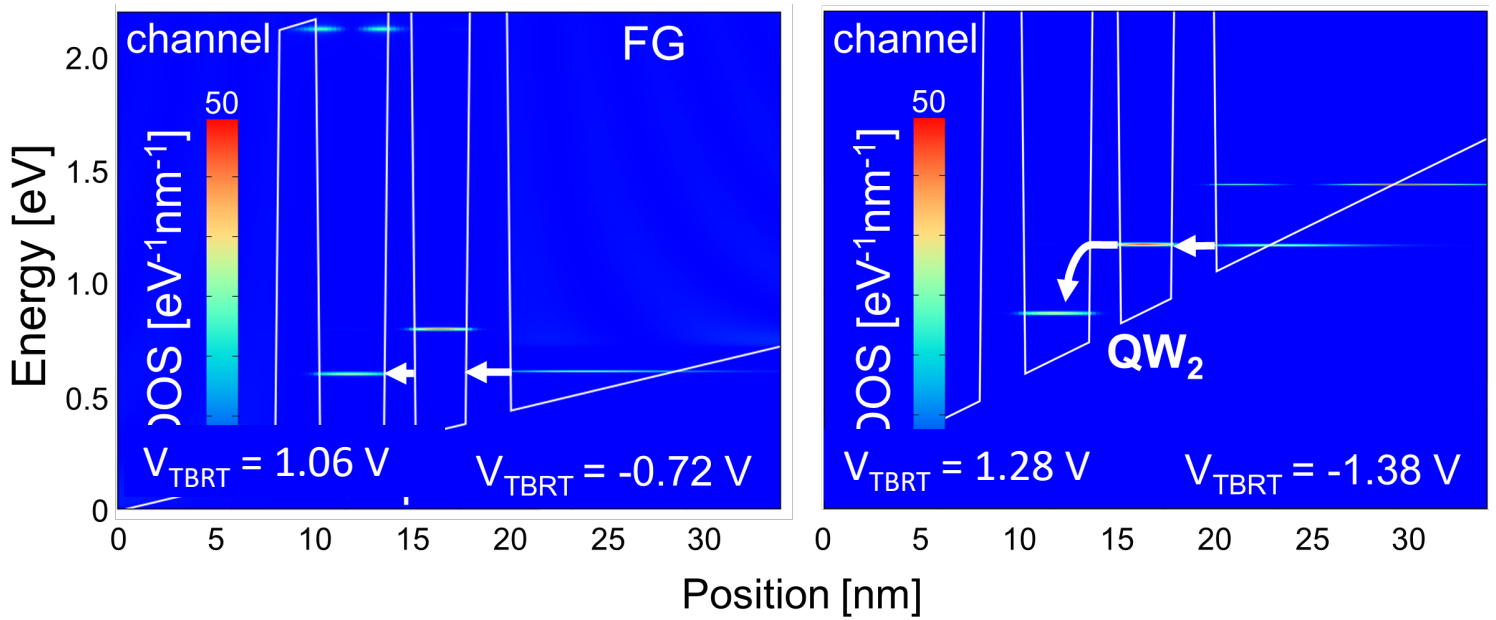
floating gate (**FG**) InAs

TBRT region InAs/AlSb

channel InAs

back gate (BG) and substrate layers

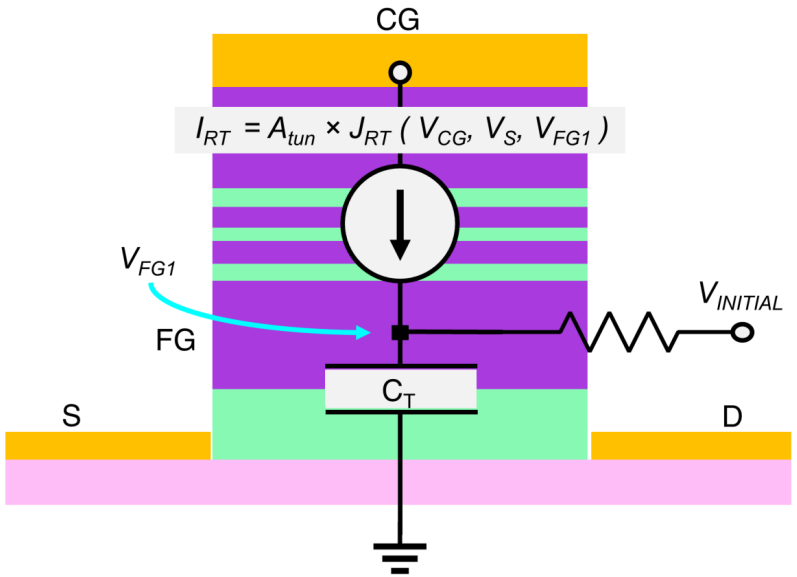
Erase (E) cycle: remove electrons from the floating gate
V_{CG-S} < -2.5 V

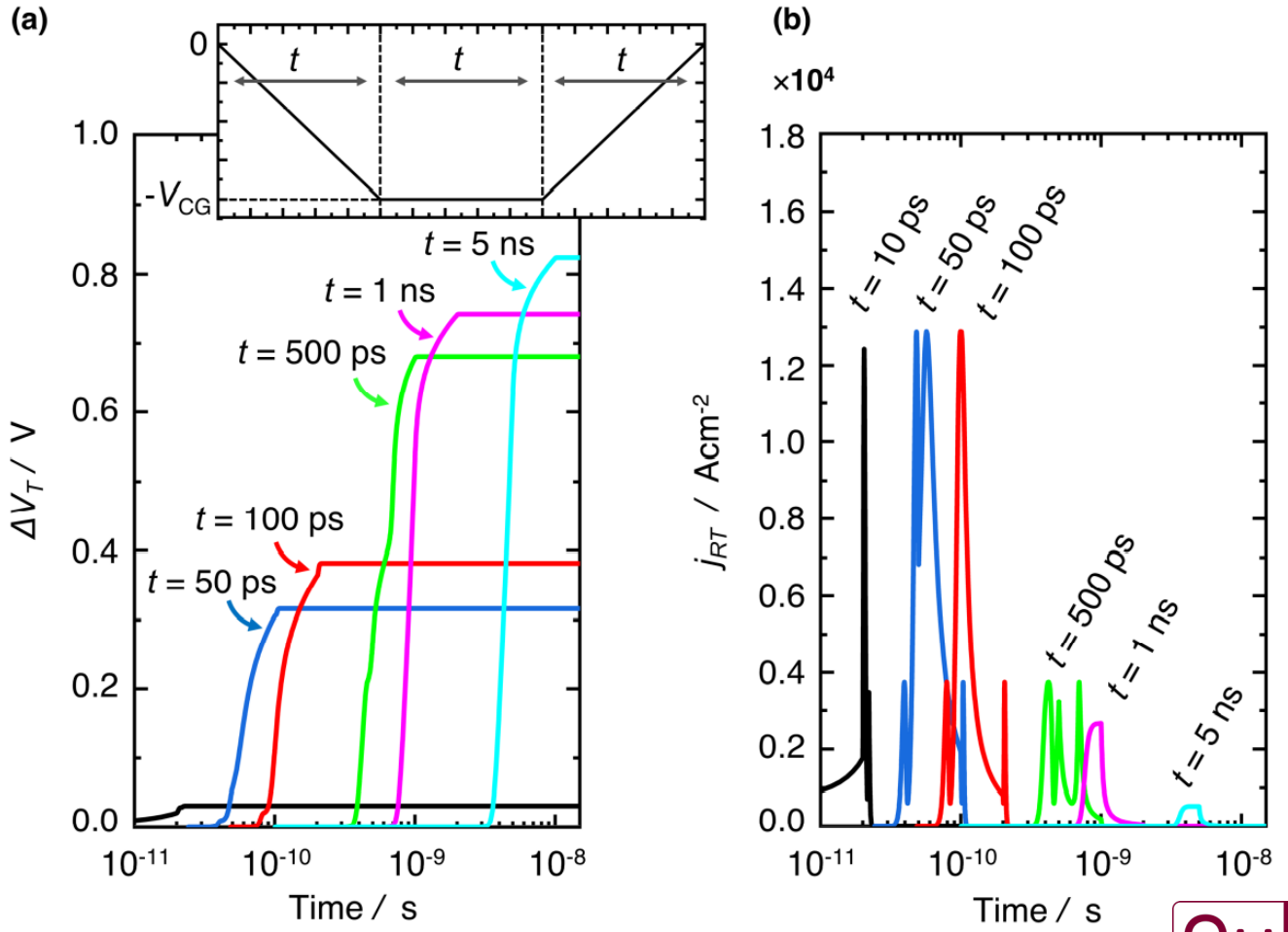


Lane and Hayne, IEEE Trans. Electron Devices **67**, 474 (2020).
Lane and Hayne, J. Phys. D: Appl. Phys. **54**, 35104 (2021).

Program and erase speed

$$\Delta V_T = Q_{FG}/C_{FG}$$

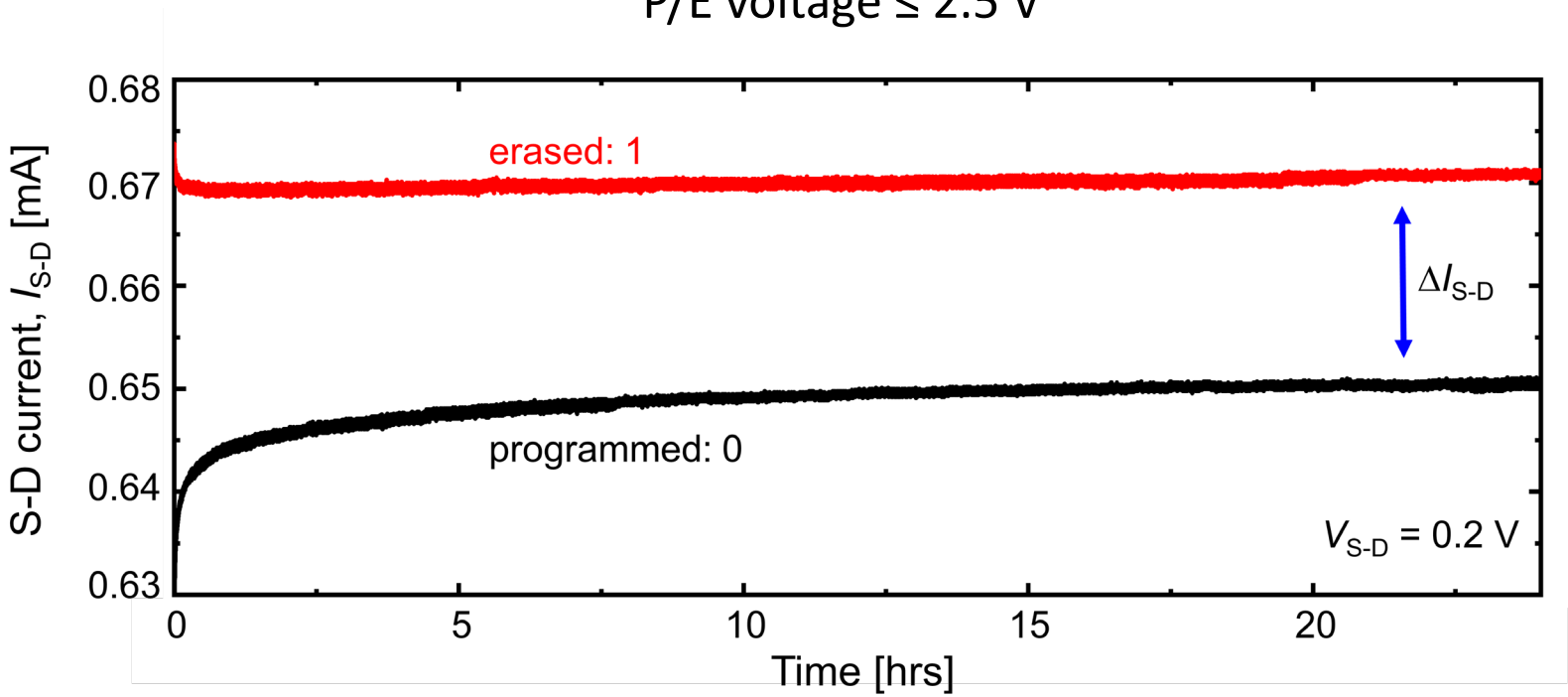




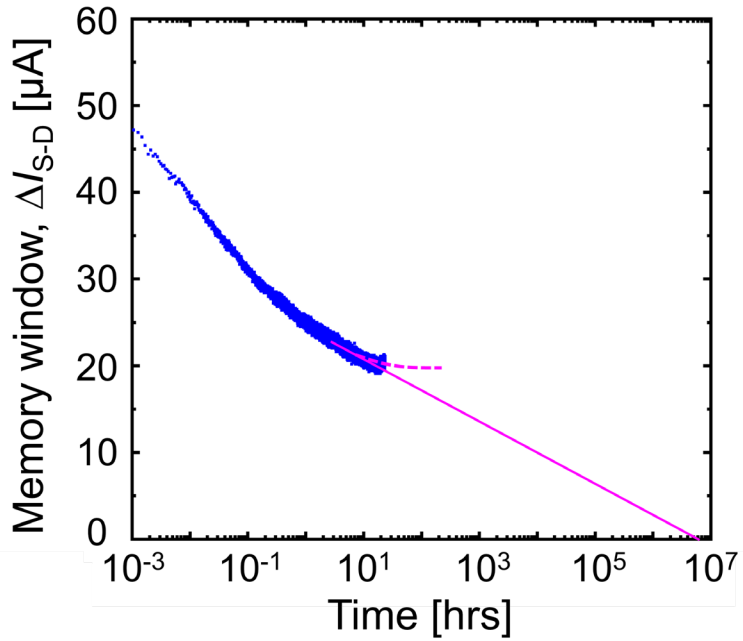
Lane, PhD Thesis, Lancaster University (2021)

Non-destructive read and retention

P/E voltage ≤ 2.5 V

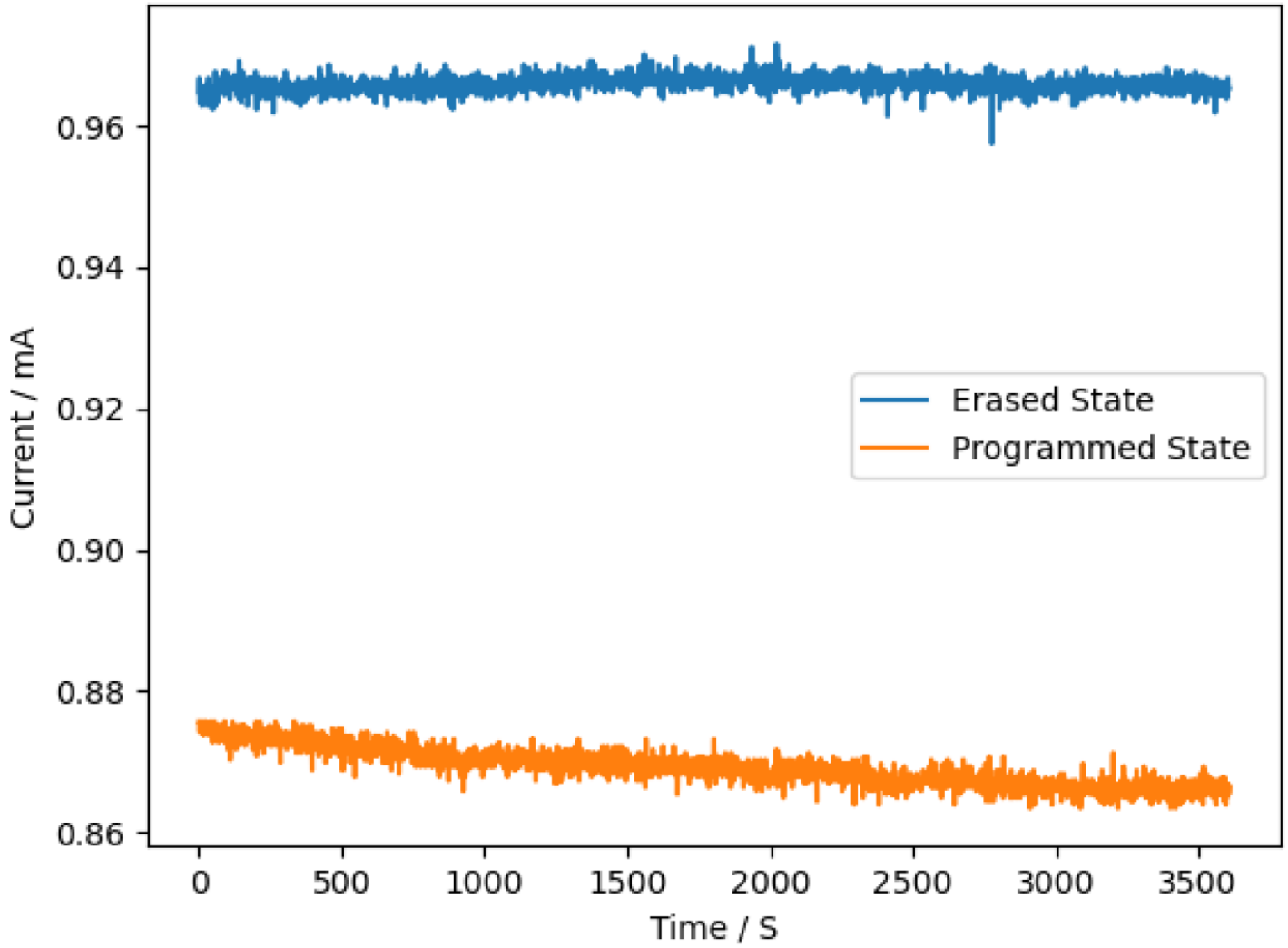


Retention >1000 years



Hodgson *et al.*, Adv. Electron. Mater. 2101103 (2022)

Retention @ 100°C



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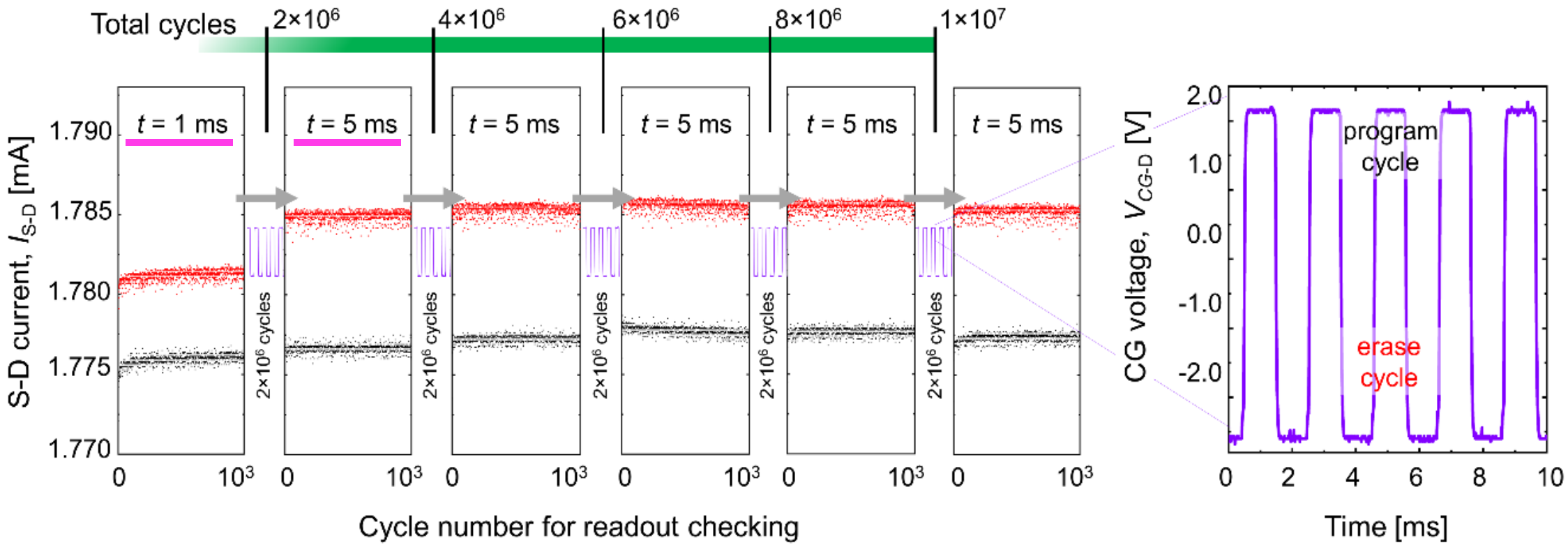
Endurance

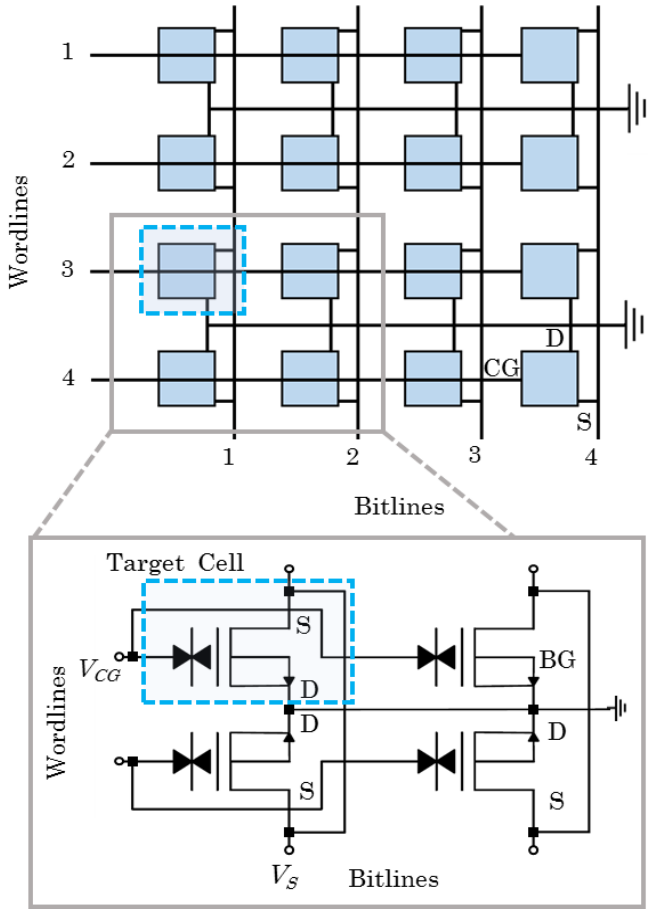


P/E pulse duration of 1 ms at 20 µm gate scales to 1 ns switching speed at 20 nm

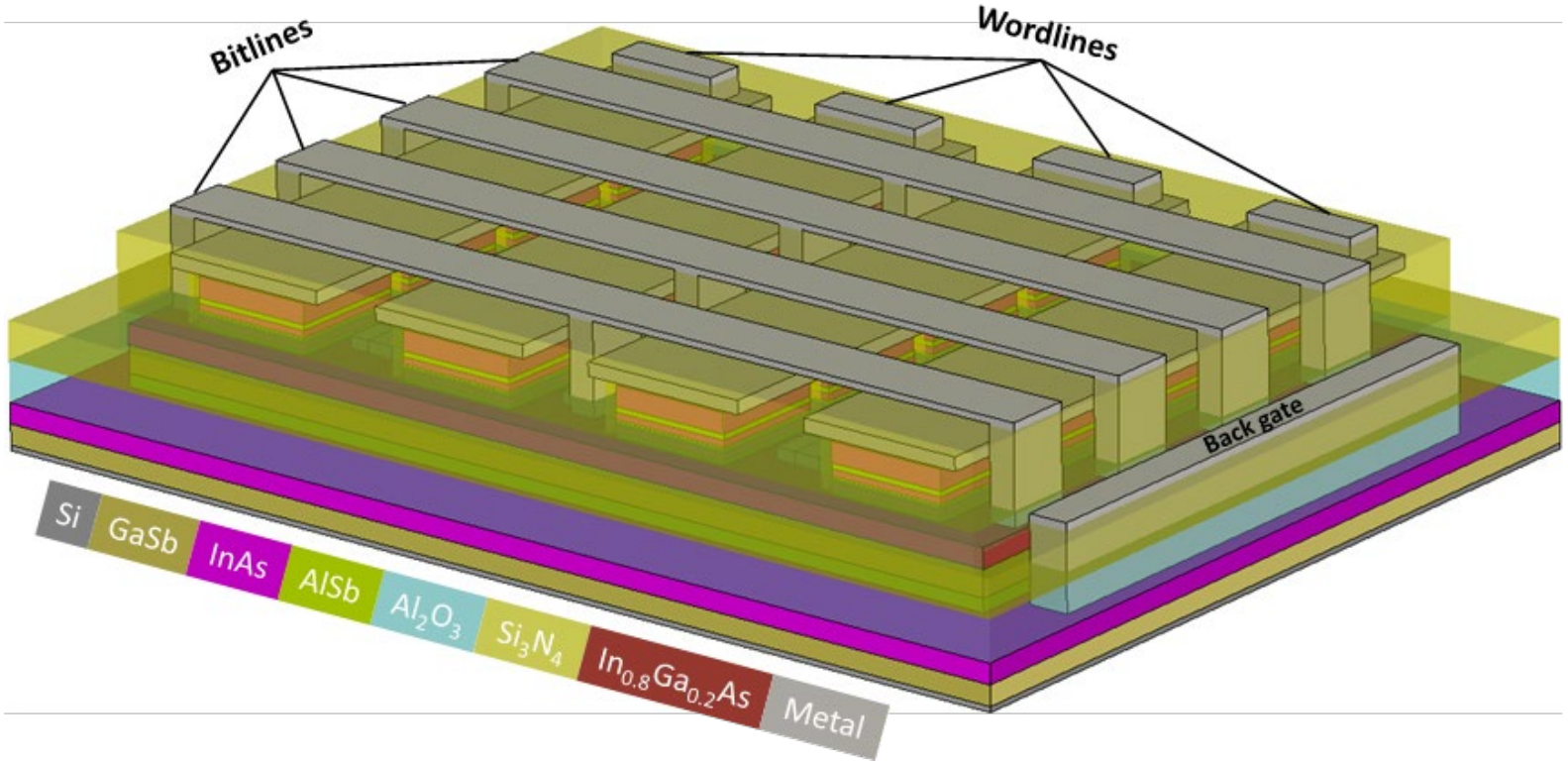
Hodgson *et al.*, Adv. Electron. Mater. 2101103 (2022)

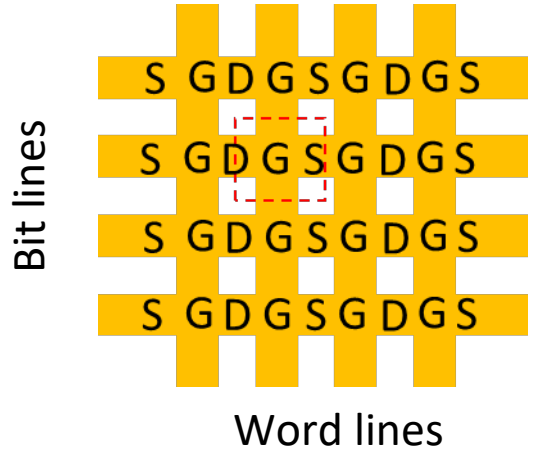
Arrays

- Highly compact design ($4F^2$) with devices back-to-back in pairs with common drain shorted to back gate
- Only word lines and bit lines need to run across the chip
- To write or erase half the voltage required is applied to word line (source) and bit line (gate)
- Due to sharp onset of resonant tunnelling very low disturb



16-bit RAM array design @ $4F^2$





Currently being implemented in cleanrooms at Lancaster University

ULTRA**RAM**™ in summary

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- Non-volatile with retention of at least 1,000 years
- Low voltage program erase (+1.25 V and -1.25 V using half-voltage)
- Intrinsically fast switching speeds (sub-ns)
- Ultralow switching energies
- Degradation-free endurance of at least 10^7 program/erase cycles (experiment limited)
- Compact array architecture ($4F^2$)
- Intrinsically excellent properties require minimal peripheral circuitry (non-destructive read, no refresh, no charge pumps, no wear-levelling)

For further information find us at Booth 656

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