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QLC High Density Storage

Flash Memory Summit 2023

Presenter

Ray Tsay | Co-Founder and VP Engineering

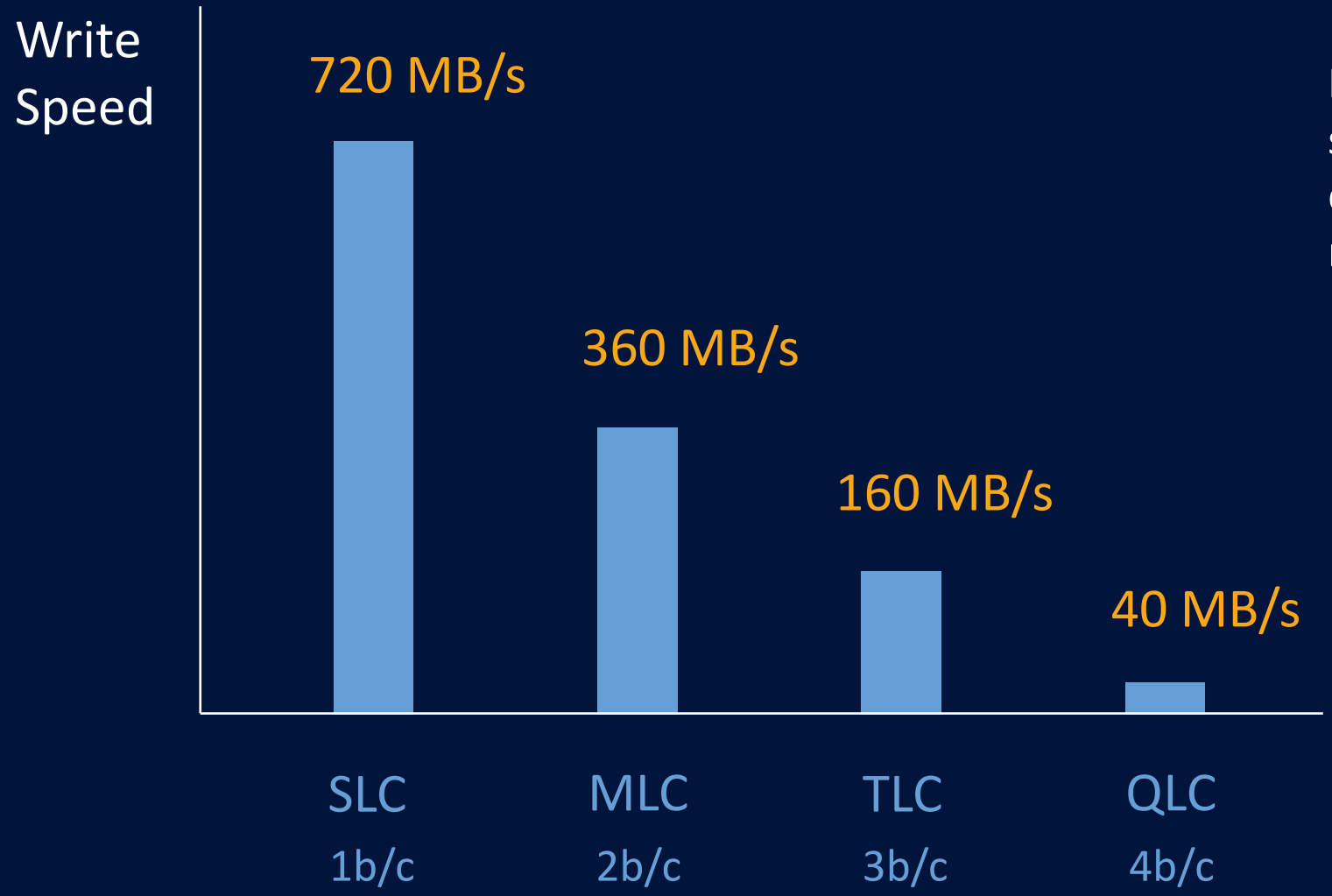
Ray has over 30 years of experience in the semiconductor industry. He led engineering teams for testing, product and manufacturing. He has broad experience in various products such as CCD, CPLD, SRAM, EEPROM, EPROM and flash memory.

https://www.neosemic.com

Agenda

1. NAND QLC Challenges
2. X-NAND Architecture
3. X-NAND Performance

Each Generation's Speed Has Become Slower



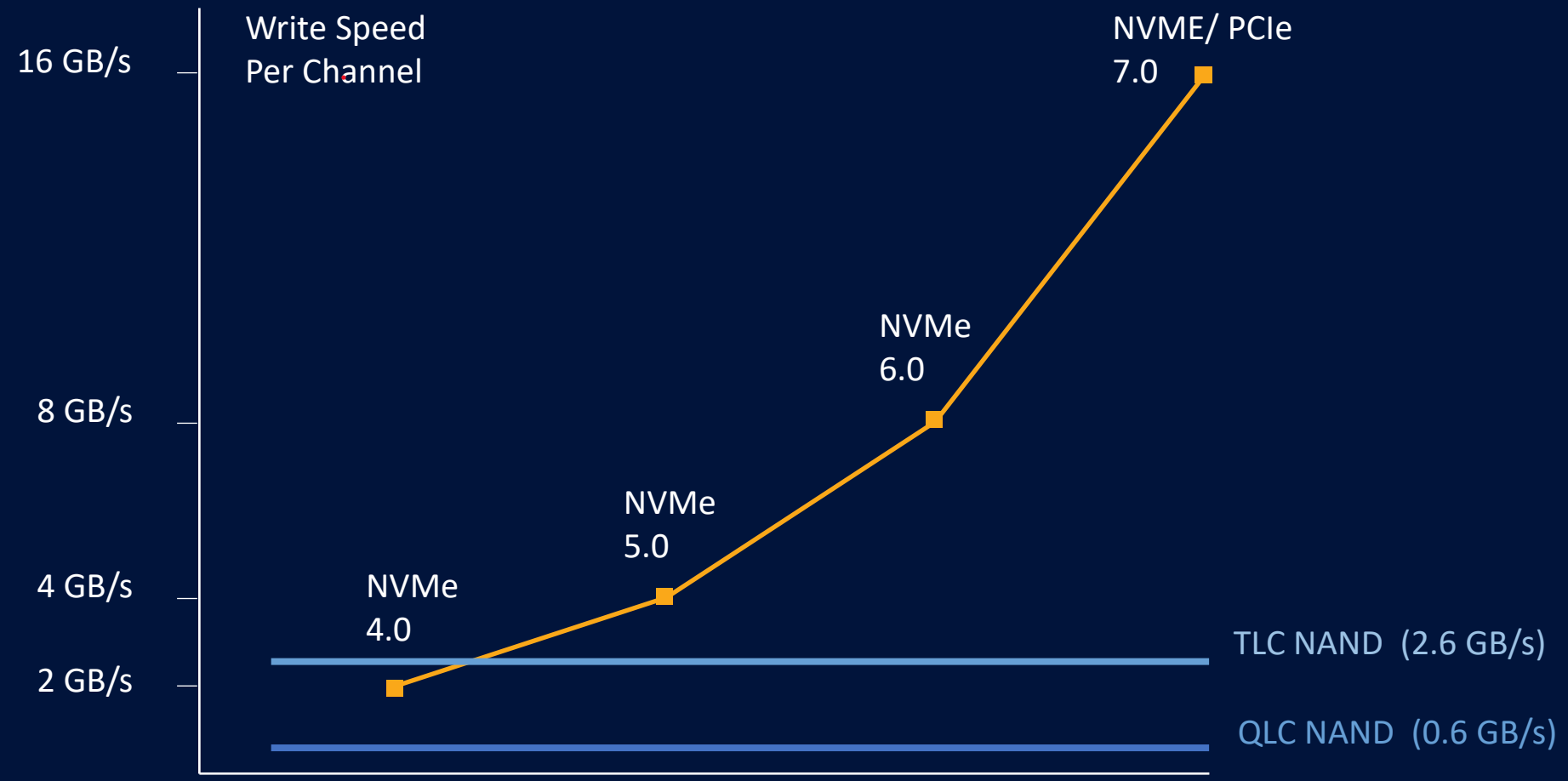
Each generation's write speed becomes 2X slower due to a doubling of Vt levels needing verification.

NAND Flash's Slow Speed Is A Bottleneck

NVMe M.2 PCIe		Per Channel	Write Throughput	
			TLC	QLC
4.0	8 GB/s	2 GB/s	160 MB/s X 16 chips	40 MB/s X 16 chips
5.0	16 GB/s	4 GB/s		
6.0	32 GB/s	8 GB/s	2.6 GB/s	0.6 GB/s

16 chip MCP

NAND Flash's Slow Speed Is A Bottleneck



* 16 chip MCP, 4 planes/chip

Next Gen Memory Architecture

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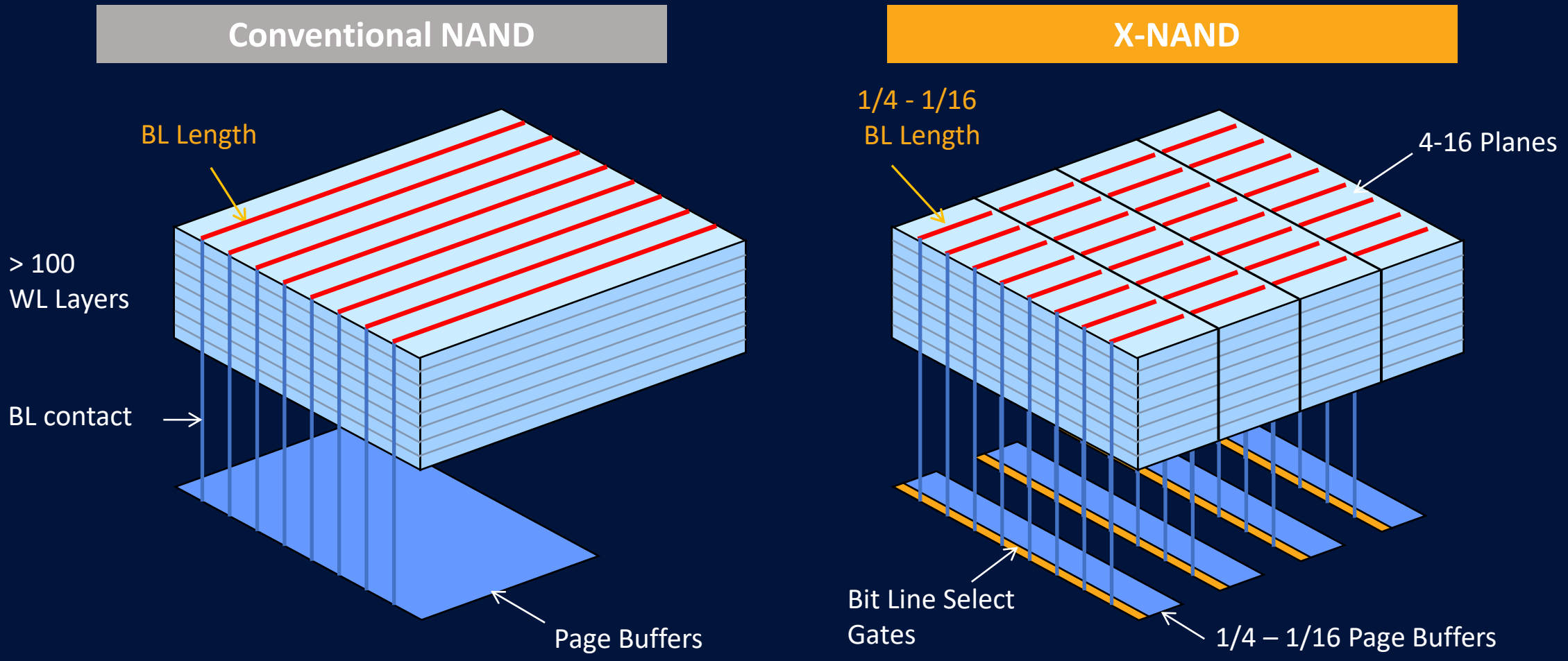
X-NAND™ QLC

0%	3X	16X	40X
Die Size Increase	Random R/W Speed	Gen1 Sequential Write Speed	Gen2 Sequential Write Speed

* Based on simulation

NAND vs. X-NAND



X-NAND architectural innovations to bit length, page buffer and circuit creates a performance advantage

Page Buffer Architecture / Bit Line Select Gate Operation

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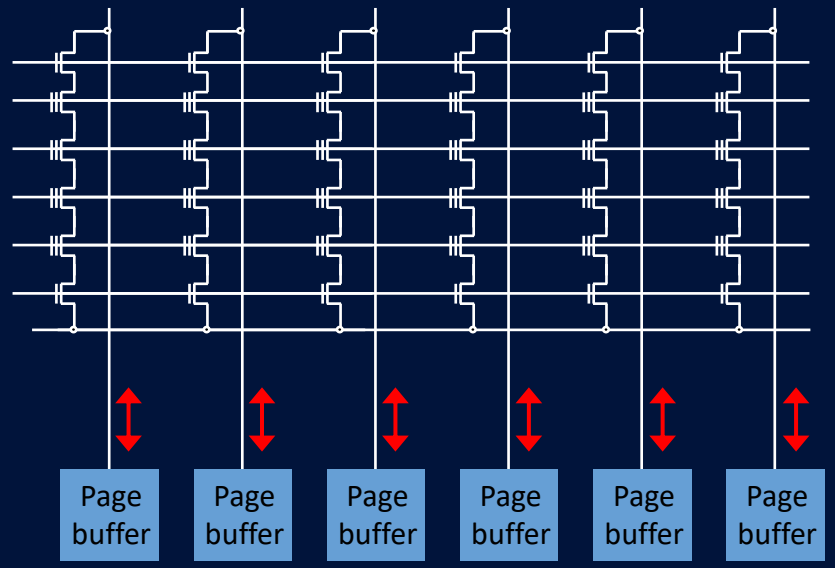
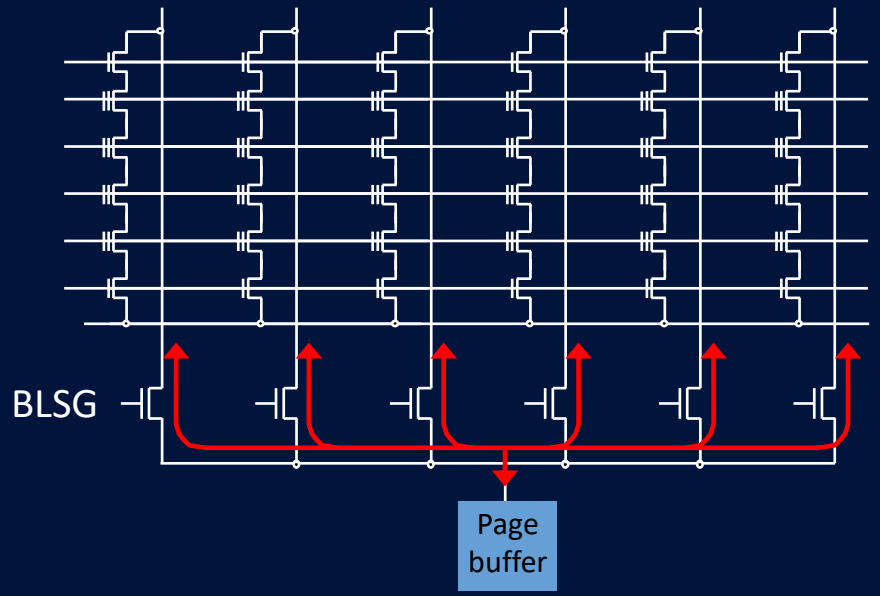
Conventional NAND



One page buffer to read and write data to one bit line (BL).

X-NAND



Shared page buffer to multiple bit lines and reduced layout size.

Bit Line Architecture/ Read Throughput Comparison

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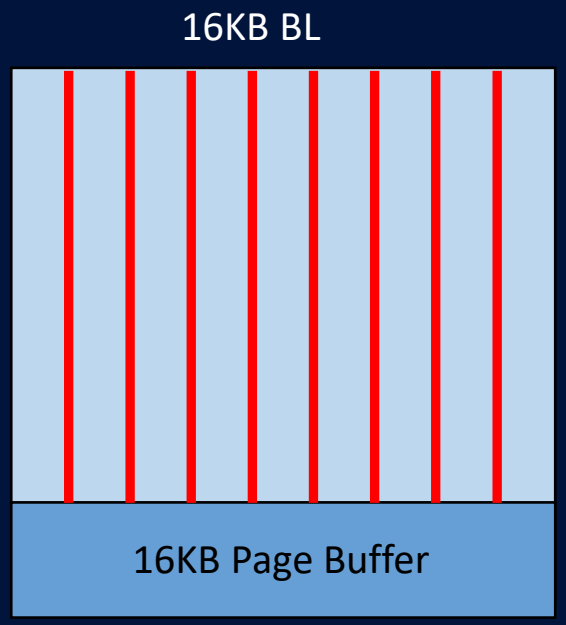
Conventional NAND

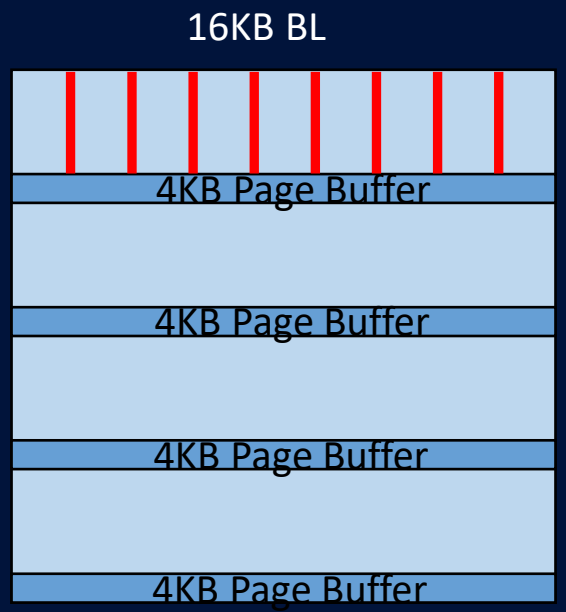


Full BL length

1 plane

X-NAND has 4X more planes plus ¼ shorter bit lines that increases read throughput by 16X.

X-NAND



1/4 BL length

4 planes

Shorter bit lines and more planes without increasing die size.

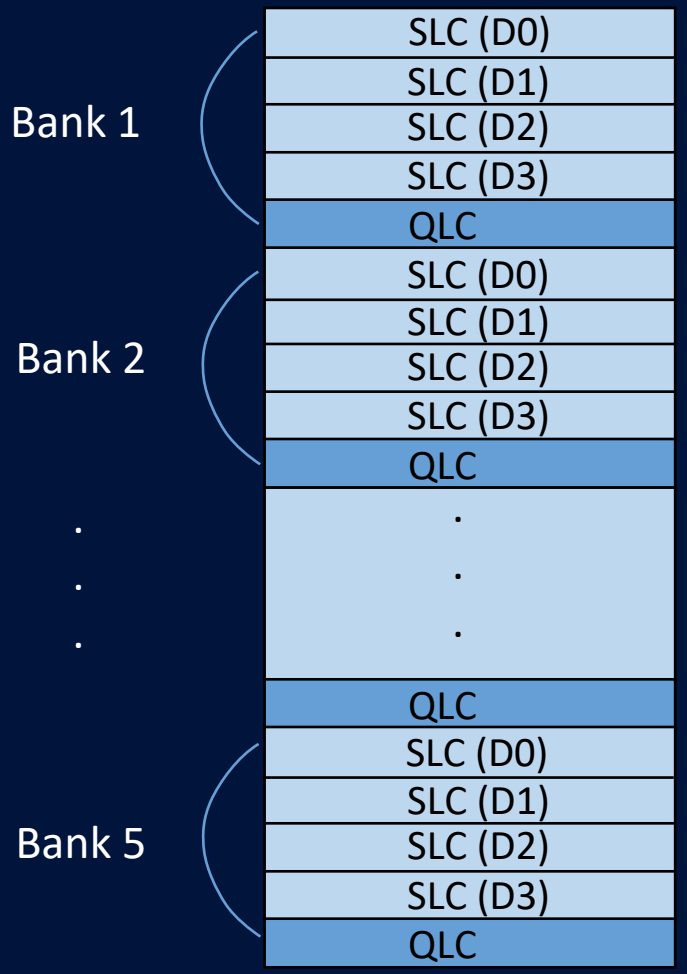
1/4
BL Delay

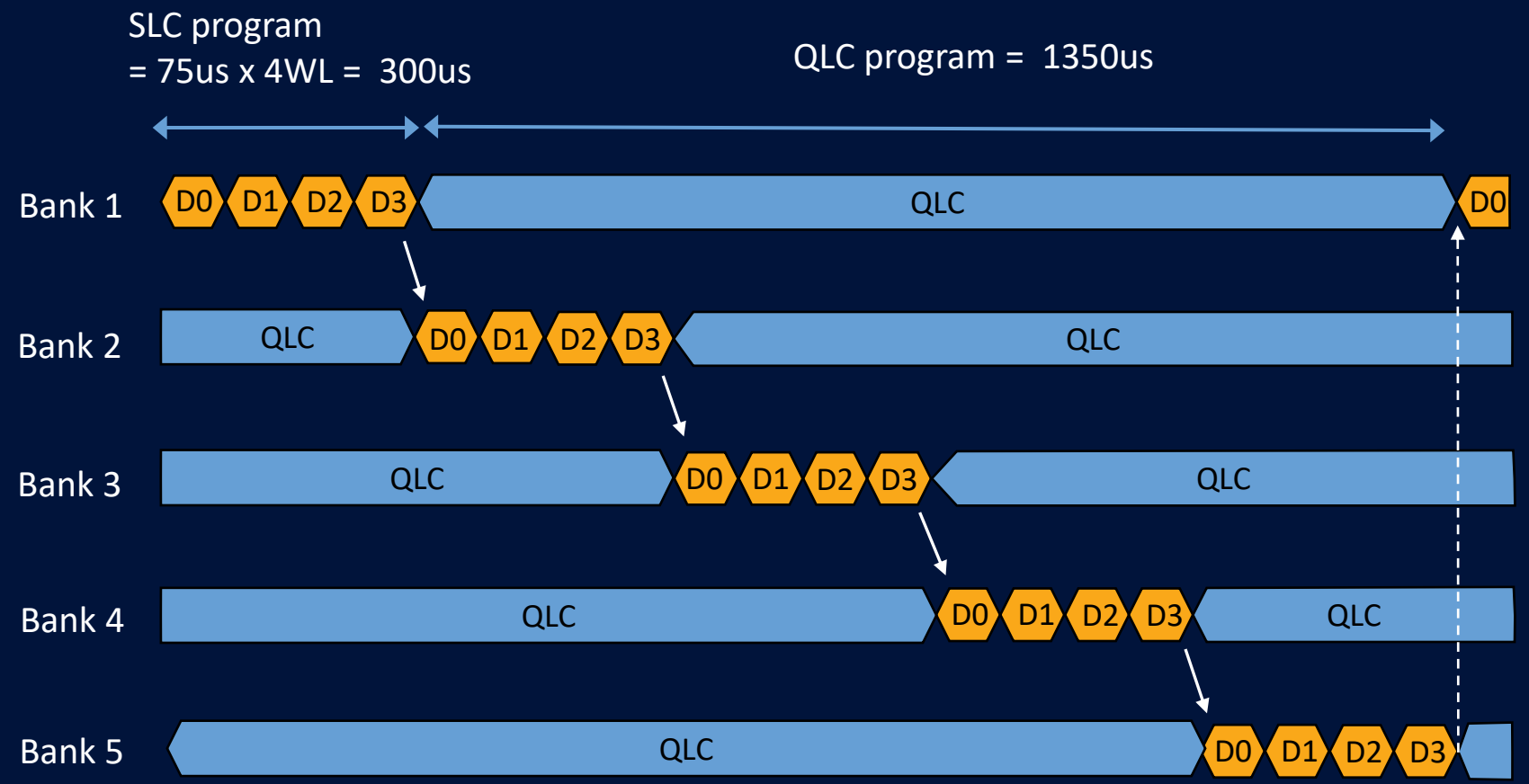
4X
Parallelism

16X
Read Throughput

X-NAND Gen 1: SLC/QLC Parallel-Programming

X-NAND Architecture





Data can be continuously programmed in SLC speed !

*Based on simulation

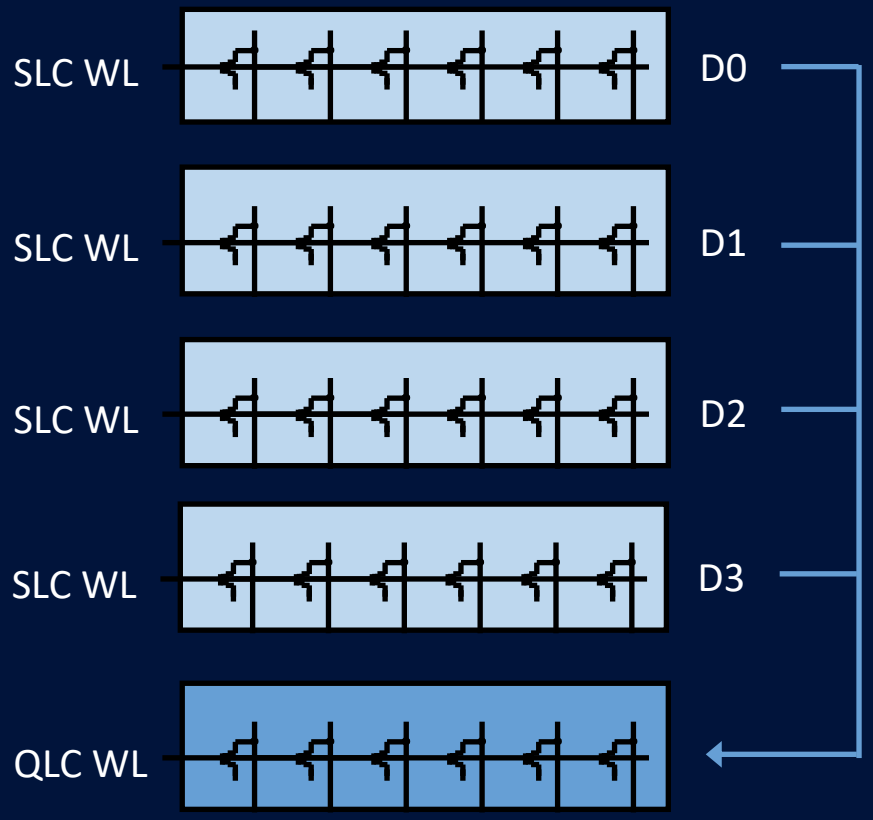
16X

Write Throughput

Evolution from X-NAND QLC Gen 1 to Gen 2

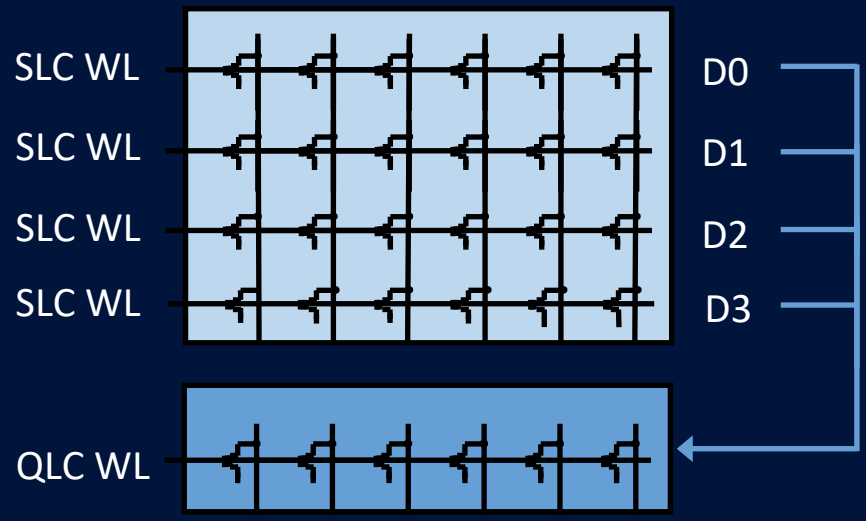
X-NAND Gen1

5 planes



X-NAND Gen2

2 planes



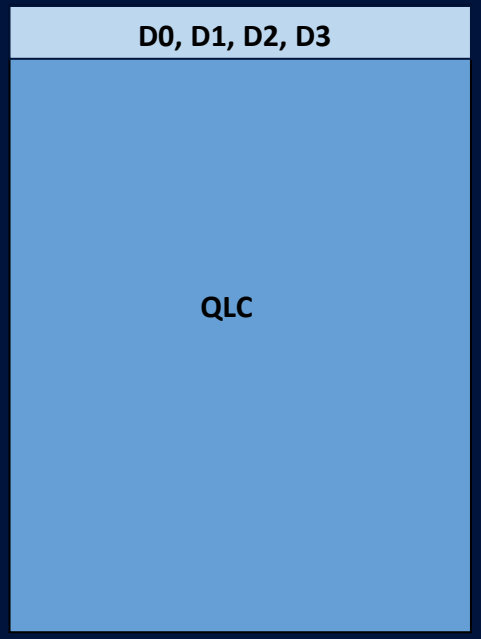
2.5X Program Throughput

QLC Program Throughput

X-NAND Performance

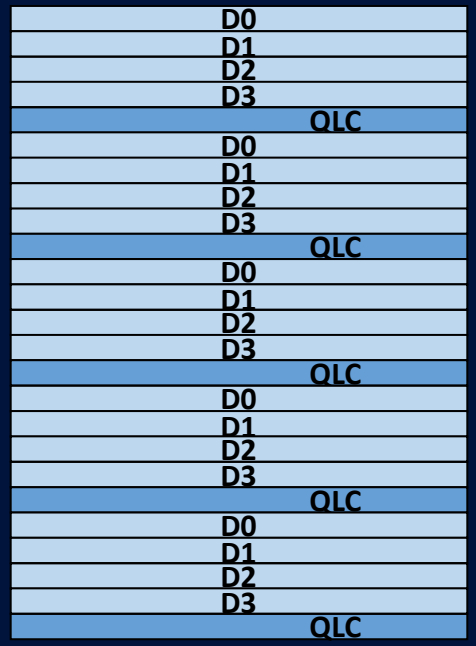
NAND

40 MB/s



X-NAND Gen1

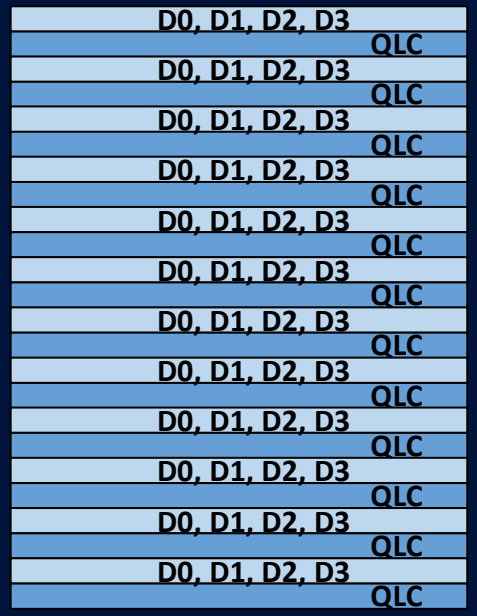
0.64 GB/s



16X

X-NAND Gen2

1.6 GB/s



40X

* Based on simulation

X-NAND QLC Estimated Write Speed

X-NAND Performance

NVMe M.2/ PCIe		Per Channel
4.0	8 GB/s	2 GB/s
5.0	16 GB/s	4 GB/s
6.0	32 GB/s	8 GB/s

Write Throughput

QLC (convent.)

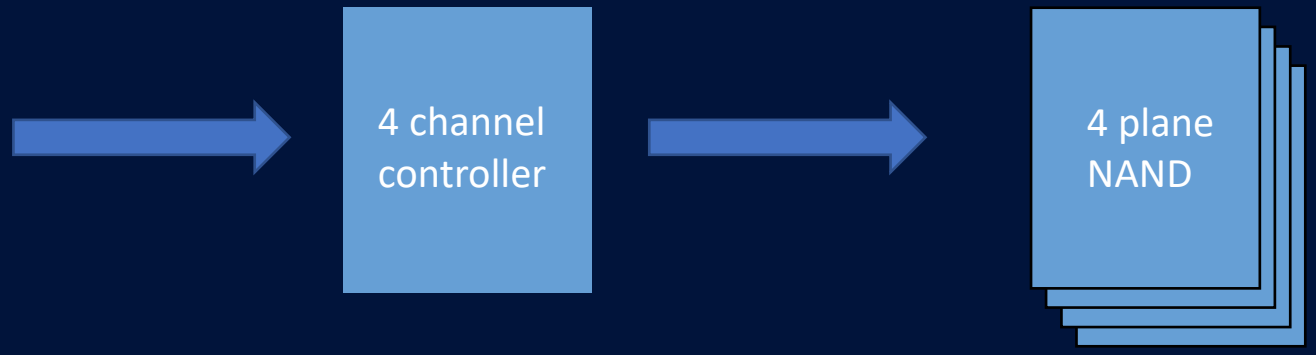
40 MB/s
X 16 chips

0.6 GB/s

QLC (X-NAND Gen2)

40x40 MB/s
X 16 chips

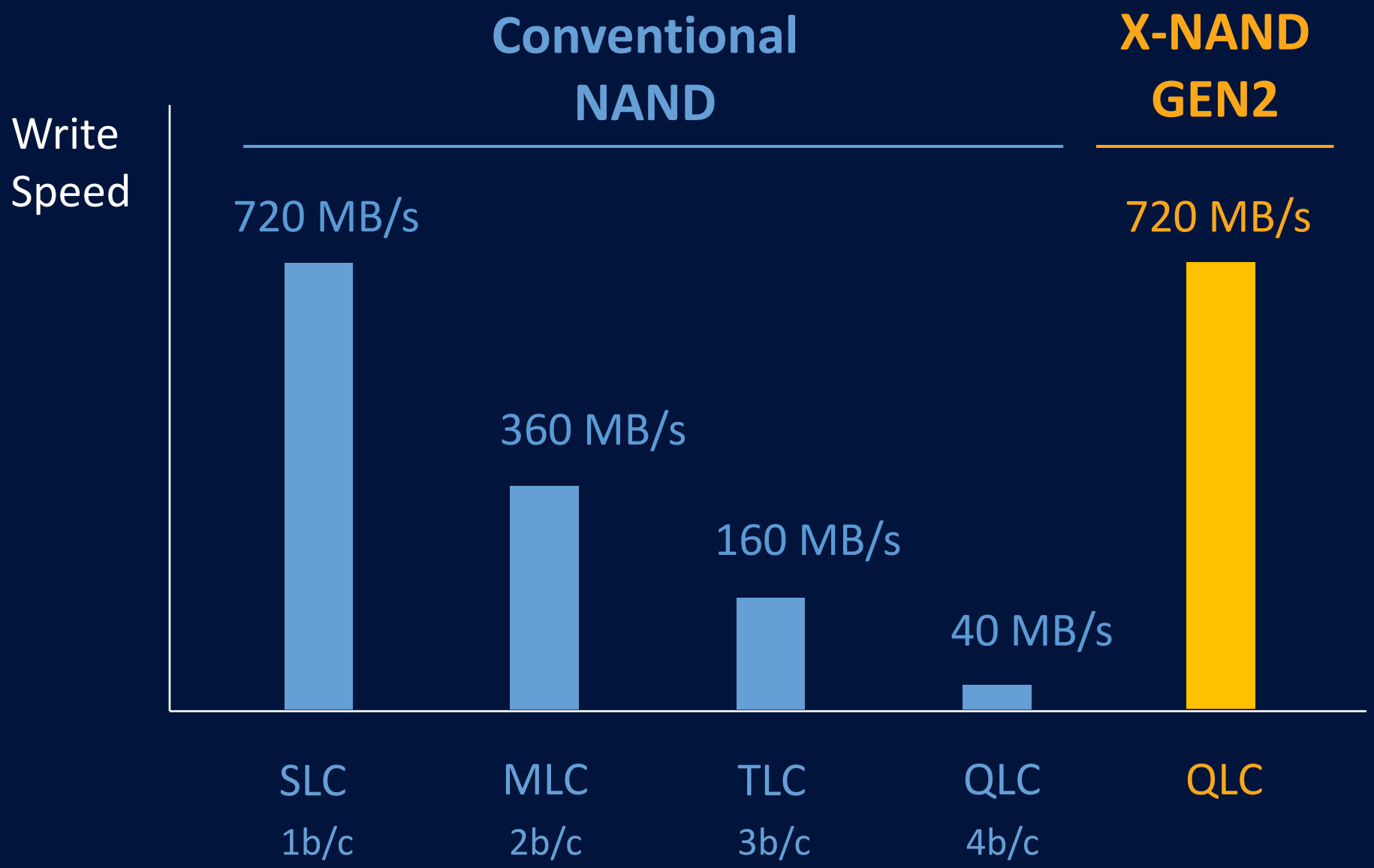
25 GB/s

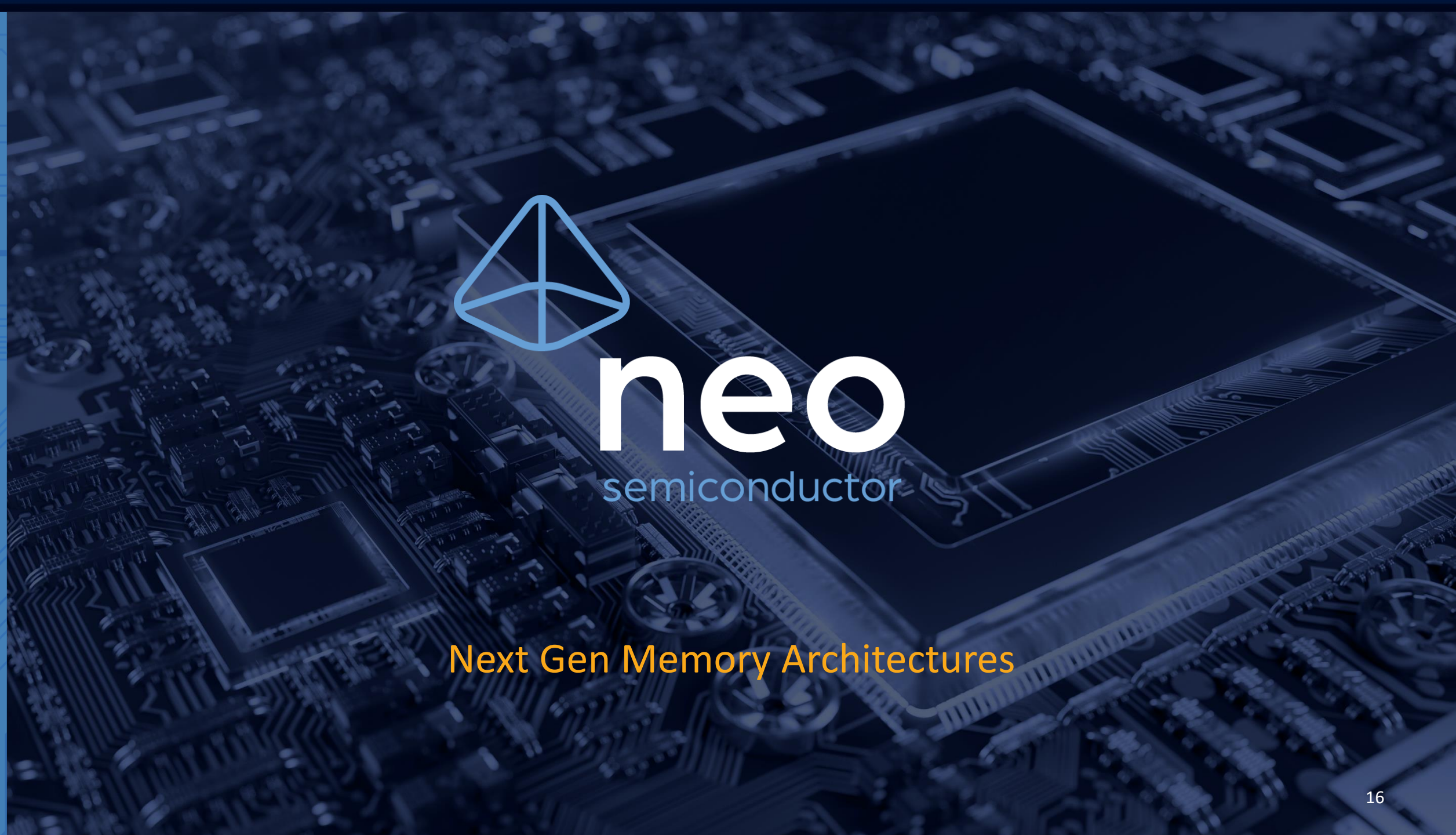


16 chip MCP

QLC Density with SLC Speed

X-NAND Performance





Next Gen Memory Architectures