Technical innovation in designing next generation PCIe Gen5 Client SSD

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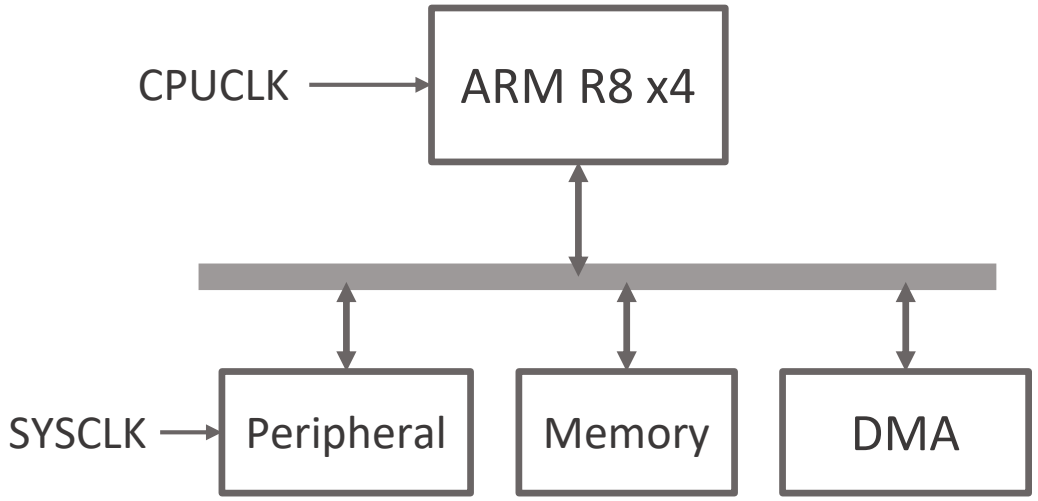
Agenda

- Performance optimized design
- Power optimized design
- Flexible peripheral design

SiliconMotion Perf. Emulation by Synopsys Zebu

Seq. Read (MB/s)	Seq. Write (MB/s)
15,009	14,450
Ran. Read (IOPS)	Ran. Write (IOPS)
2,500K	2,400K

Better SYSCLK/CPUCLK RATIO



- CPUCLK is 2x SYSCLK in SM2508 (1.25GHz vs 625MHz)
- Faster CPUCLK can execute instructions faster
- Lower SYSCLK can meet the performance target and keep lower power
- Only CPU cluster runs higher clock, overall power consumption can be reduced
- ARM R8 can run higher frequency than R5

Advantages of ARM R8

Feature	Cortex-R5	Cortex-R8
Instruction Set Architecture	Armv7-R	Armv7-R
Pipeline Depth	8 stage in-order	11 stage out-of-order, superscalar
Symmetric Multi-Processing (SMP)	Only AMP (Asymmetric multiprocessing)	SMP support, up to Qual-core
Dhrystone Benchmark MIPS/MHz	1.67 DMIPS/MHz	2.5 DMIPS/MHz
CoreMark®/ MHz*	3.47	4.62

1.5X

- Cortex R8 support SMP to automatically balance the loading from multi-cores, best for the mixed workload
- Out of Order execution allows processors to execute instructions by the availability of input data and execution unit, the processors can avoid being idle while waiting for the preceding instruction to be completed

3 CPU Core for 4CH design

* Based on B58R

# of CH	# of CPU	NAND I/F	Seq. R	Seq. W	Ran. R	Ran. W
8CH	4 CPU Cores	2,400MT/s	14,715	13,685	9,752	9,796
4CH	2 CPU Cores	2,400MT/s	7,117	7,275	4,544	5,668
4CH	2 CPU cores	3,200MT/s	9,474	9,544	4,704	5,908

- Sequential read and write speeds are proportional to the number of NAND channels and the NAND interface frequency
- Random read: When NAND=2400MT/s, the ratio of 4544MBs to 9752MB/s is 46%. NAND=3200MT/s, the ratio of 4704MB/s to 9752MB/s is 48%. However, random read speed is not proportional to the number of NAND channels even the NAND frequency is increasing
- In order to achieve 6GB/s (1.5M IOPS) random read in a 4CH controller, an additional CPU is needed. The CPU also offer better flexibility than a hardwired circuit

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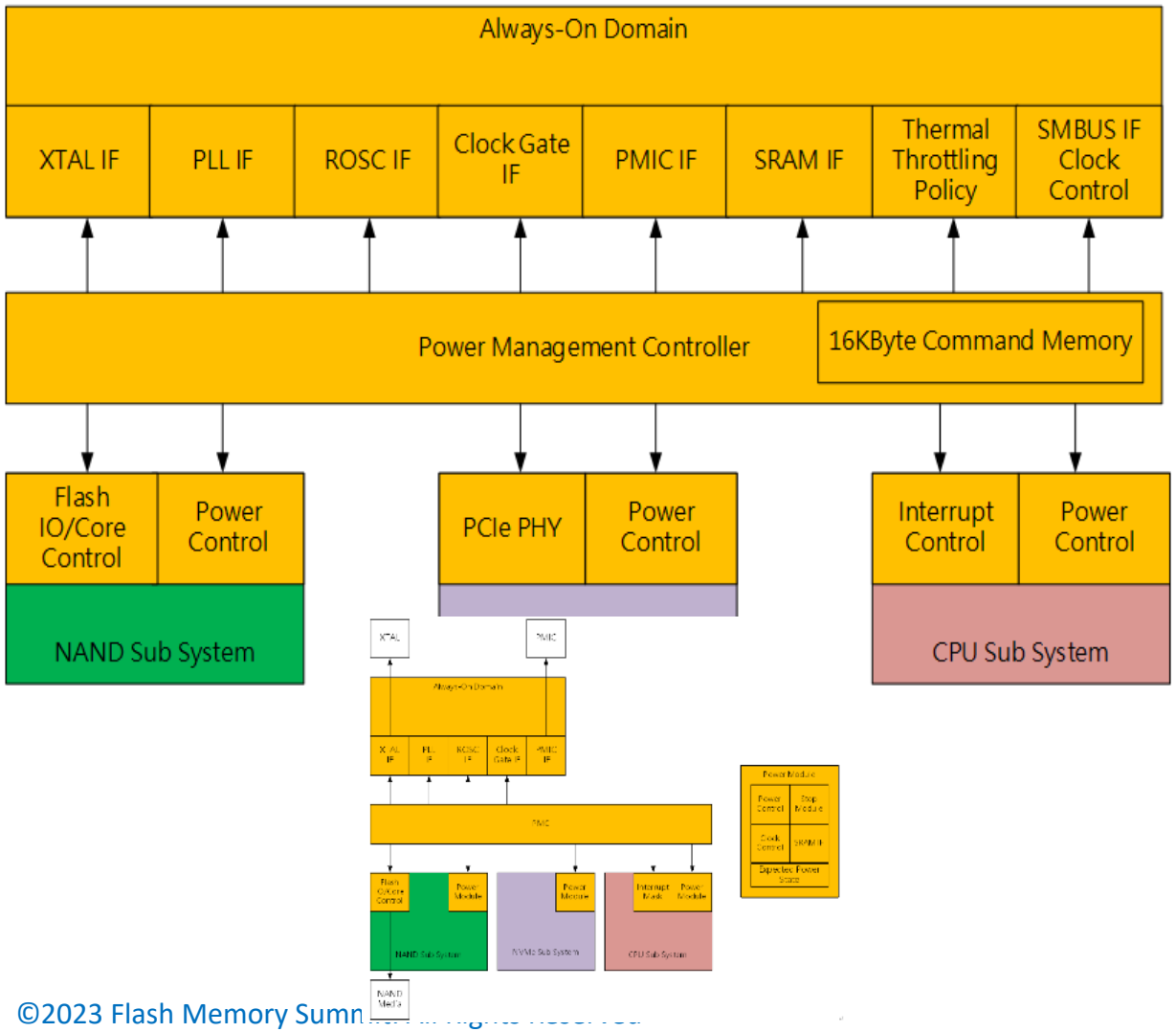
Power optimized design innovation



- New Power Controller and Power Domain Structure. A dedicated sequencer “Power Management Controller” for flexible power management.
- Programmable power policy through a simple instruction set including AND/OR/XOR/Access register/Event input/output control
- Multiple power domain (CPU, Frontend and NAND) and Multiple interface (PCIe, NAND, SMBUS, External/Internal Clock source) can be independently controlled
- Very Low Leakage: 45uW, Low Gate Counts: 13K gates including PMC and all control

The Advantages with PMC

No PMC	With PMC
CPU needs to keep alive until IDLE timer timeout due to CPU is the one to execute power policy	CPU can enter sleep first when there is no task. The power policy is executed by PMC
Different power domains need to be turned on-off by a specific order (Power domain 1 first and then power domain 2) due to power flow is controlled by CPU.	No limitation due to PMC is an always alive circuit. SMI can customize the power management policy
CPU needs to be woke up. It takes long latency to resume and re-entry low power. It was caused by generic flow (ROM code > Boot ISP > ISP)	No need to wake up CPU in PS4 for some cases (Host access Register via SMBUS/PCIe/NVMe)

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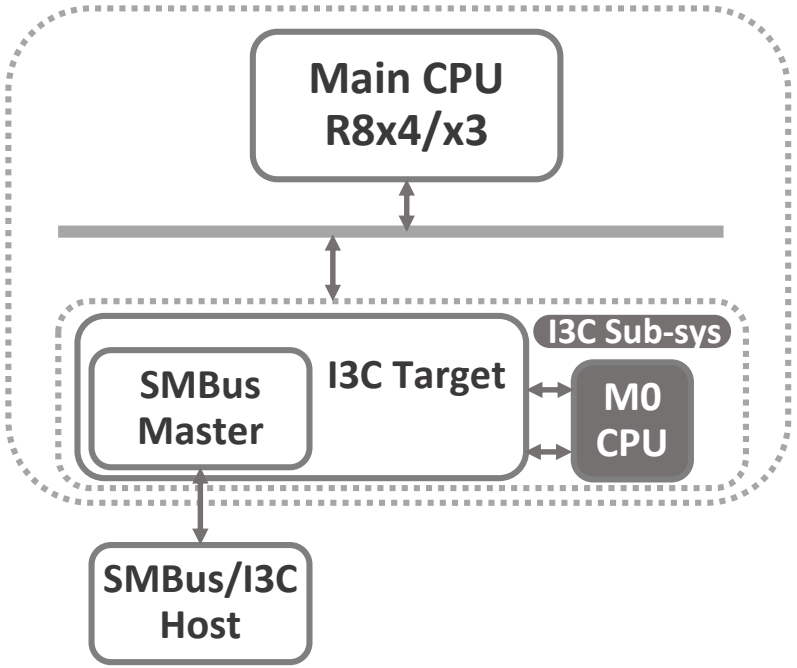
SiliconMotion Peripheral for more system usage



- SSD involve more in system usage like system management, recovery, Attestation, etc..
- Traditional ways is pure hardware circuit
- SMI gen.5 controller introduce a ARM M0 CPU to do dedicate control
- Flexible and upgradeable

Peripheral capability on Gen5

	SM2508/SM2504XT
SMBus Spec	3.1
NVMe MI Spec	1.2
I3C Spec	1.1.1
Operation freq.	≦12.5MHz
Low power resume time	M0 CPU resume time (<5us, depends on M0 power resume)
Address Resolution Protocol (ARP)	Support
Alert	Support
Vital Product Data	Support
NVMe Basic Management Command (NVMe MI Appendix A/C)	Support
MCTP SMBus/I3C	Support
SPDM SMBus/I3C	Support
NVMe MI SMBus/I3C	Support

SiliconMotion

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