Jedec LPDDRx Technology

August 2023

Agenda

- LPDDRx Technology Overview
- LPDDR5 Solution
- What’s next?!
  - LPDDR6
  - Automotive Opportunities

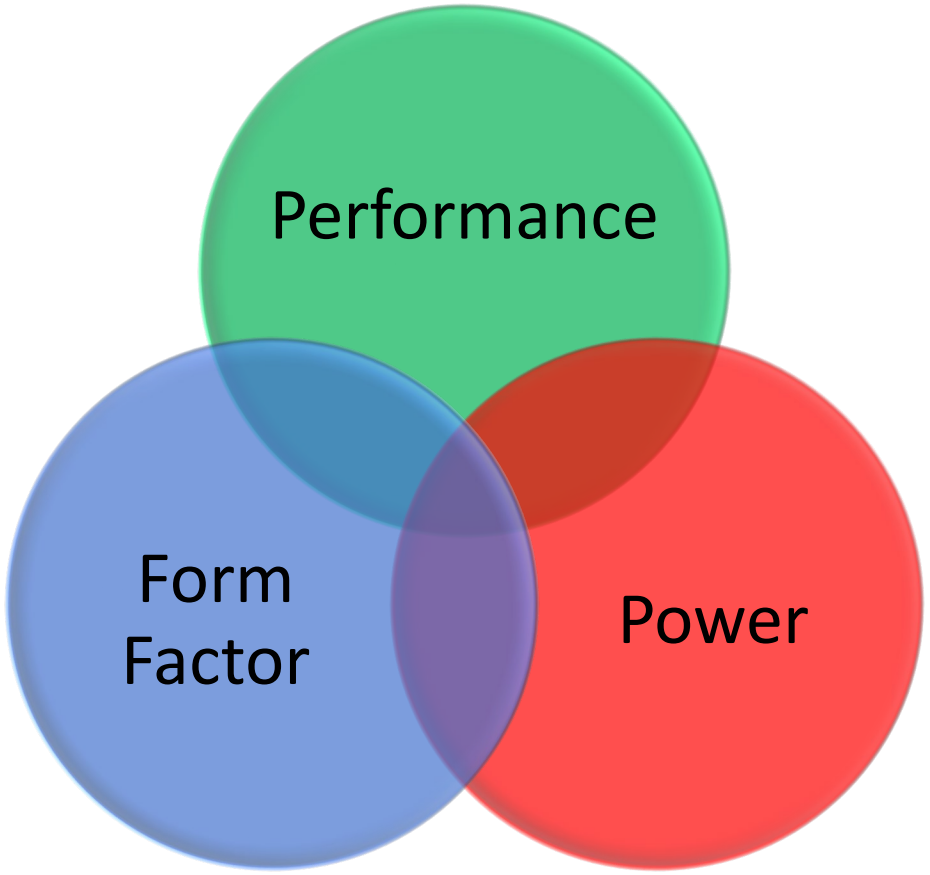
Flash Memory Summit

LPDDRx Technology Overview

LPDDRx Memory Trends & Direction

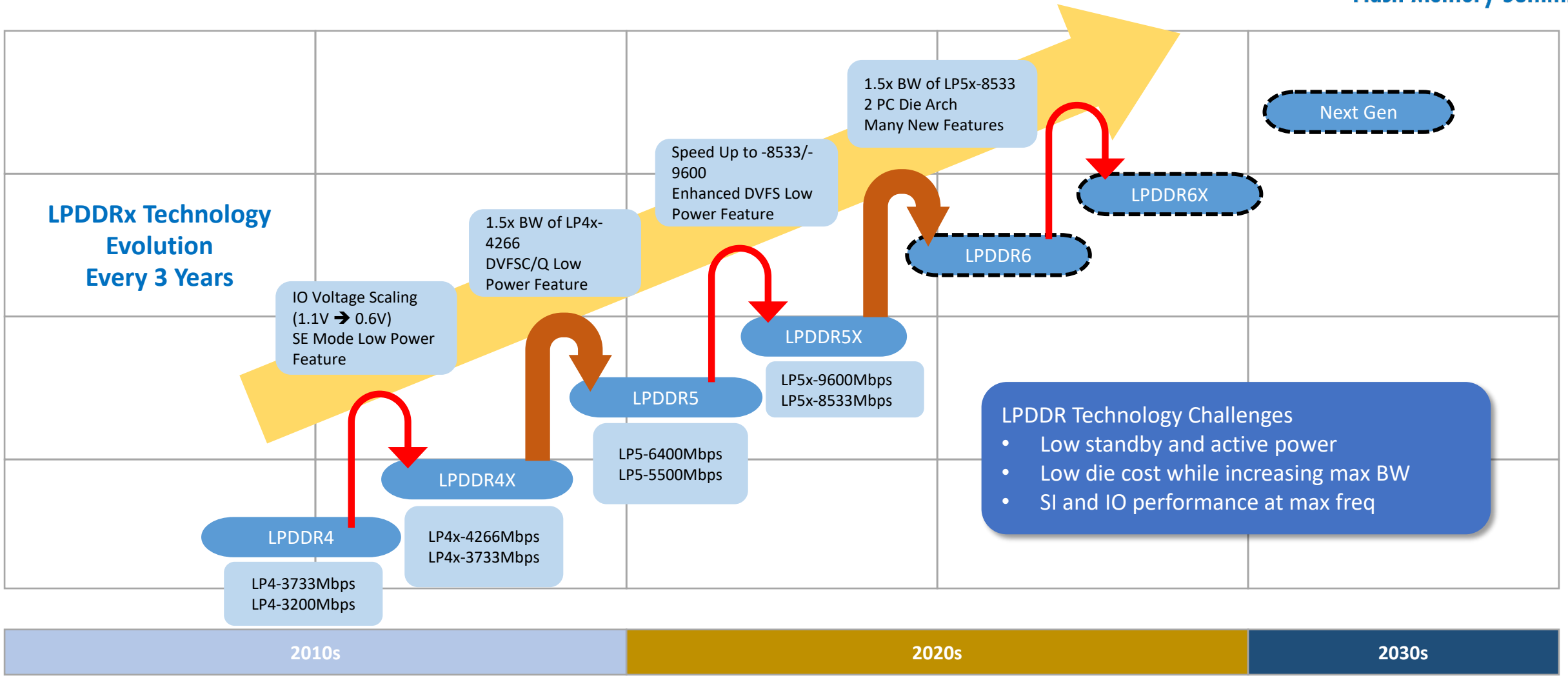
Flash Memory Summit

- LPDDRx memory trends have always been about Performance, Power efficiency, and smaller form factor
- Jedec continue to address growing opportunities – compute, IoT, XR, etc.
- Automotive market brings new challenges

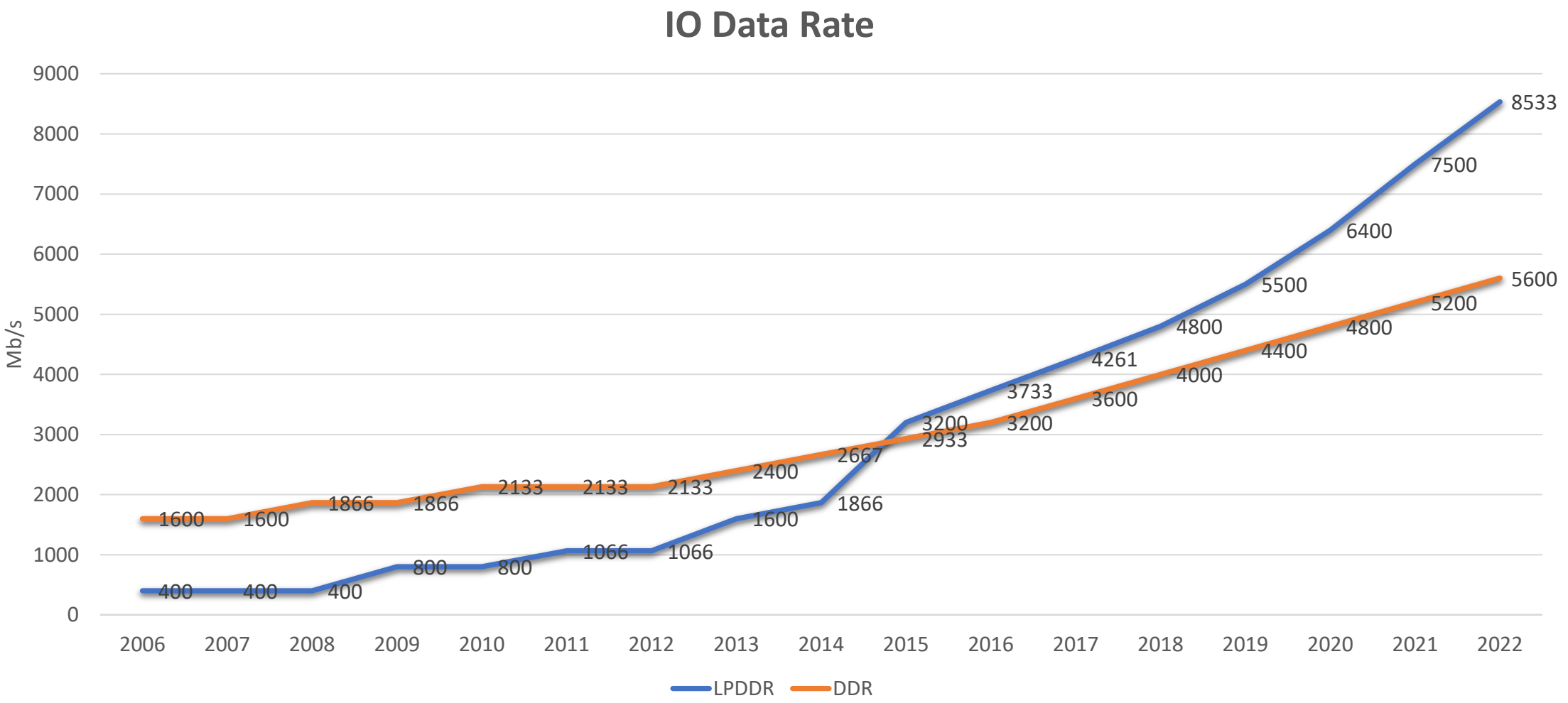


LPDDRx Technology Trends

Flash Memory Summit



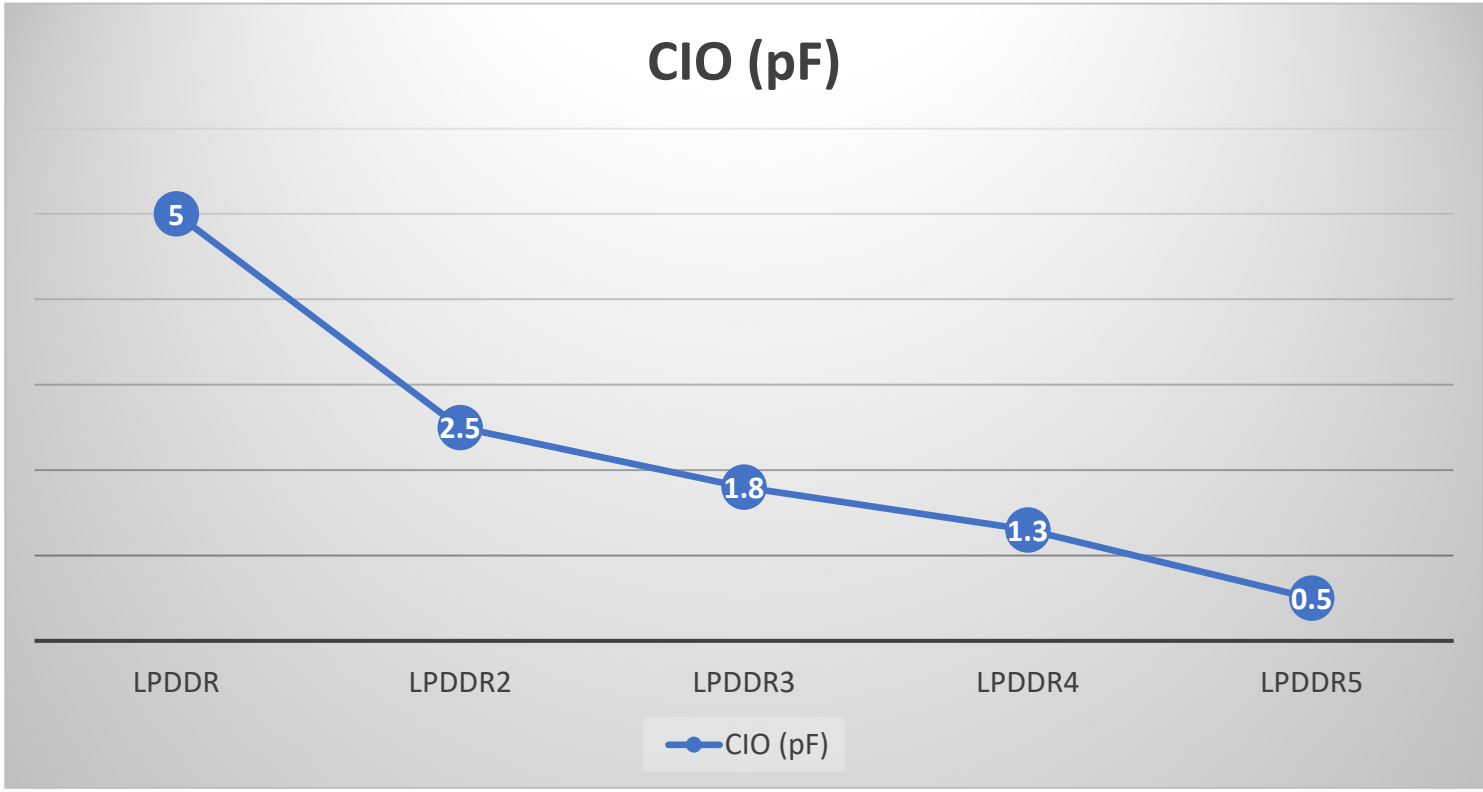
LPDDRx & DDRx IO Data Rate



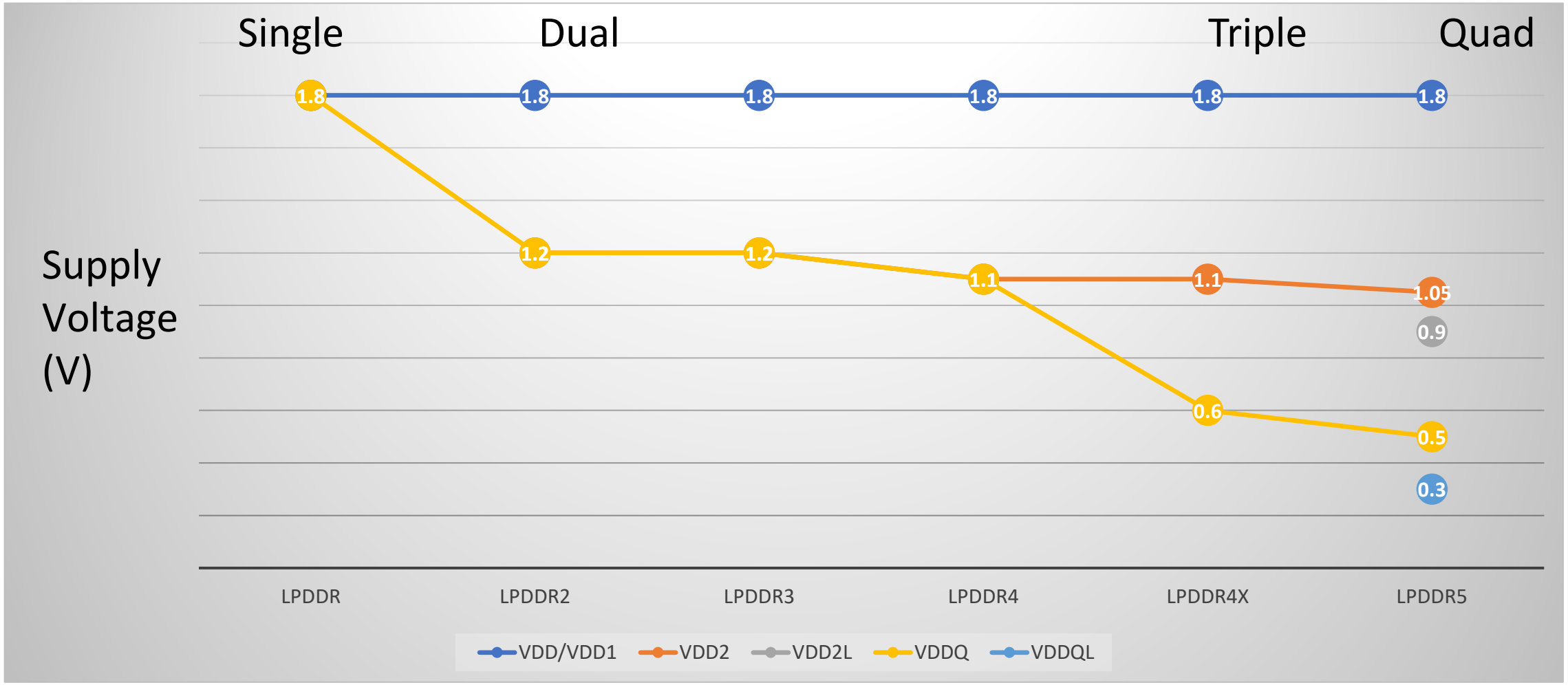
LPDDRx Channel Improvement

- CIO reduction
  - CIO is essential parameter for both eye opening and Channel power
  - Challenge is ESD & pin leakage
- Channel power considerations
  - Channel power consumption is reduced
    - Lower VDDQ
    - Channel load reduction
  - Large power consumption
    - Tx Pre-driver
      - Optimize Driver strength

1.03mW/byte
@6G, 0.3Vswing
100% toggle



LPDDRx - Supply Voltages

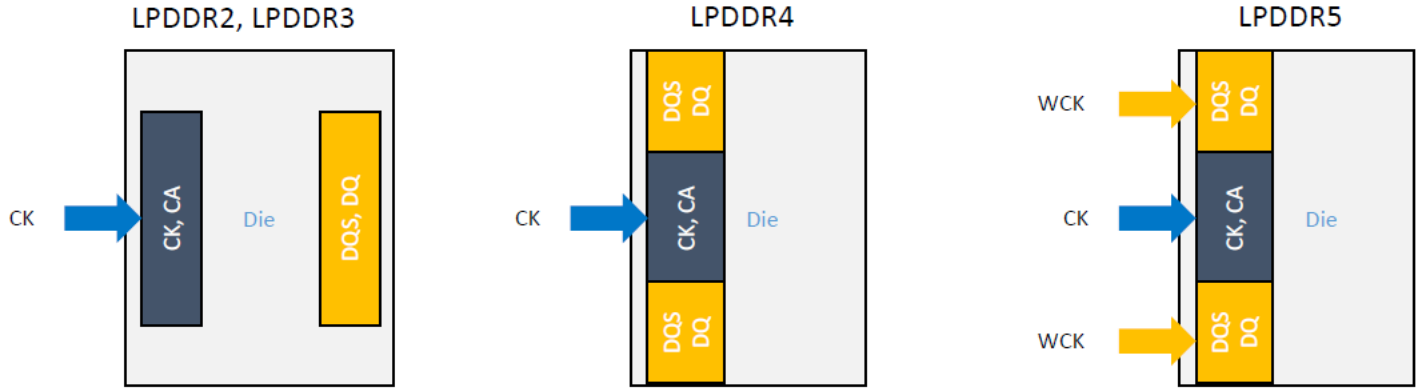


LPDDRx - Supply Voltages & DVFSC

- DRAM power reduction by using lower power supply for low frequency operation
- Two DVFS schemes defined
  1. DVFSQ - Interface voltage (VDDQ/VDDQL)
     - Low voltage can be applied during un-terminated operation.
       - DRAM and SOC can use same receiver mask spec. LPDDR5 use VDDQ=0.5V and VDDQL=0.3V.
       - This help to reduce mobile system DOU power.
       - Even during VDDQ transition LPDDR system can continue to work with limited frequency operation.
  2. DVFSC - DRAM peripheral (VDD2L)
     - VDD1=1.8V and VDD2H=1.05V is essential for DRAM memory cell operation.
     - Adding power rail for peripheral circuits power reduction, VDD2L=1.05V/0.9V
       - Higher voltage supply for high-speed operation
       - Lower voltage supply for low-speed operation
     - Extending lower voltage supply region step by step

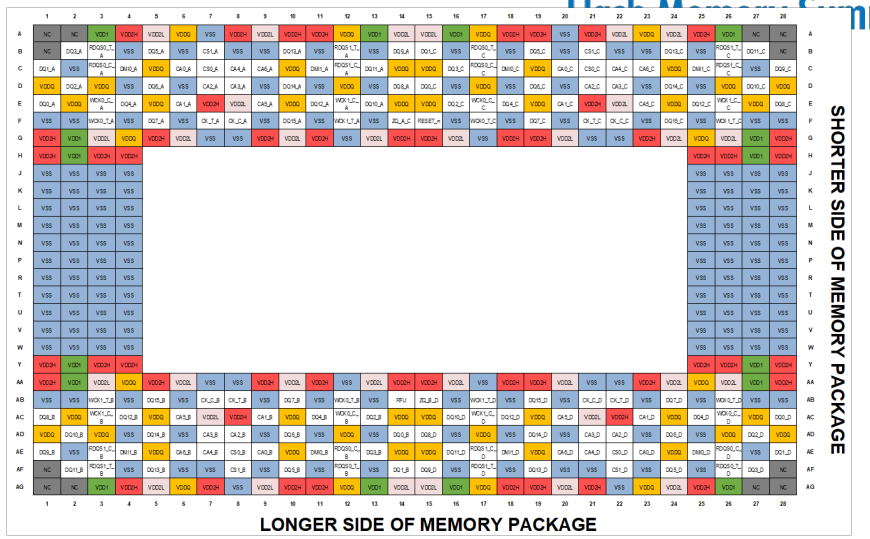
LPDDRx - Clocking Architecture Improvement

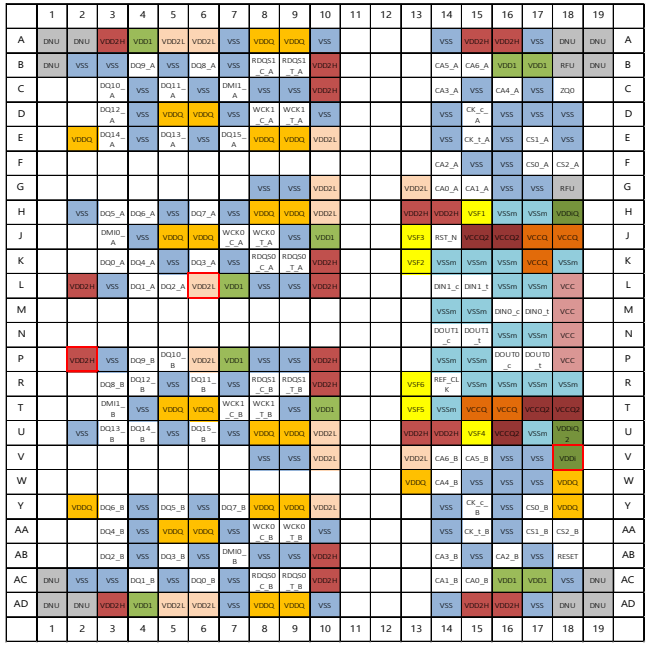
- LPDDR2/3/4 uses single clock
- To improve timing, LPDDR5 introduce forwarded clock, differential
- WCK operates at twice or quardruple the frequency of CMD/Address clock

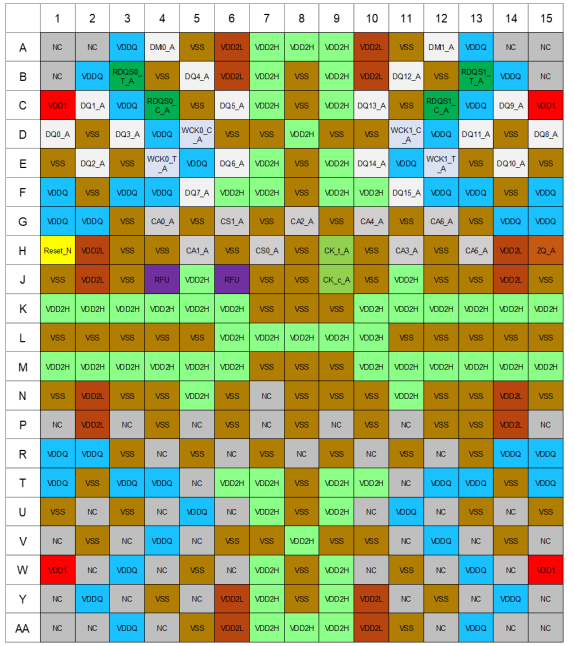


LPDDRx Packaging Configurations

- Packaging variation
  - POP
    - Suitable formfactor for wide system bus configuration with limited space
    - Can create small formfactor system like IOT
  - xMCP
    - Multi chip PKG with non-volatile memory (UFS, EMMC, etc)
    - One PKG provide total memory system
  - FBGA
    - Multi channel FBGA with multi rank capable





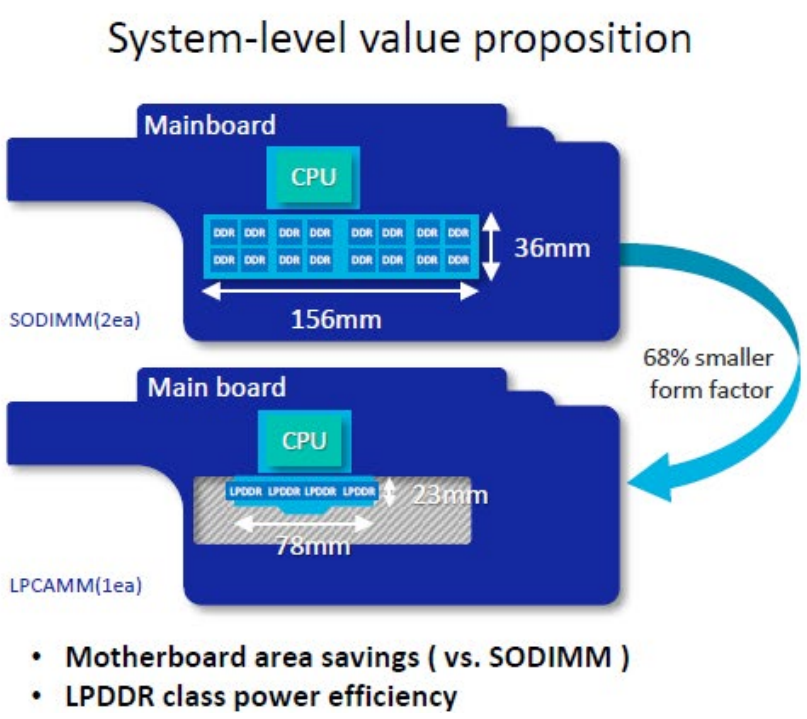


LPDDR5/5X Small Form Factor PKG Options

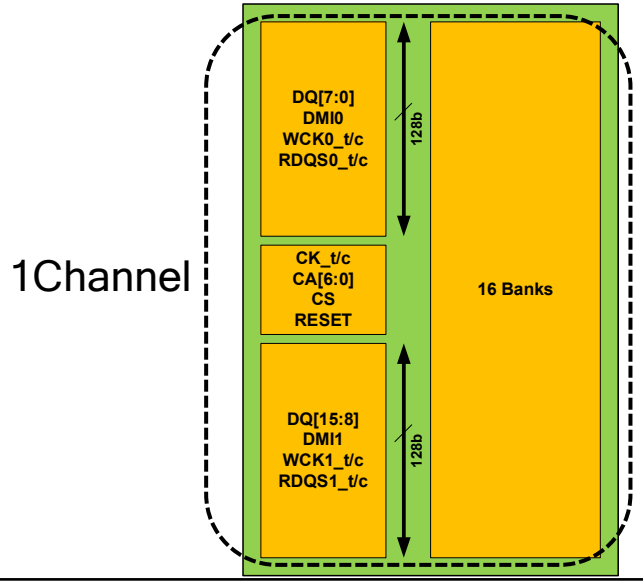
PKG Configuration	Ball Count	Ball Pitch (X x Y)	PKG Dimension	Comments
X64 (4Ch X16)	563b	0.35mm x 0.4mm	7mm x 12.4mm	
	561b	0.4mm x 0.4mm	8mm x 12.4mm	
	573b	0.29mm x 0.29mm	7.2mm x 12.4mm	
X128 (8Ch X16)	1013b	0.4mm x 0.4mm	14mm x 12.4mm	
	1159b	0.29mm x 0.29mm	14.1mm x 13mm	
1Ch ePoP	210b			#79.00. LP5/5X.
uMCP 11.5x13				#50.15A. LPDDR5/5X UFS4.x
2ch PoP	320b			#76.00. LPDDR4 /X
Small MCP				#73.06. LPDDR5/5X small MCP

Client new Form-Factor - LPCAMM

- [JEDEC Expands CAMM Standardization to include Two Key Memory Technologies | JEDEC]



LPDDR5/5x - Summary

	LPDDR5/5x
Die Diagram	
Max BW per Die	17GB/s (1Ch X16)
IO Speed	8533Mbps or higher (X16 NRZ)
Data Clock Freq	4266MHz or higher
CA Bus, Speed	CA[0:6], 2133MT/s (DDR)
Bank Architecture	1 Channel, 16Bank (4BG/4Banks)
Access Data Size, Page Size	32Byte per Ch, 2KByte
PDN	VDD1, VDD2H, VDD2L, VDDQ
Features	DVFSC, DVFSQ, SE Mode, RFM, Link ECC

LPDDRx, What's Next?!

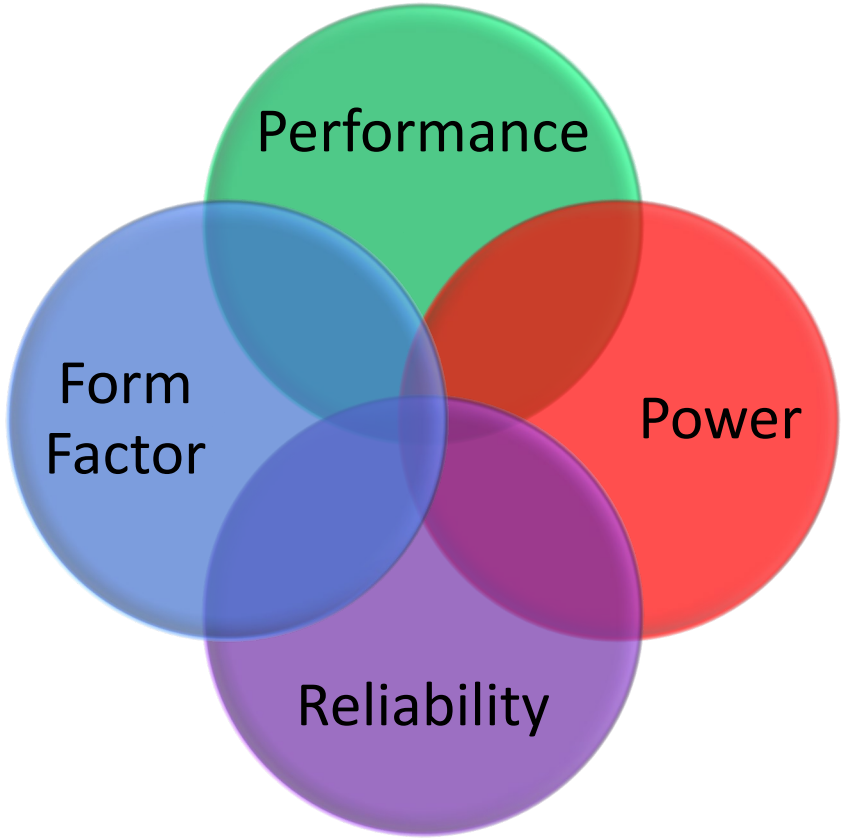
LPDDR6 – High Level Goals

- Doubling of LPDDR5x bandwidth
- Improved low-power schemes
- Improved idd4 reduction
- One standard to comprehend all speeds and features
- Improvement of low-rank performance (e.g. more banks, better core params)
- Improved clocking architecture
- Evolutionary packaging technologies
- Improved Data Integrity
  - RFM solutions
  - On-die ECC, Link ECC, Link CRC

Automotive Memory Challenges

Flash Memory Summit

- LPDDRx performance & power efficiency are attractive, even for automotive market
  - LPDDR4x performance
  - Low latency
- But there are challenges for LPDDRx in the automotive market
  1. Improving Boot time
     - *Current boot memory* - xSPI-NOR
     - XiP architecture
  2. Data Reliability
     - High temp (>125°C)
     - Improve RFM solutions
     - On-die ECC, Link ECC, Link CRC



JEDEC LPDDR-NVM

- **Automotive ecosystems use-cases have a problem!**
  - Legacy NVM (xSPI-NOR) will not meet the READ performance requirements
  - Automotive SoC & constraints when using advanced process nodes
    - No e-flash → *e-flash is not available below ~20nm*
    - High temp (>125°C)→ *DRAM is problematic*
    - e-RAM is expensive at smaller geometries *(area sometimes increases on a more expensive wafer)*
    - Multi-core is now the norm
- **Opportunity –**New TG to address executable memory (NOR) on LPDDRx bus
  - Improve boot time for automotive application; xSPI → LPDDR4 READ performance gap *(lower latency, pipelined accesses)*
  - LPDDR4 interface flexibility *(single/dual channel, x8/x16, differential/single-ended)*
  - Adoption of standardized (LPDDR) bus transactions; simplified
  - Use of a low-latency, high-throughput NVM process technology *(e-flash, MRAM, …)*
  - XiP architecture support. One interface for both LPDDR & XiP memory
- **LPDDR-NVM TG was created in Q4/2022. Participation are welcome**

Thank You