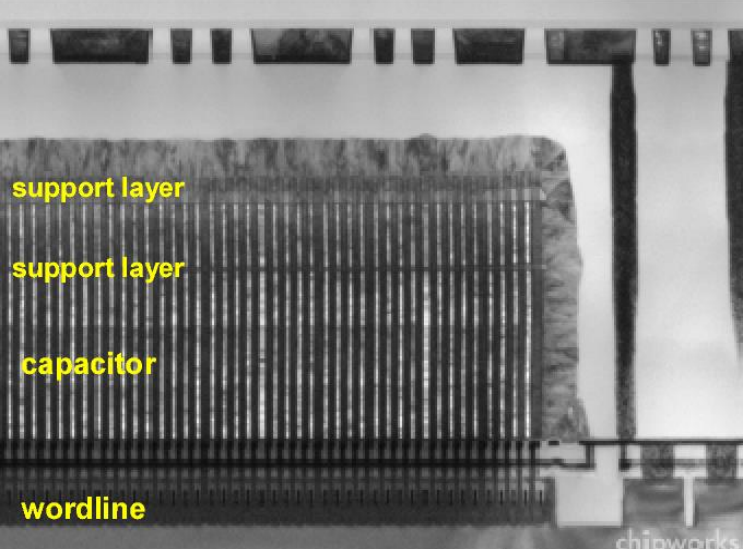
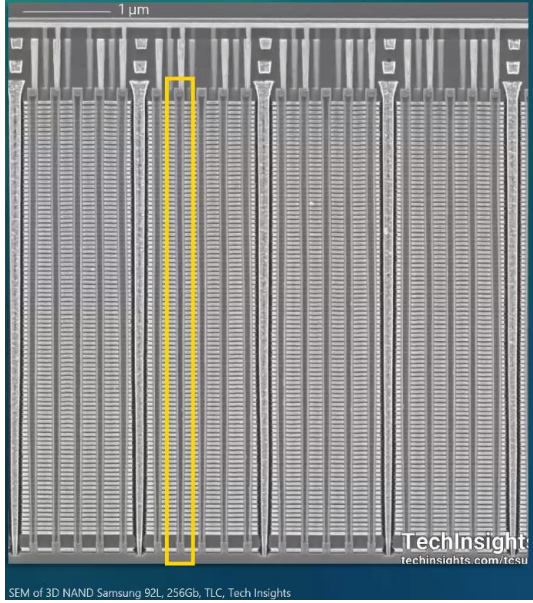


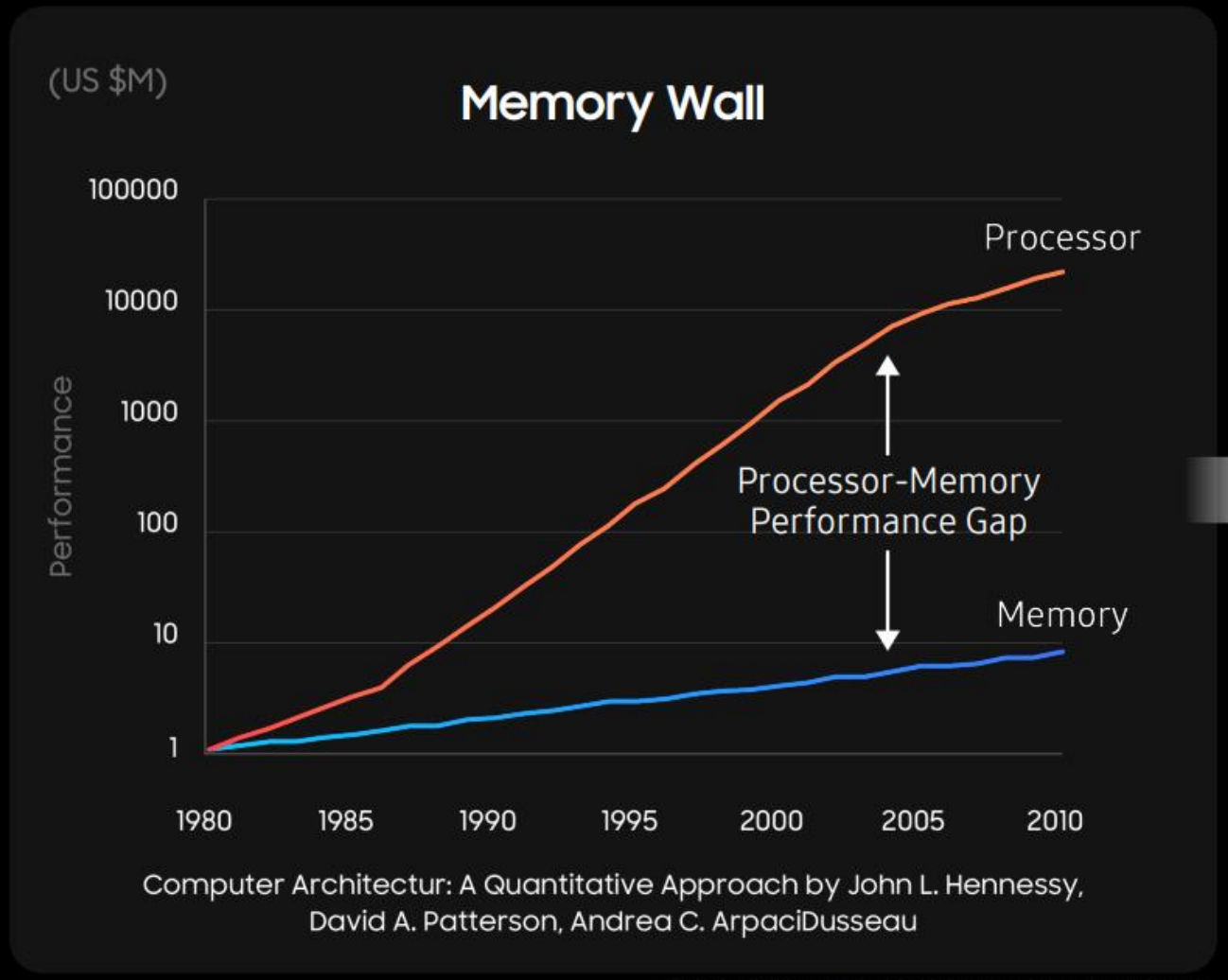


Future of DRAM…..A Perspective

Aug. 9, 2023 FMS Jian Chen

Memory Wall

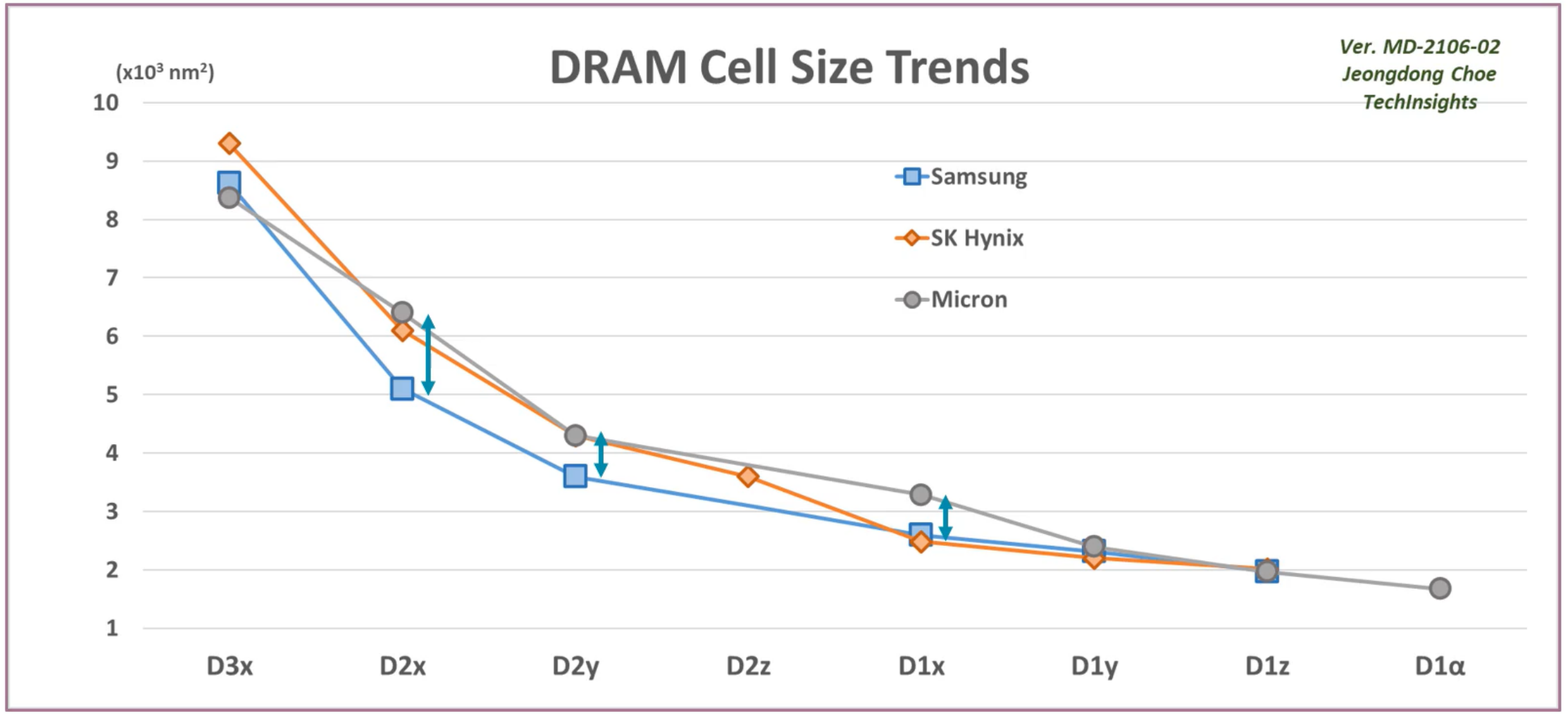
Challenge in memory to keep up with CPU performance



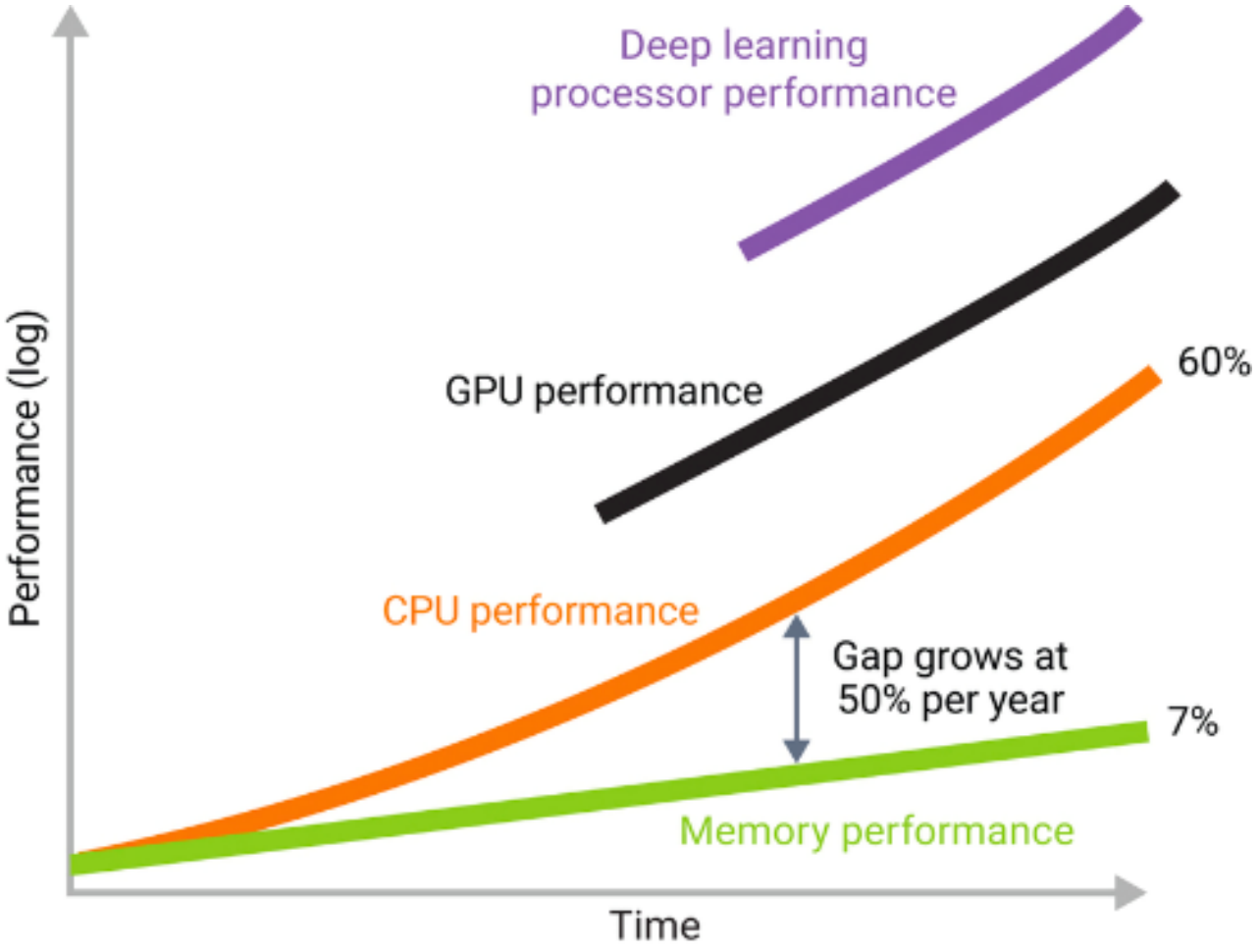
Source: https://bitbashing.io/memory-performance.html

Cost

The Elephant in the room: DRAM Not Scaling



OK, We Know the Motivation, But Solutions?

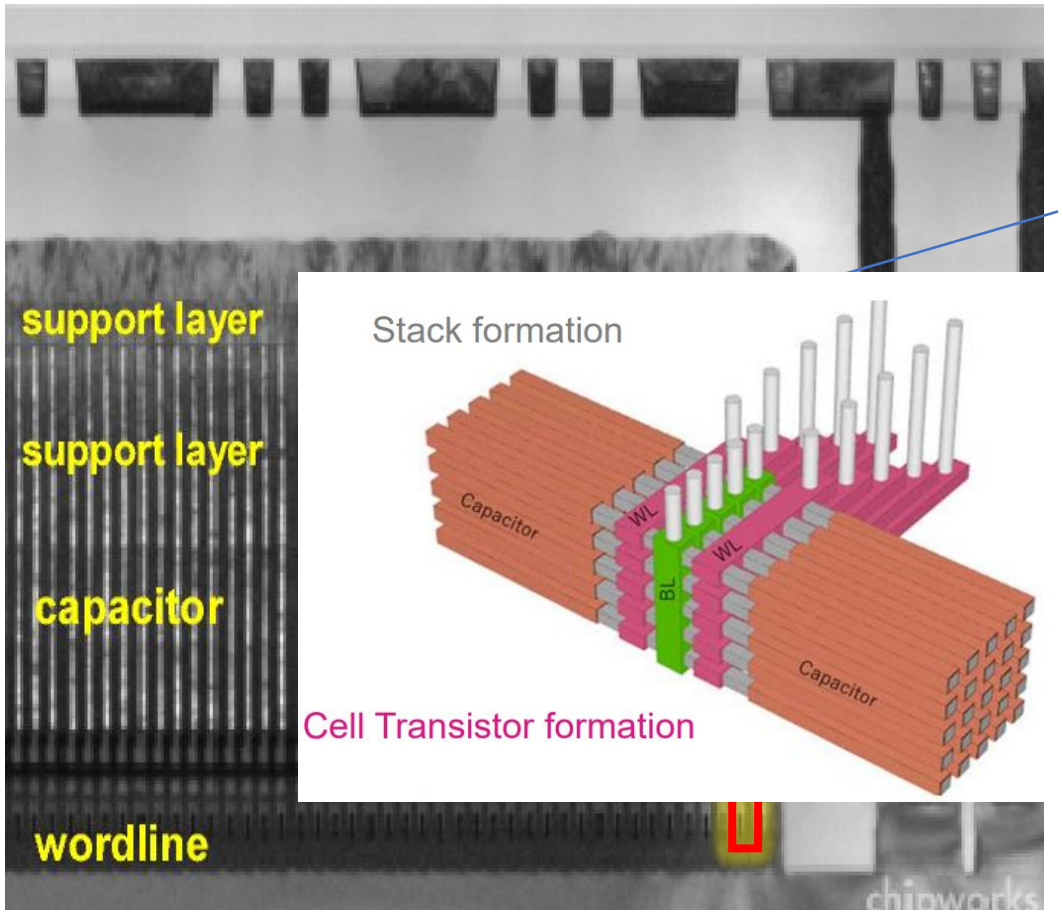


- Continue 2D scaling...$4F^2$(?)
  - +HBM…
- CIM (??)
- Emerging Memory (???)
- System: CXL (?)

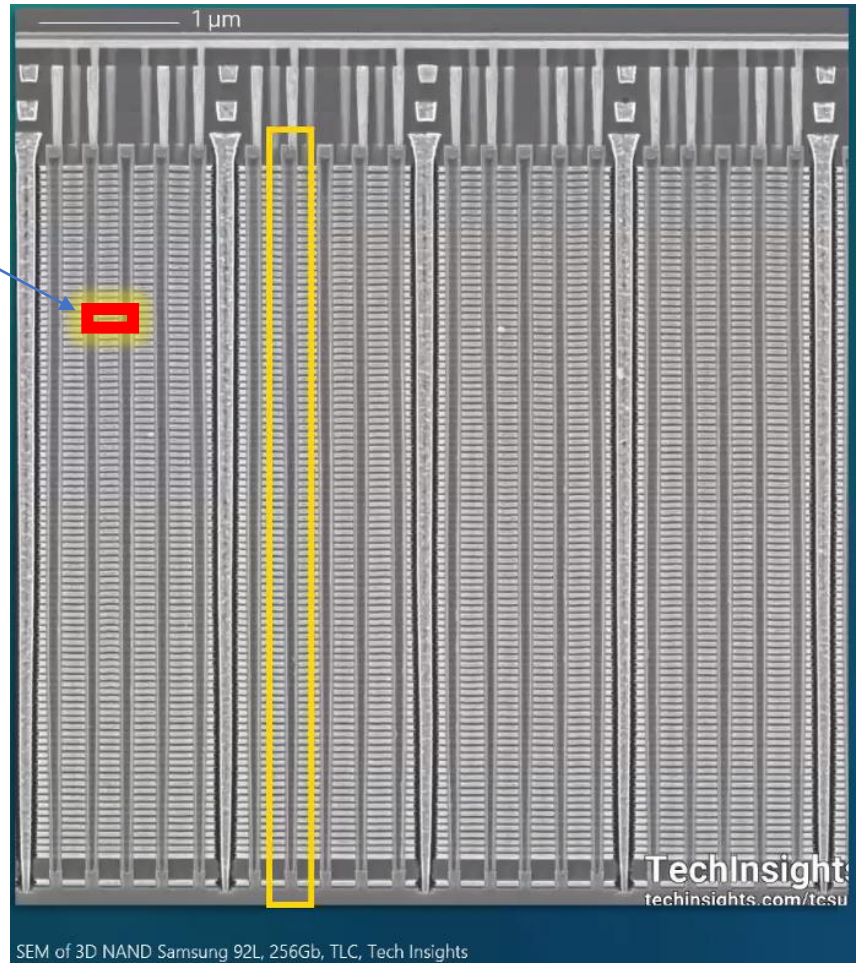
- **3D DRAM (?)**

How to Have More Bits Per Unit Area?
And to Meet Perf./Cost/Bandwidth/Power Needs?

Similar height



1 bit / 3bits

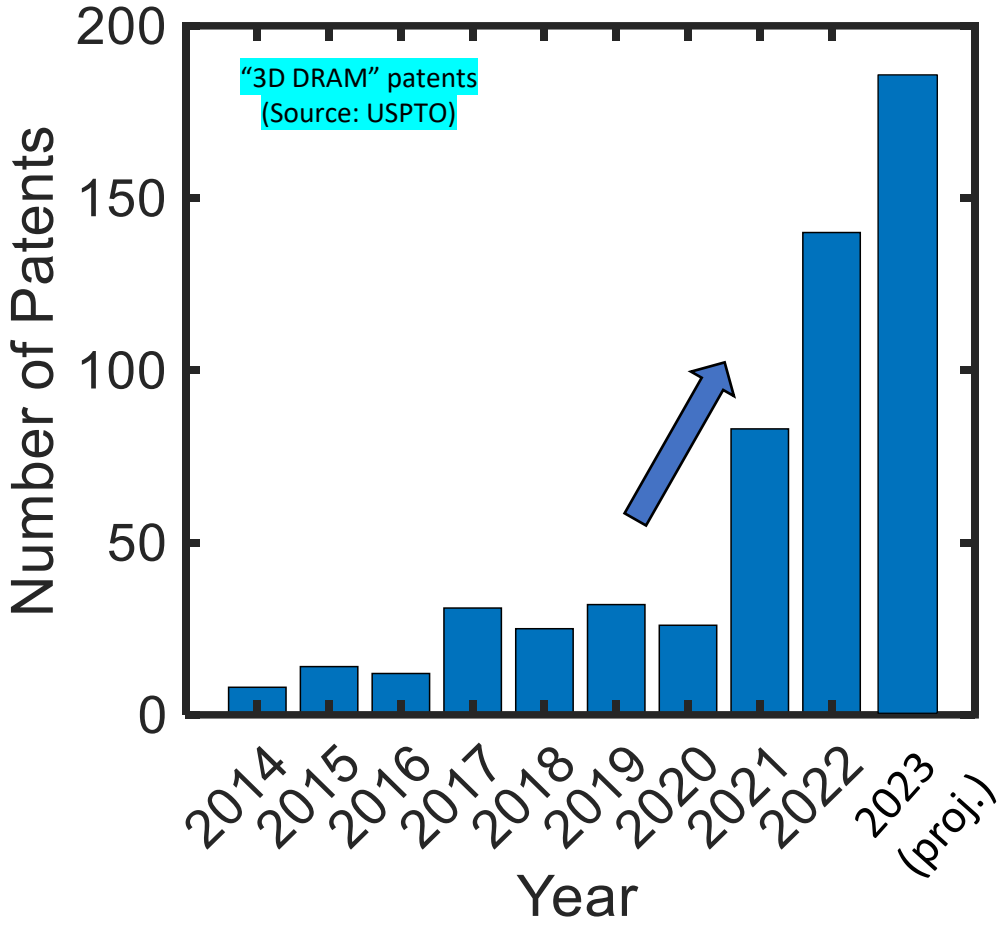


Similar height

Advanced DRAM and NAND are of similar heights (w/ same dry etch tools).
Photos here are not the most up to date nodes.

Looks Who's Not Talking…

- Near zero technical publications.
- The major players are not talking, but busy filing tons of patents the past few years.



Only two 1T1C 3D DRAM papers published in technical conf. by DRAM vendors.

- 2023 IMW Conf. "A 3D Stackable 1T1C DRAM: Architecture, Process…" by CXMT
- 2023 VLSI Symp. " Ongoing Evolution of DRAM Scaling via 3rd Dimension: V-DAM" by Samsung

Also, capacitorless DRAM approaches: 2T0C Gain cell(mostly academic), and Gate-controlled-thyristor DRAM (Macronix)

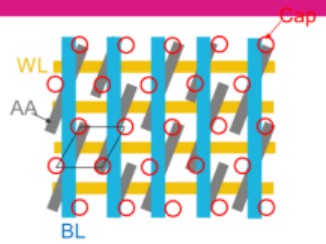
What Some Tool Vendors Are Saying

Source: TEL estimates

Year of HVM (20k/month)	2020	2021	2022	2023	2024	2025	2026	2027~28	2029~30
F* [nm]	16	15~14		13~12		12~11		≦10	<10

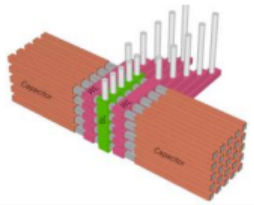
Cell / Peri. layout

6F²



*Feature size: STI hp along WL = STI hp / COS(21°)

3D



Patterning

193i SAQP, DP (+ EUV)

Pillar cap. A.R. >40 >45 >50 >55 >60

Capacitor

ZAZ CIP

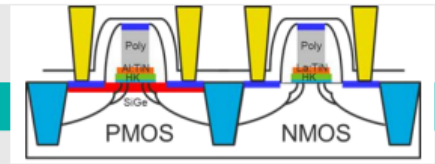
Alternative: STO etc.

M. Popovici (imec) et al. IEDM 2018
Schematic by TEL

Peri. CMOS

Poly SiON

High-k Metal Gate



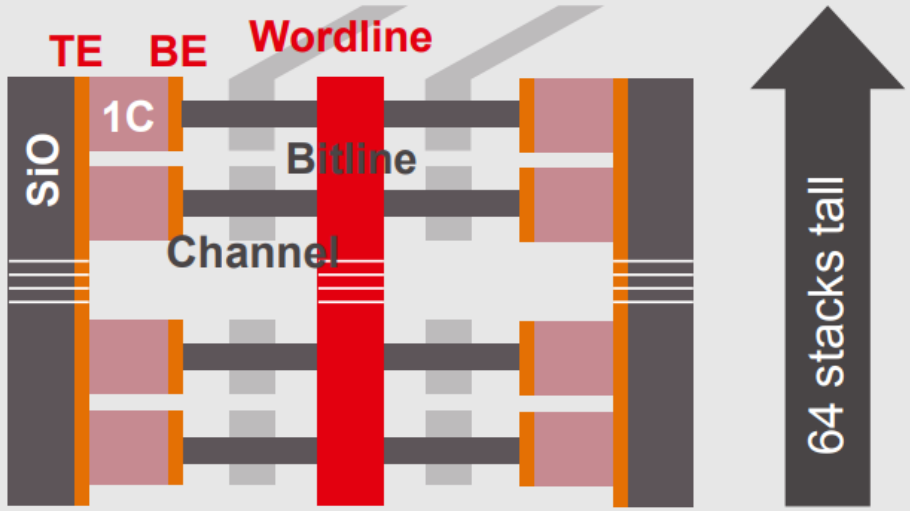
FinFET

Tool Vendors: Can Make Lots of $$$ like in 3D NAND

3D-DRAM DRIVES MORE ALD AND EPI OPPORTUNITIES

ASM INTERNATIONAL

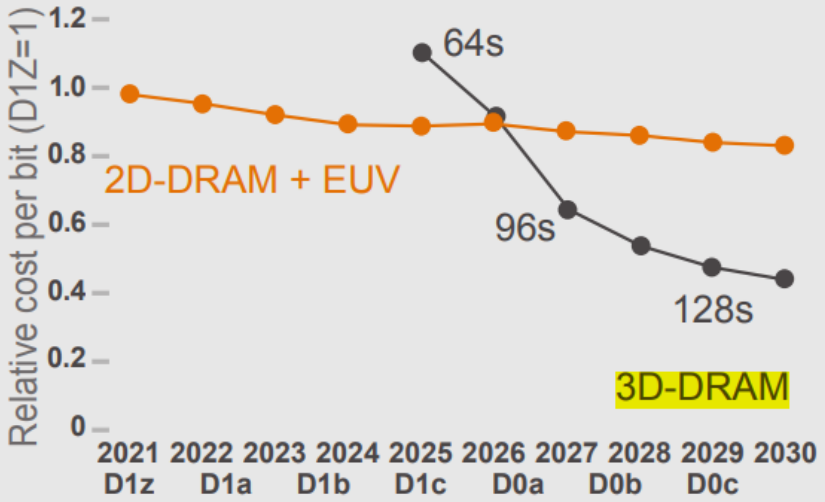
3D-DRAM



Monolithic 3D-DRAM is likely to happen around 2026

- Scale beyond 64Gb/chip limit for DIMM package
- Eliminate expensive EUV steps

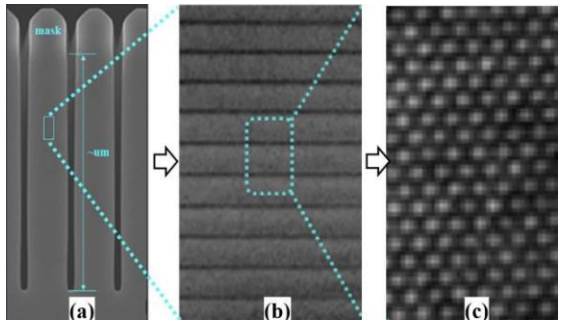
Cost per bit scaling

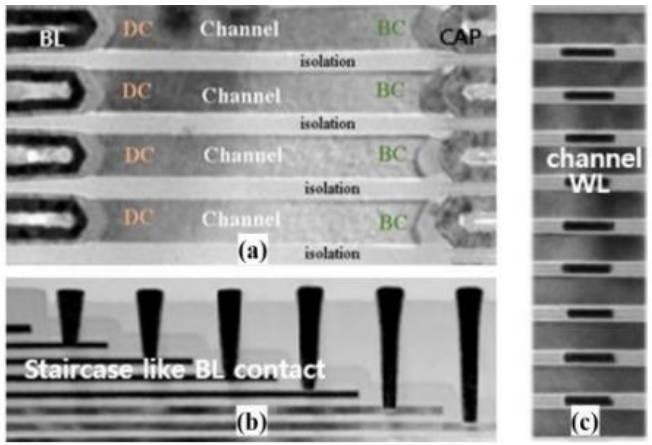


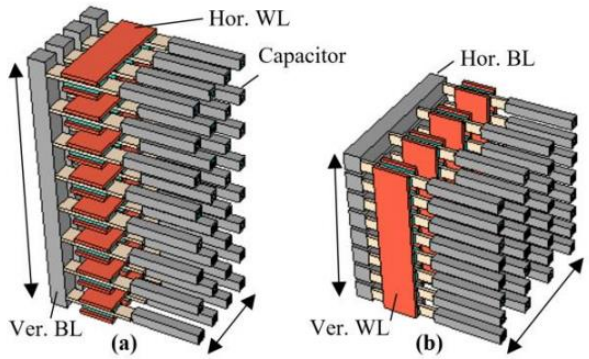
Key opportunities

- Channel: Si from Si/SiGe 64 (initially) Epi multi-layer stack
- Second generation 3D-DRAM: capacitor scaling with ALD Ultra High-k MIM cap

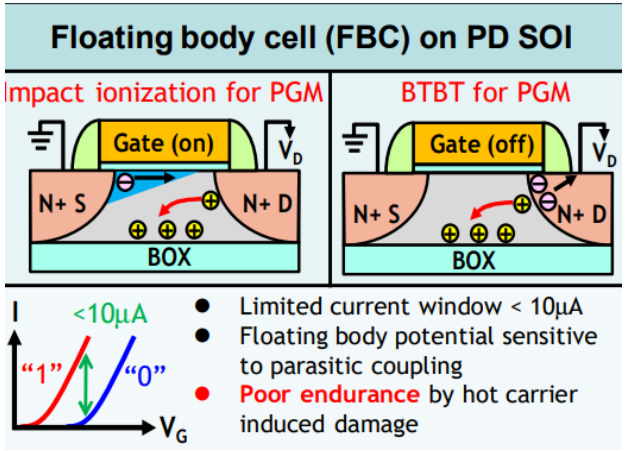
Some Options and A Million Challenges

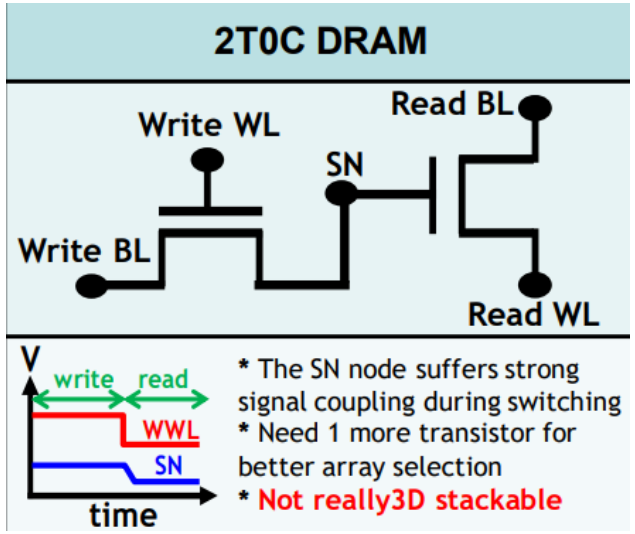


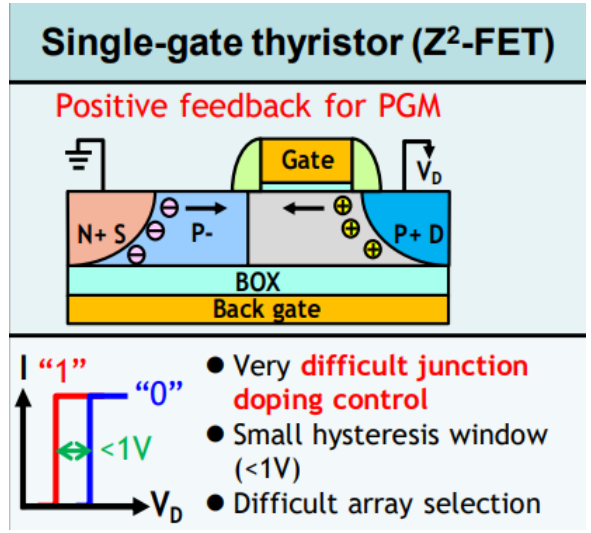


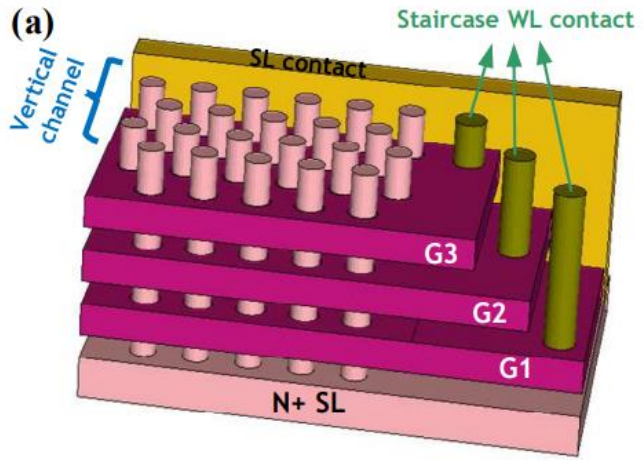


Source: 2023 VLSI Symp. "Ongoing Evolution of DRAM Scaling via 3rd Dimension: V-DAM" by JW Han et al.









Vertical 3-WL GCT (Micronix)

Source: 2023 IEDM. "A 3D Stackable DRAM: Capacitor-less …" by W.C. Chen et al.

Outlook: Wild Wild West

- For DRAM timing/perf., Si channel needed? (Si/SiGe)
- Still need sizable capacitor/area/high-K.
- Architectures: Vertical BL or Vertical WL? Staircase contact?
- Access transistor? How to fix peripheral with scaling?
- Chances of the capacitorless approaches?
- Many more process challenges:
  - HAR etch, lateral etch, ALD, ALE, Epi, deposition,
  - Doping, silicide, contact, stress management…

Further:

- Does it really need to be compatibility w/2D DRAM?
- Another memory layer? (lower perf./cost but higher capacity), taking advantage of CXL?
- Today, cost of DRAM/NAND>65X, maybe, 3D DRAM is the new SCM.
- Fertile ground for research and innovation, full of opportunities.
- What about Rowhammer problem? Coming patent war?
- And, then what? If CapEx too high, fall into the situation like 3D NAND today?