Flash Memory Summit

Understanding UCIe™ Protocols

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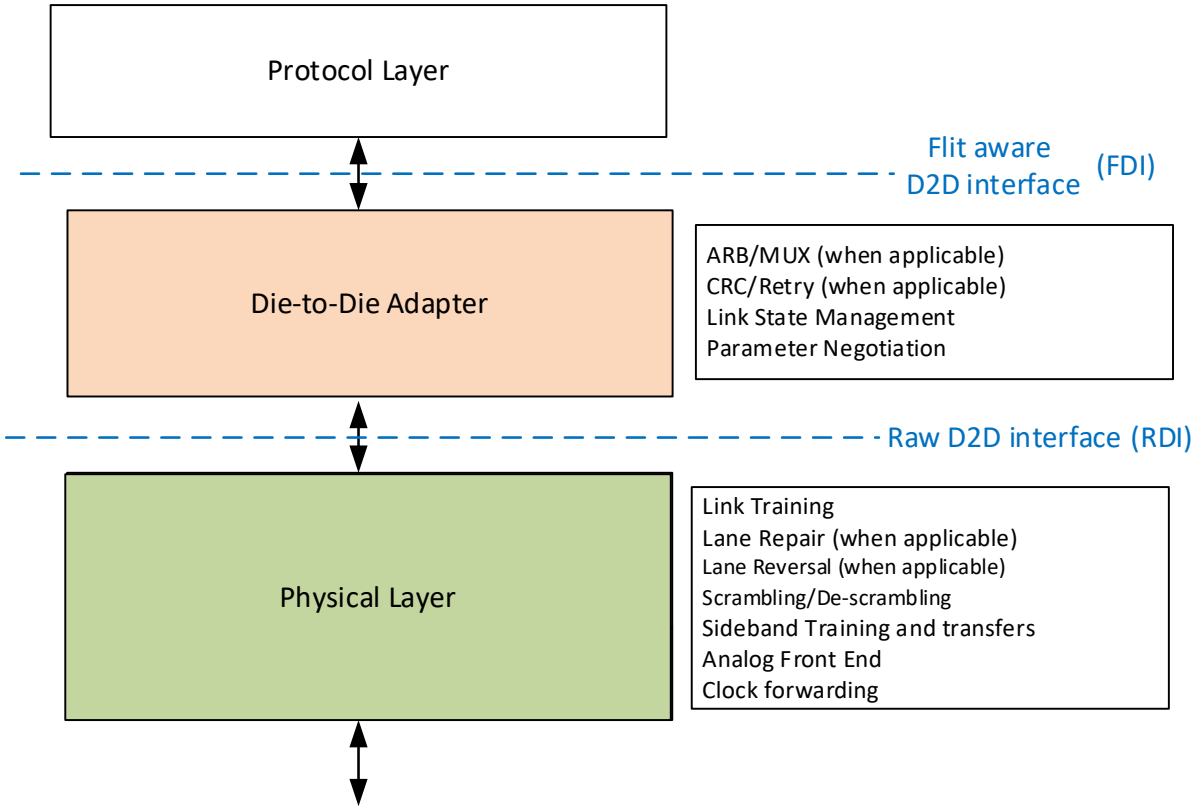
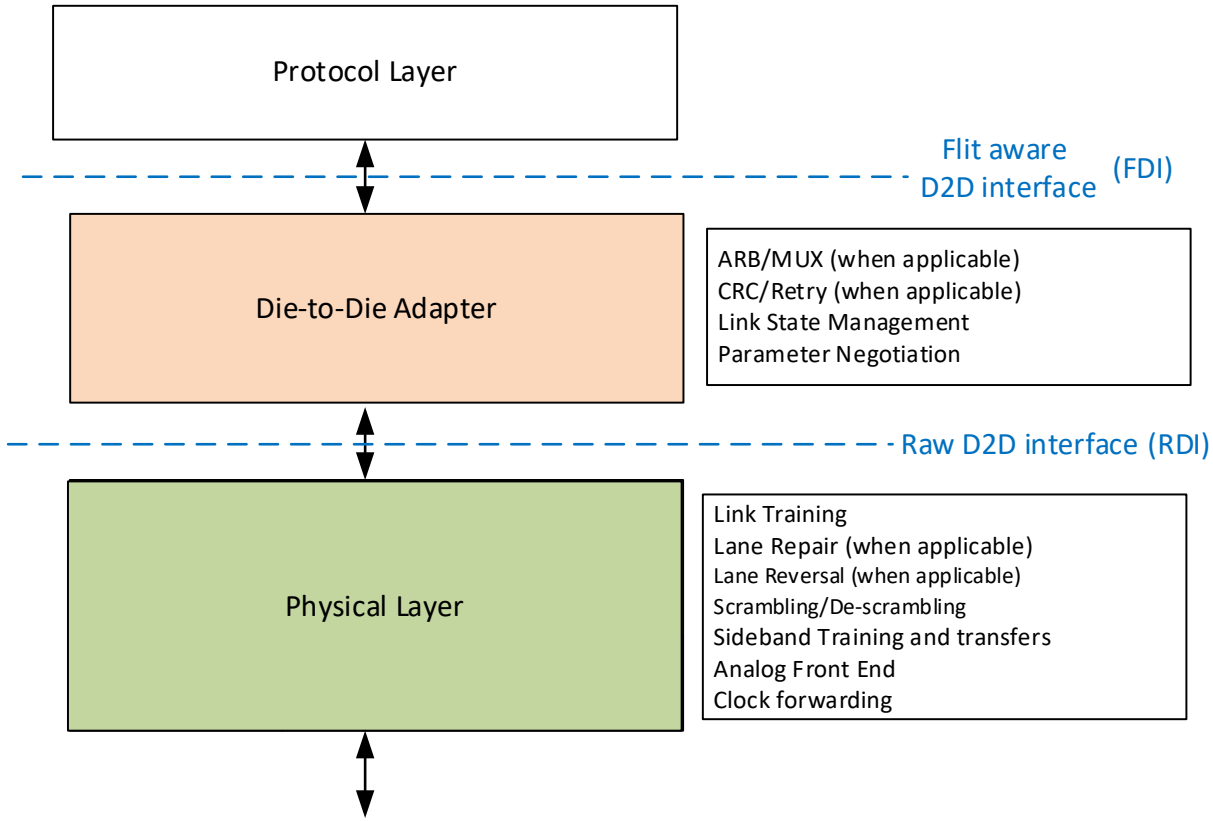
UCIe™ Protocols



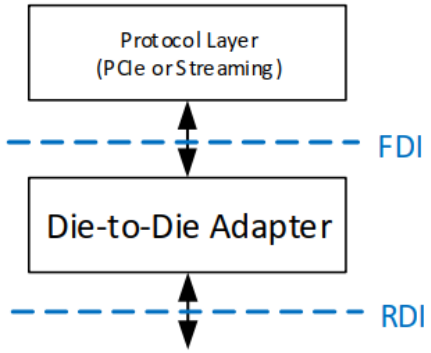
- Protocols supported
  - PCIe®
  - CXL™
  - Streaming: Vendor defined protocol
- Multiple Flit formats are permitted as a transport mechanism
- Raw formats are supported where Adapter CRC/Retry is bypassed – supported for all protocols

Adapter Functionality

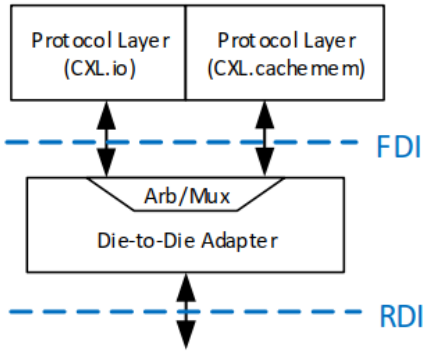
- For CXL™, ARB/MUX functionality is absorbed in the Adapter
- Lightweight CRC computation
- Flit Retry mechanism leveraged from PCIe® Flit Mode
- Link State Management for Reset/Active/PM/Error flows
- D2D specific or Protocol specific parameters negotiated with remote Link partner



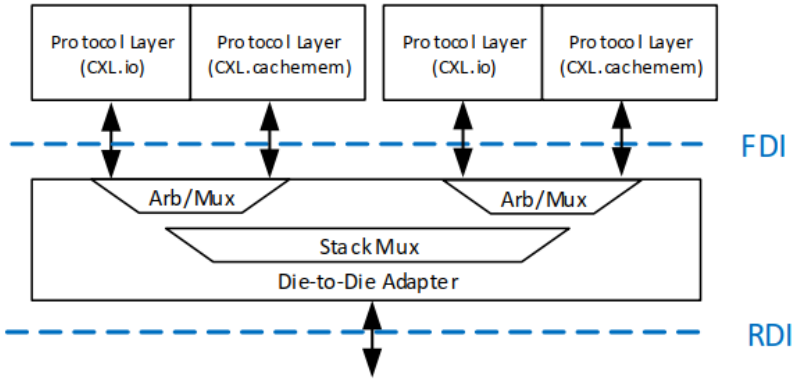
Example Configurations



(a) Single Protocol



(b) Single CXL Stack



(c) Two CXL stacks multiplexed inside the adapter

Raw Format (Format 1)

Byte	
0	64B (from Protocol Layer)

- All examples show 64B data width on FDI
- For Raw format, all bytes are populated by the Protocol Layer, and Adapter data path is bypassed
- Adapter simply forwards all the bytes to RDI without any modifications or additions
- Raw format is permitted for all Protocols

68B Flit Format (Format 2)

Byte									
0	Flit Hdr (Byte 0)	Flit Hdr (Byte 1)	62B of Flit 1 (from Protocol Layer)						
64	2B of Flit 1 (from Protocol Layer)		CRC (Byte 0)	CRC (Byte 1)	Flit Hdr (Byte 0)	Flit Hdr (Byte 1)	58B of Flit 2 (from Protocol Layer)		
128	6B of Flit 2 (from Protocol Layer)						CRC (Byte 0)	CRC (Byte 1)	bytes from next flit

- Used for PCIe non-Flit Mode and CXL.io 68B Flit Mode protocols
- Protocol Layer presents 64B of the Flit on FDI
- Adapter adds 2B Flit Header, 2B CRC and performs the required barrel shifting before transmitting over RDI
  - CRC covers the 2B Flit header as well as the 64B of Protocol information
- Flit header carries protocol identifier, stack identifier, sequence number, Ack/Nak completion, pause of data stream indication

Standard 256B End Header Flit Format (Format 3)

Byte									
0	Flit Chunk 0 64B (from Protocol Layer)								
64	Flit Chunk 1 64B (from Protocol Layer)								
128	Flit Chunk 2 64B (from Protocol Layer)								
192	Flit Chunk 3 44B (from Protocol Layer)	Flit Hdr (Byte 0)	Flit Hdr (Byte 1)	DLP Bytes 2:5	10B Reserved	CRC0 (Byte 0)	CRC0 (Byte 1)	CRC1 (Byte 0)	CRC1 (Byte 1)

- Used for PCIe® Flit Mode protocol
- Protocol Layer sends the Flit over FDI, drives 0b on the bits filled in by the Adapter (Flit Marker populated by Protocol Layer in DLP Bytes 2:5)
  - DLLPs sent/received over separate signals on FDI
- Adapter fills in DLLP if Flit Marker is not present in DLP Bytes 2:5

Standard 256B Start Header Flit Format (Format 4)

CXL.cachemem

Byte								
0	Flit Hdr (Byte 0)	Flit Hdr (Byte 1)	62B of Flit Chunk 0 (from Protocol Layer)					
64	Flit Chunk 1 64B (from Protocol Layer)							
128	Flit Chunk 2 64B (from Protocol Layer)							
192	50B of Flit Chunk 3 (from Protocol Layer)			10B Reserved	CRC0 (Byte 0)	CRC0 (Byte 1)	CRC1 (Byte 0)	CRC1 (Byte 1)

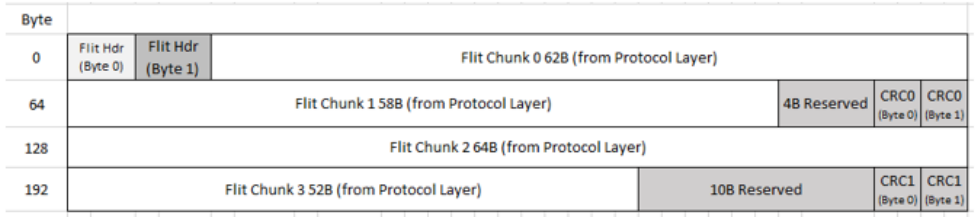
CXL.io

Byte								
0	Flit Hdr (Byte 0)	Flit Hdr (Byte 1)	Flit Chunk 0 62B (from Protocol Layer)					
64	Flit Chunk 1 64B (from Protocol Layer)							
128	Flit Chunk 2 64B (from Protocol Layer)							
192	Flit Chunk 3 46B (from Protocol Layer)			DLP Bytes 2:5	10B Reserved	CRC0 (Byte 0)	CRC0 (Byte 1)	CRC1 (Byte 0)	CRC1 (Byte 1)

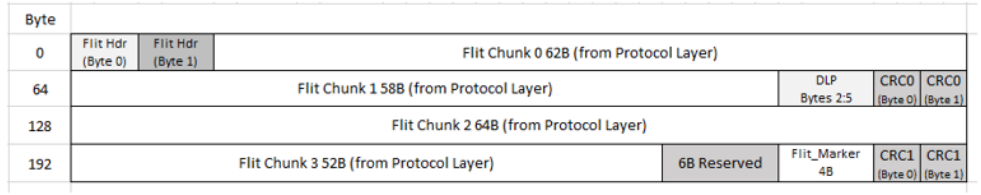
- Used for CXL™ 256B Flit Mode protocol
- Protocol Layer sends the Flit over FDI, drives 0b on the bits filled in by the Adapter
  - For CXL.io, Flit Marker populated by Protocol Layer in DLP Bytes 2:5. DLLPs sent/received over separate signals on FDI
- Follows the Framing rules for the Standard Flit in CXL™ Specification

Latency Optimized 256B without Optional Bytes (Format 5)

CXL.cachemem



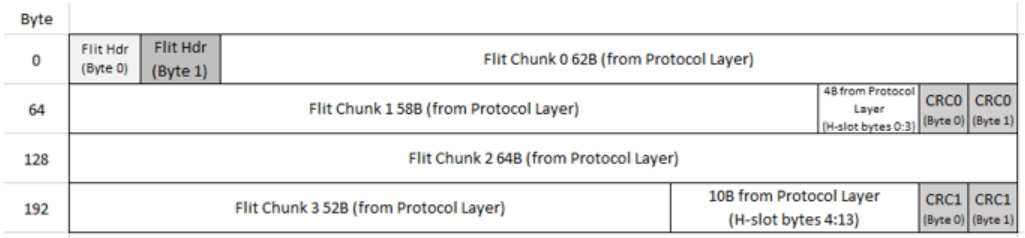
CXL.io



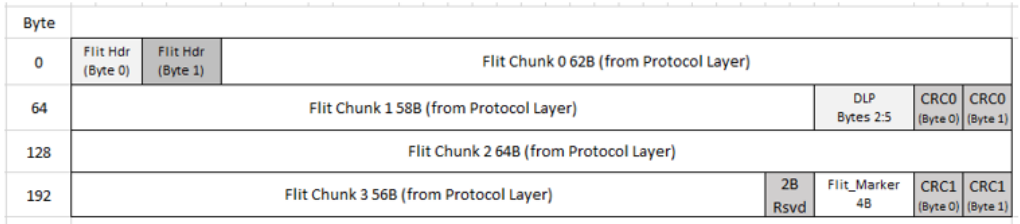
- Used for CXL™ 256B Flit Mode protocol
- Protocol Layer sends the Flit over FDI, drives 0b on the bits filled in by the Adapter
  - For CXL.io, Flit Marker populated by Protocol Layer in DLP Bytes 2:5. DLLPs sent/received over separate signals on FDI
- Follows the Framing rules for Latency Optimized Flit in CXL™ Specification

Latency Optimized 256B with Optional Bytes (Format 6)

CXL.cachemem



CXL.io



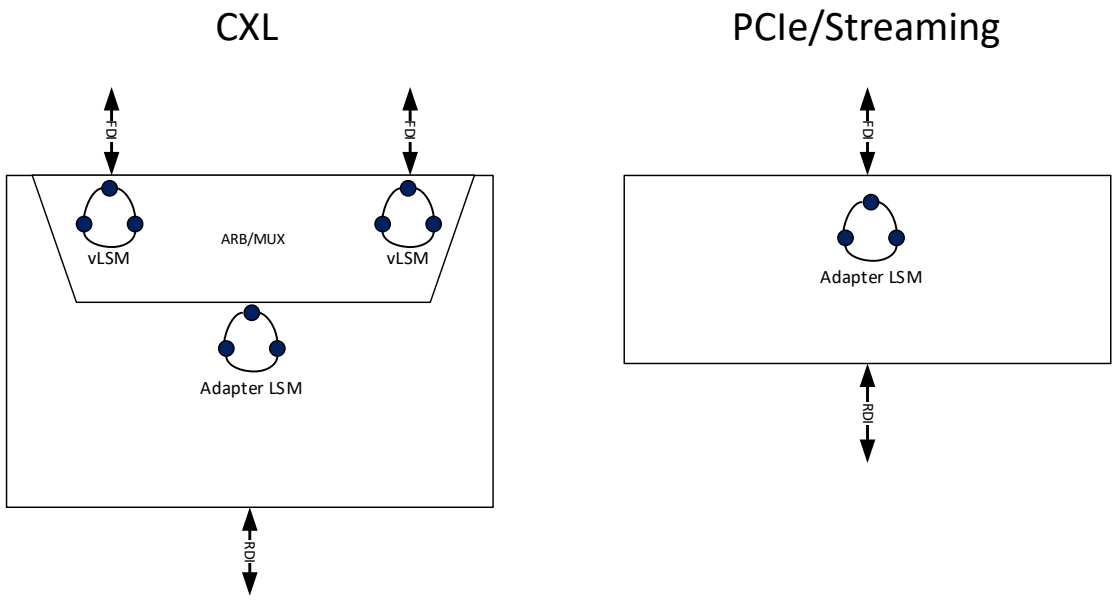
- Used for CXL™ 256B Flit Mode protocol
- Protocol Layer sends the Flit over FDI, drives 0b on the bits filled in by the Adapter
  - For CXL.io, Flit Marker populated by Protocol Layer in DLP Bytes 2:5. DLLPs sent/received over separate signals on FDI
- Follows the Framing rules for Latency Optimized Flit in CXL™ Specification with additional bytes from Protocol Layer for added efficiency
  - CXL.io gets an extra DWord of TLP information
  - CXL.cachemem gets an extra H-slot (14 Bytes)

Protocol and Flit Format Matrix (UCIe™ 1.0)

Format Number	Flit Format Name	PCIe Non-Flit Mode	PCIe Flit Mode	CXL 68B Flit Mode	CXL 256B Flit Mode	Streaming*
1	Raw	Optional	Optional	Optional	Optional	Mandatory
2	68B	Mandatory	N/A	Mandatory	N/A	N/A
3	Standard 256B End Header	N/A	Mandatory	N/A	N/A	N/A
4	Standard 256B Start Header	N/A	N/A	N/A	Mandatory	N/A
5	Latency Optimized 256B without optional bytes	N/A	N/A	N/A	Optional	N/A
6	Latency Optimized 256B with optional bytes	N/A	N/A	N/A	Strongly Recommended	N/A

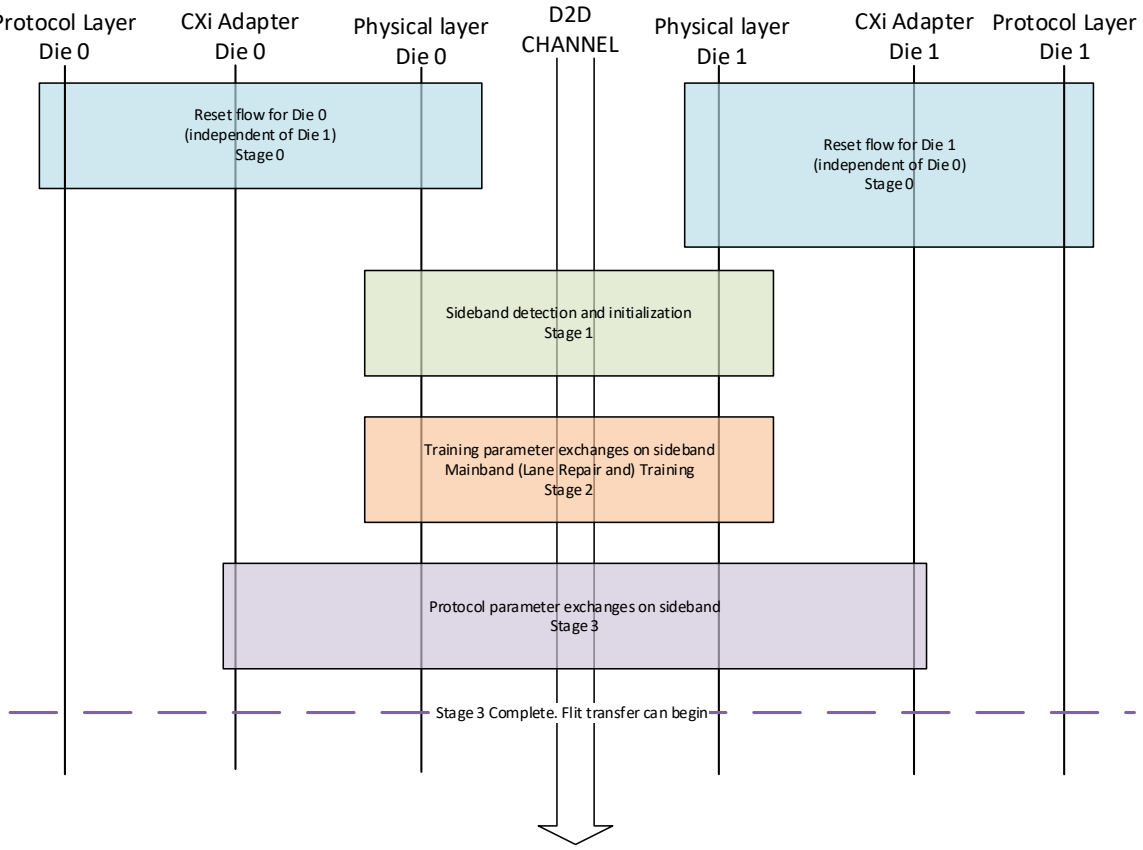
*Streaming column is for Adapter. Protocol Layer interop is vendor specific

State Machine Hierarchy



- For CXL™, vLSM is exposed on FDI
- For PCIe®/Streaming, Adapter LSM is exposed on FDI
- vLSM handshakes with remote Link partner use ALMPs and follow CXL™ 256B Flit Mode rules and format
- Adapter LSM handshakes with remote Link partner use sideband Link

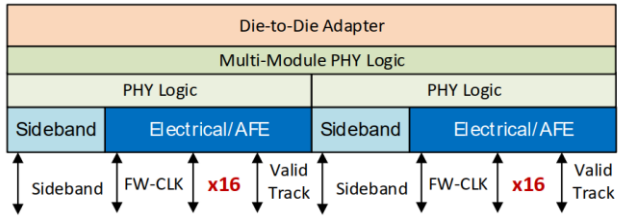
Link Initialization Flow

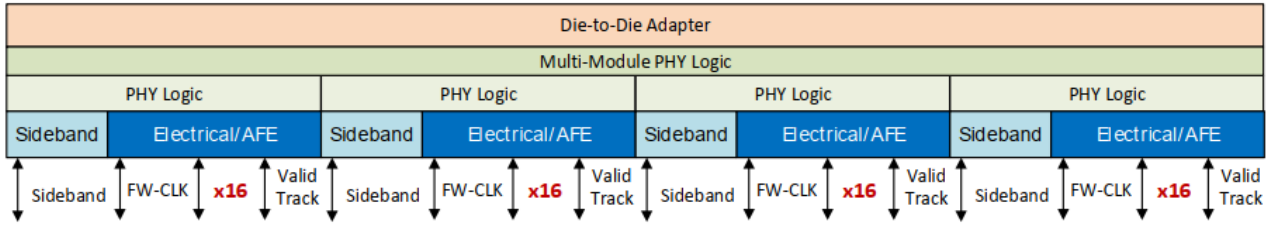


Logical PHY Functions

- Byte to Lane mapping for data transmission over Lanes
  - Separate Valid Lane for indicating data transfer
- Interconnect redundancy remapping for Advanced Package configurations
- Width degradation support for Standard Package Configurations
- Scrambling and training pattern generation
- Lane reversal
- Link initialization, training and power management states
- Transmitting and receiving sideband messages

Multi-Module Support





- One, two or four module per Adapter are allowed
  - Both Advanced and Standard Package

- Standard package example configurations shown here

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UCIe™
Universal Chiplet Interconnect Express

THANK YOU

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