Flash Memory Summit

# Perspectives on Developing 3D Resistance Memory with Multi-level Capability

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# Outline

- Motivation
- Basics of a Resistive-gate flash, RG-Flash,
  - A simple MIM on top of FinFET, and
  - forming-free and bipolar switching operation,
  - compatible with the CMOS process
- Demonstration of QLC (Quad-Level-Cell)
- 3D Resistance Memory- Perspectives
- Conclusions

# Motivation- Why 1T1R(gate-type) was chosen in this study ?

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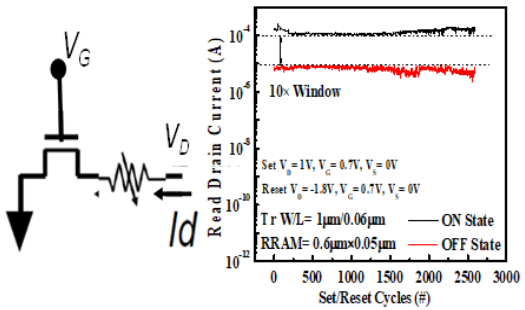
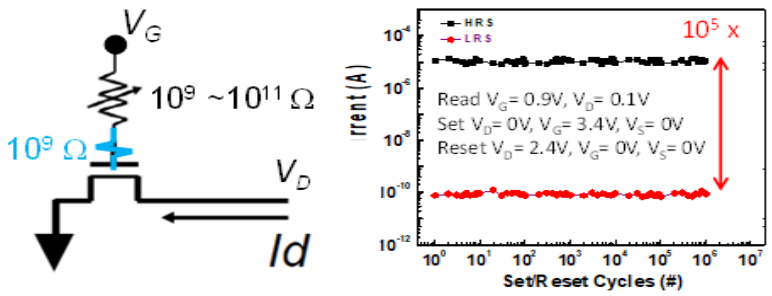
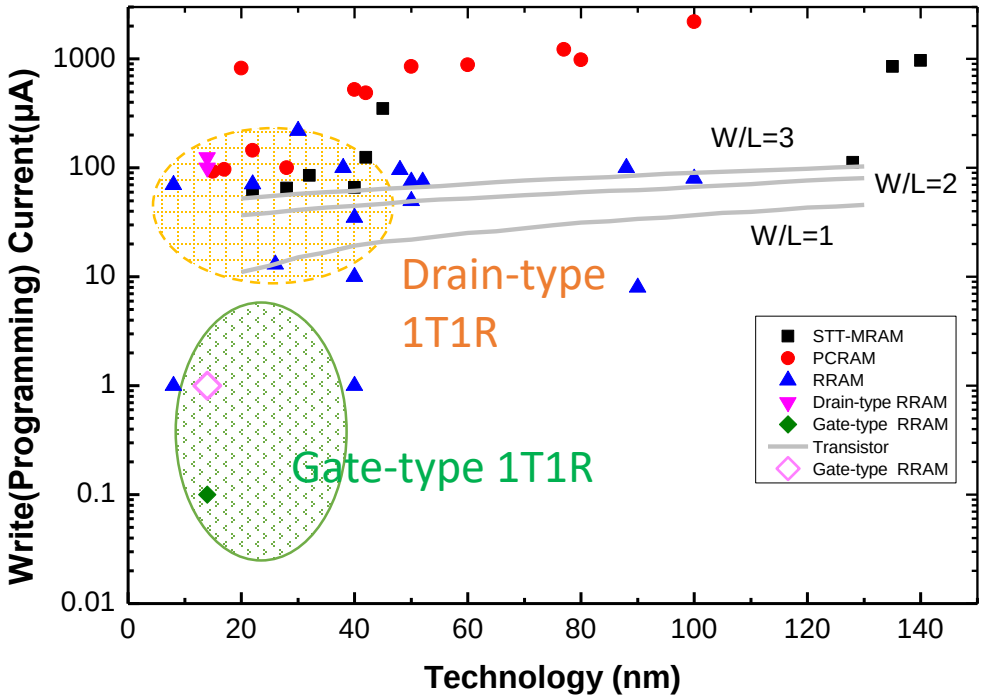
- Conventional 1T1R (drain-type) has
  - ✓limited window (10x or larger)
  - ✓Multi-level operation becomes non-realistic,
- Major advantage of gate-type 1T1R
  - ✓Huge window
  - ✓Very low write current
  - ✓High density for both NOR/NAND

**Drain-type 1T1R**




**Gate-type 1T1R**




*Modified from S. Yu, IEEE Solid-State Circuits Mag., 2016.*

# RRAM- Technology Advances

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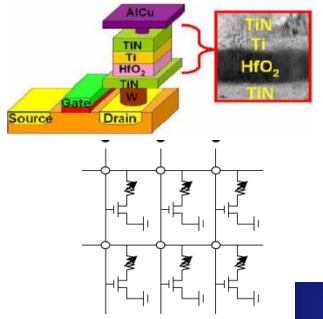
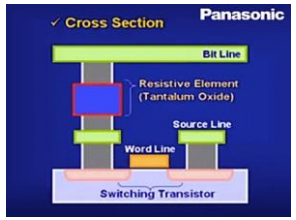
2010 2013 2015 2017 2021 2023 2025

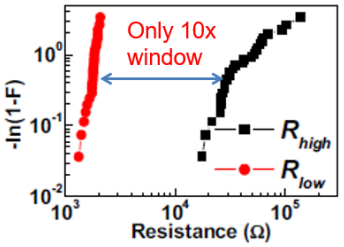
## Drain-type 1T1R




*S-S. Sheu VLSI 2010*

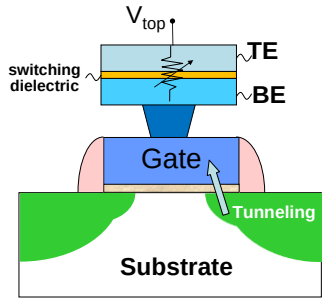



*RRAM Embedded 8-bit MCUs (Panasonic)*



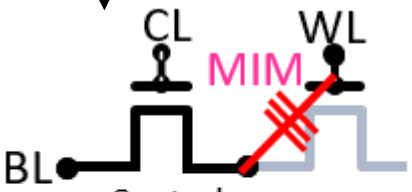

40nm CMOS

## Gate-type 1T1R

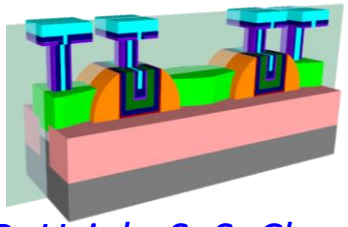



*1T RG-Flash S. S. Chung, 2015DRC*

16nm FinFET



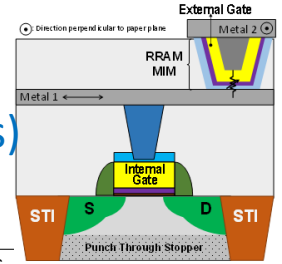

1T1R(drain-type)

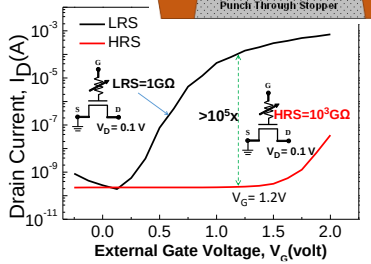


*E. R. Hsieh, S. S. Chung et al., Symp. VLSI, 2017*

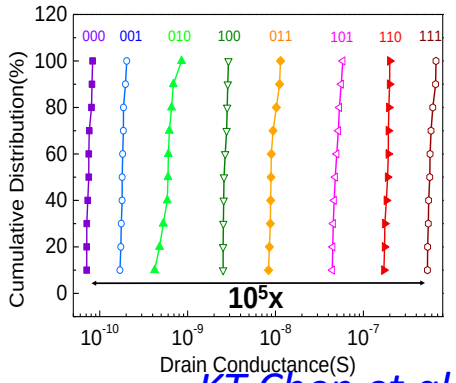
## TLC

(2021irps)




Window > $10^5$x

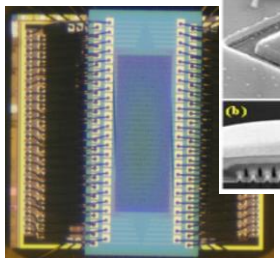


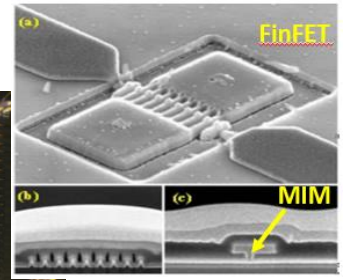

*KT Chen et al., IRPS, 2021*

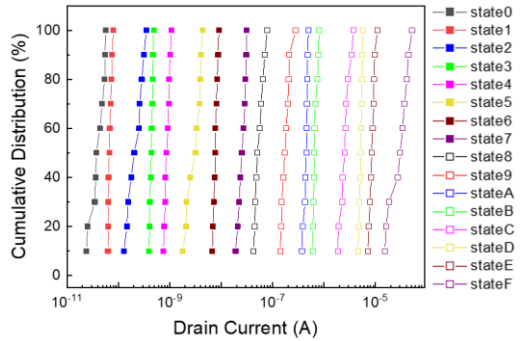
## QLC

14nm FinFET

(2023irps)





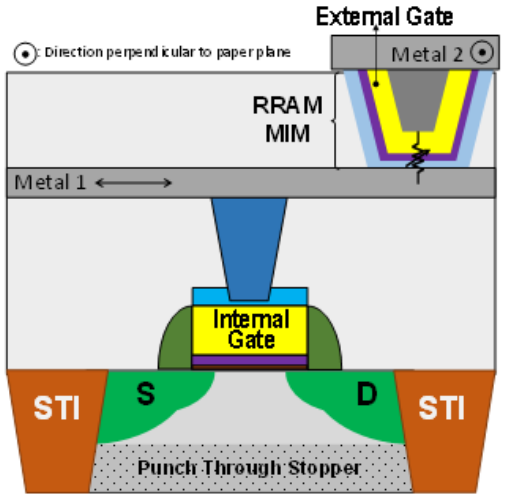



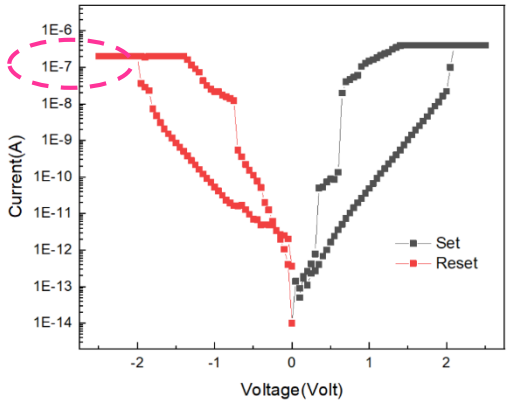

*M. Y. Lee et al., IRPS, 2023*

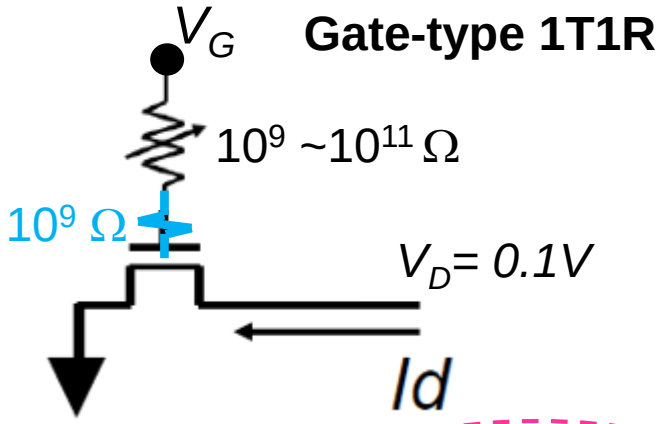
## 3D ?

# Resistive-gate Flash NVM: RG-Flash

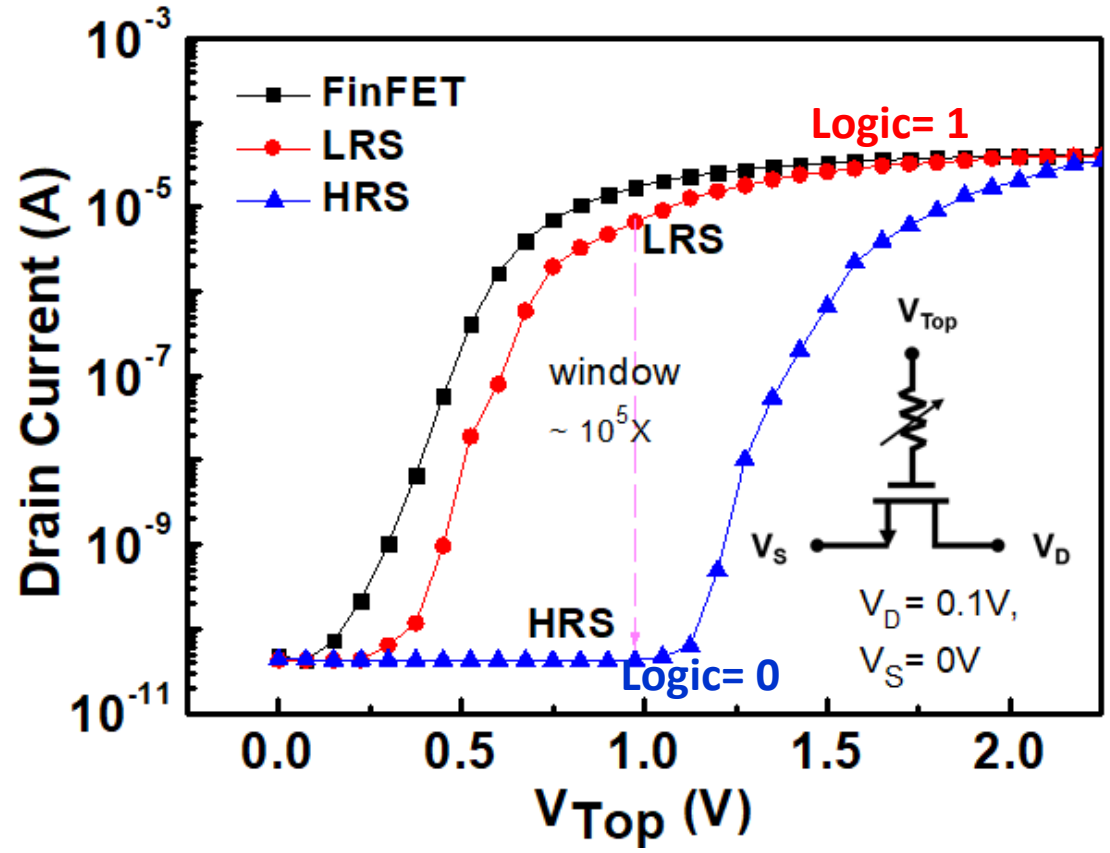
- To develop an MIM with high resistance up to $10^9\Omega$ is the key which enables the resistive switching.




| | |
|---|---|
| Forming Voltage | Forming-free |
| SET Voltage | 2.4 V |
| RESET Voltage | -1.8 V |
| Compliance Current | 0.4 μA |
| HRS | $3\times10^{11}\ \Omega$ |
| LRS | $2\times10^9\ \Omega$ |
| ON/OFF Ratio | 150 |
| Speed(SET/RESET) | 10 ns/4ns |



# QLC- 4 bit/cell (RG-Flash)

**A World First QLC RRAM: Highly Reliable Resistive-Gate Flash with Record $10^8$ Endurance and Excellent Retention** (IEEE-IRPS, 2023)

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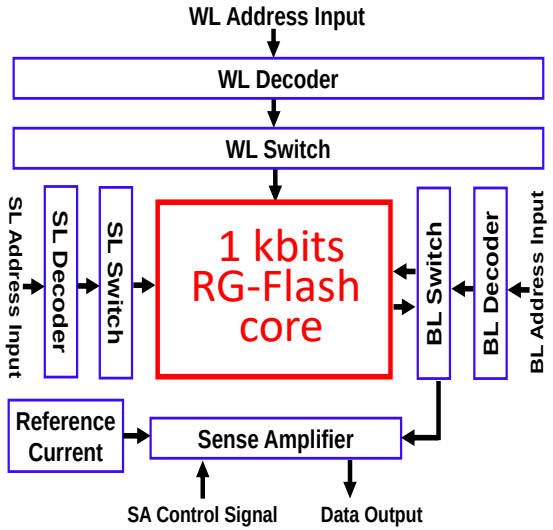
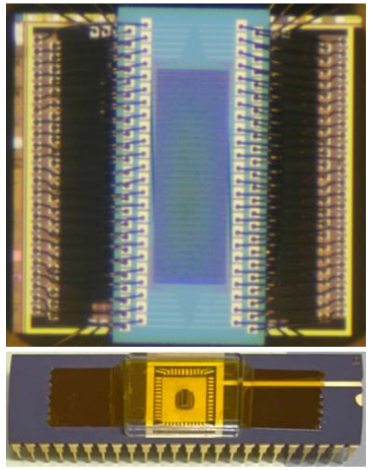
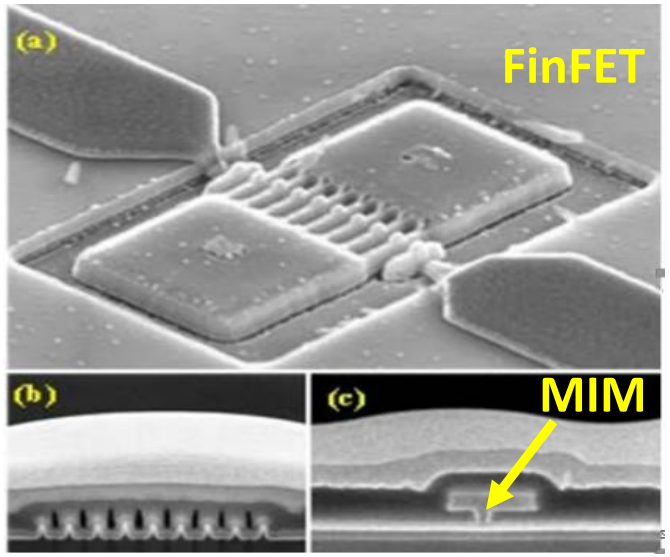
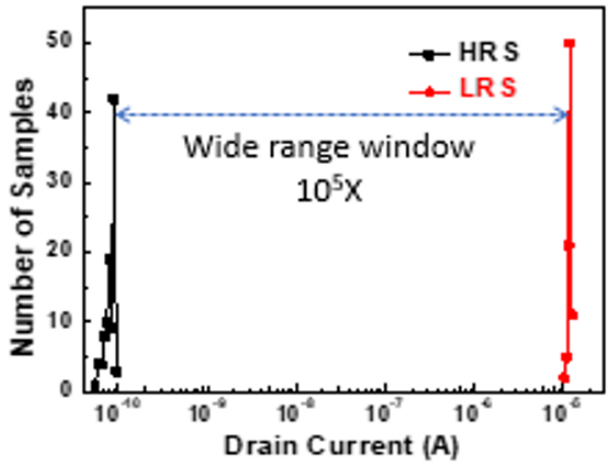


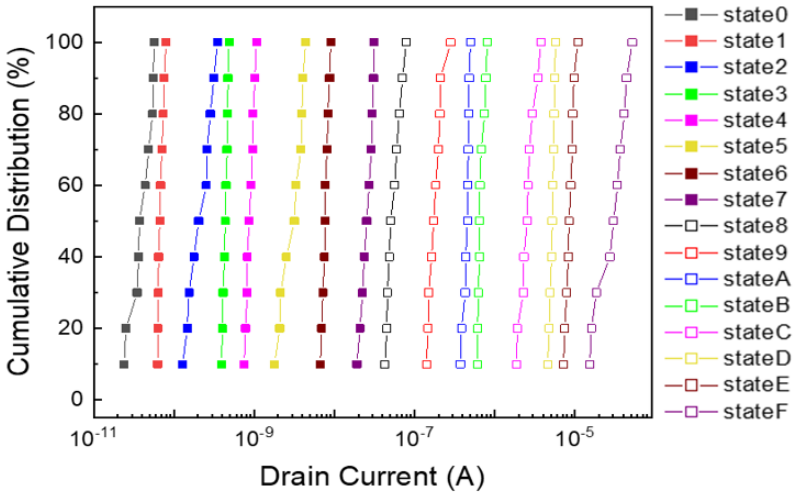


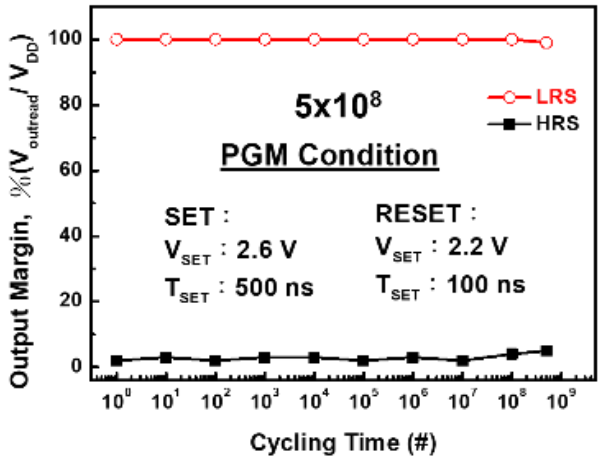

SLC Operation= 2 levels




4-Bit-Per-Cell

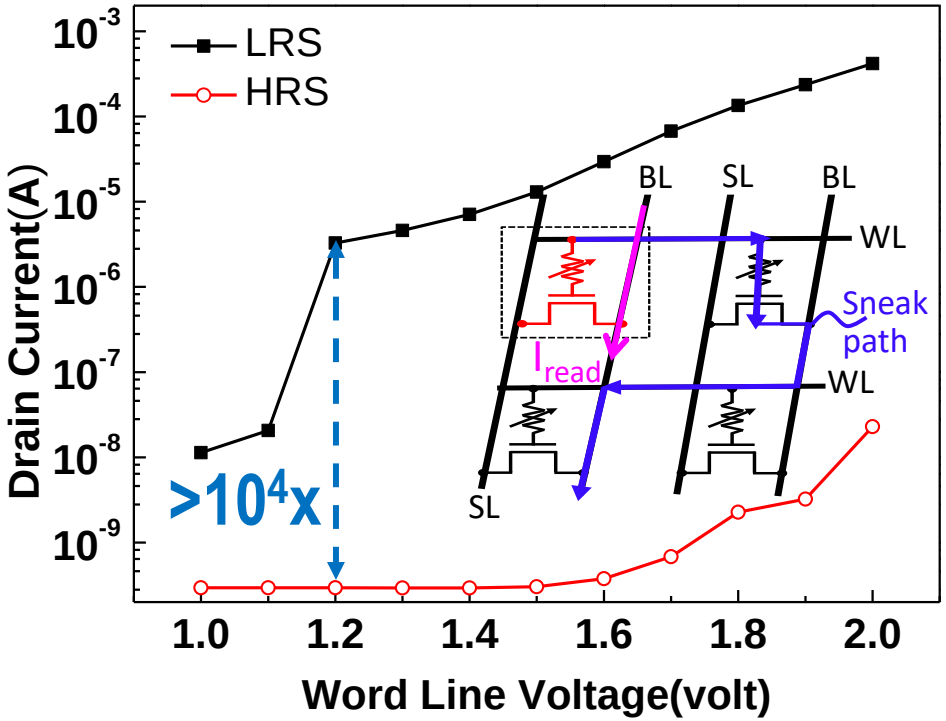
QLC Operation= 16 levels



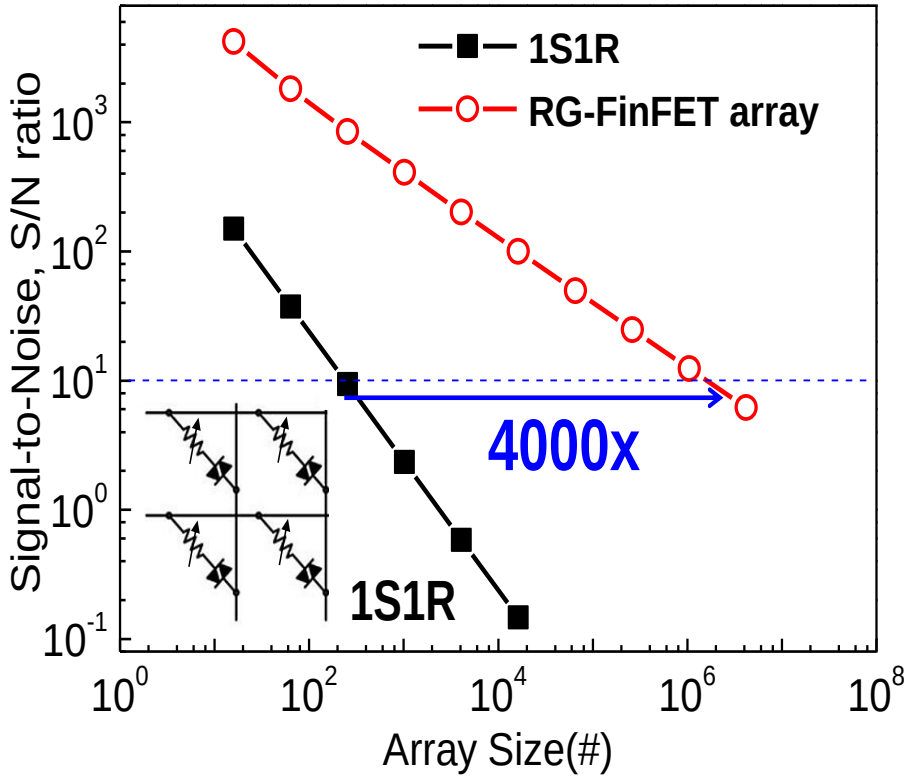

- Endurance of RG-Flash- showing more than $5x10^8$ cycles
- The best comparing to reported results

# Evaluation of the Sneak-current




- RG-Flash: sneak current can be reduced to 1nA.

# Comparison with Cross-bar



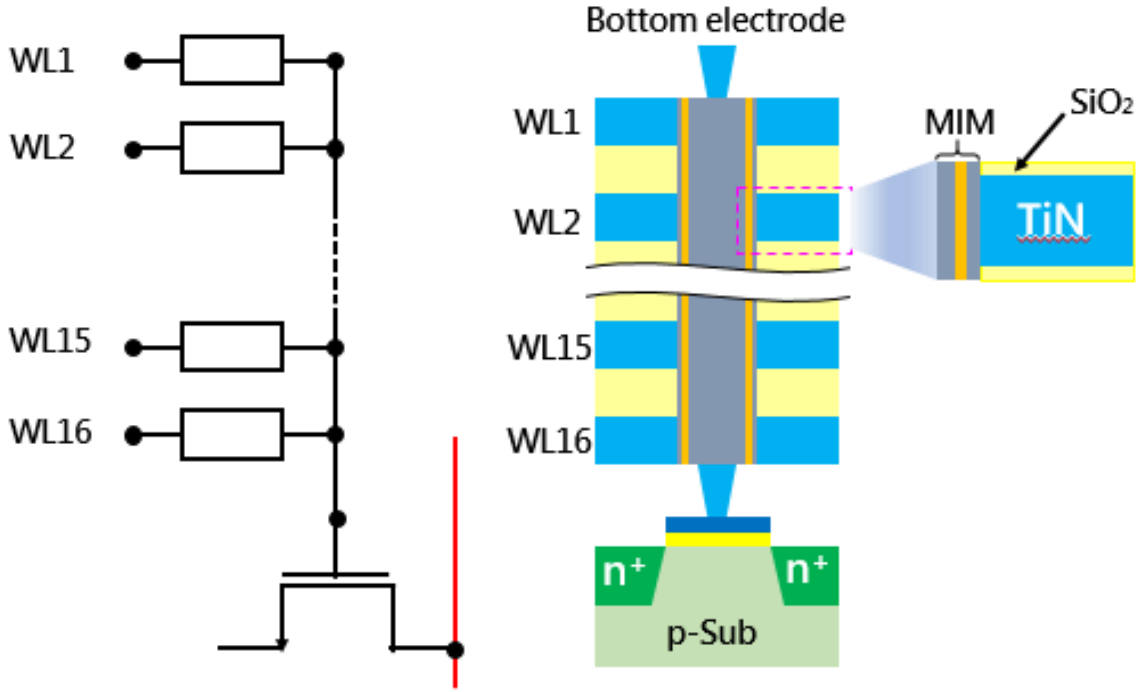

- The S/N ratio can still be maintained even if the array size is expanded up to 1 million cells.

# The comparison with reported results



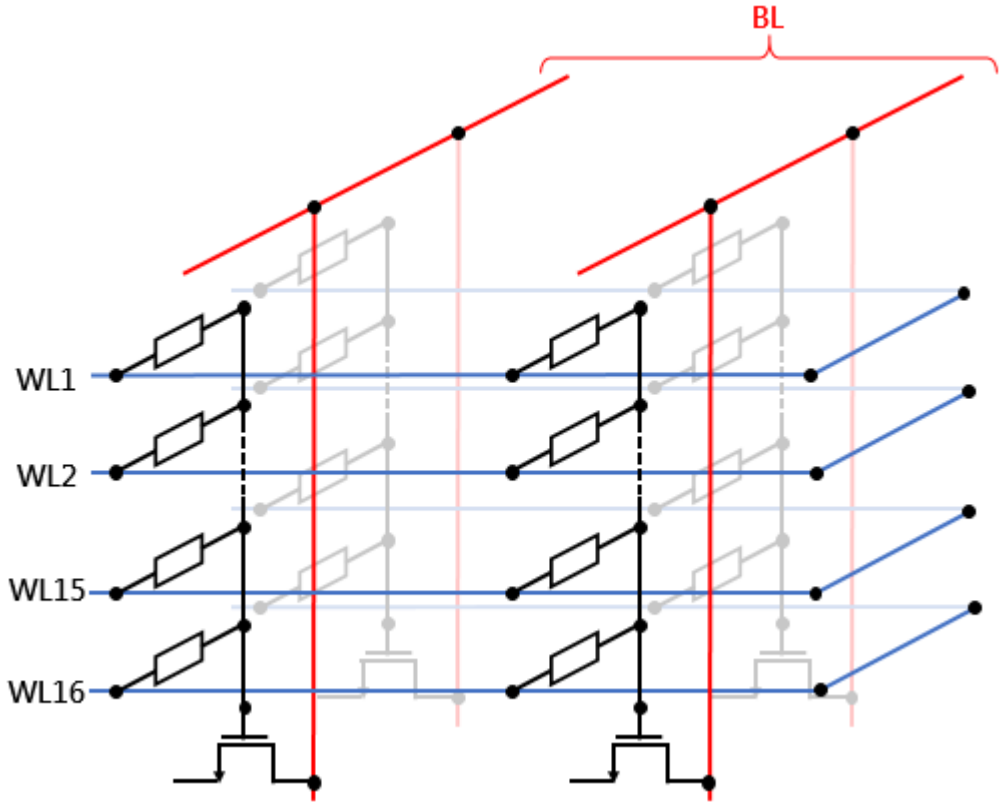
| Ref. | Yang irps'21 | Hsieh EDL'21 | LE TED'21 | Feng TED'21 | This Work |
|---|---|---|---|---|---|
| Memory Window | $10^5$ | 50 x | 10 x | N/A | $10^6$ |
| Multiple Bits | 3 | 3 | 3 | 3 | 4 |
| Endurance | $10^5$ | $10^5$ | 8 x $10^3$ | NA | 5x$10^8$ |
| Retention | 1 month @125°C | 10 years @110°C | 30 min @110°C | 30 min @110°C | 10 years @138°C |
| Program Speed | SET：10 ns RESET：5 ns | N/A | N/A | N/A | SET：10 ns RESET：4 ns |
| Program Voltage | 3 V | 3 V | 4 V | 3 V | SET(1.8 V ~ 3.8 V) RESET(-1.6 V ~ -3 V) |

# Perspectives- 2D/3D Architecture




**Schematic of 1T16R**

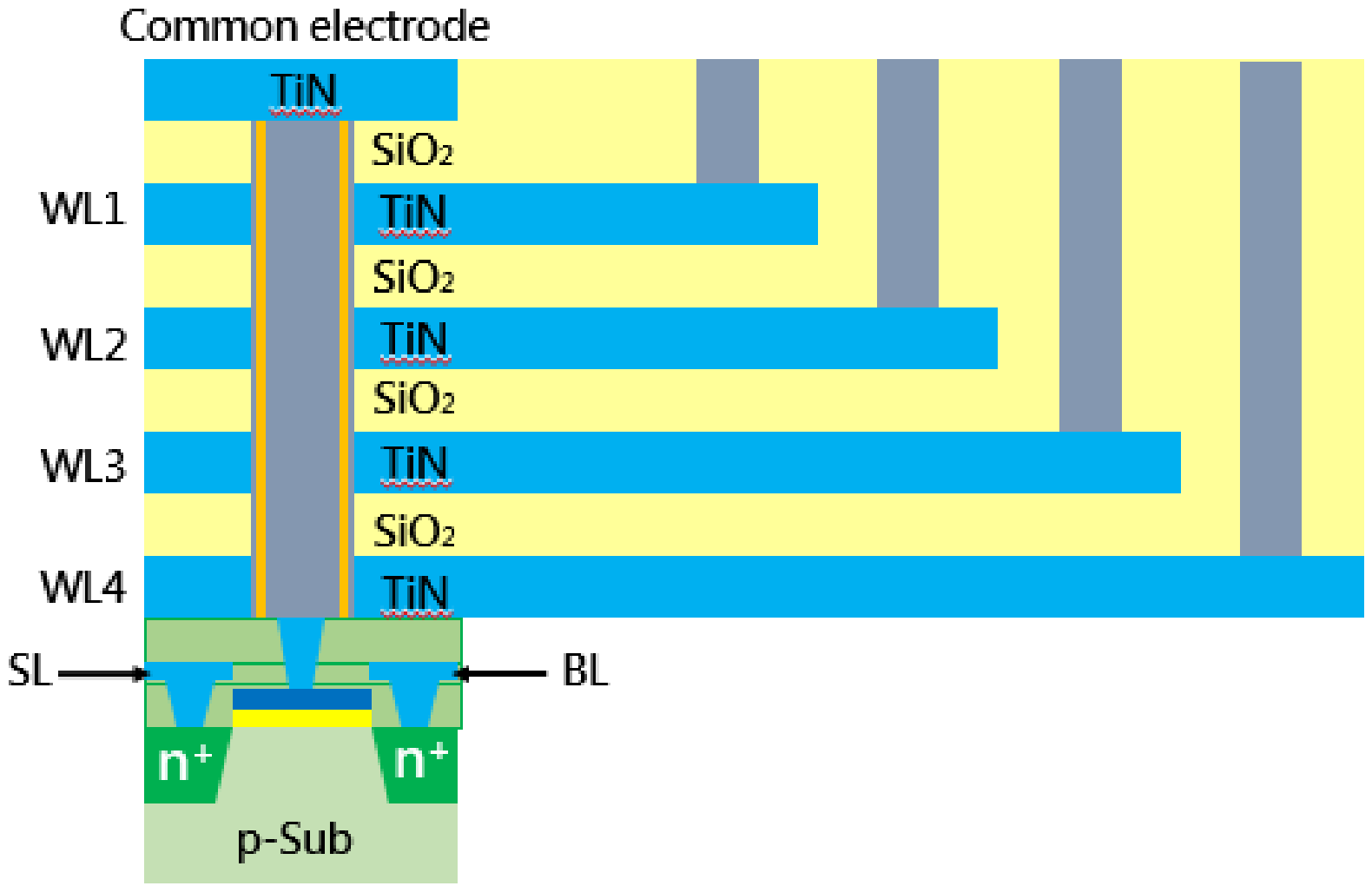
- **Transistor: Front-end**
- **MIM: backend**
- **$4F^2$/cell**
- **Low operation voltage < 3V (14nm)**
- **Scalable (e.g., FinFET, Nanosheet)**




**3D NOR architecture with 1T16R**

- **fast access time for each bit (~nsec)**
- **Can be reconfigured as NAND**

# 3D Architecture




*Back-end*

*Front-end*

# Summary and Conclusions


- An 1T1R Gate-resistive switching flash, RG-Flash, was proposed,
  - Compatible with the CMOS process,
  - A simple MIM on top of FinFET, and
  - A forming-free and bipolar switching operation
- A quad-level cell (QLC) was successfully demonstrated.
- Compared to conventional drain-type 1T1R, RG-Flash is better for a larger window, smaller cell-size, excellent immunity to disturbs, no sneak path, and lower power consumption.
- Perspectives-
  - for embedded and stand-alone products either in 2D or 3D architectures,
  - extended down to FinFET, nanosheet generations.

# Thank you for your kind attention !!

*More inquires, send to schung@nycu.edu.tw*

# SET/REST Conditions and Shmoo Plots

# Disturb Tests

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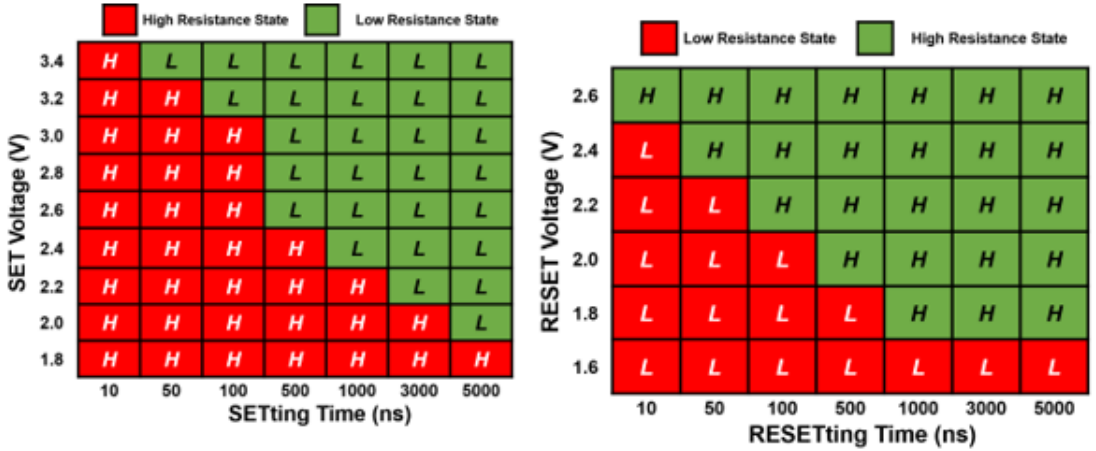
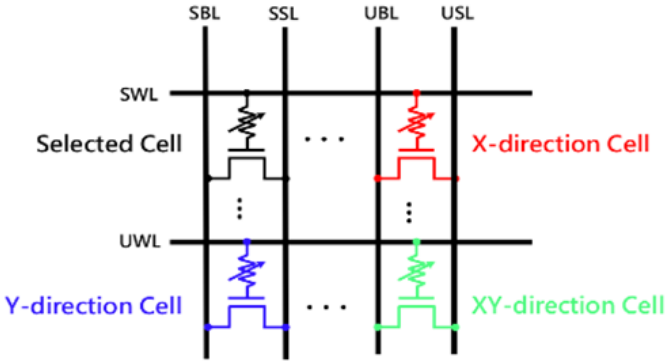
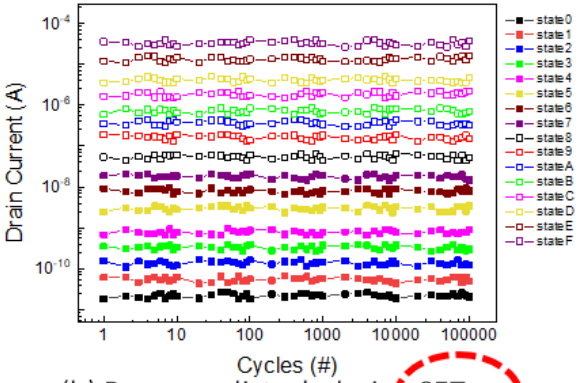
| | SET | RESET |
|---|---|---|
| Selected | $V_{WL}= V_{SET}$, $V_{BL}= 0V$, Floating | $V_{WL}= 0V$, $V_{BL}= V_{RESET}$, Floating |
| Unselected (Worst case) | $V_{WL}= V_{SET}$, $V_{BL}= V_{SET}/2$, Floating | $V_{WL}= V_{RESET}/2$, $V_{BL}= V_{RESET}$, Floating |



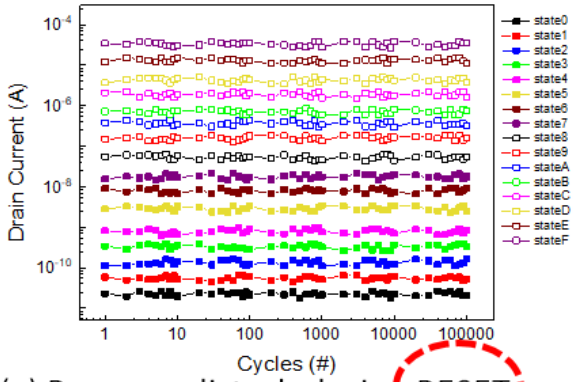

2V < Operating bias < 3V



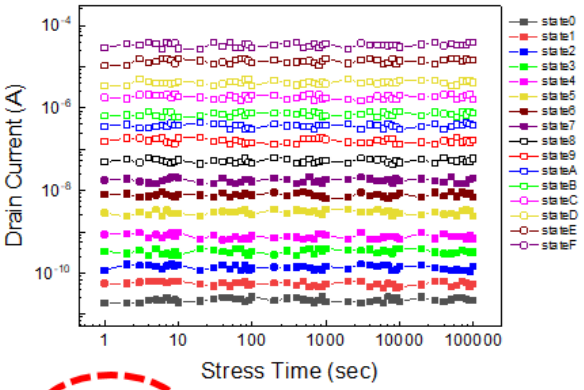

(a) Array definition




(b) Program disturb during SET (x-direction cell)

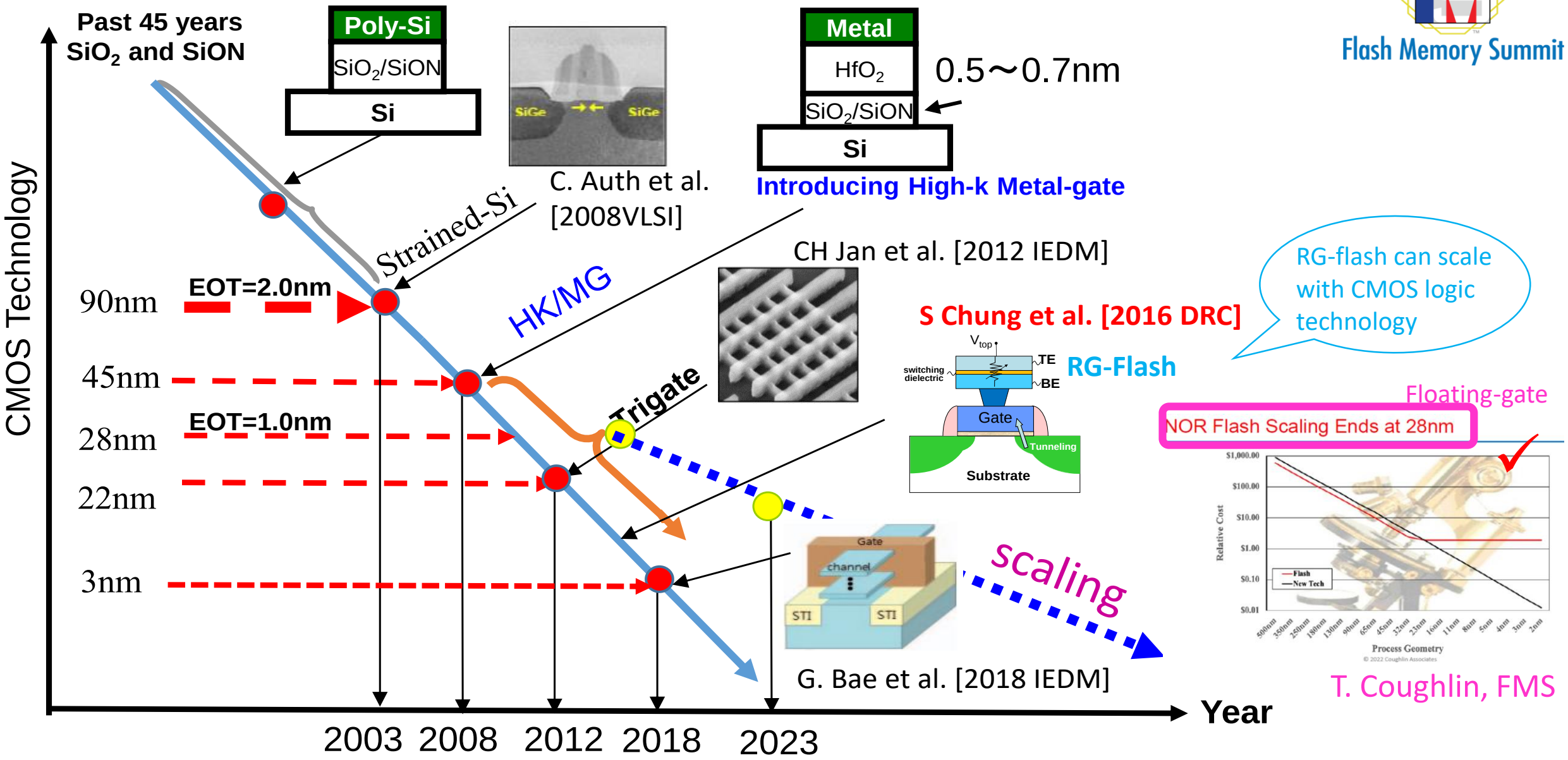



(c) Program disturb during RESET (y-direction cell)




(d) READ disturb (X-direction cell)

# Technology Roadmap

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