Innovations in SSD Controller Architecture for Next Generation Data Center SSDs

Adam Jachniewicz, Principal Applications Engineer
Microchip Technology Inc.

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Agenda

- Requirements and Challenges in NVMe™ SSDs
- Solutions on the Horizon
- Flexible Programming Architecture for Evolving Challenges
- Conclusion

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Requirements and Challenges

Modern SSD Requirements and Challenges

Requirements:

- Performance and power
- Capacity
- SMART monitoring and maintenance in the enterprise infrastructure
- Debug capability
- Security

Challenges:

- Increasing amounts of data
- Evolution of NAND, DDR, SSD, etc.
- Supply chain
- Multiple product SKUs
- Interoperability
- Security protocol changes

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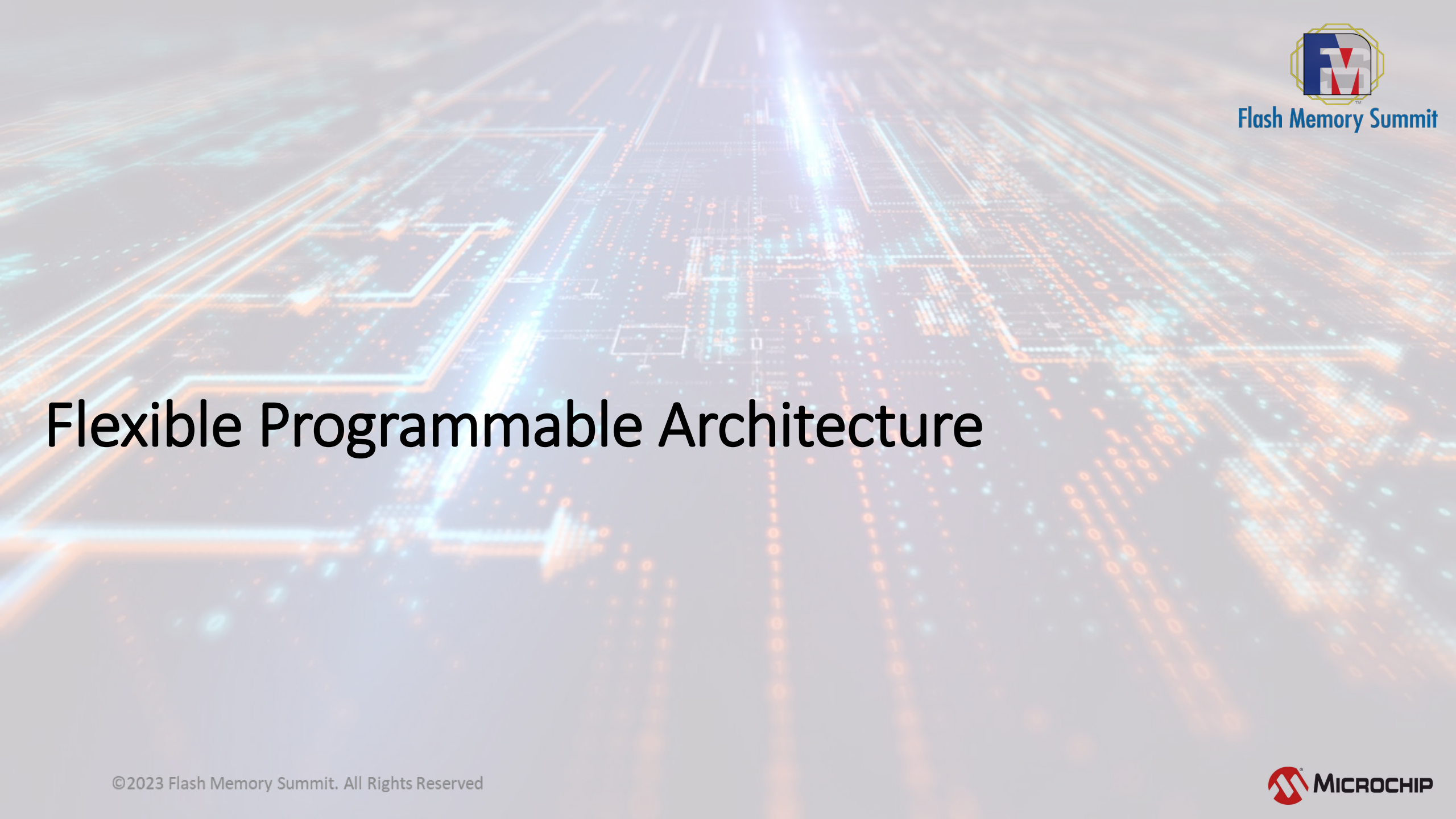

Flexible Programmable Architecture

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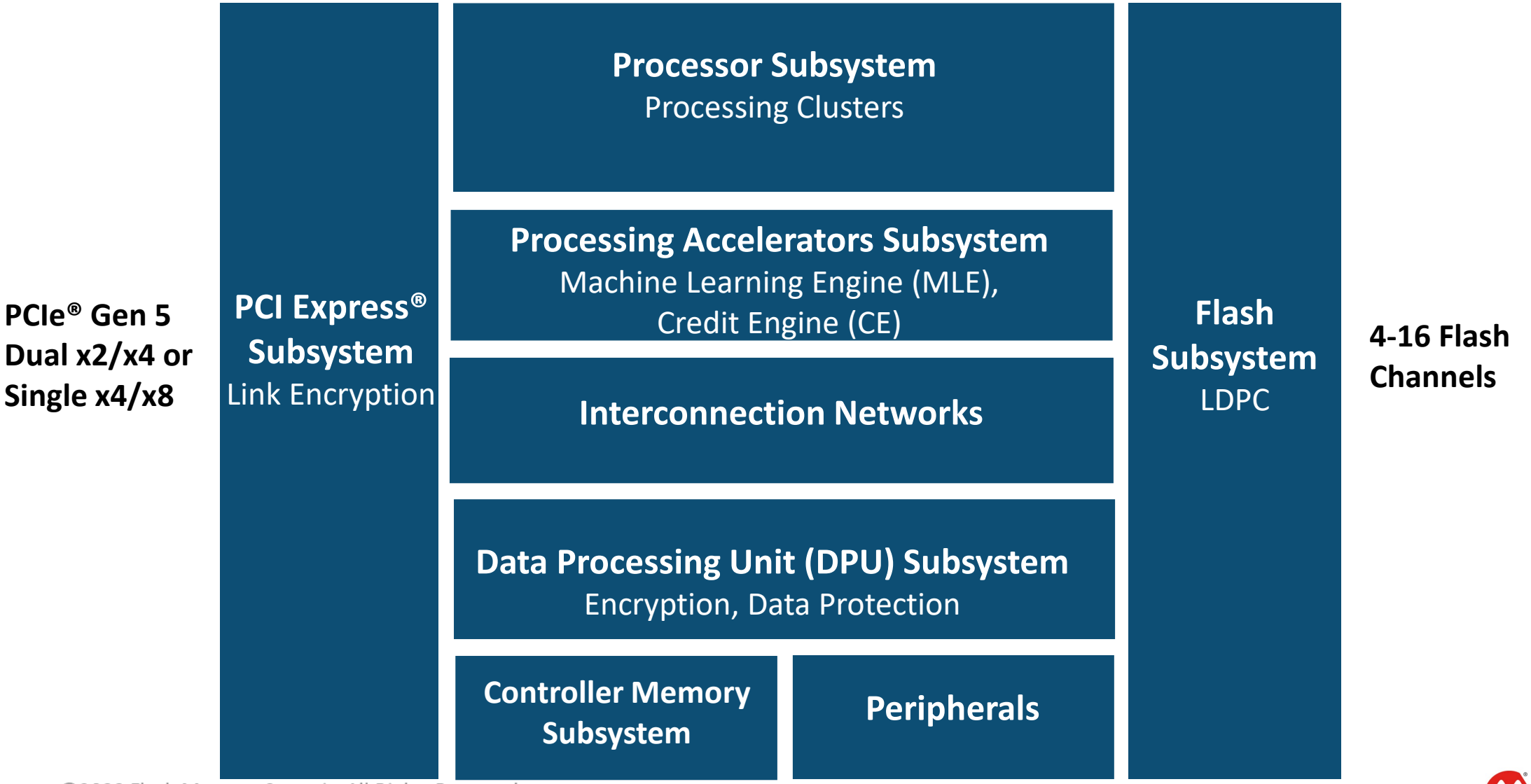
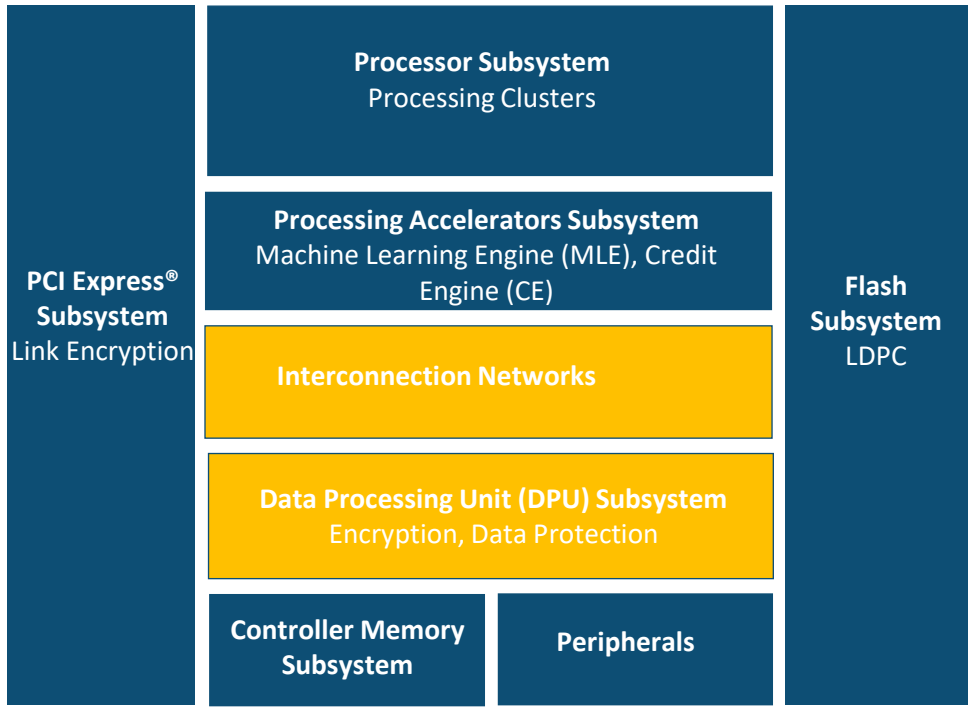
Flexible Flash Controller Architecture

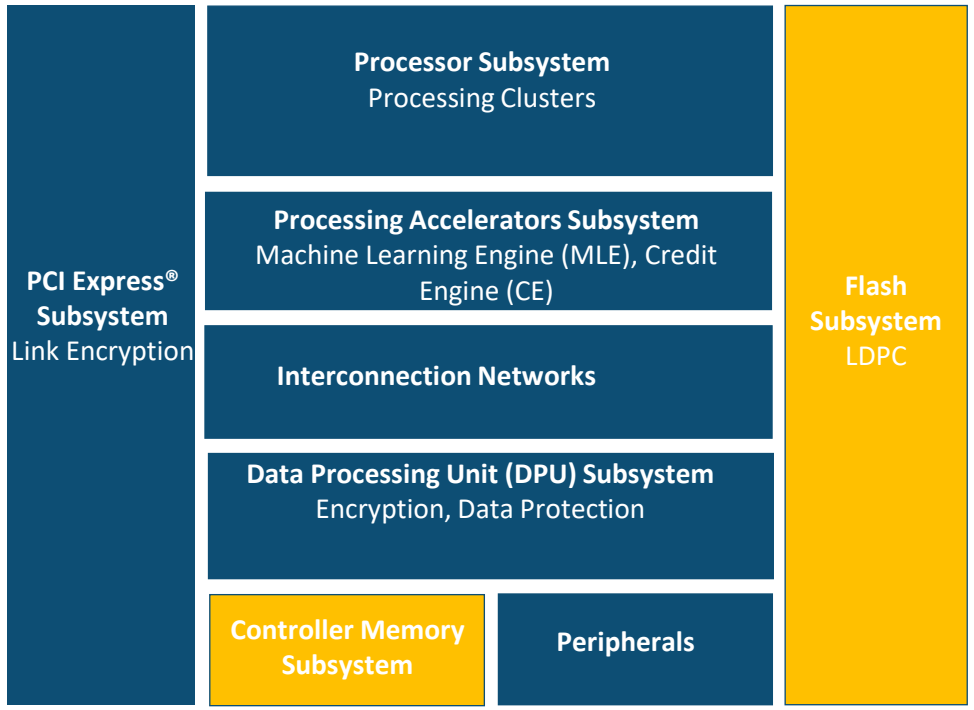


Performance



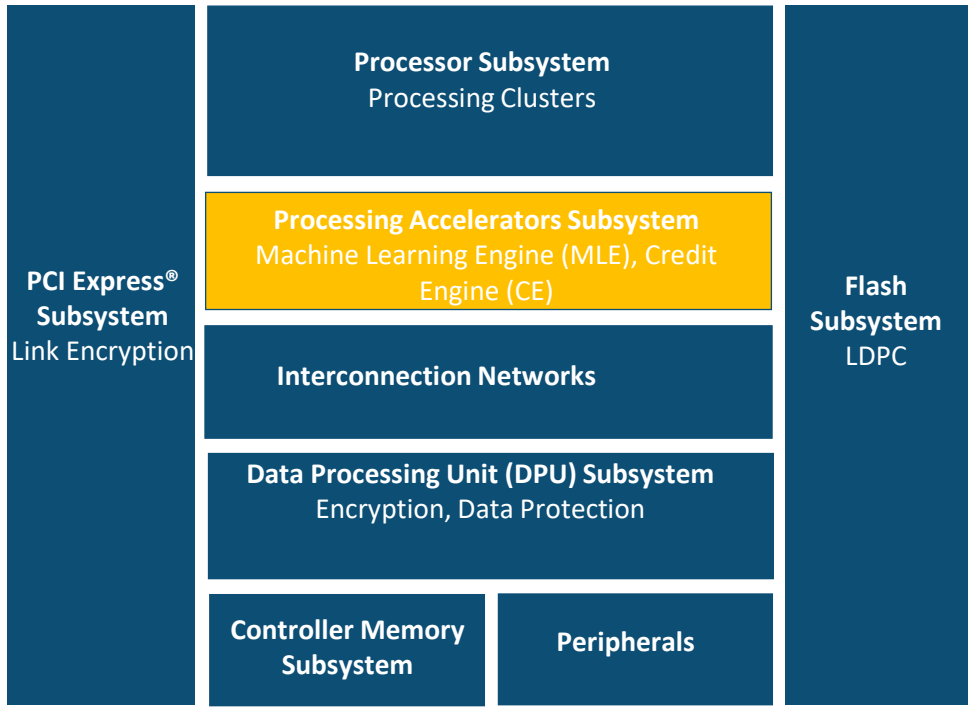
- For performance, optional NVMe® streams and key value features can be improved with data processing accelerator engines
- Architecture optimized for most commonly used IO sizes, such as 4K, 512 + protection bytes, etc.
- Cache coherent interconnection networks
  - Parallel operations among subsystems
- Higher number of queue pairs for scaling
- Optimized on-chip buffers and controller memory buffers
- Configurable options for achieving desired IOPS/Watt or GBPS/Watt

Amount of Data and Evolution of Flash, DDR



- Flash and DDR devices have gone through a lot of evolution to provide better density and faster performance to meet industry requirement
- Flash devices have evolved in terms of increase in the number of layers such as SLC, MLC, TLC and QLC and by adapting newer technologies such as 3D
- This limitation enforces a strong need to provide a flexible and more adaptable way to easily migrate to newer generation of NAND devices
- This flexibility can be achieved by limiting the control in the HW and enabling flexible programming architecture
- The flexible programming architecture means all the NAND commands are controlled by FW or a small piece of FW called a microcode

Solutions to Monitoring and Maintenance



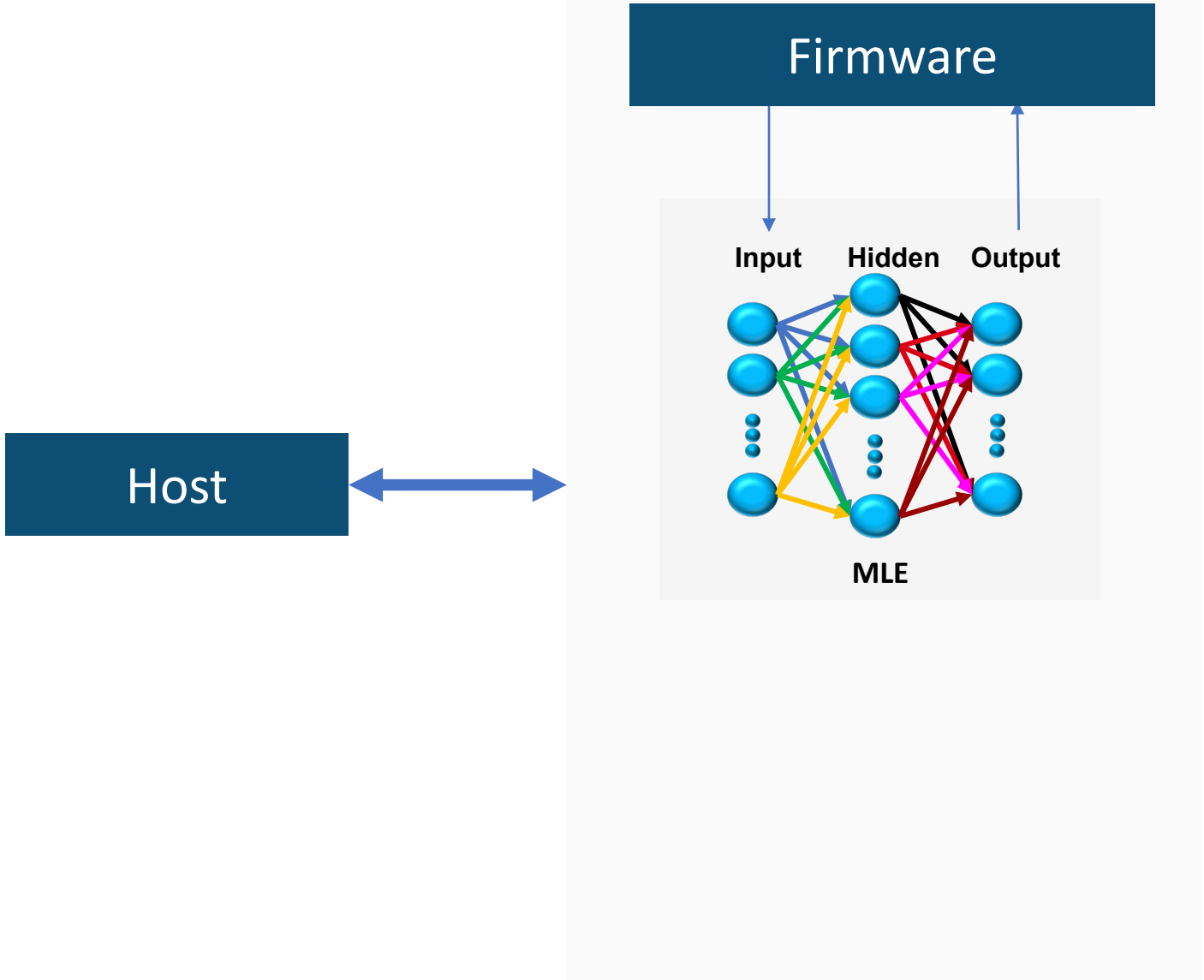
MLE and AI engines on the flash controller can be used for monitoring and maintenance

An MLE algorithm has potential to reduce BER on flash reads

- Top-tier enterprise SSD controllers already include MLE
- MLE total node count, depth, power optimization expected to grow in coming iterations
- MLE for order of magnitude drive BER reduction
- Flashtec® PCIe® Gen5 controller has an in-built application agnostic MLE engine

A credit engine can be used for managing arbitration of PCIe channels to optimize read and write performance as well as monitor minimal performance requirements.

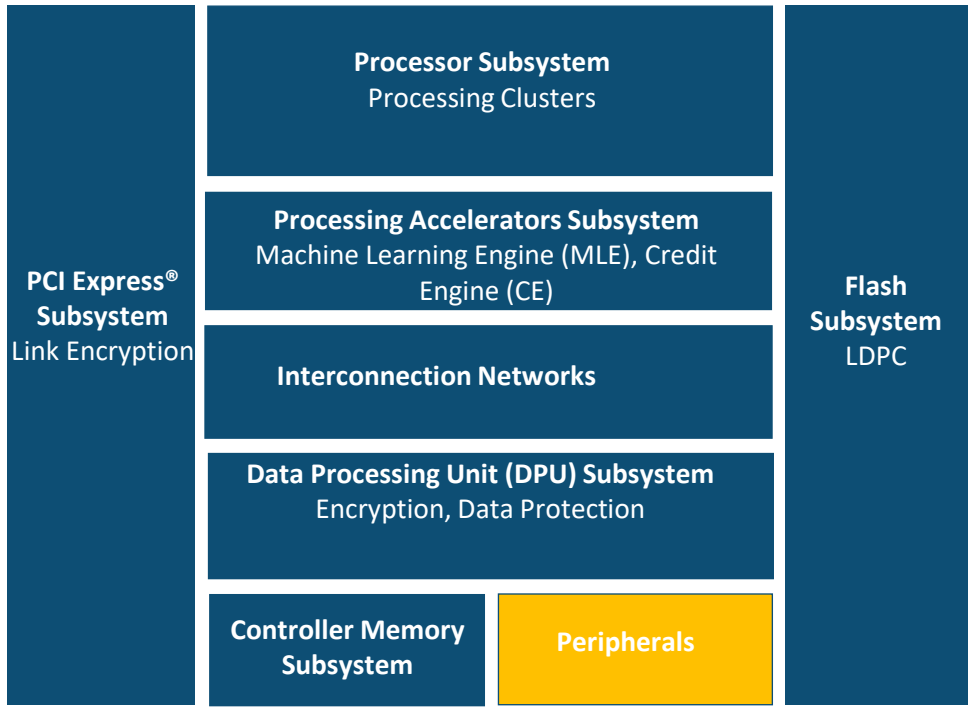
Flexible Machine Learning Engine Technology



Application Agnostic MLE

- Computational Storage
- Smart NAND Management
- Improved Performance
- QoS
- Many More

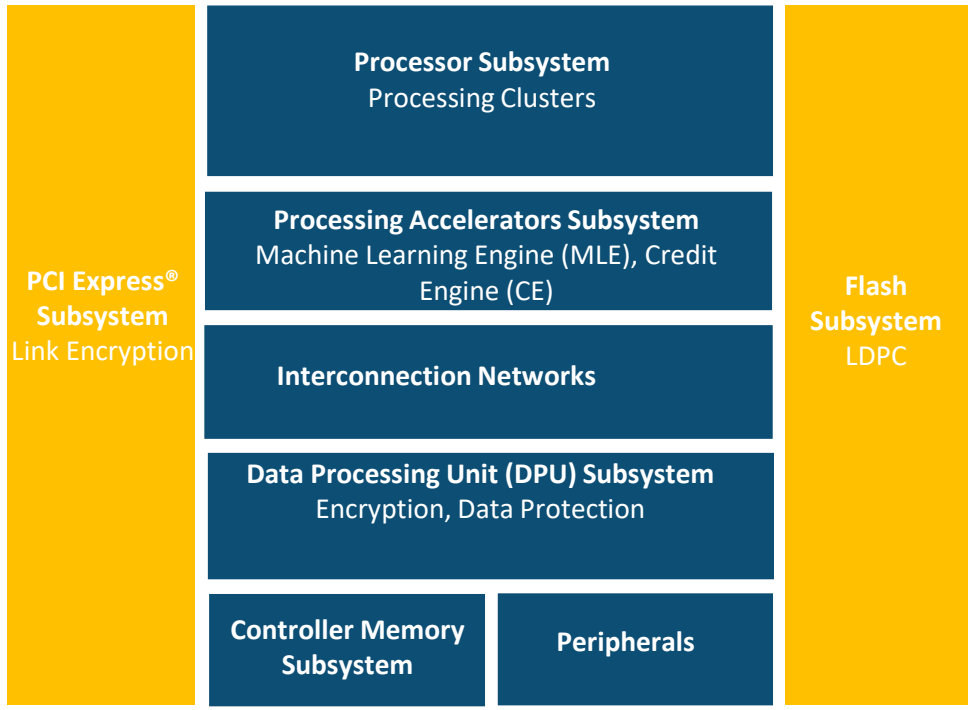
Solutions to Debug Capability



Flash controller can be architected such that:

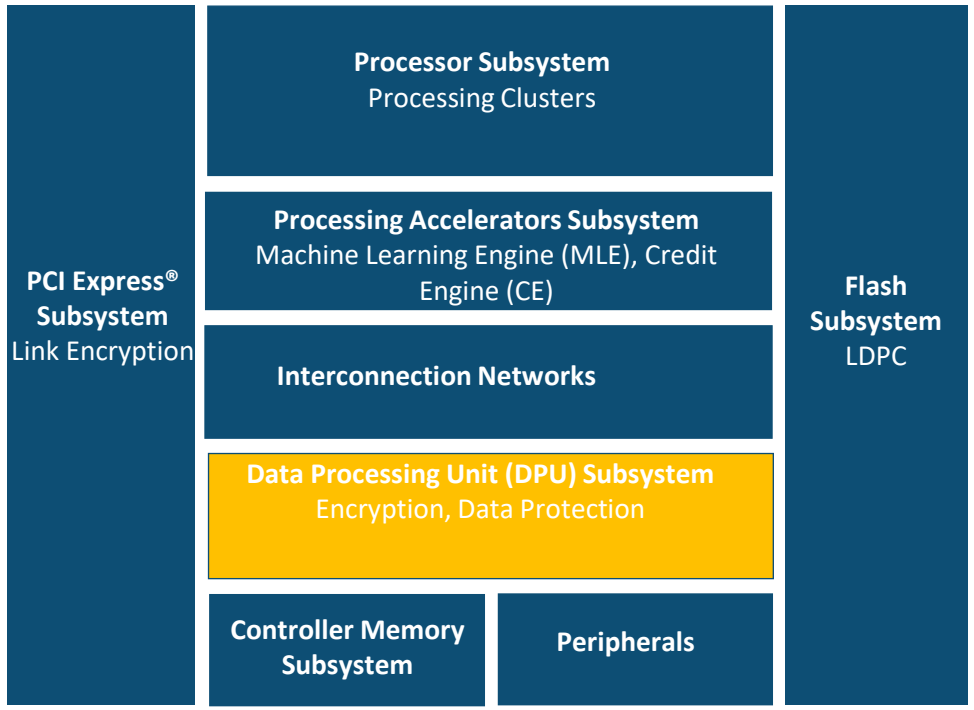
- Flash, PCIe®, or DDR (i.e., initialization, margining data) diagnostics are available to be collected in-field
- Security bits can be used to lock out debug interfaces
- Register status bits for major interfaces
- Debugging (software tool) to streamline process

Solutions to Interoperability



- Flexible hardware components can be architected
  - PCIe® analog front-end (serdes HW) controlled by FW to allow "tuning"
  - Lightweight microcontrollers to create custom commands to allow flexibility in changes to NAND protocol

Security Solutions



A flexible architecture can provide

- Single chip hardware root of trust
- FIPs140-3 level 2 compliance
- Provide one-time programmable bit fields to lock down interfaces after manufacture
- Instrument on controller an engine for cryptographic operations to speed up security processing

Conclusion

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Flexible Architecture

Visit Microchip at booth 419. Gen 5 SSD performance demo.