Application of Machine Learning for NAND Management in SSD

Presenter: Ramyakanth Edupuganti, Applications Engineering

Microchip Technology Inc.

Agenda

- Advanced NAND Management Challenges
- Valley Search Usage Model
- Example Valley Search Usage Model for NAND
- Using MLE for Vt Tuning
- MLE – Data Collection and Training Phase
- NAND BER Analysis

Advanced NAND Management Challenges

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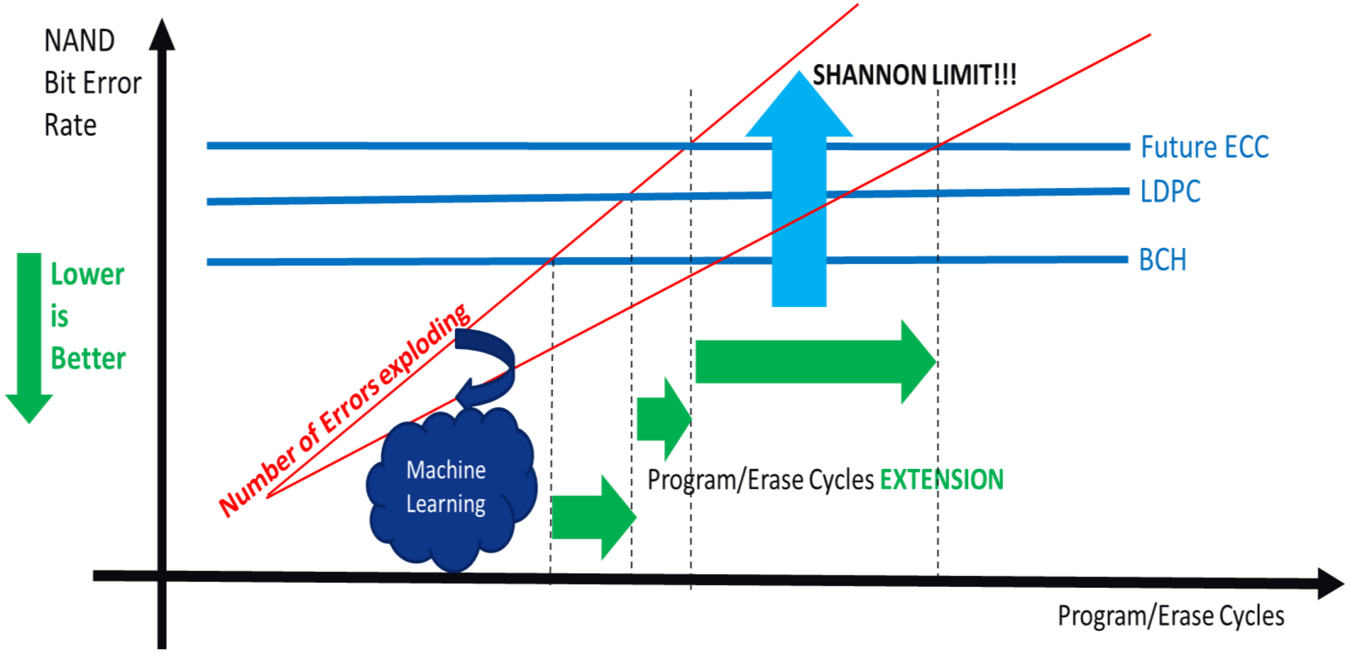
As NAND technology advances, effective NAND management is becoming challenging

- Layer count increasing
- New NAND technologies
- Number of bits/cell increasing



Need to improve error correction and develop techniques to reduce errors to take advantage of newer, denser and cost-efficient NAND

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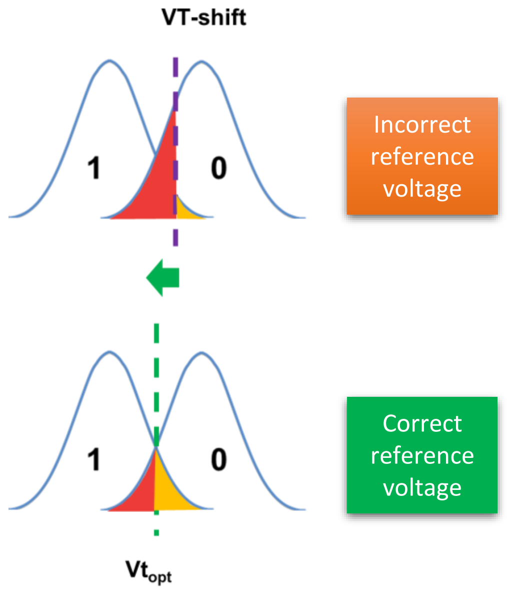
Increased NAND Layer Count

- Layer count increase means Bit Error Rate (BER) will increase
  - Most bit read errors are unrelated to physical damage
  - Read errors mostly due to tighter Vt distributions in denser cells
  - Need to retry the read with the correct reference voltage
  - A QLC-NAND (four bits per cell) may require up to 15 Vt reference voltages for 16 states to retry

- Vt Shift and read-retry based algorithms exist for error recovery Require extensive characterization to optimize
  - Trial and error based, less precise
  - Impact read bandwidth with background read overhead
  - Very challenging to optimize – the Vt distribution can change between every layer
  - NAND is at 128L today and growing

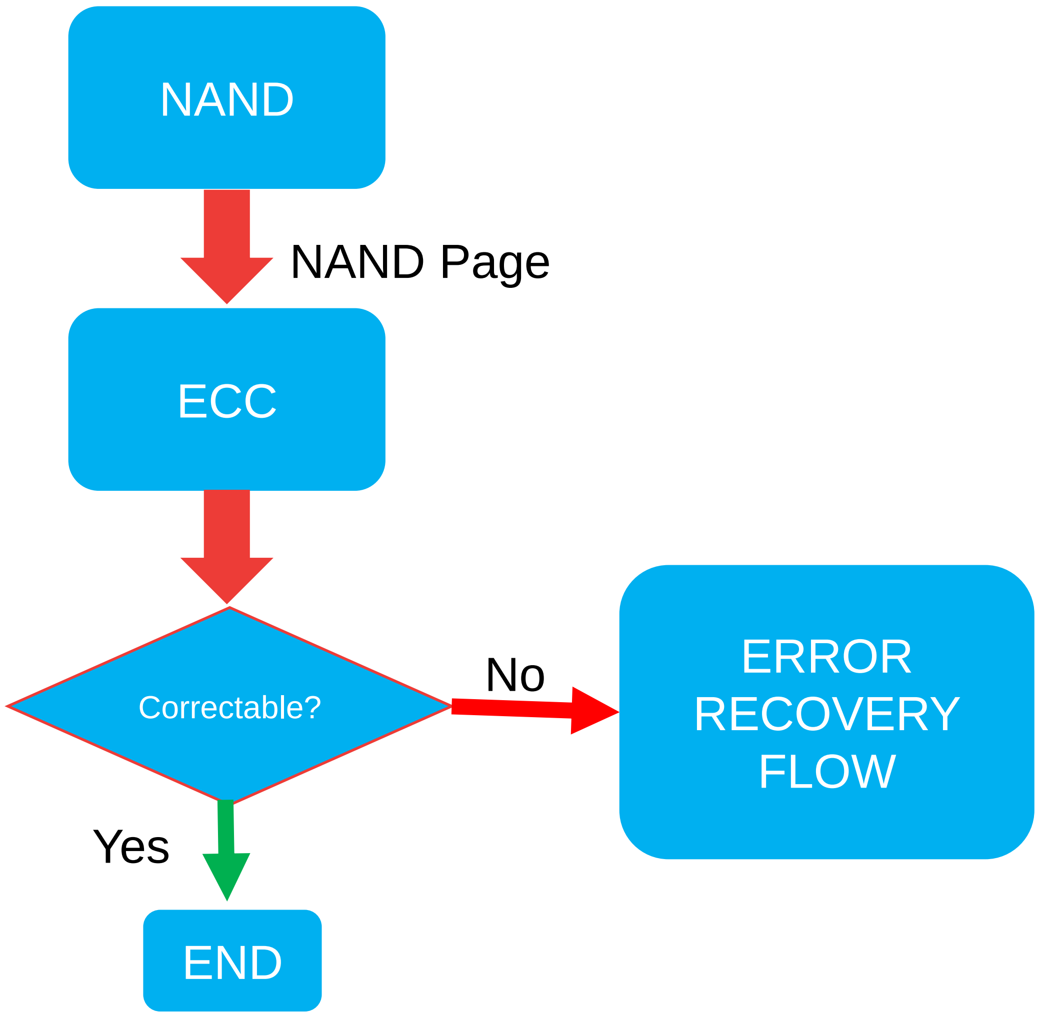
- Need a solution to optimize the Vt reference voltage and reduce correctable errors to improve read QoS



Increased Number of Bits per Cell

- Bits per cell increase means cell reliability will degrade faster
  - Errors occur when a ‘worn out’ block is accessed and firmware (FW) ECC fails to correct the block
  - Need to initiate soft correction and/or RAID operations to recover the user data
- NAND Block Program/Erase counters and retention times are some of the metrics used by FW to track NAND reliability state
  - FW structures don’t recognize if a block is “more sensitive” and wears out faster than expected – reactive only
  - All reliability states must be rebuilt if FW structures are corrupted before NAND access is enabled
  - Error correction overhead can impact bandwidth, latency and QoS
- Need a solution to measure and track the ‘effective’ reliability of each NAND block to optimize accesses with minimal error correction requirements

Existing Error Recovery Flow



- BER reduction
- Soft decoding
- RAID

Vt Reference Tuning Comparison with Existing Solutions

SOLUTION	DESCRIPTION	NAND CHAR EFFORT	QOS IMPACT	PRECISION	SCALABILITY (QLC, PLC, High Layer Count)
Read Retry	Defined by Flash vendors	High	High	Low	Low
Vt-shift	Custom Reference Voltages	High	High	Low	Low
BRP-like	Background Reference Positioning	Med	0	Good	Poor because of the background reads
Neural Network	VT Reference Tuning with Machine Learning	Med	0	Excellent	Excellent

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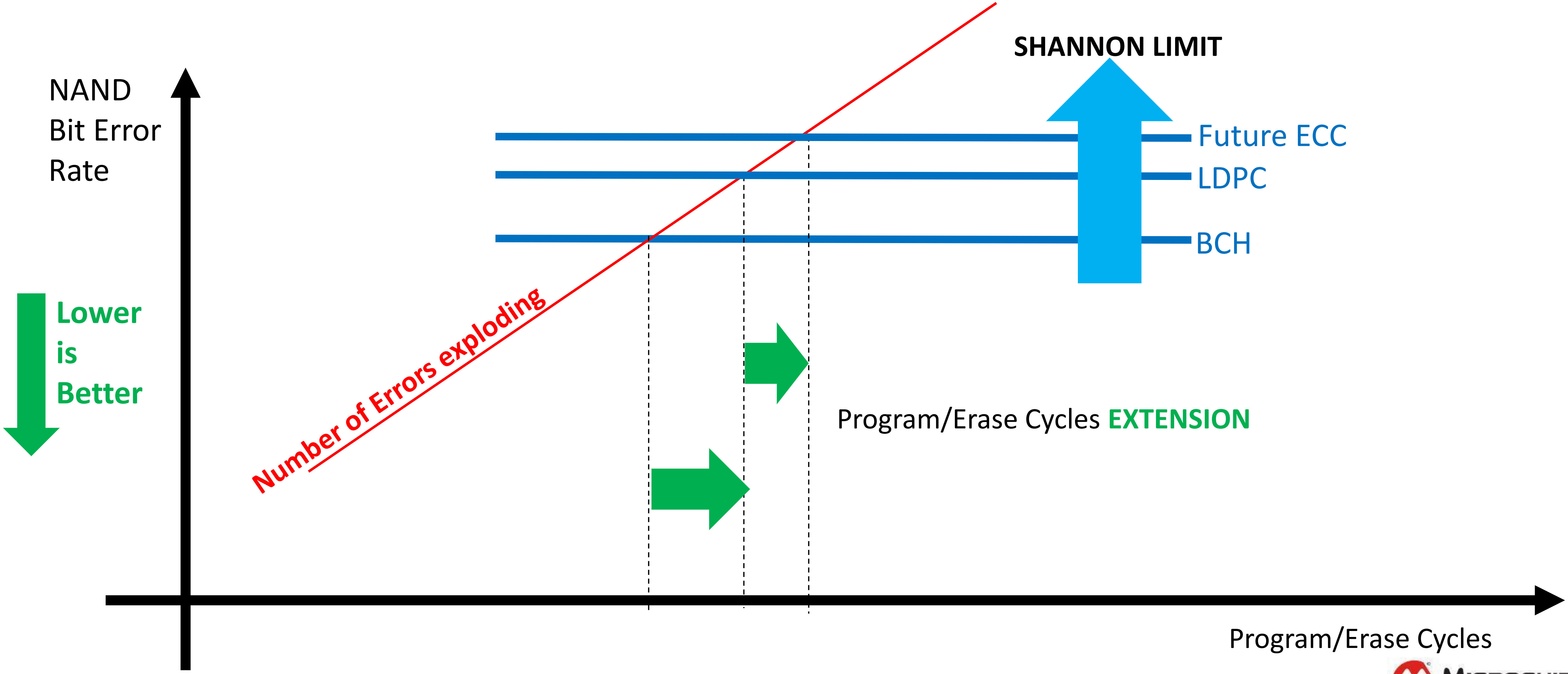
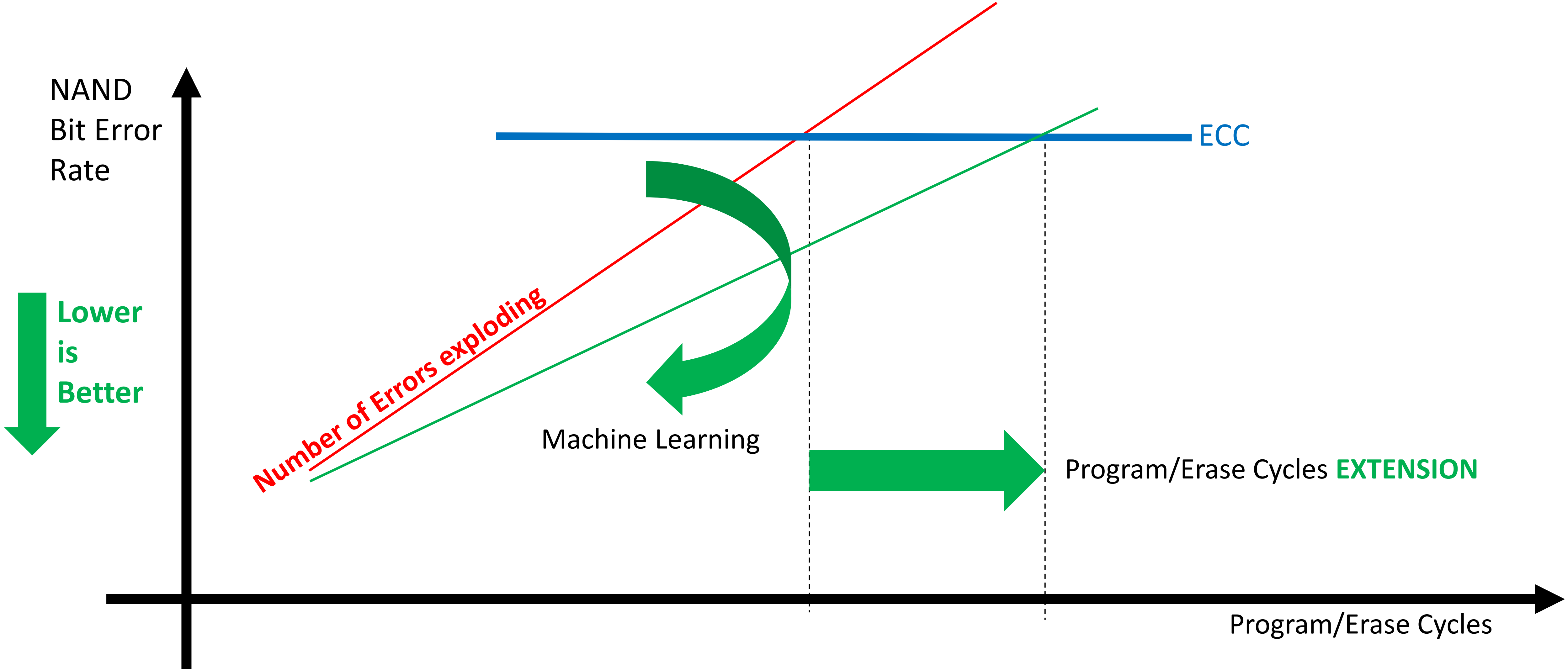
How to Address the NAND BER Increase
ECC

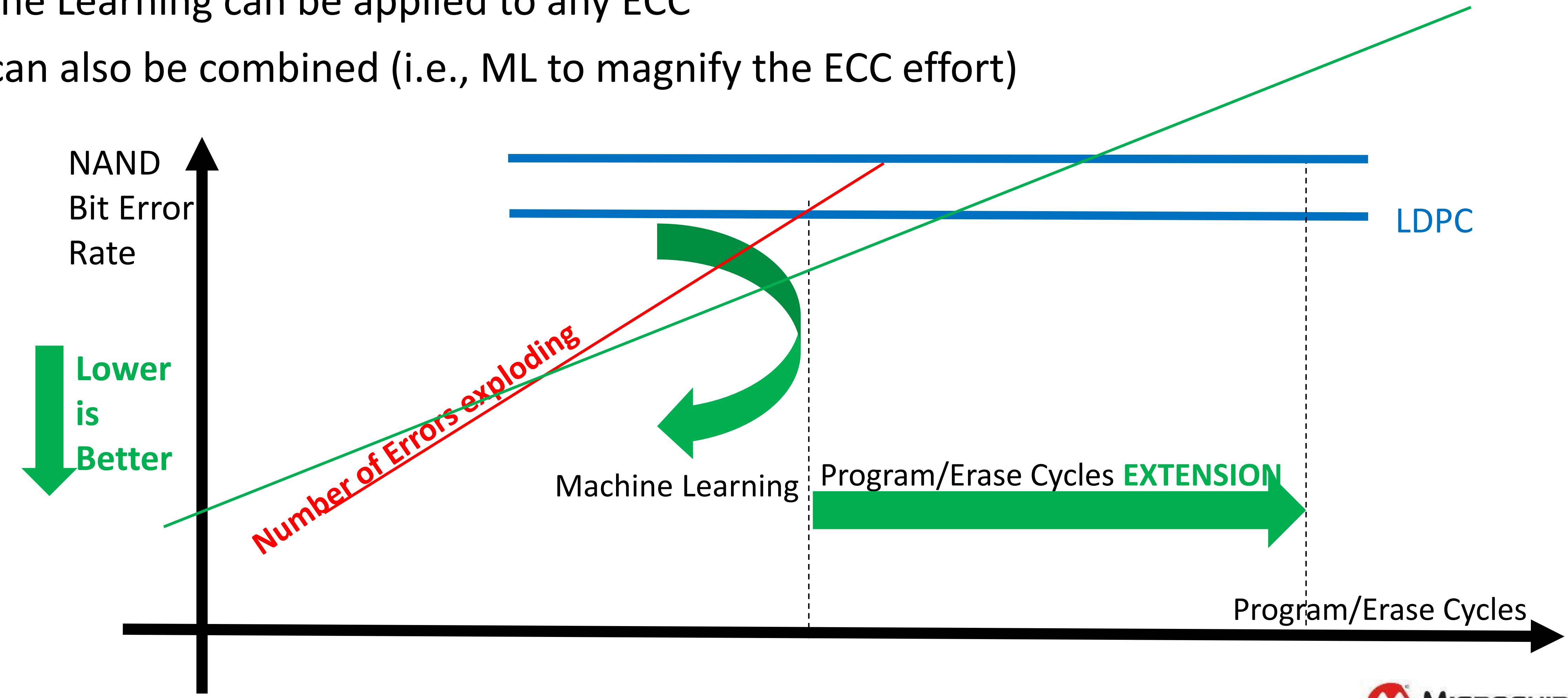


How to Address the NAND BER Increase
Machine Learning



Considerations

- Machine Learning and ECC are orthogonal to each other
- Machine Learning can be applied to any ECC
- They can also be combined (i.e., ML to magnify the ECC effort)



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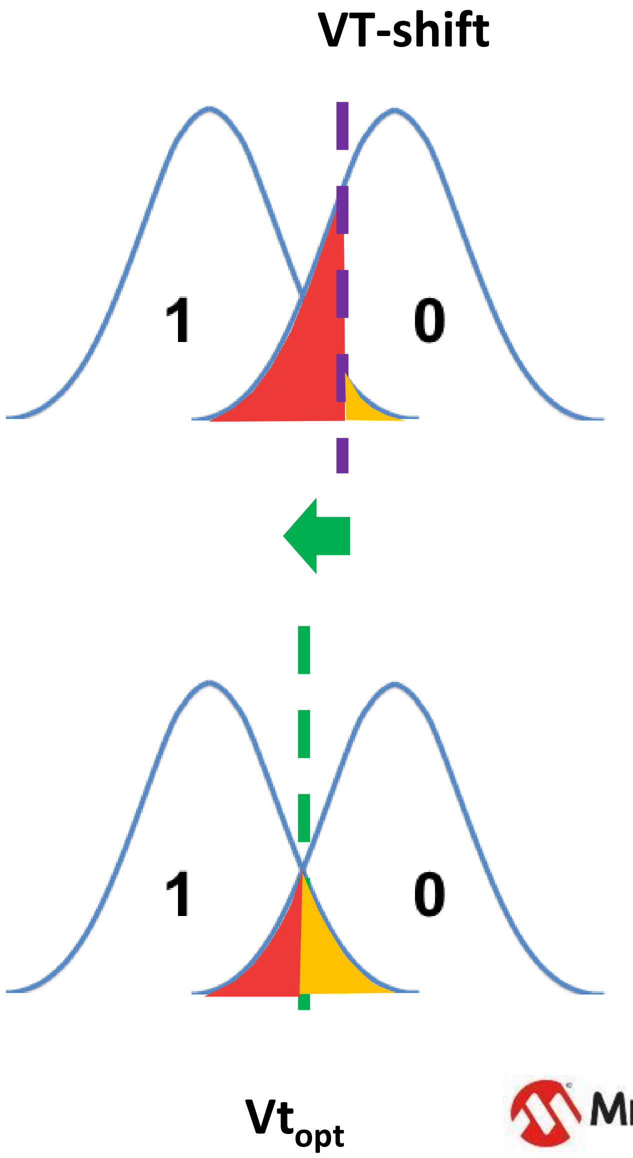
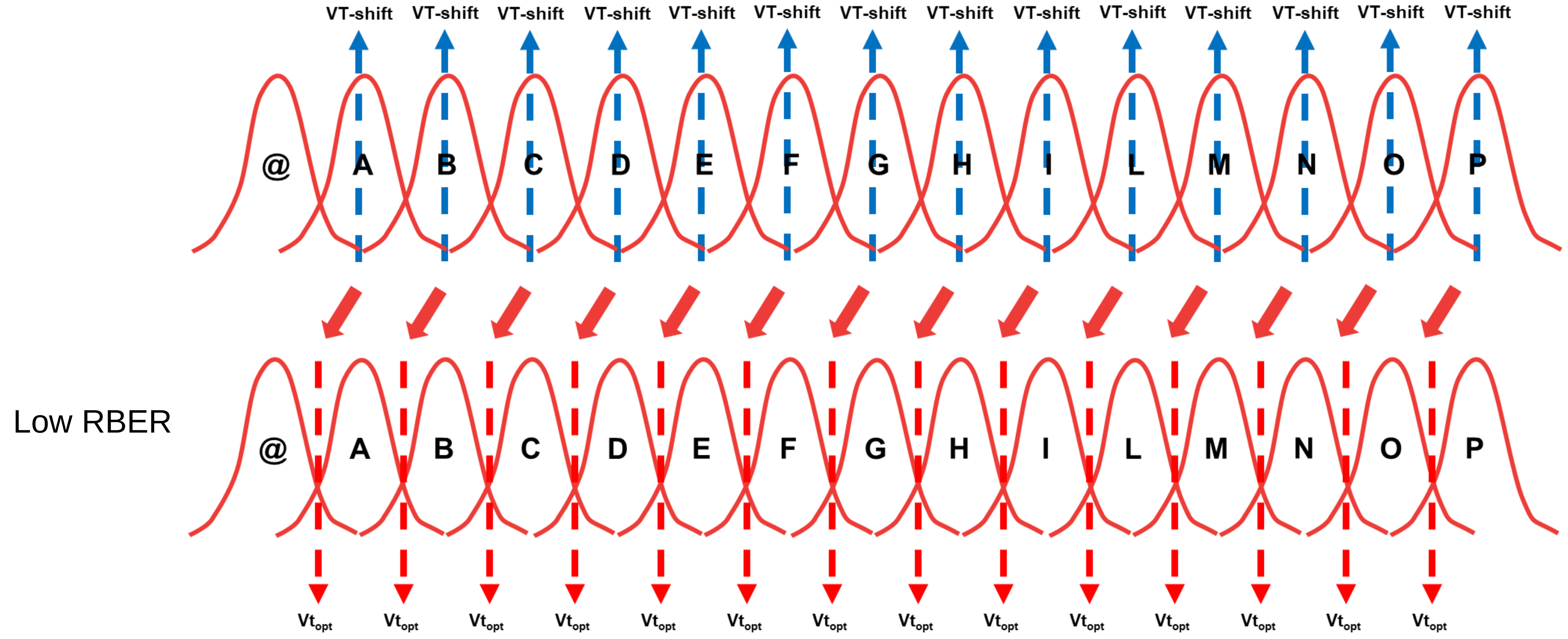
NAND RBER vs. Read Reference Voltage

- NAND raw BER is a function of PE, time, read disturb
- In 3D NAND most of the errors are recoverable;
- To minimize the RBER it is necessary to “center” the reference voltage
- Min RBER is when all the Reference Voltages (7 for TLC, 15 for QLC, 31 for PLC) are in the corresponding Vt_{opt}



Problem Statement

How to predict the best placement (Vt_{opt}) for each NAND reference voltage



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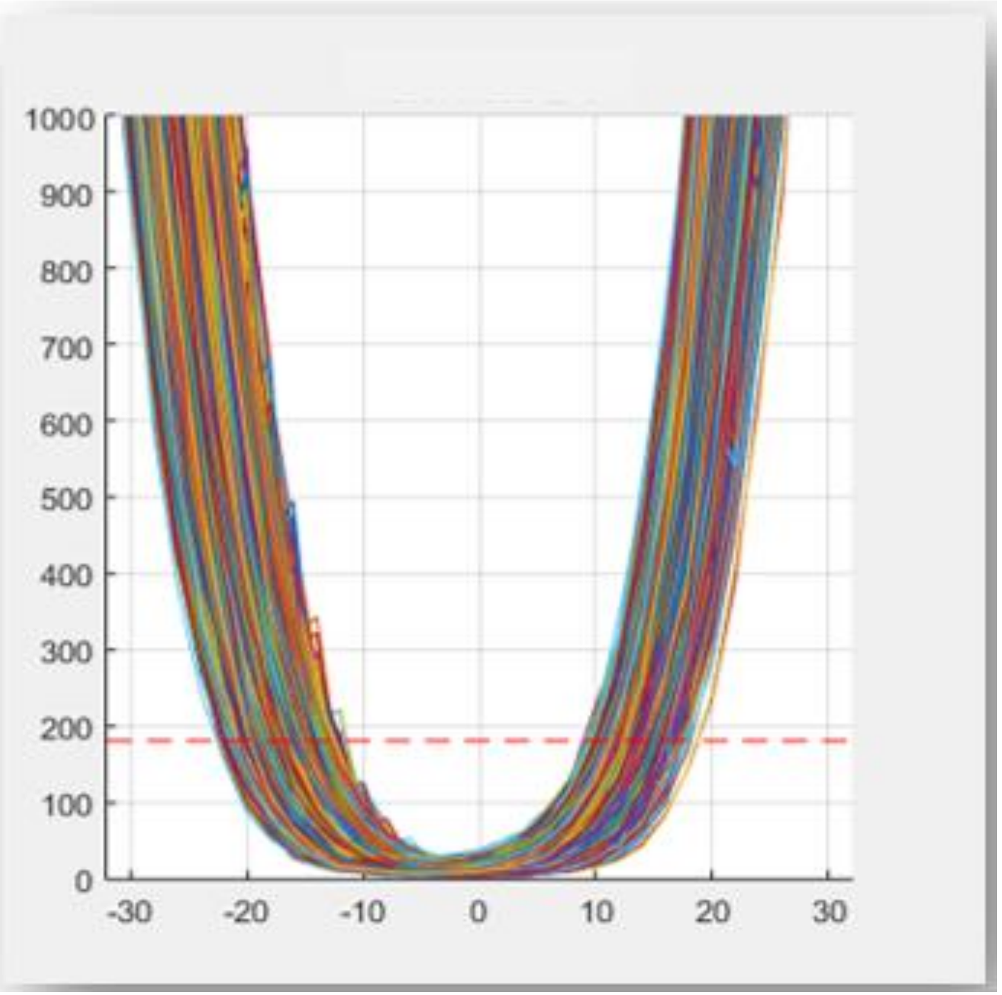
What is Vt Tuning Algorithm?

- Vt tuning algorithm uses small number of samples – error data(from 3 Vts) to rebuild continuous valley (9 Vts) and find lowest point of the valley that corresponds to Vt with smallest number of errors
- Vt tuning utilizes interaction between NAND management SW and MLE HW
- MLE HW is based on Neural Network (NN) and requires pre-trained NN models for operation
- Reliability states are defined based on endurance, retention and read disturb parameters

What is Vt Tuning Algorithm?



- Training phase
  - Pick three samples below the error threshold
  - The training is done on the target of (for example) 9 VTs
  - After the training you get the model
- Inference phase
  - Read the 3 VT samples, use the model, obtain the bottom of the parabola
  - From these numbers calculate the minimum values
  - The output are the minimum related VT and the second minimum VT

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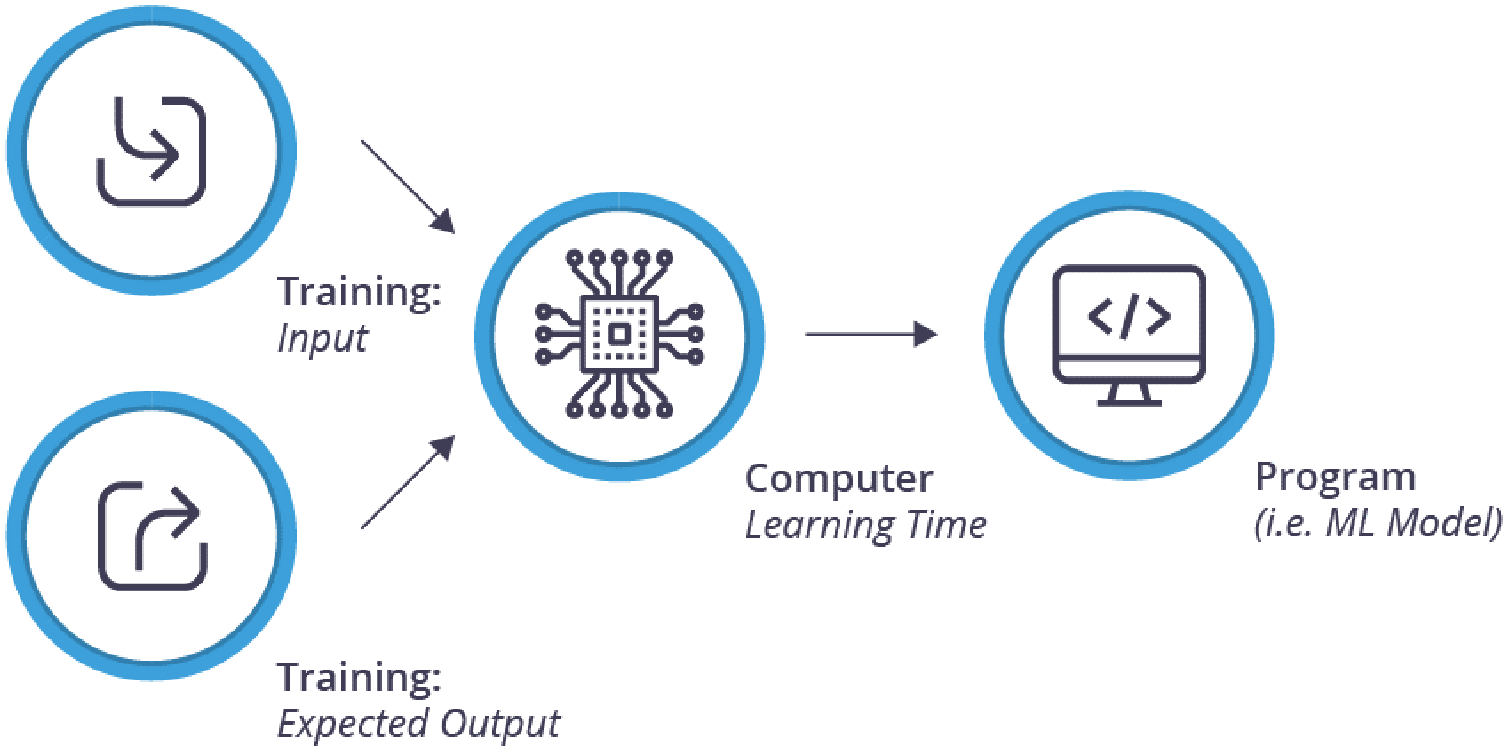
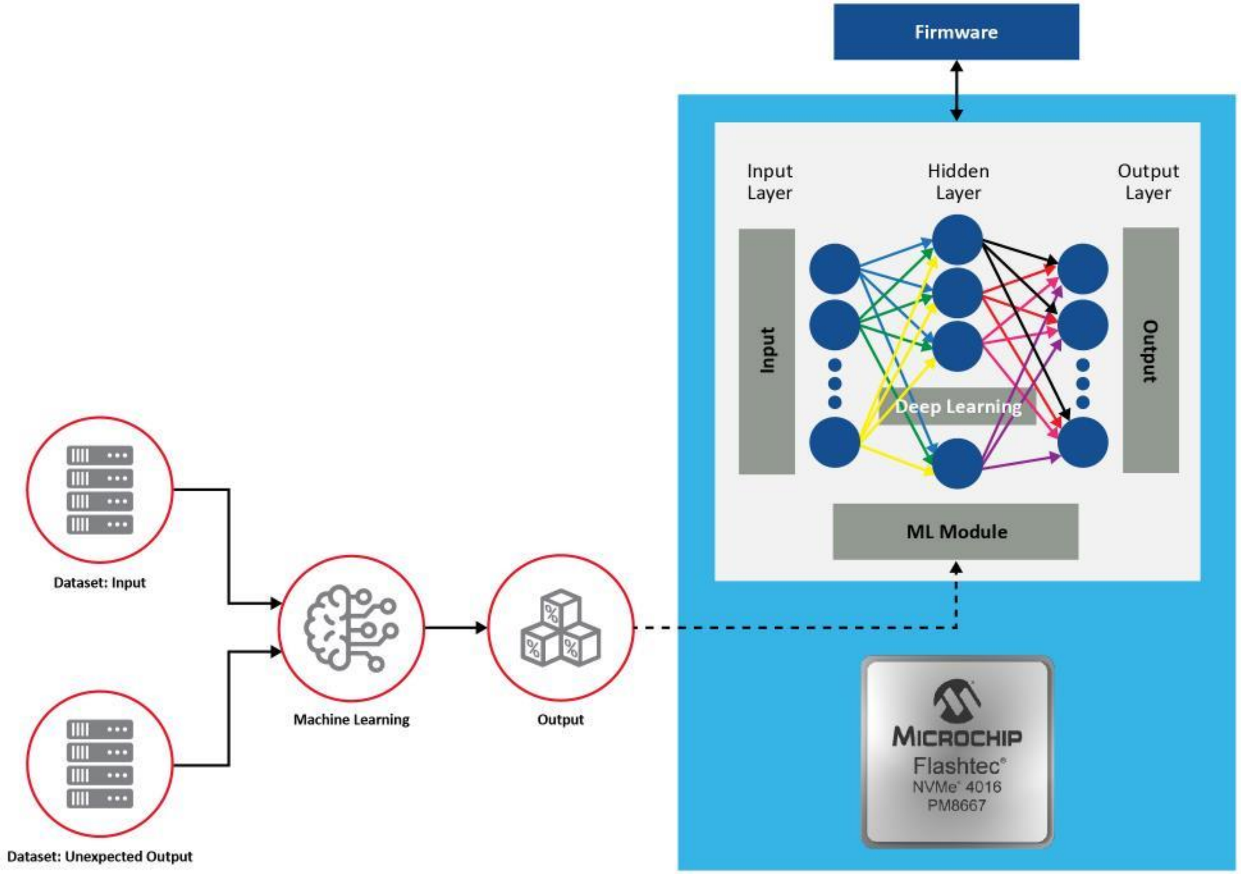
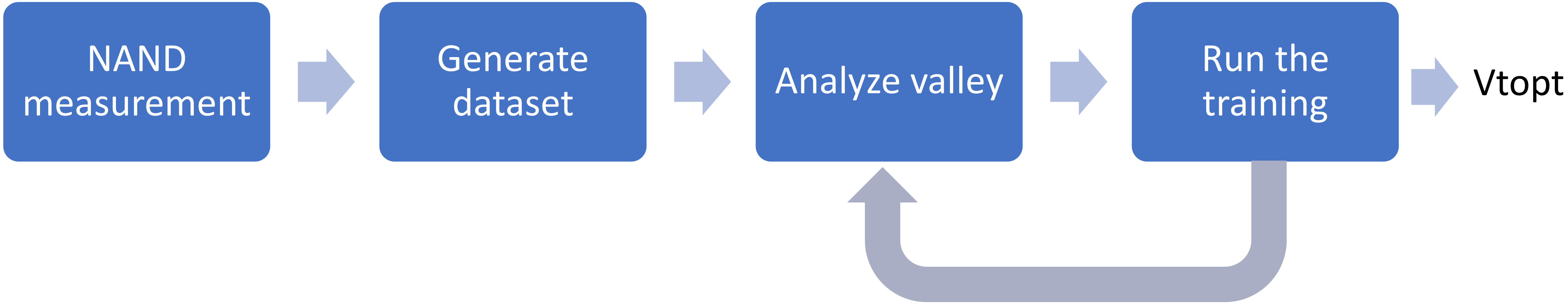
Neural Network Training



NVMe® SSD MLE Architecture Flashtec® NVMe® 4016



Data Collection and Training Phase Steps



Training Results

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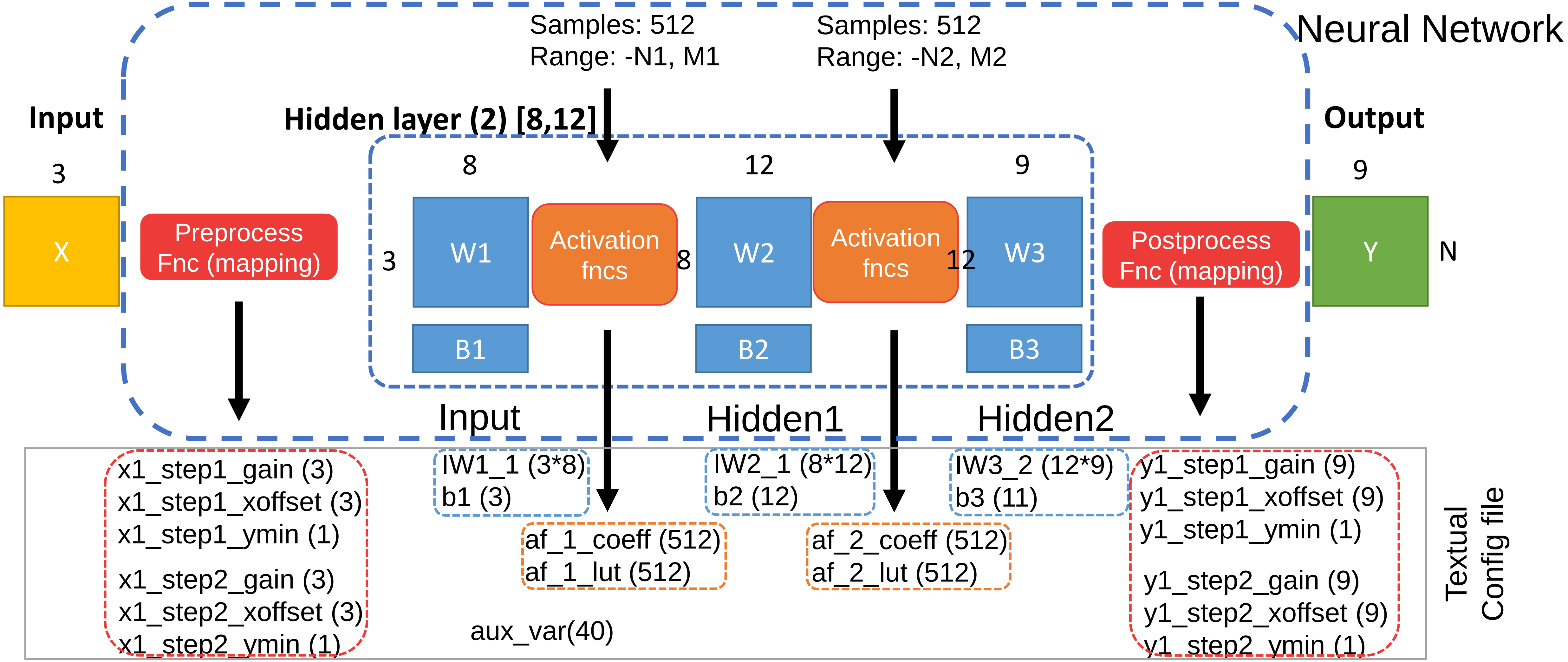

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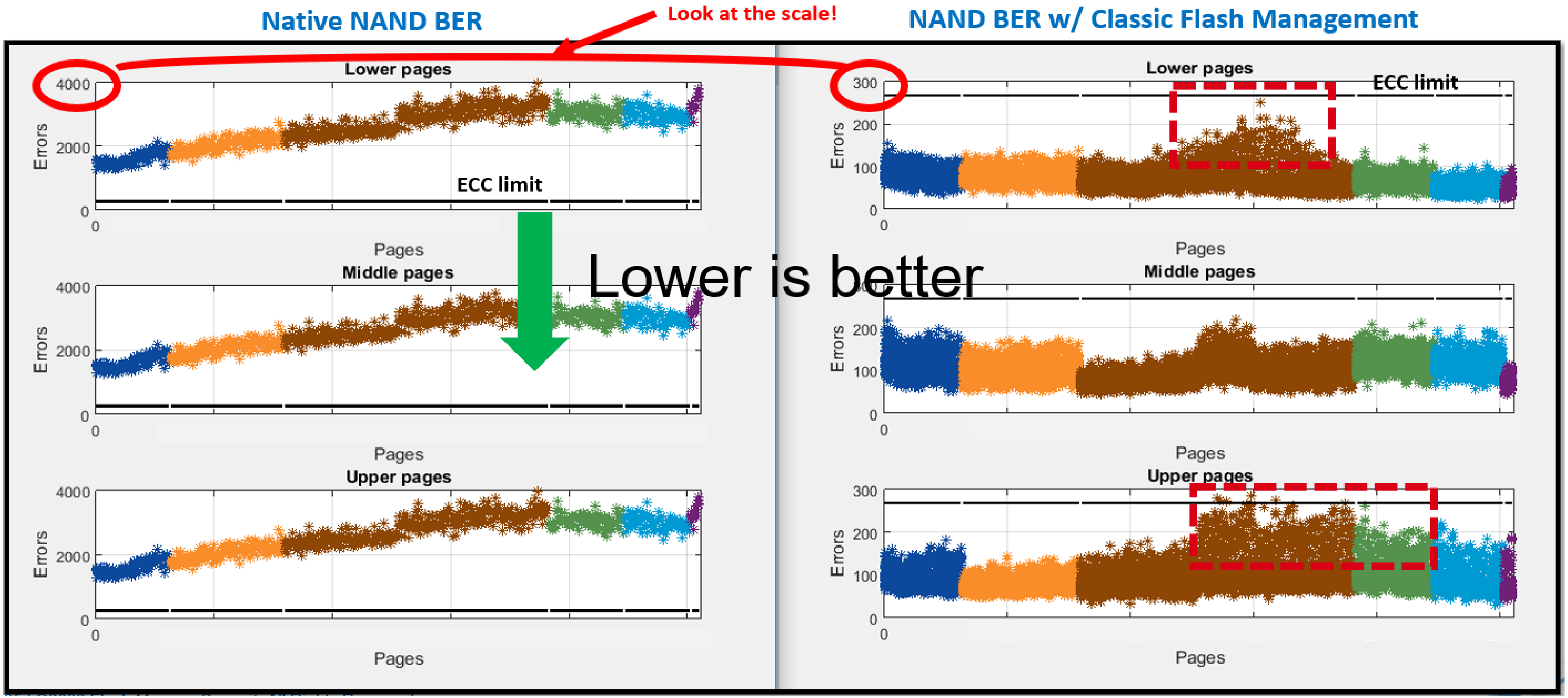
“Classic” Flash Management (BRP-Like)



NAND BER After Applying Machine Learning

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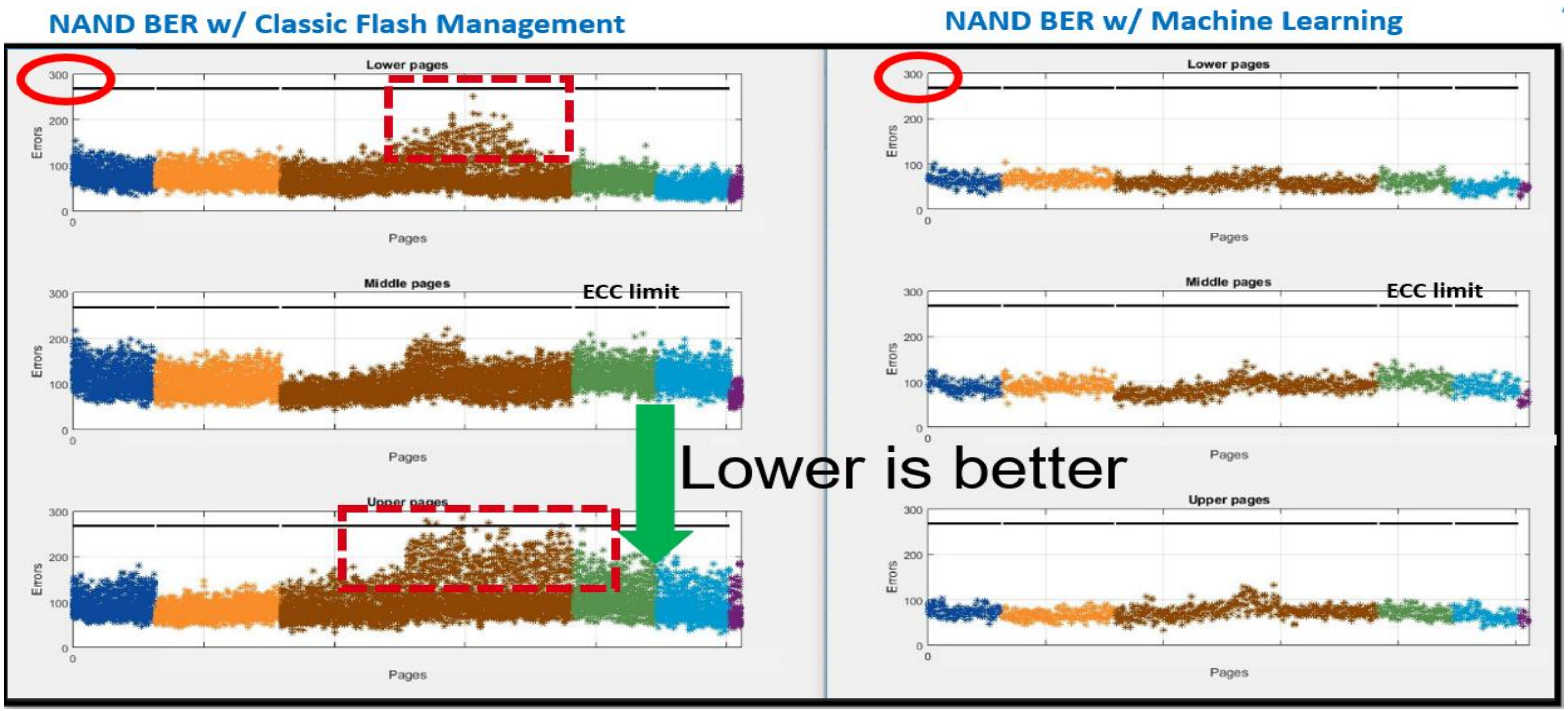

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