Memory & Flash Storage Resilience & Quality Future Directions

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Modern System Infrastructure Technology Priorities

Predict and Automate for Increased Decision Velocity

Decision velocity means having real-time insights on real-time data in every transaction, all the time

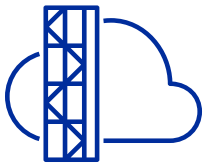
- in-transaction AI inferencing at the speed and scale
- Exponential increase in AI model size – driving memory & storage capacity, Bandwidth

Resilient & Secure System

Plan and mitigate risk of potential future outages – IBM Z 99.99999% resilience

E2E Security for enterprise Cloud – full stack encryption, Quantum-safe protection

Address ever-increasing regulations with automation for compliance



Modernize with Hybrid Cloud

Empower developers with agile DevOps to accelerate modernization of existing workloads

Cloud Modernization Stack providing flexible and integrated platform to support infrastructure automation, application and data modernization

Infrastructure Technology & Quality – Driving Forces

Flash Memory Summit

Performance

Si scaling, Heterogeneous integration, Low latency Thruput

AI inferencing & training acceleration

Bandwidth – Memory, PCIe Gen5/6

Density

Memory, Storage, Tape Capacity
I/O density

Quality & System Resilience

E2E Supplier Quality

Systems RAS

Supply Chain Resilience

Component design

Geo Political factors

Sustainability

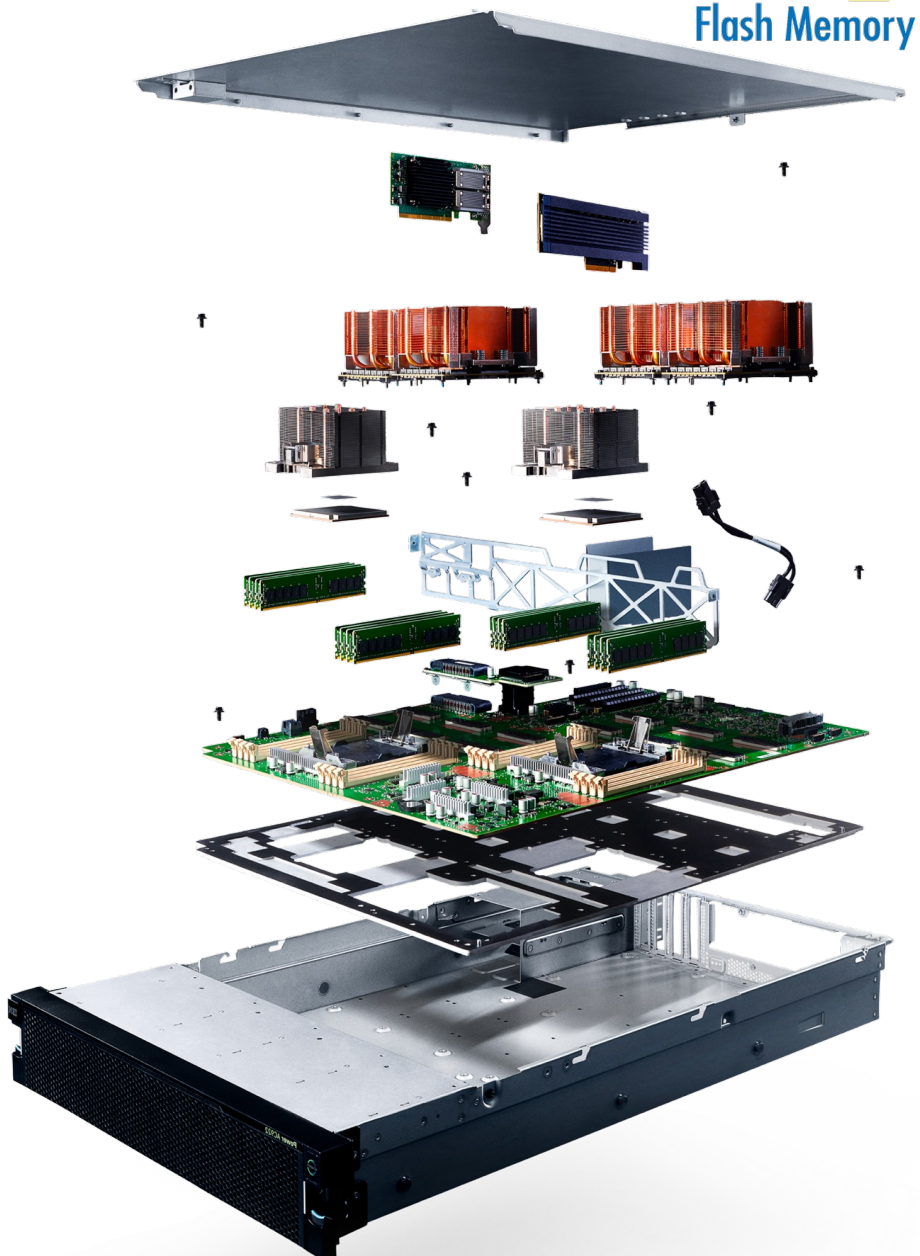
Energy & Carbon Footprint, TCO

Cost

$/GB Semiconductor scaling

Component & Subsystem Commonality

CXL Disaggregated infrastructure



AI driving IT infrastructure transformation

Flash Memory Summit

Memory

- Foundation models & Generative AI – Large Neural network enabling business automation everywhere
- Memory with high capacity & BW is necessary to enable exponential increase in AI inferencing and training model size
  - Computation intensive workloads performing complex calculations
  - Data-intensive workloads associated with AI & ML – data movement within the systems from the main memory to computational elements is a large portion of the latency & energy consumption.
- Higher Performance Computing (HPC) – keeping computational engines fed with instructions and data requires immense bandwidth from main memory. Maximizing memory bandwidth and minimizing memory energy is critical
- CXL enables efficient memory data movement and cost (low cost DRAM vs RAS features)

Flash Storage

- Increasing AI, Big Data analytics, Database applications and lower TCO enabled by flash storage
- AI is the fastest growing application in Data Centers – “More Data”, “FASTER”
- AI/ML applications require vast amounts of Low Latency, High IOPS, High Thruput Flash Storage at Low TCO. ML driving QLC adaptation (5000:1 read to write ratio, improving decision making capabilities w/out needing human intervention)
- 3D-NAND scaling, TLC>QLC and Computational Storage are key enabling technologies
- Cloud vs Edge processing, critical business decision => enabled by Flash Technology

Infrastructure System Resilience & Quality

- ITICs 2022 Hourly Cost of Downtime survey indicates single hour of server downtime costs exceed one million ($1M) to over five million ($5M).
- Downtime is disruptive and expensive. It can also irreparably damage a company's reputation.
- In extreme cases, business and monetary losses as a result of unreliable servers can cause the company to go out of business due to sustained losses and possible litigation in the wake of a particularly severe or prolonged outage from unreliable hardware, natural disasters or a targeted security incident like a ransomware attack
- Memory & Storage subsystem quality is important to understand from a DRAM & Flash Si scaling – defect mechanism vs system RAS mitigation standpoint

Service Downtime Impact & Memory Problem Portion

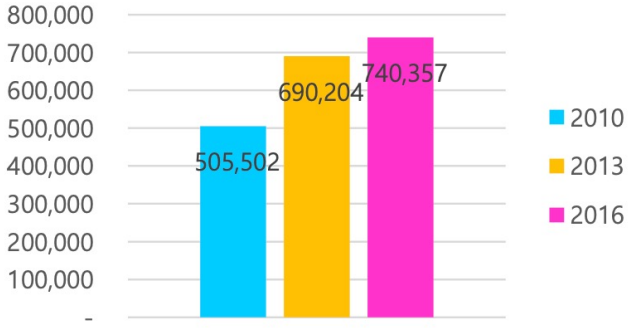


Fig.1 Mean downtime Cost for Data Center

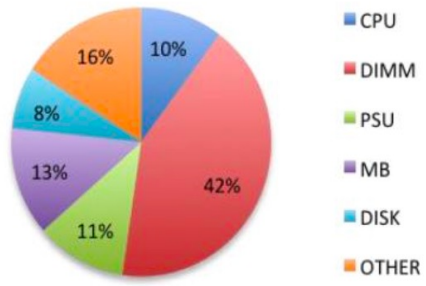
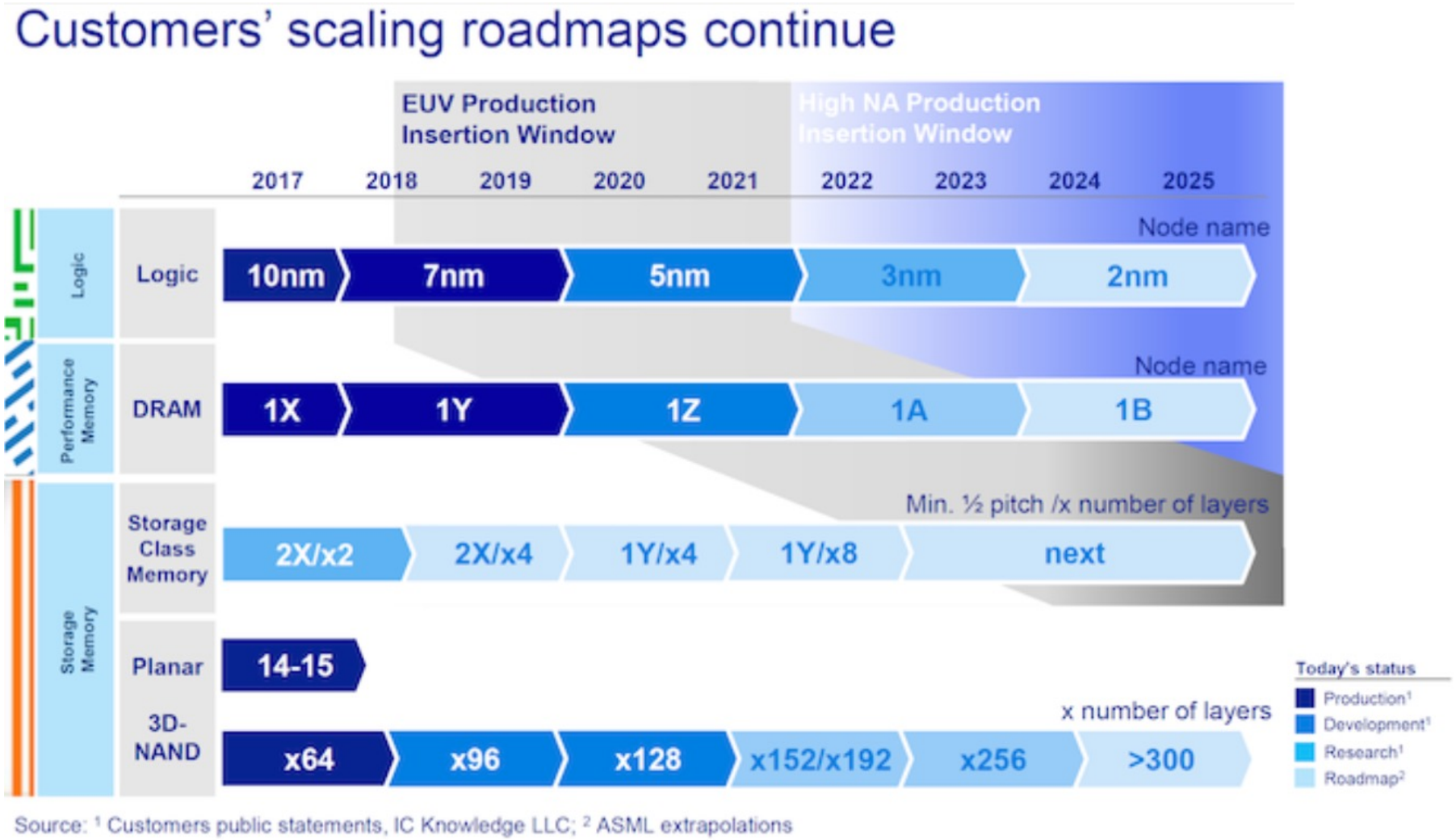


Fig.2 Top 5 hardware components failure ranking in Baidu's datacenter Year 2019

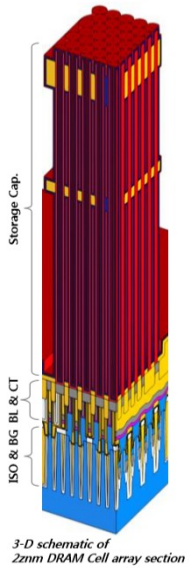
Source: ITIC 2022

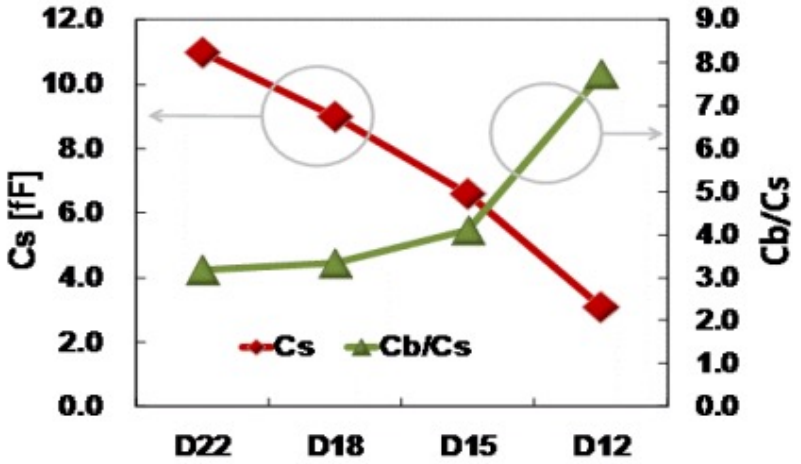
Semiconductor Technology Scaling



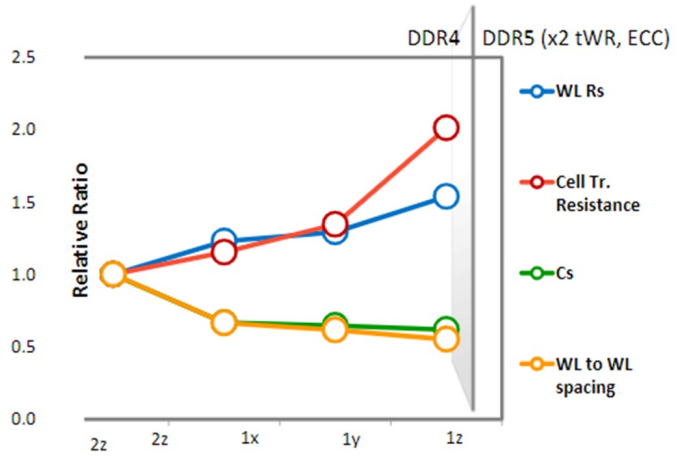
Source: ASML

DRAM Scaling challenges & quality implications





Hwang, Y., Park, J., Jin, G.Y., & Chung, C. (2012). An Overview and Future Challenges of High Density DRAM for 20 nm and Beyond.



Source: SKHynix

- Cell capacitor (Cs) decreasing with smaller dimension of capacitor
- AR (Aspect Ratio) of physical cell capacitor increased to boost capacitance
- high K dielectric material innovation

- Retention time decreases with Cs reduction and leakage current increase
- Main source of leakage current is GIDL and Junction Leakage

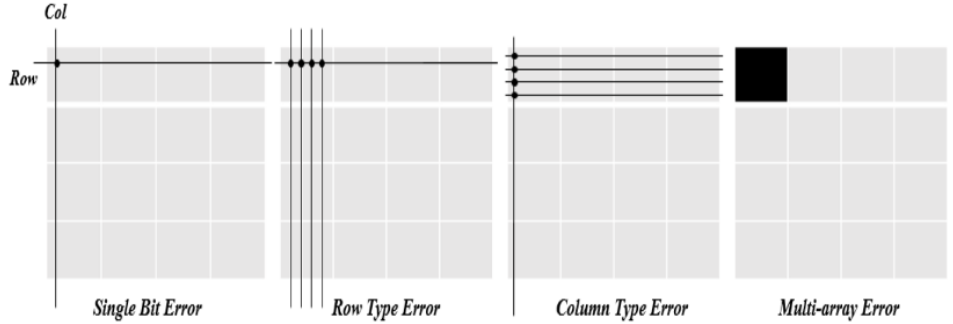
$$t_{ref} \propto \frac{Cell\ Capacitance}{I_{leakage}}$$

- WL resistance, Cell transistor resistance increase slows down the operation of DRAM due to RC delay
- Limited WL to WL spacing – row hammer
- Vth variation driven by Short Channel Effect

DRAM Quality & Reliability - Mechanisms

In addition to DRAM scaling related Refresh, Sensing Margin, tWR fail modes, focus required to below reliability mechanisms

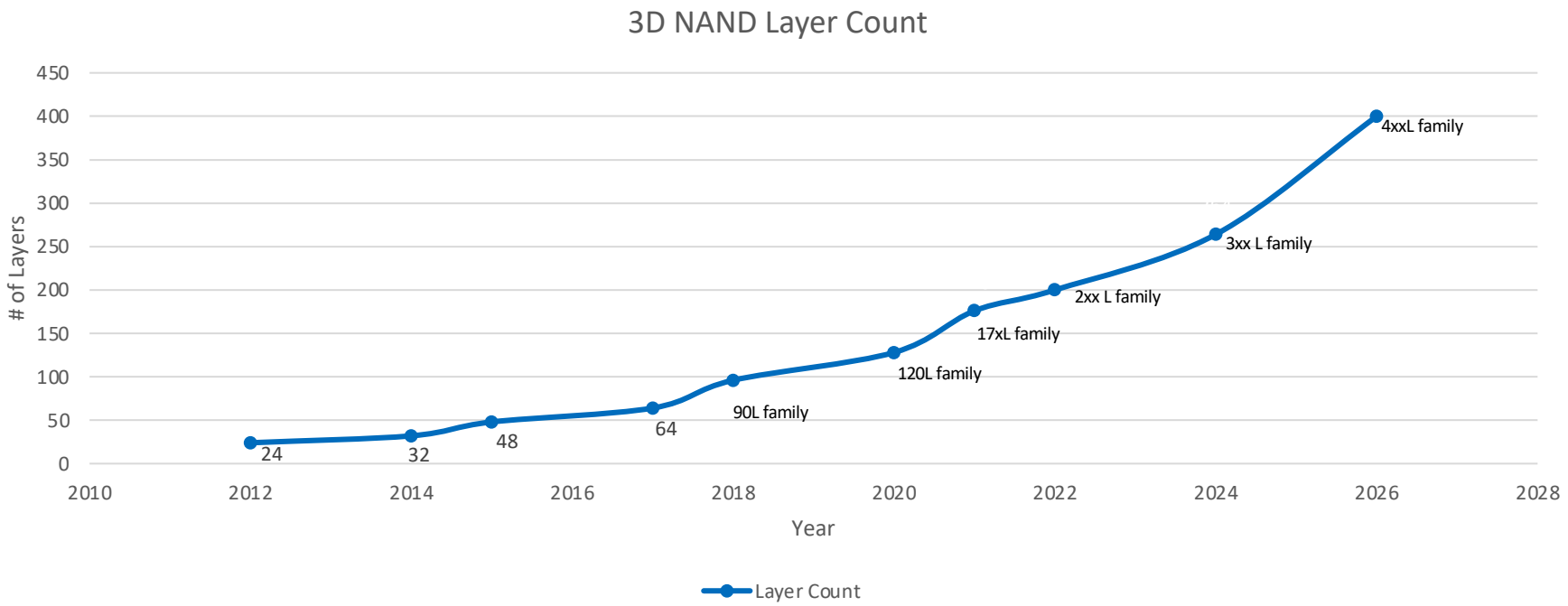
1. **Gate Oxide Integrity** – fab process control, wafer parametric & final test, package test, Burn-in acceleration
2. **Contact integrity** – bottom of contact reaction, dislocation formation, alignment accuracy
3. **Row/Column/Block fail mechanisms** – mostly early life fail nature, due to process margins and/or particle control
4. **VRT (variable retention time)** – related to charge trap or crystalline defects at gate oxide/drain interface
   - Cell refresh has RTN (Random Telegraph Noise) characteristics, 2 leakage rates
   - Temperature & mechanical stress alters 'Trap states' => post solder fuse repairs of VRT bits
5. **Row Hammer** – aggressor row affects the charge of neighbor 'Victim' rows via parasitic capacitive coupling
   - Continued degradation with DRAM scaling
   - In-DRAM design counter logic – victim row refreshed to avoid data corruption
6. **Hot Electron/Chisel mechanism**
   - Early Reliability Assessment via accelerated Wafer Level Reliability test key for sub 1z nm DRAM nodes
7. **Soft Errors** – Alpha particles, thermal neutron inducing single bit errors
8. **PMIC** – voltage margins, Hot electron, Time dependent dielectric breakdown

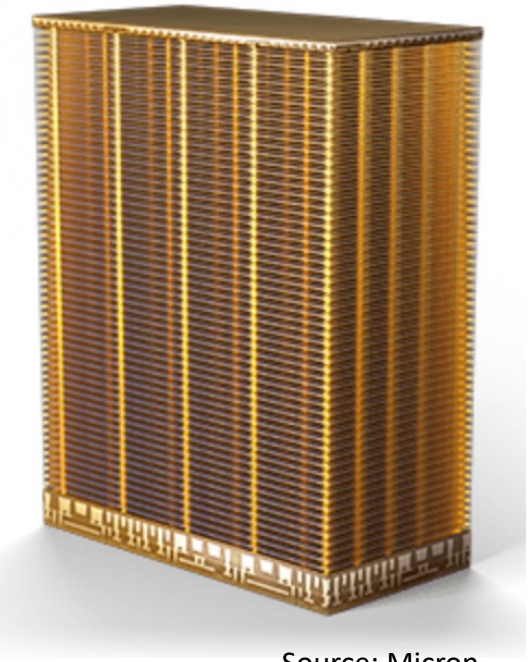


Memory Quality key requirements & directions

- **'Shift Left' proactive quality vs DRAM scaling** – i) DRAM & DIMM design, ii) early reliability assessment, iii) fab process quality, wafer variability, iv) Wafer test, e-fuse repair, v) package test, Burn-In, vi) stacked package quality, vii) reliability monitors
- **Maverick lot prevention –** focus needed in understanding reliability mechanism vs wafer lot process variability
- **Memory Intensive AI workloads –** computation intensive, temperature sensitive failure modes
- **Post package repair (PPR)** – enabling field repair of row and single bit fails
- **Row hammer** – advanced mitigation schemes needed vs DRAM scaling at sub 1a nm nodes, key focus from infrastructure memory subsystem security perspective
- **DDR5 on-die ECC, Memory Controller** – single bit, row & column fail mitigation, ECC correction, UE prediction
- **Field Telemetry** – Bit map special & temporal CE analysis, ML based UE prediction capabilities, big data & AI based DRAM quality analytics

3D-NAND Scaling trends & outlook





Source: Micron

- Growing #of layers enabling 3D NAND manufacturers to drive Density & $/GB scaling
- Z-height reduction critical for continued 3D-NAND scaling – Channel etch control, cleaning, stress management, die thinning & stacked package quality
- Staircase contact process and real estate
- Cell current challenges resulting in larger block size vs 3D-NAND generation

3D-NAND Quality & Reliability Challenges

- **Endurance** – # of Program/Erase cycles a cell is expected to withstand, Failure mechanism caused by charge traps in ONO

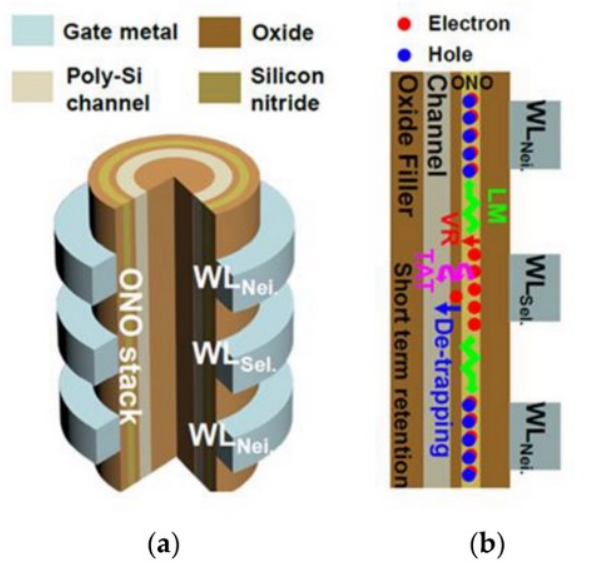
- **Data Retention**– charge is lost in the 3D-NAND cell over time
  - High Temperature accelerates rate of charge loss
    - Charge de-trapping can occur
    - Charge loss mechanism, Activation Energy needs to be well understood
  - Stress induced Leakage current (SILC)
    - Degradation caused by P/E cycles

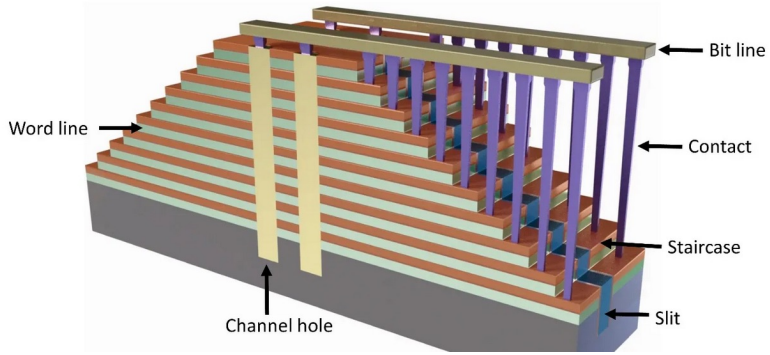
- **Read Disturb**– Pages not selected for read see elevated voltage stress, causing bit flip

- **Staircase contact**– alignment accuracy, contact resistivity

- **Stacked package quality –** Si die & mold compound interactions, die cracking

- **Early Life Fails** – i) Fab particle driven manufacturing quality, ii) Intrinsic failure modes





Flash Storage Quality key requirements & directions

- **'Shift Left' proactive quality vs 3D-NAND scaling** – i) Reliability (Endurance, Data Retention, read/write disturb) robustness, ii) fab process quality, wafer variability, iii) wafer test, trims for Vth variability compensation, iv) package test & Burn-In, v) stacked package quality, vi) reliability monitors
- **Maverick lot prevention –** focus needed in understanding reliability mechanism vs wafer lot process variability
- **Z-height, stacked package quality** – cell to cell interference, die cracking
- **Flash Controller management schemes** – Vth evolution control thru EOL, advanced ECC, Bad block management/wear leveling, Garbage Collection
- **Field Telemetry** – ML/AI analytics failure prediction. Flash reliability indicators (PE cycles, retired blocks, Temperature)
- **Storage Data resilience** – often achieved thru the use of redundant components. When one component fails the redundant one takes over seamlessly – reducing risk of Single Point of Fail
- **Storage System Resilience** - capable of 2-site and 3-site replication configurations – on premises, on cloud, or hybrid

Summary

- System infrastructure technology focused on enabling AI driven decision velocity, resilience & hybrid cloud modernization
- AI driving accelerated growth in Memory & Flash storage technology
- DRAM scaling to continue into sub 10nm nodes, while 3D-NAND scaling expected to continue into 500+ layer modes in the next 5+ years
- DRAM quality & reliability and system RAS mitigation schemes critical in meeting memory subsystem quality requirements
- Flash reliability challenges vs 3D-NAND scaling critical in storage system resilience
- E2E & ‘Shift Left’ Quality approach needed for meeting system level resilience goals

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