

Smart Debugging Capabilities in SSD Controllers

SSDS-101-1: Controller Capabilities
Aug 8, 2023

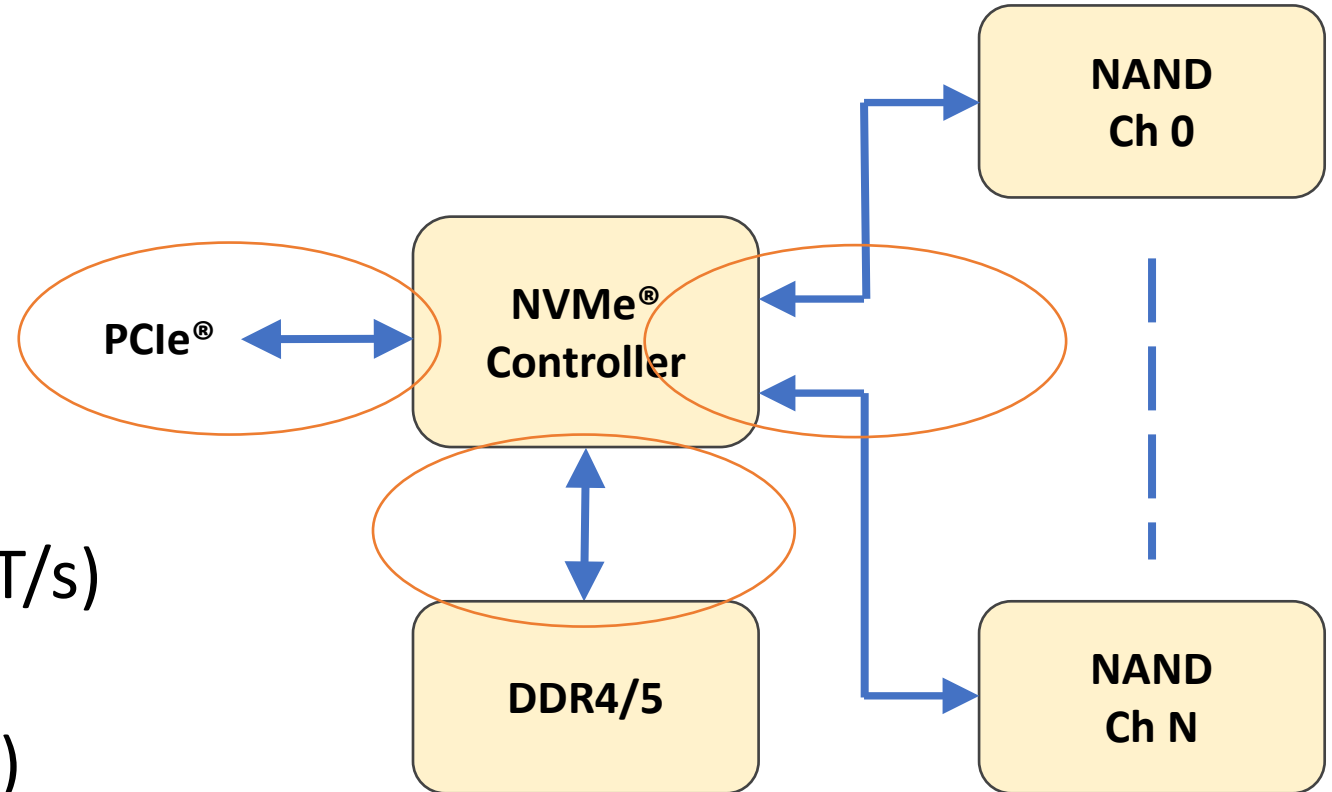
Presenter: Phillip Arellano, Sr. Engineer, Applications
Microchip Technology Inc.

Agenda

- High-Speed Interfaces in SSD
- Problems and Challenges of High-Speed Interfaces
- Smart Debugging Capabilities in SSD Controller
- Summary

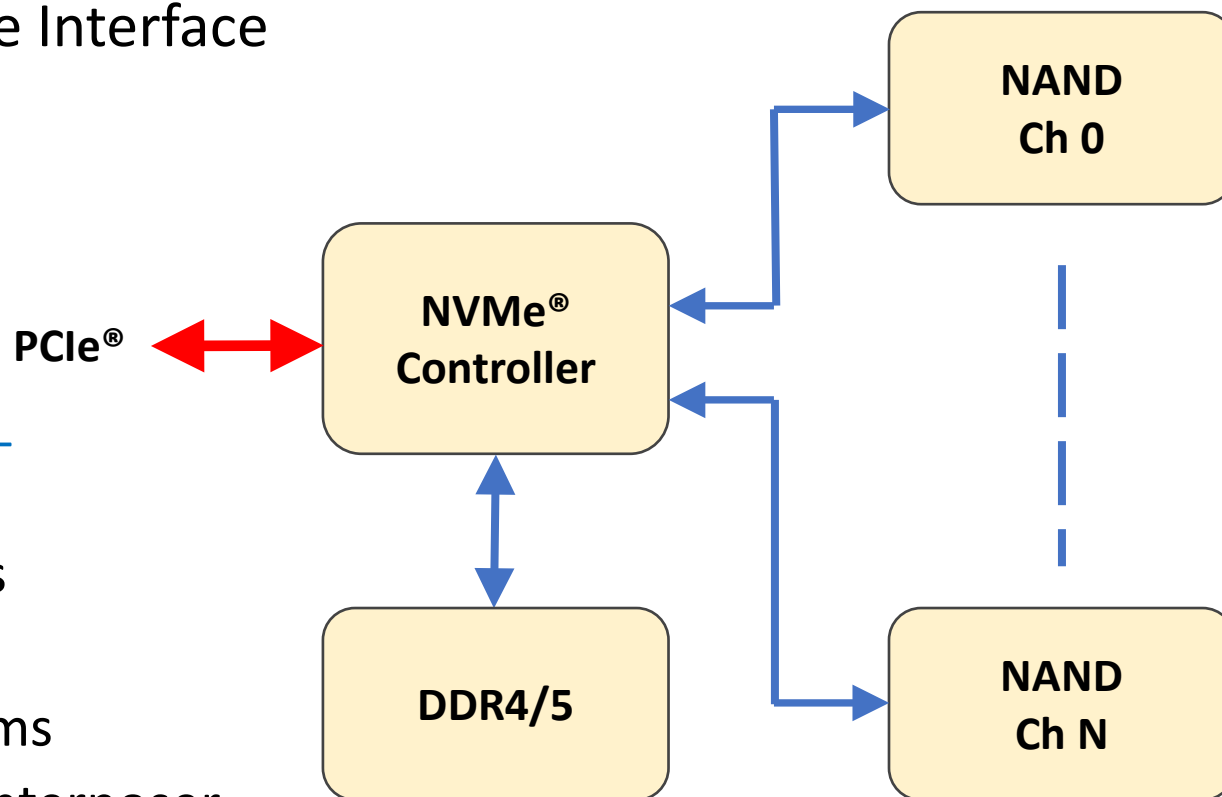
High Speed Interfaces in an SSD

- An SSD has three main functional blocks:
 - Controller
 - DDR SDRAM Memory
 - NAND Flash Memory
- The three high-speed interfaces:
 - PCIe® Host to Controller (32GT/s)
 - DDR to Controller (3200MT/s)
 - Flash to Controller (2400MT/s)



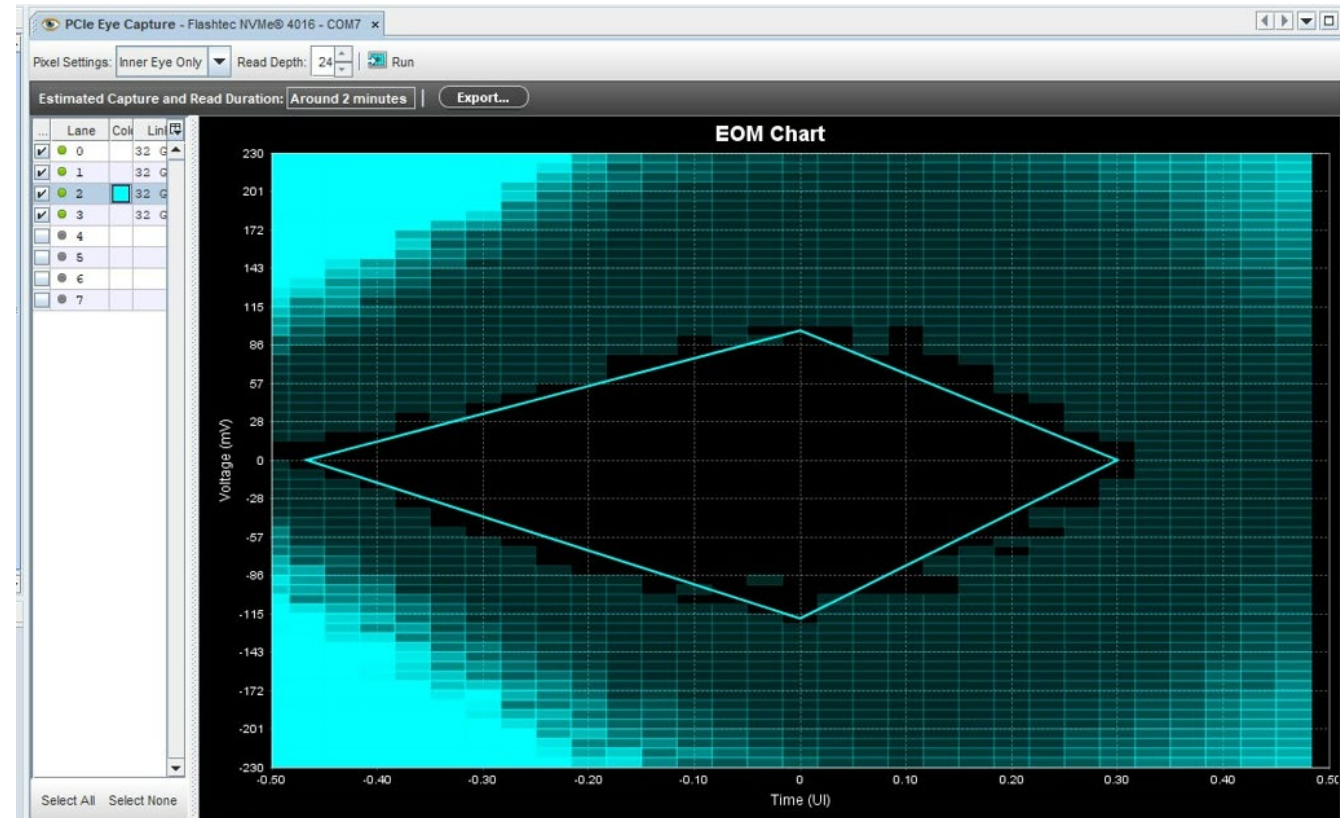
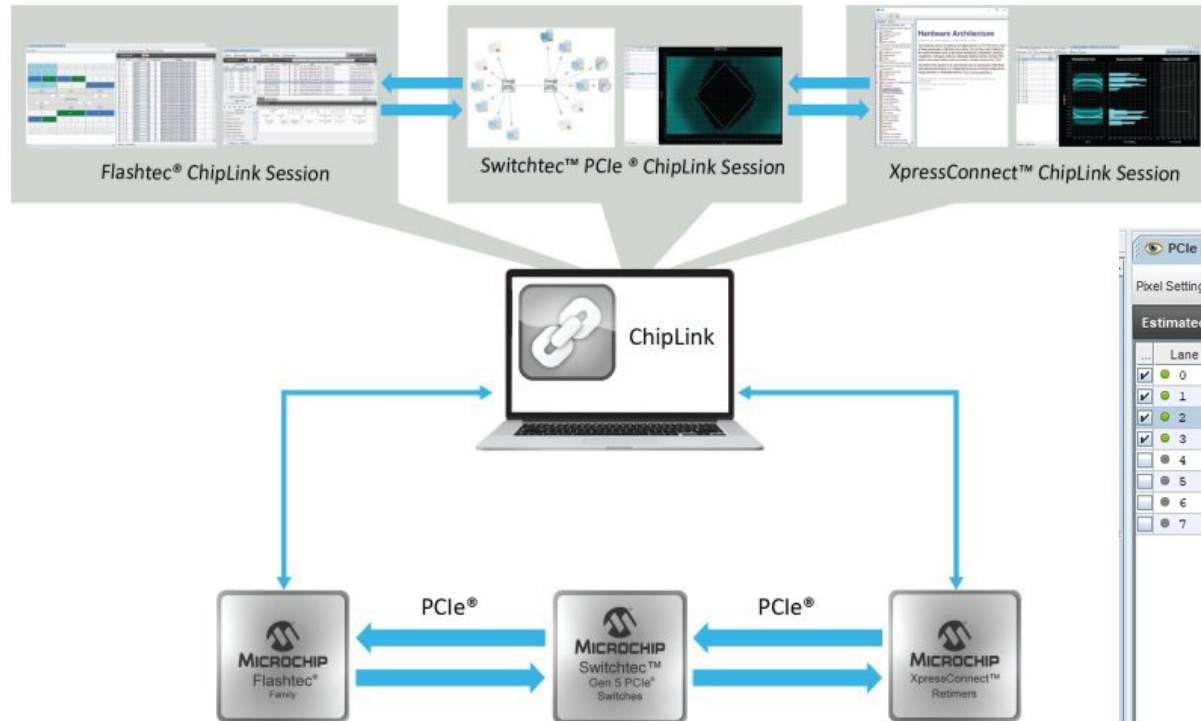
High Speed Interfaces in an SSD - PCIe®

- PCIe problems due to high speed are highly elusive to debug
- Testing and debugging the Controller PCIe Interface
 - Proactive testing can be done by
 - **In-system via Loopback with PRBS** –
Only Demonstrates the physical connection
 - **In-controller Loopback** –
Only demonstrates the IO buffer
 - **Insert an interposer to capture link states** –
Effective for analysis but adds
 - Insertion loss and delay to the signals
 - May add a retimer in the data path
 - Could mask or introduce new problems
 - Requires an expensive analyzer and interposer
 - Difficult to reproduce



Smart Debug Capabilities - PCIe®

- End-to-end debug tools – RX Eye capture built into controller



Smart Debug Capabilities - PCIe®

- End-to-end debug tools – PHY Analyzer, LTSSM state capture



Flash Memory Summit

Device Info - Flashtec NVMe® 4016 - COM6 x Phy Analyzer - Flashtec NVMe® 4016 - COM6 x PCIe Status - Flashtec NVMe® 4016 - COM6 x

Refresh Configuration Run Trigger Stop Read Trace Clear Export Import Toggle Details

Auto-Refresh 4 Analyzer Status: Buffers: LTSSM State Transitions: 0.0%

OS	Time	Source	Direction	Symbol	Raw Data
54 OS	00:00:27.462,407.703	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 78 00 00 00 00 00 00 00 00 00 00 00	
55 OS	00:00:27.462,412.281	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 00 00 00 00 00 00 00 00 00 00 00	
56 OS	00:00:27.462,415.336	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 00 00 00 00 00 00 00 00 00 00 00	
57 OS	00:00:27.462,418.392	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 00 00 00 00 00 00 00 00 00 00 00	
58 OS	00:00:27.462,421.451	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 00 00 00 00 00 00 00 00 00 00 00	
59 OS	00:00:27.462,424.507	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 00 00 00 00 00 00 00 00 00 00 00	
60 OS	00:00:27.462,427.558	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 00 00 00 00 00 00 00 00 00 00 00	
61 OS	00:00:27.462,430.604	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 00 00 00 00 00 00 00 00 00 00 00	
62 OS	00:00:27.462,434.885	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 17 de 40 00 00 00 00 00 00 00 00 00	
63 OS	00:00:27.462,447.866	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 a9 91 de 00 00 00 00 00 00 00 00 00	
64 OS	00:00:27.462,450.851	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 70 cb e5 00 00 00 00 00 00 00 00 00	
65 OS	00:00:27.462,453.837	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 e7 b1 c6 00 00 00 00 00 00 00 00 00	
66 OS	00:00:27.462,456.831	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 0a 8a 8e 00 00 00 00 00 00 00 00 00	
67 OS	00:00:27.462,459.822	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 05 a3 c1 00 00 00 00 00 00 00 00 00	
68 OS	00:00:27.462,462.815	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 ld 4f 85 00 00 00 00 00 00 00 00 00	
69 OS	00:00:27.462,465.803	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 ac fe 3e 00 00 00 00 00 00 00 00 00	
70 OS	00:00:27.462,468.790	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 c7 00 e7 00 00 00 00 00 00 00 00 00	
71 OS	00:00:27.462,471.774	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 6e bc 5c 00 00 00 00 00 00 00 00 00	
72 OS	00:00:27.462,474.755	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 7c 5d a6 00 00 00 00 00 00 00 00 00	
73 OS	00:00:27.462,477.734	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 89 c1 ab 00 00 00 00 00 00 00 00 00	
74 OS	00:00:27.462,480.716	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 e8 5d 76 00 00 00 00 00 00 00 00 00	
75 OS	00:00:27.462,483.706	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 fa a9 83 00 00 00 00 00 00 00 00 00	
76 OS	00:00:27.462,486.693	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 5f 7f fc 00 00 00 00 00 00 00 00 00	
77 OS	00:00:27.462,489.683	32 GT/s Stack 0/Lane 0	SKP	Raw Data: 99 99 99 99 e1 79 a5 fa 00 00 00 00 00 00 00 00 00	

Ordered Set Details

Type: SKP

PCIe Rate: 32 GT/s

Direction: Transmitted

Source: Stack 0/Lane 0

Graph Text Raw

Width DWord

Symbol	Width	DWord
Symbol 3	99h	
Symbol 7	0h	
Symbol 11	0h	
Symbol 15	0h	

LTSSM State Transitions: 0.0%

Info: 0x01000002

Info: 0x02050040

TS1 Link: 4 Lane: 0 Max Rate: G4 TC: Full EQ required Phase 0 Use Coeffs Tx Preset: P8 C-1: 0x06 C0: 0x2a C+1: 0x0c

TS1 Link: 4 Lane: 1 Max Rate: G4 TC: Full EQ required Phase 0 Use Coeffs Tx Preset: P8 C-1: 0x06 C0: 0x2a C+1: 0x0c

TS1 Link: 4 Lane: 1 Max Rate: G5 TC: Full EQ required Phase 0 Use Coeffs Tx Preset: P5 C-1: 0x03 C0: 0x1d C+1: 0x00

TS1 Link: 4 Lane: 0 Max Rate: G5 TC: Full EQ required Phase 0 Use Coeffs Tx Preset: P6 C-1: 0x02 C0: 0x1e C+1: 0x00

TS2 Link: 4 Lane: 0 Max Rate: G4 TC: Full EQ required

TS2 Link: 4 Lane: 1 Max Rate: G4 TC: Full EQ required

RECOVERY_RCVR_LOCK Info: 0x01000004

TS2 Link: 4 Lane: 0 Max Rate: G5 TC: Full EQ required

TS2 Link: 4 Lane: 1 Max Rate: G5 TC: Full EQ required

RECOVERY_RCVR_CFG Info: 0x04000000

SDS Raw Data: e1 55 55 55 55 55 55 55 55 55 55 55 55 55 55 55

SDS Raw Data: e1 55 55 55 55 55 55 55 55 55 55 55 55 55 55

SDS Raw Data: e1 55 55 55 55 55 55 55 55 55 55 55 55 55 55

SDS Raw Data: e1 55 55 55 55 55 55 55 55 55 55 55 55 55 55

RECOVERY_IDLE Info: 0x0b000000

RECOVERY_INACTIVE Info: 0x16000000

CfgRd1 Requester ID: 00:00.0 Tag: 0 Completer ID: 02:01.0 1st BE: 0b0011 Register: 0x012

CfgRd1 Requester ID: 00:00.0 Tag: 0 Completer ID: 02:02.0 1st BE: 0b0011 Register: 0x012

CfgRd0 Requester ID: 00:00.0 Tag: 0 Completer ID: 01:00.0 1st BE: 0b0011 Register: 0x012

CfgRd1 Requester ID: 00:00.0 Tag: 0 Completer ID: 02:00.0 1st BE: 0b0011 Register: 0x012

CfgRd1 Requester ID: 00:00.0 Tag: 0 Completer ID: 02:01.0 1st BE: 0b0011 Register: 0x012

CfgRd1 Requester ID: 00:00.0 Tag: 0 Completer ID: 02:02.0 1st BE: 0b0011 Register: 0x012

CfgRd0 Requester ID: 00:00.0 Tag: 0 Completer ID: 01:00.0 1st BE: 0b0011 Register: 0x012

CfgRd1 Requester ID: 00:00.0 Tag: 0 Completer ID: 02:00.0 1st BE: 0b0011 Register: 0x012

CfgRd1 Requester ID: 00:00.0 Tag: 0 Completer ID: 02:01.0 1st BE: 0b0011 Register: 0x012

Smart Debug Capabilities - PCIe®



Flash Memory Summit

- End-to-end debug tools – Lane Margining, LTSSM state capture

```
C:\Users\C67106>Lane Margining
```

Read Clear Logs Export Logs

PCIe Link Status

Link #: 0

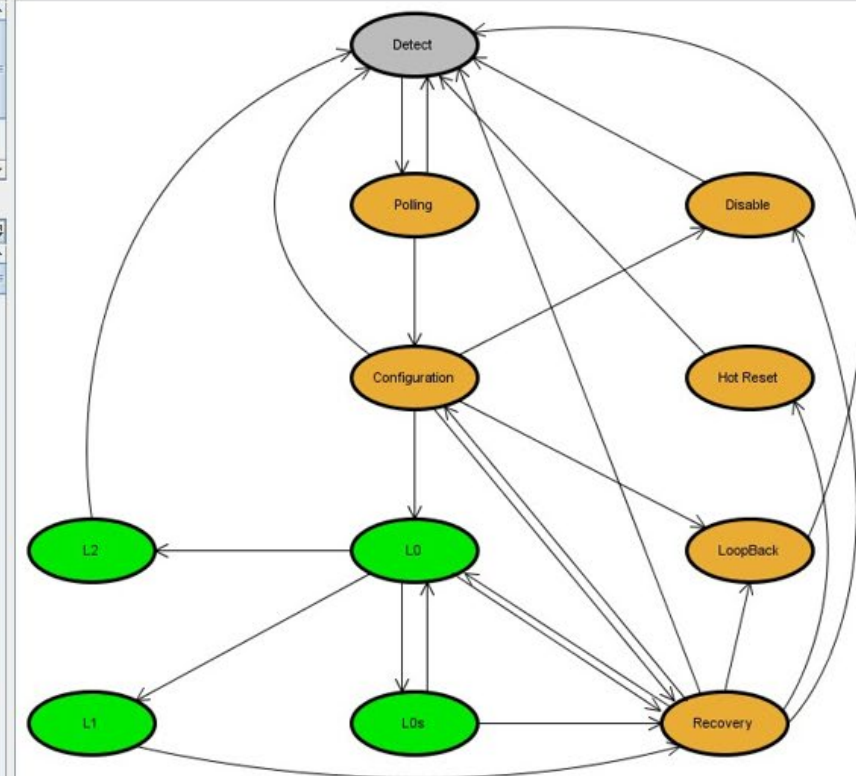
LTSSM State: L0_0

Links:

Speed: 32 GT/s

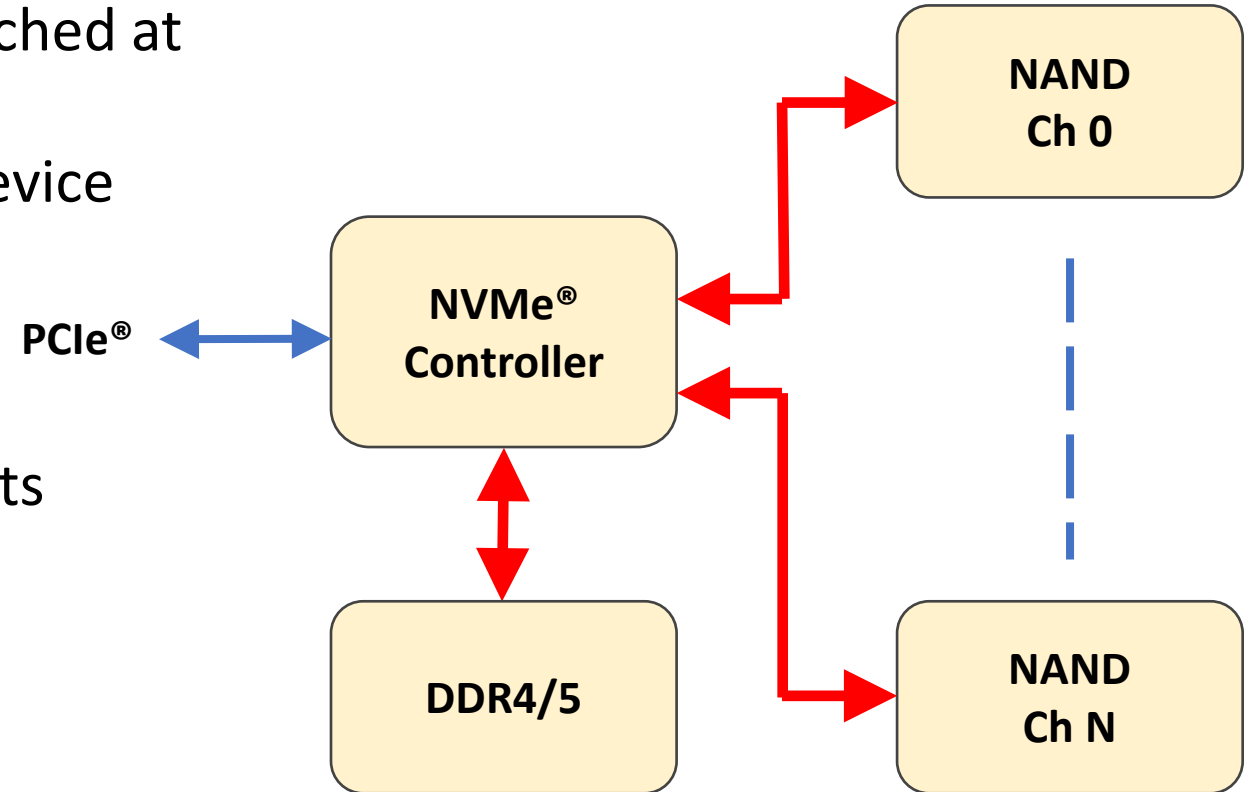
Link #0 LTSSM Logs

Entry #	LTSSM State	Link Sp...	Time in State	Arc Code	Reason
0	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
1	Detect_Active0	2.5 GT/s	6,072	0x05000000	
2	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
3	Detect_Active0	2.5 GT/s	6,072	0x05000000	
4	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
5	Detect_Active0	2.5 GT/s	6,072	0x05000000	
6	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
7	Detect_Active0	2.5 GT/s	6,072	0x05000000	
8	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
9	Detect_Active0	2.5 GT/s	6,072	0x05000000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
10	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
11	Detect_Active0	2.5 GT/s	6,072	0x05000000	
12	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
13	Detect_Active0	2.5 GT/s	6,072	0x05000000	
14	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
15	Detect_Active0	2.5 GT/s	6,072	0x05000000	
16	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
17	Detect_Active0	2.5 GT/s	6,072	0x05000000	
18	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
19	Detect_Active0	2.5 GT/s	6,072	0x05000000	
20	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
21	Detect_Active0	2.5 GT/s	6,072	0x05000000	
22	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
23	Detect_Active0	2.5 GT/s	6,072	0x05000000	
24	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
25	Detect_Active0	2.5 GT/s	6,072	0x05000000	
26	Detect_Quiet	2.5 GT/s	12,118,152	0x0b800000	mgmt_rx_detect_override: 1, int_rx_det_status: 00000000
27	Detect_Active0	2.5 GT/s	6,072	0x05000000	



High-Speed Interfaces in an SSD - DDR

- DDR and Flash buses are parallel interfaces with 18 - 32 devices, with >40 signals per device
- Testing can be done with interposer attached at a DDR/Flash device
 - Interposer is mounted between the device and the PCB footprint
 - Cannot install interposer in production SSD
 - Interposer nets are stubs which impacts signal integrity
 - Signal level reduction
 - Reflections
 - Ringing
 - Noise
 - Cannot be probe at the controller



DDR BIST Diagnostic Commands

The following is a list of DDR BIST diagnostic commands that are available in our DDR Diagnostic Manager.

- `ddr_BistInit <ps>`
- `ddr_BistSetup`
- `ddr_BistSetupPrint`
- `ddr_BistSequenceRun <pattern> <timeout>`
- `ddr_BistSet_rankIndex <rankIndex>`
- `ddr_BistSet_cid <cid>`
- `ddr_BistSet_length <length>`
- `ddr_BistSet_numReadWrite <numReadWrite>`
- `ddr_BistSet_patternStyle <patternStyle>`
- `ddr_BistSet_addressMode <addressMode>`
- `ddr_BistSet_tWrRd <tWrRd>`
- `ddr_BistSet_tWrWr <tWrWr>`
- `ddr_BistSet_tRdWr <tRdWr>`
- `ddr_BistSet_tRdRd <tRdRd>`
- `ddr_BistSet_userData0 <userData0>`
- `ddr_BistSet_userData <userData1>`
- `ddr_BistSRE <csn>`
- `ddr_BistSRX0 <csn>`
- `ddr_BistZQCS <csn>`
- `ddr_BistMaskOverride <0=Read, 1=Write>`

DDR Diagnostic Tools



Flash Memory Summit

- Firmware Command Line Interface (CLI) command set to aid in DDR and Flash Debug
- Manual Step through initialization sequence
- BIST capability
- Margining capability
- Diagnostic information (MR Register DDR)

```
DiagMgr> help
Help [<command>] - Provides help for the specified command.
MemRead <address> <DWord-count> - Read DWords from memory
MemWrite <address> <data-word> - Write DWord to memory
ddrTest - run ddr configuration
addrTest <start_address> <num_bytes>
addrTest <start_address> <num_bytes>
ddr_VerboseSet <debug|acc|hist> <on|off>
ddr_CtlPrint
ddr_DimmPrint
ddr_PhyPrint
ddr_TimingMeasure <rank> <timingTagNum> [skipBistFail]
ddr_TrainPrep
ddr_VrefMeasure <rank> <dram|device>
ddr_ApiCfgSet_hdtCtrl <hdtCtrl>
ddr_ApiCfgSet_sequenceCtrl <train2d> <sequenceCtrl>
ddr_ApiCfgSet_freqMhz <pstate> <freq_MHz>
ddr_ApiCfgSet_phyOdtImpedance <pstate> <value>
ddr_ApiCfgSet_phyDrvImpedancePu <pstate> <value>
ddr_ApiCfgSet_phyDrvImpedancePd <pstate> <value>
ddr_ApiCfgSet_aTxImpedance <value>
ddr_ApiCfgSet_dramRttNom <rank> <pstate> <value>
ddr_ApiCfgSet_dramRttWr <rank> <pstate> <value>
ddr_ApiCfgSet_dramRttPark <rank> <pstate> <value>
ddr_ApiCfgSet_dramDic <pstate> <value>
ddr_ApiCfgSet_dramWritePreamble <pstate> <value>
ddr_ApiCfgSet_dramReadPreamble <pstate> <value>
ddr_ApiCfgSet_odtWrMapCs <pstate> <value>
ddr_ApiCfgSet_odtRdMapCs <pstate> <value>
ddr_ApiCfgSet_caLatencyAdder <pstate> <value>
ddr_ApiCfgSet_rcdDic <pstate> <value>
ddr_ApiInit
ddr_ApiFwTrain
ddr_ApiSavedMarginResultsLoad
ddr_MarginTimingPerBitPrint <rank> <timingTag>
ddr_MarginTimingSummaryPrint <rank> <timingTag>
ddr_MarginTimingFinalPrint <timingTag>
ddr_MarginTapSizePrint
ddr_MarginVrefPrint <rank> <device|dram>
ddr_VrefPrint <rank> <dram|device>
```

Flash Diagnostic Tools

- Firmware Command Line Interface (CLI) command set to aid in DDR and Flash Debug
- Manual Step through initialization sequence
- BIST capability
- Margining capability
- Diagnostic information (MR Register DDR)

[0] - FlashInit - Flash Initialize
[0] - fccTraceLog - <channel> Print FCC Trace log of the given FCC channel
[0] - FlashECCstats - Prints ECC Error stats for Flash Reads
[0] - FlashReadRetryCounters - Prints Flash Read Retry Counters
[0] - clearFlashReadstats - Clear ECC Error stats and Flash Read Retry stats for Flash Reads
[0] changeReadType - <readType> Change read operation type
[0] changeWriteType - <writeType> Change write operation type
[0] - FlashRead <channelNum> <ctxtNum> <blockNum> <pageNum> <blockType> <opMode> <startECCChunk> <numECCChunk> - Flash Read
[0] - FlashWrite <channelNum> <ctxtNum> <blockNum> <pageNum> <blockType> <opMode> <numPlanes> - Flash Write
[0] - ReadId <channel> <context> <address> - Flash Read Id
[0] - EraseBlock <channelNum> <ctxtNum> <blockNum> <blockType> <opMode> - Flash Erase Block
[0] - BadBlockScan <startBlock> <scanOption> - Scan Flash Bad Block
[0] - DumpVLInfo <vlun> <vBlkSize> - Print Virtual LUN details
[0] - FccTestDebuglevel <option> <SET/UNSET> - Set Debug level for prints
[0] - FccTestStartRegression <vlun> <vBlock> <phyBlkIndex> <blockType> - Run Regression test
[0] - SetFeature <channel> <context> <address> <data> - Flash Set Feature
[0] - GetFeature <channel> <context> <address> - Flash Get Feature
[0] - SetLunFeature <channel> <context> <address> <data> - Flash Set Feature by LUN
[0] - GetLunFeature <channel> <context> <address> - Flash Get Feature by LUN
[0] - SetDataPattern <patternType> - Set Data Pattern
[0] - FlashOpConfig <blockOpMode> <vblockSize> - Flash Operation Config
[0] - forceProgramError - Force program error

Flash Diagnostics Functionality

- The Flash Diagnostic Tool provides the following functions
 - Flash Margin Test
 - Basic CLI commands to configure Flash Phy registers, set drive strength, ODT, change flash clock frequency, perform error injections
 - Standard diagnostic commands to execute read, write and erase tests
 - Flash Diagnostic tool is part of Diagnostic Manager

```
[0] - FlashEraseLatency <channelNum> <ctxtNum> <blockNum> <blockType> <opMode>
[0] - FlashWriteLatency <channelNum> <ctxtNum> <blockNum> <pageNum> <blockType> <opMode> <numPlanes>
[0] - FlashReadLatency <channelNum> <ctxtNum> <blockNum> <pageNum> <blockType> <opMode> <startECCChunk> <numECCChunk>
[0] - FlashMarginTest <startChannel> <numChannels> <numTargets> <blockNum> <training> .....
[0] - FlashReadUtilization <channelNum> <ctxtNum> <blockNum> <numReqs>
[0] - StopFCCUtilization <Flag - Enable or Disable>
[0] - GetFCCUtilization <channel>
```

Summary

Challenges of debugging high-speed interfaces in an SSD

- PCIe® smart debugging capabilities
 - Rx eye capture
 - Built-in PHY analyzer
 - LTSSM state capture
 - Margining tools
- DDR smart debugging capabilities
 - Comprehensive diagnostic commands
 - Trace capture
 - Margining tools
- NAND Smart debugging capabilities
 - Built-in comprehensive diagnostic commands
 - Margining tools

Thank you!
Visit Microchip at Booth 419.



PCIe® Gen 5 NVMe® Flash Controller