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3D NAND Process Technology : 2023 & Beyond

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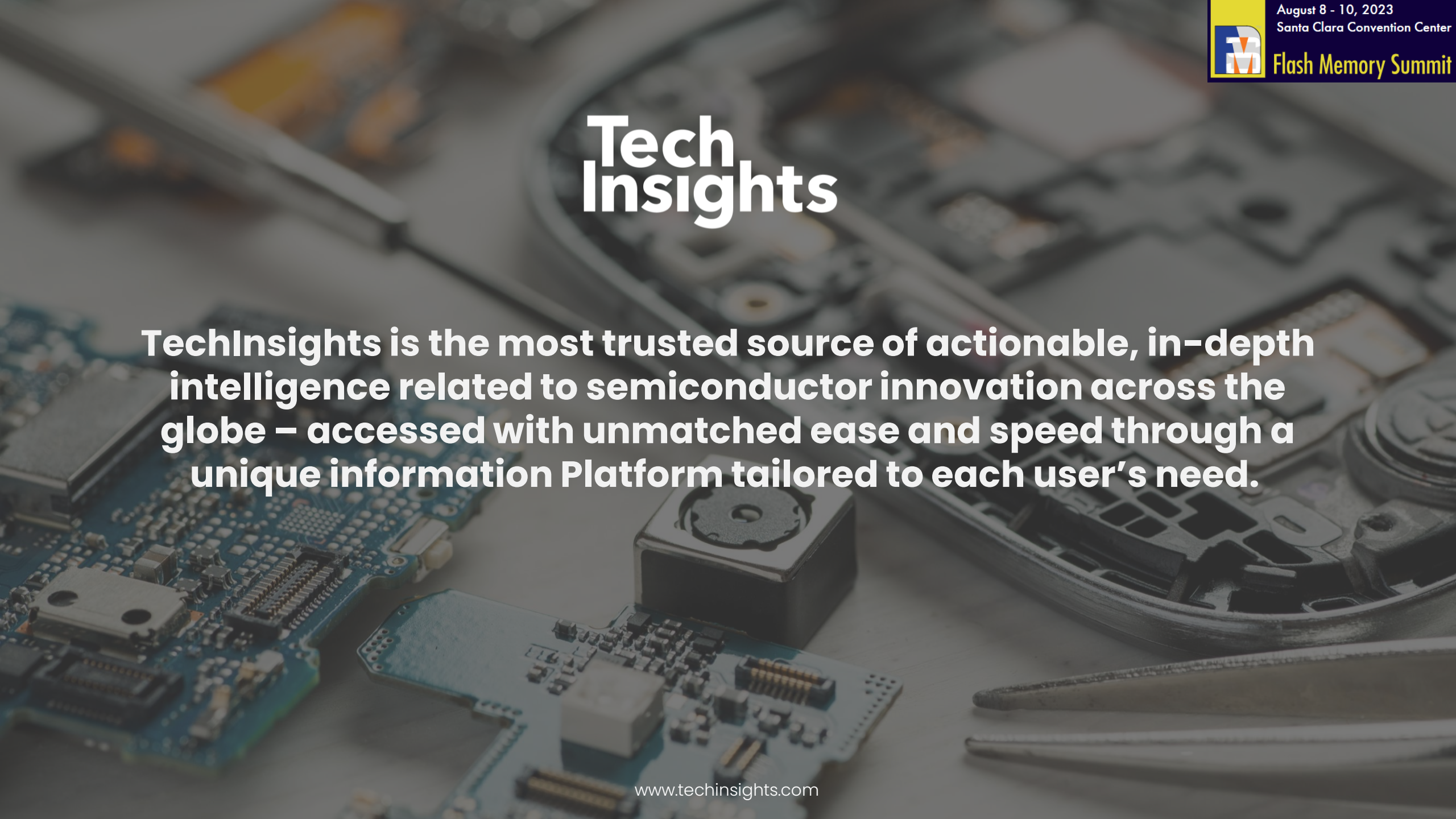
Dr. Jeongdong Choe
Senior Technical Fellow, SVP
www.techinsights.com



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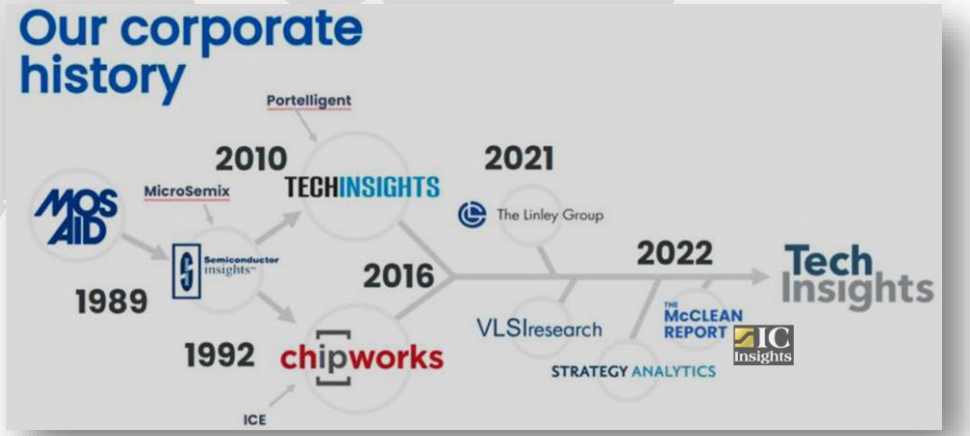

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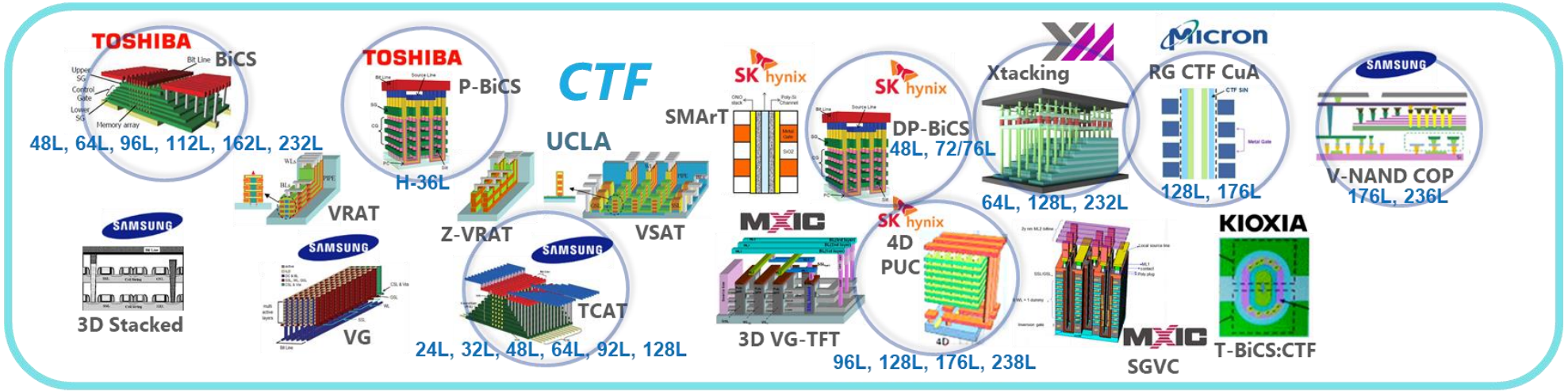
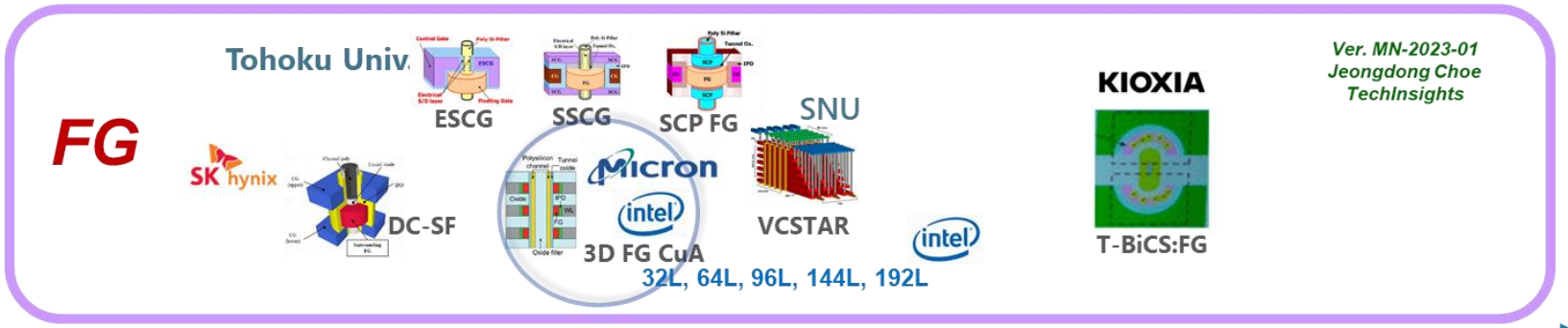
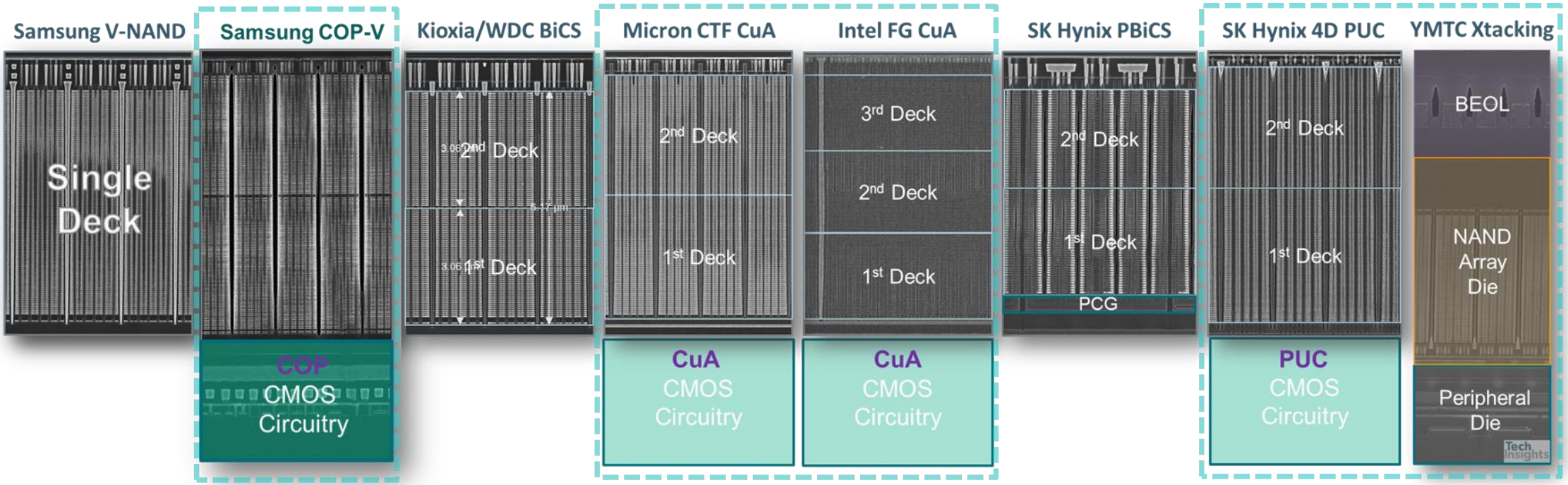
History of 3D NAND Cell Architecture



1) VRAT: Vertical Recess Array Transistor
2) Z-VRAT: Zigzag VRAT
3) VSAT: Vertical Stacked Array Transistor
4) ESCG: Extended Sidewall Control Gate
5) SSCG: Separated Sidewall Control Gate
6) SCP: Sidewall Control Pillar
7) VCSTAR: Vertical Channel Stacked Array
8) DC-SF: Dual Control-gate with Surrounding FG
9) SMArT: Stacked Memory Array Transistor
10) DP-BiCS: Dual PCG BiCS
11) PUC: Peri-Under-Cell
12) CuA: CMOS Under Array
13) COP: Cell-On-Peri
14) T-BiCS: Twin BiCS



3D NAND Cell Architecture on Market



- *CuA: CMOS Under Array*
- *PUC: Periphery Under Cell array*
- *COP: Cell array On Periphery*

3D NAND Die Floorplan Trend

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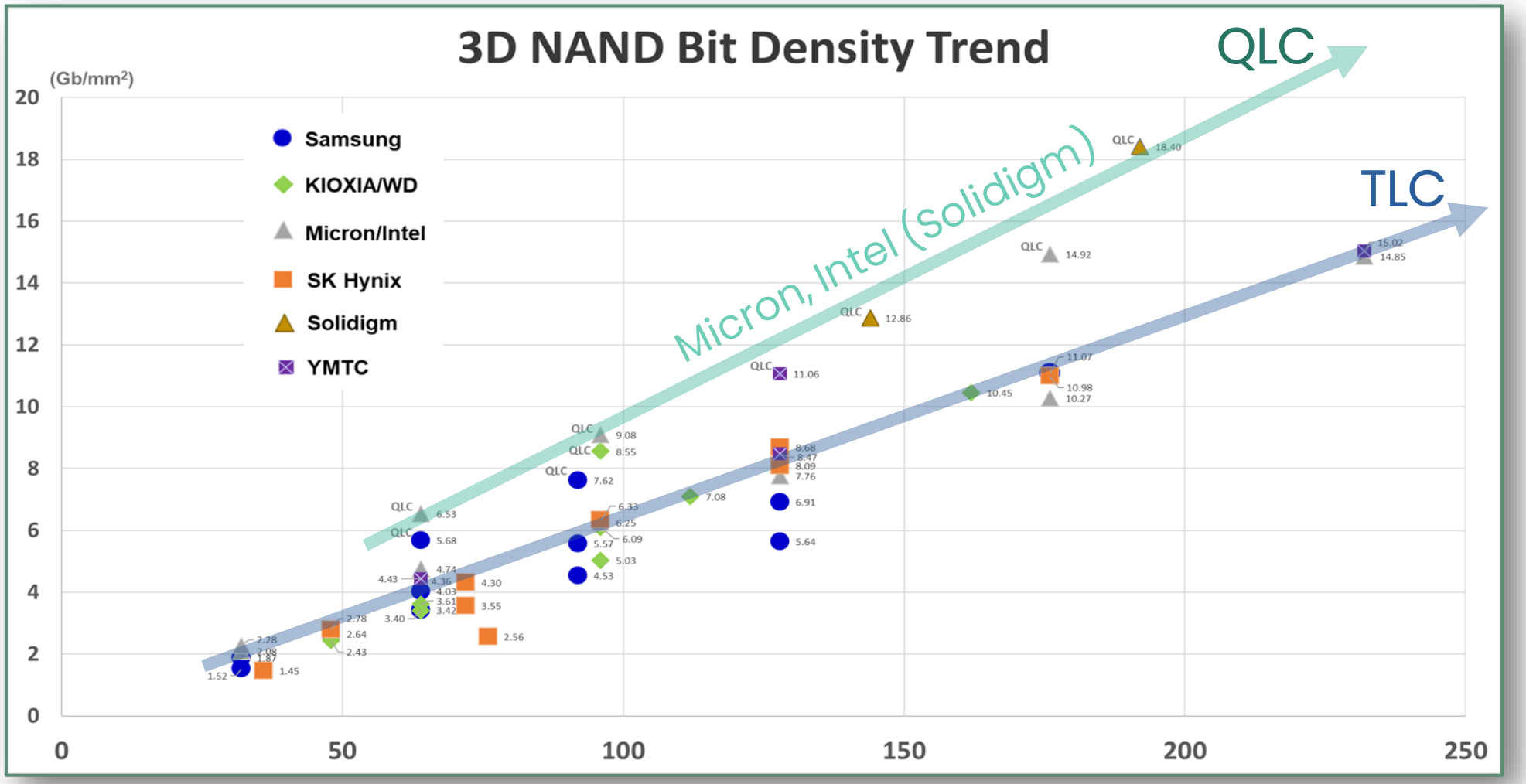
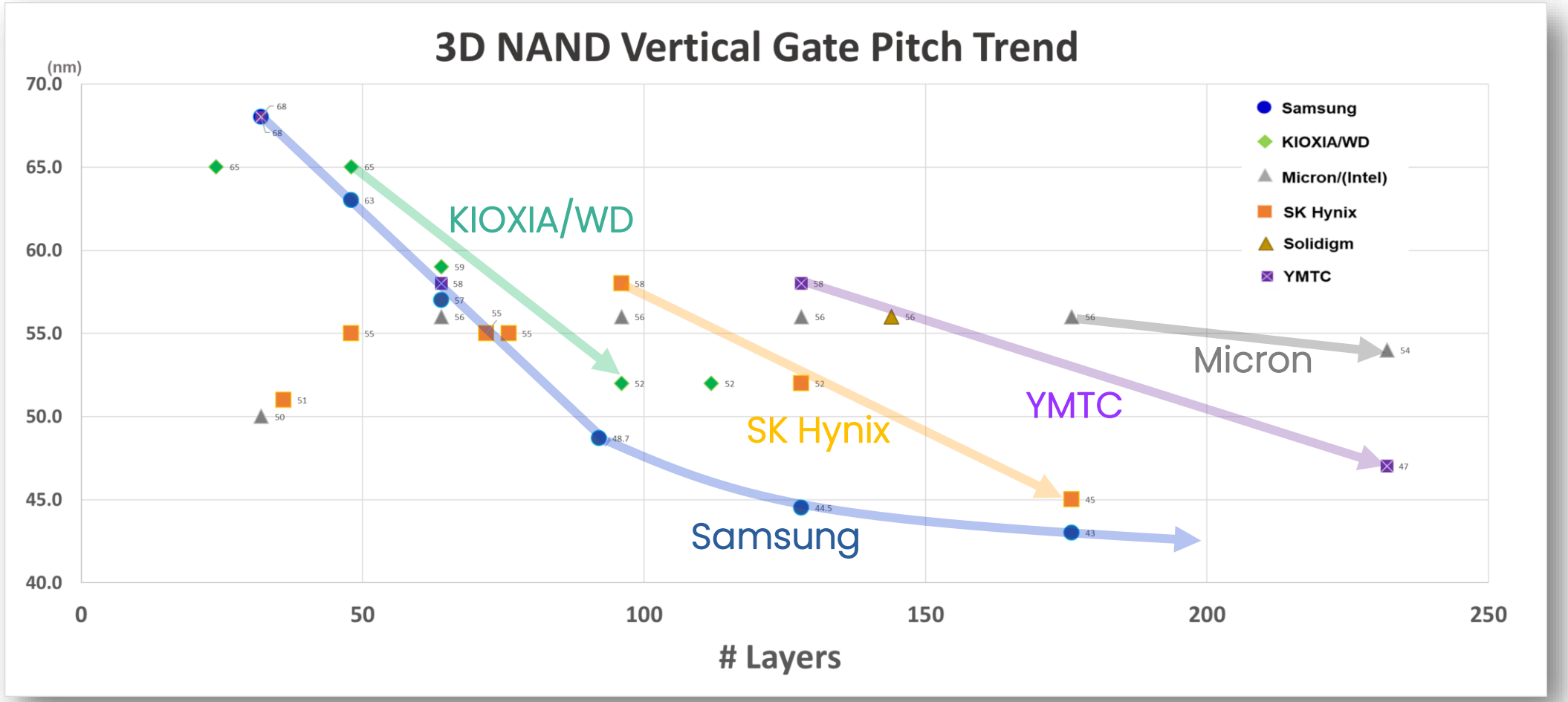
3D NAND Bit Density



3D NAND devices we found in the market

Vertical Gate Pitch Trend



YMTC Xtacking3.0 232L

ITEMS	YMTC 3D NAND Gen1 (32L MLC)	YMTC 3D NAND Gen2 (64L TLC)	YMTC 3D NAND Gen3 (128L TLC, 1B-Die)	YMTC 3D NAND Gen4 (232L TLC)
Parent Product (Example)	32GB Secure USB	Gloway YCT512GS3-S7 Pro SSD 512GB	Asgard PCIe4.0 NVMe1.4 AN4 1TB SSD	HIKSEMI CC700 PCIe 4.0 2TB SSD
Package Markings	YMEC6A1MA3A2C1	YMN08TB1B1HU1B	YMN09TC1B1HC6C	YMC6G008Tb78DA1C0
Memory/Device	256 Gb	1 Tb	2 Tb	8 Tb
Die Markings	98081A	BCT1B	CDT1B	EET1A
Architecture	T-CAT	Xtacking1.0	Xtacking2.0	Xtacking3.0
# Dice, Memory/Die	4, 64 Gb	4, 256 Gb	4, 512 Gb	8, 1 Tb
Die Size	76.30 mm^2	57.96 mm^2	60.42 mm^2	68.15 mm^2
Memory Density	0.84 Gb/mm^2	4.42 Gb/mm^2	8.48 Gb/mm^2	15.03 Gb/mm^2
#Planes	1	2	4	6 (Center-XDEC)
# Decks, # Gates	1, 39T	1, 73T	2, 141T (69 + 72)	2, 253T (128 + 125)
Vertical Cell Efficiency	82.1 %	87.7 %	90.8 %	91.7 %
# Metals	3	8	11	11 (BSSC)
Channel Hole Height	2.74 µm	4.14 µm	8.49 µm	12.0 µm
WL Pitch (Z-direction, min.)	70 nm	58 nm	58 nm	48 nm
BL Pitch	39 nm	39 nm	39 nm	39 nm
Unit Cell Area	0.021 $µm^2$	0.021 $µm^2$	0.021 $µm^2$	0.021 $µm^2$

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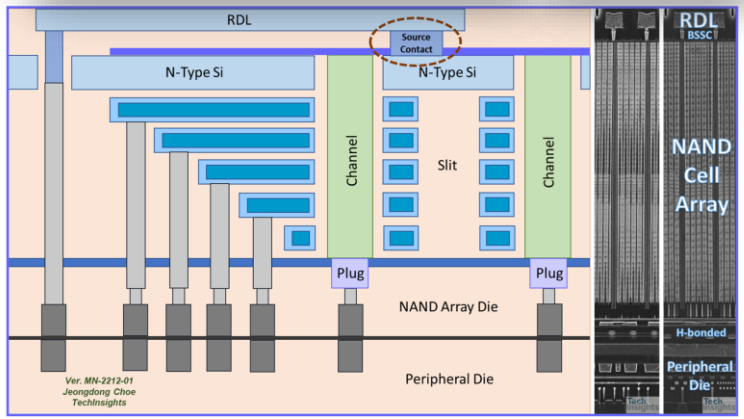
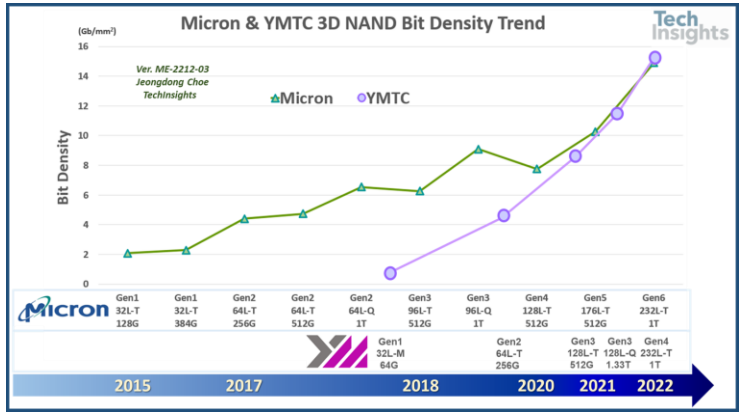
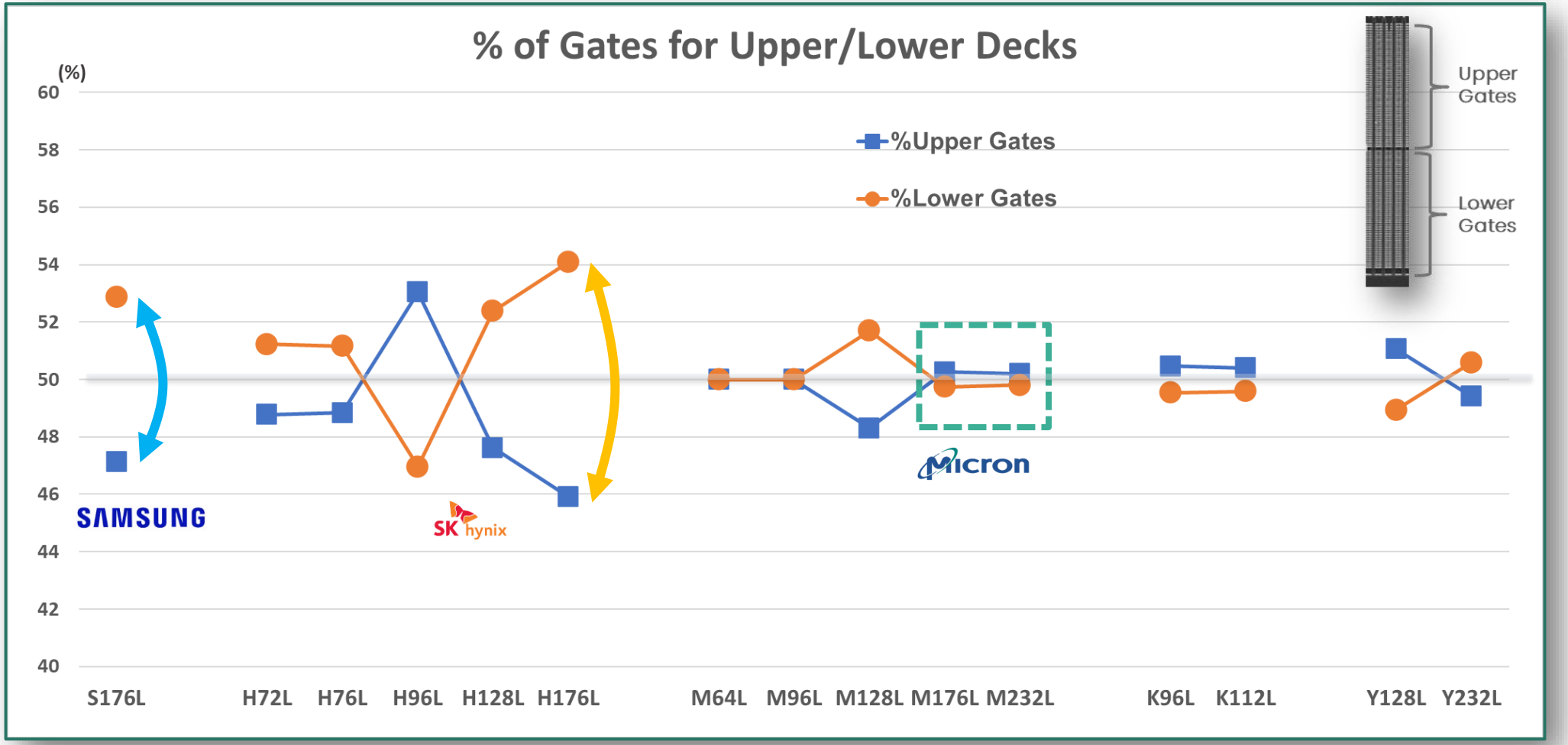


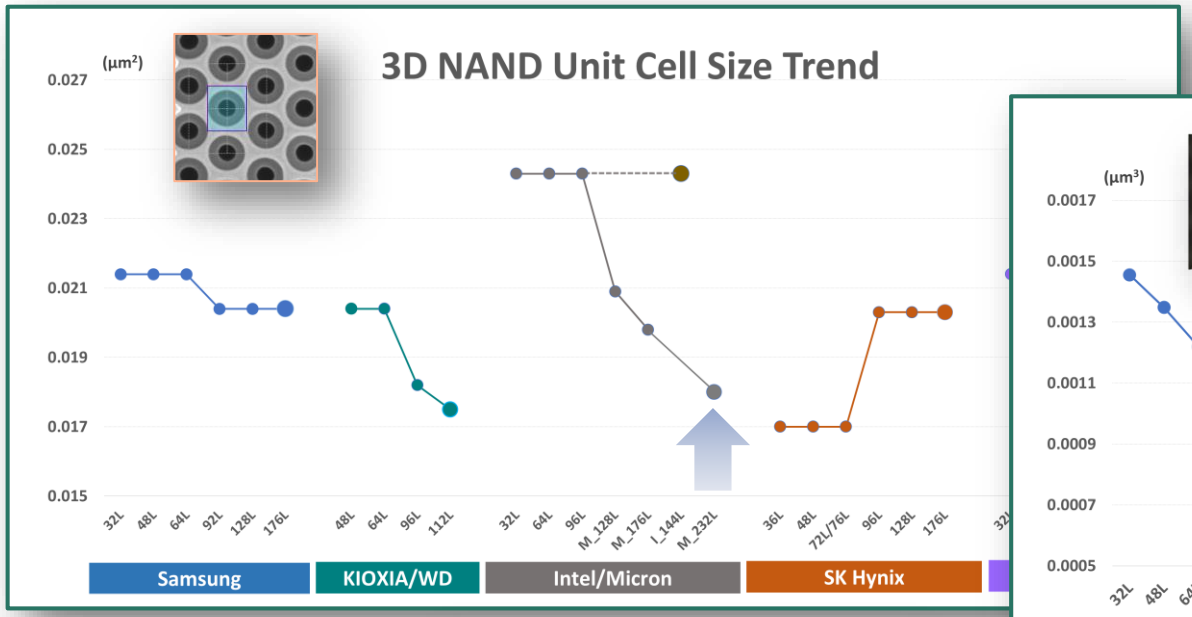
* BSSC: Back Side Source Connect

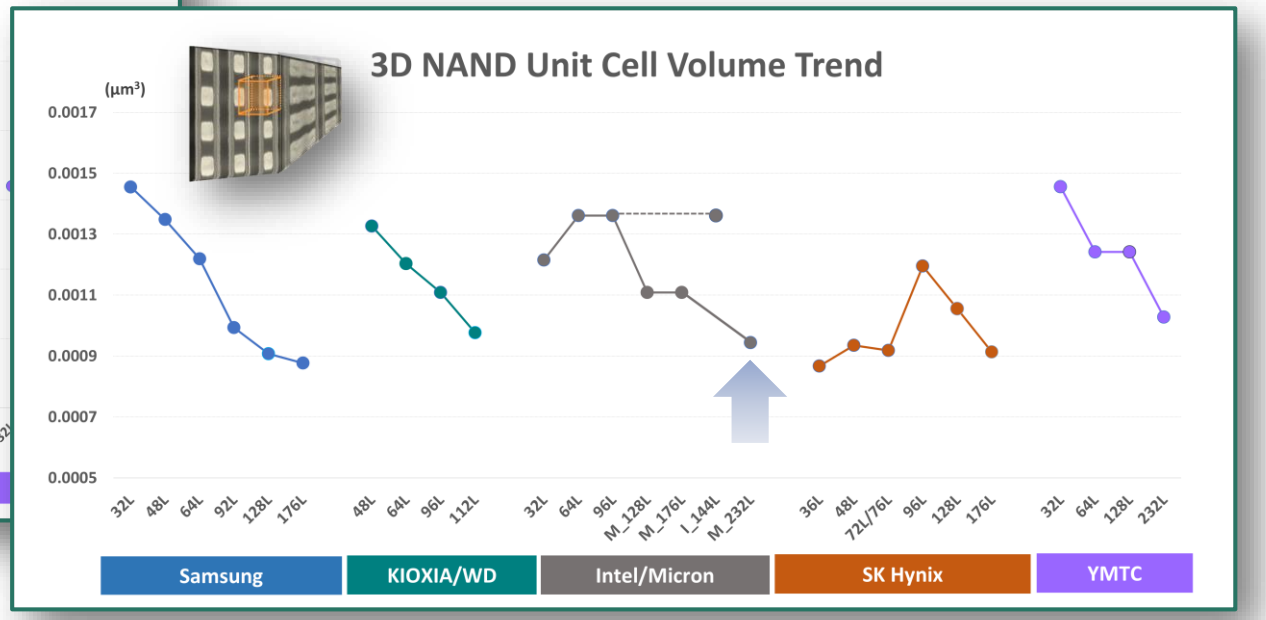


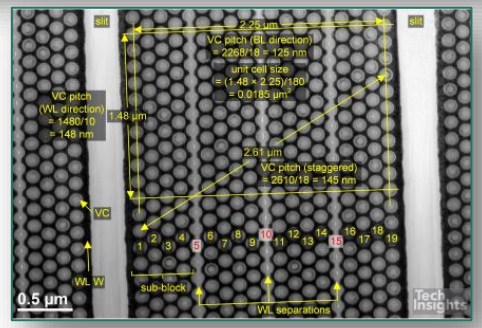
Comparison: Gate Configuration



Comparison: Unit Cell Size & Volume

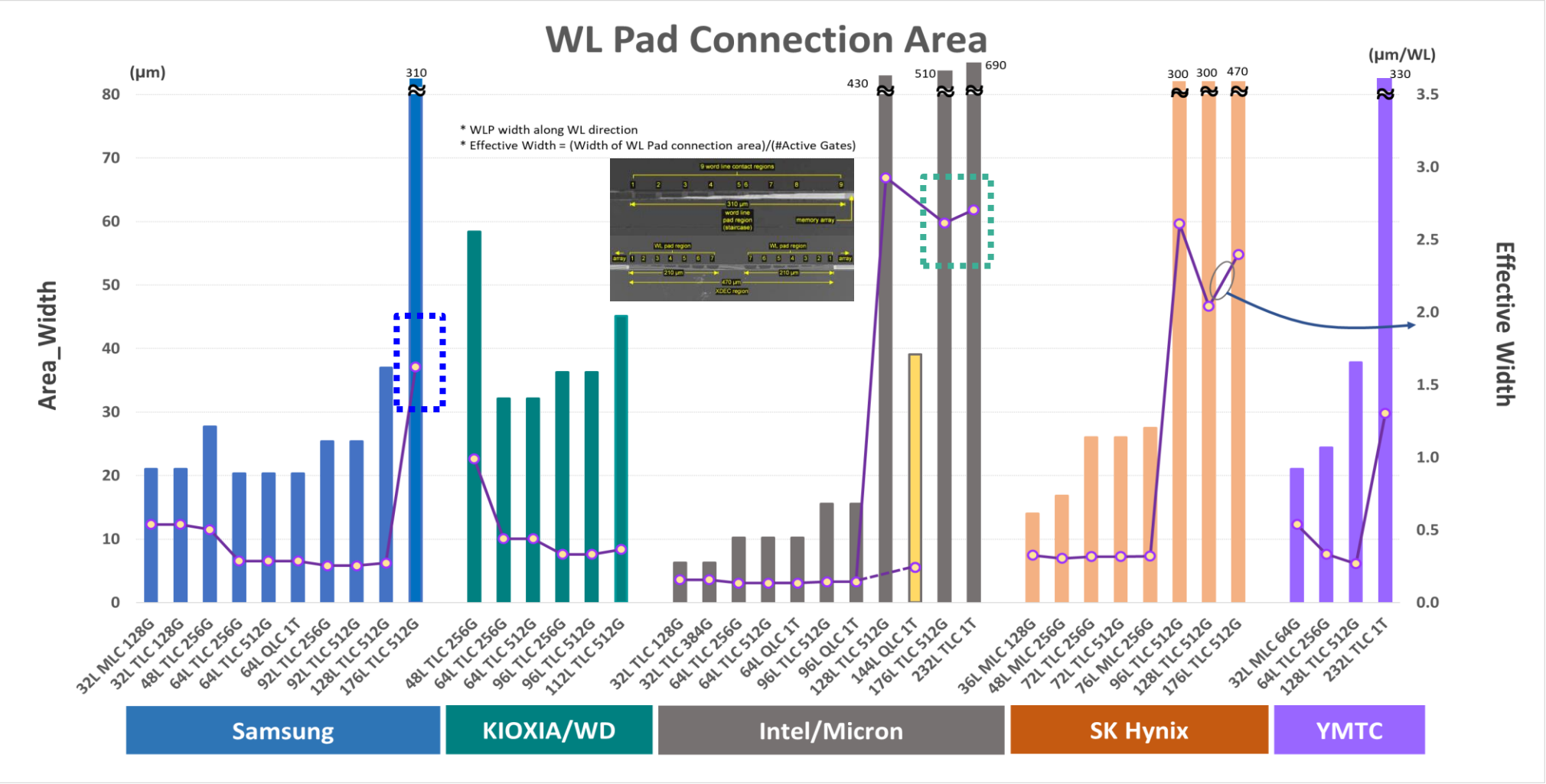






Micron: 19 rows of staggered VCs (16 Active VCs + 3 Dummy VCs)

Stair-Case WLP Layout/Width



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