Flash Memory Summit

CXL™ Memory Controllers (DRAM)

SARC-303-2 CXL Usage Models (Systems Architectures Track)

Presenter:

Tim Symons, Associate Technical Fellow
Microchip Technology Inc.

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CXL™ A Protocol For Memory

- Using PCI Express® and (PCIe®) physical and electrical interface standard
- Enables efficient high bandwidth interface between CPU, memory and accelerators
- Maintains memory coherency between CPU memory space and memory on CXL attached devices that enables resource sharing, memory disaggregation with memory pooling and sharing
- Open industry standard starting with CXL 1.0 to 3

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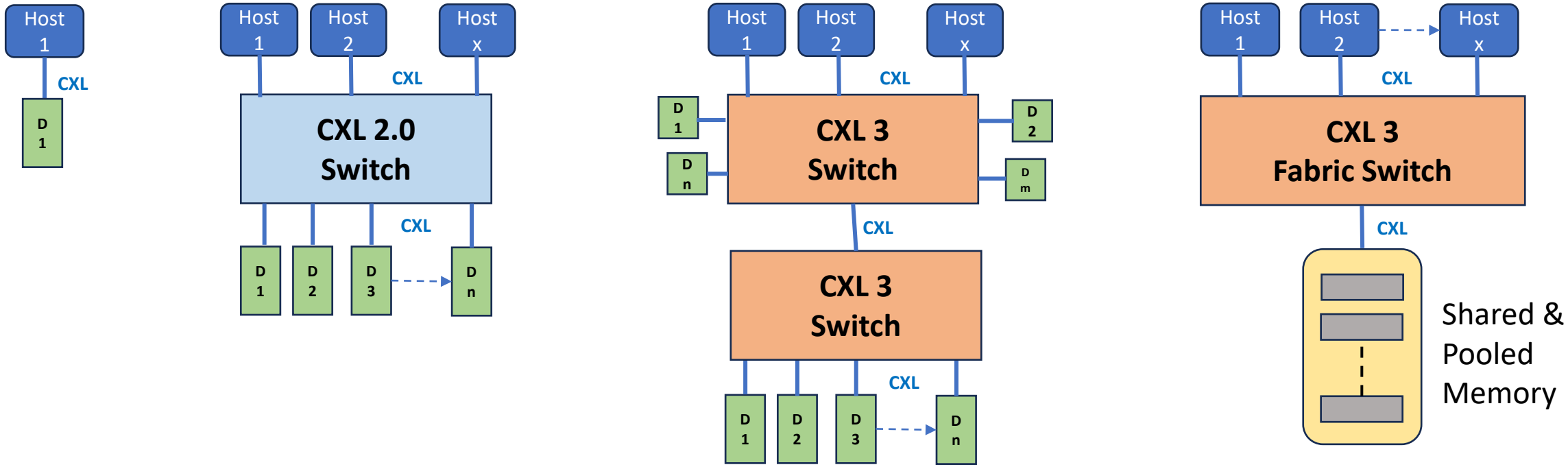
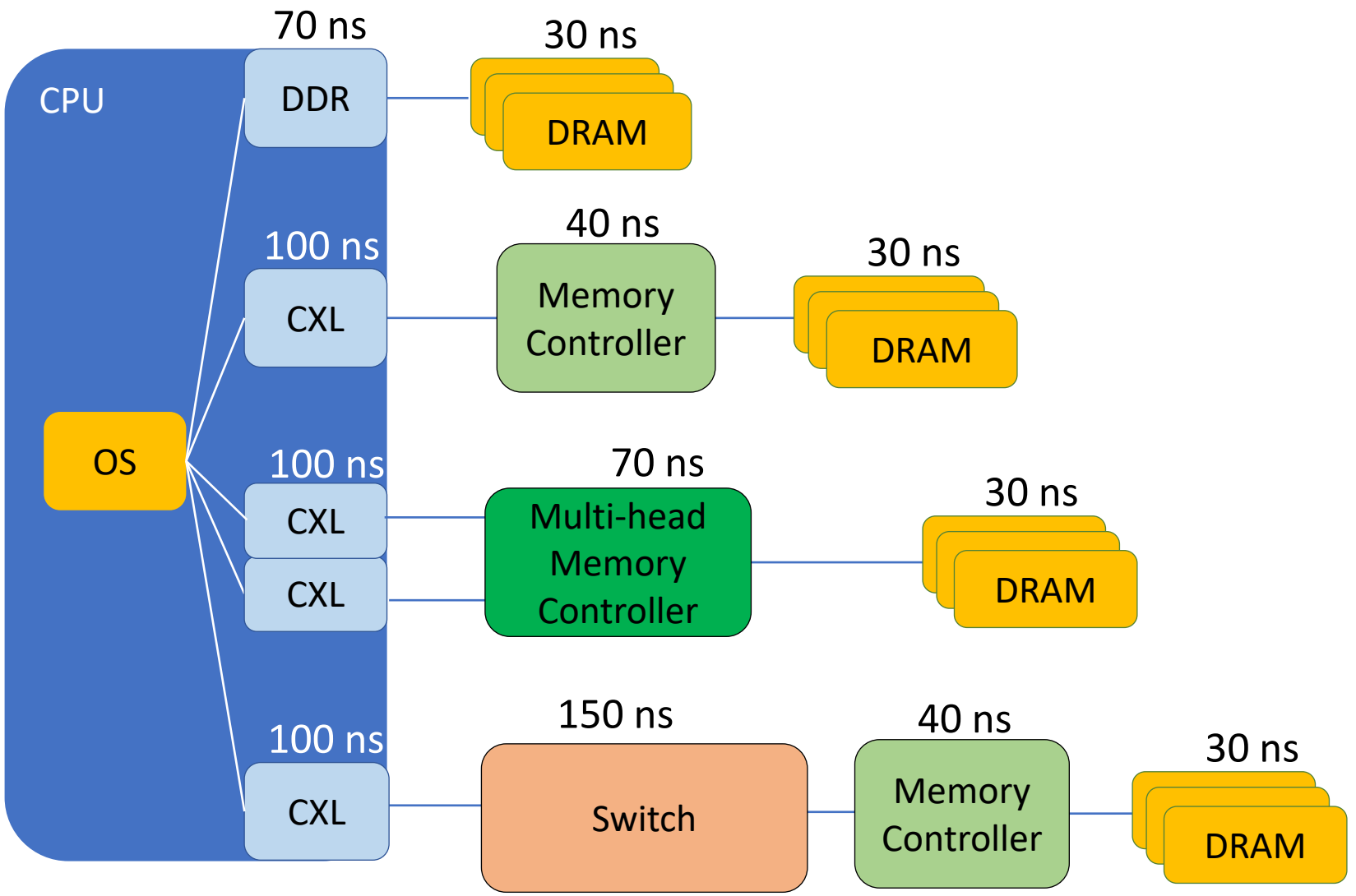
CXL™ Memory Expansion Models



CXL™ Memory Performance Comparison



Use-Case	Load to Use
Direct DDR	~100 ns
Direct CXL	~170 ns
Pooled CXL	~200 ns
Switched CXL	~320 ns

* All latencies are round trip and approximated for the purposes of comparing architectural options

CXL™ Device Types

- CXL supports different types of devices that can be interconnected using CXL interface like CPU, GPU, ASIC, FPGA, Accelerators, etc.
- Type 1
  - Processor device with shareable cache memory
  - Uses CXL.io and CXL.cache protocols
- Type 2
  - A type 1 device and has sharable data memory
  - Uses CXL.io, CXL.cache and CXL.mem protocols
- Type 3
  - Memory expansion
  - Uses CXL.io, CXL.mem protocols

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Resilience, Security and Performance

Lowest Latency Memory Controllers
Enable CXL-attached memory to be used as hot memory tier

Enterprise Class RAS (Reliability Availability Serviceability)
Advanced ECC, Data Integrity, Diagnostics, Scrub, BIST

Industry Leading Security
Secure boot with hardware root of trust
Firmware attestation
Link encryption

Ecosystem Interoperability
All CPUs, all DRAM vendors

Media Independence
Supports both DDR4 and DDR5

Lowers Total Cost of Ownership
Decreased spend per unit bandwidth
Futureproofs investment

First Instantiations of CXL™ – Memory Controllers

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EDSFF formats

9.5 mm E1.L

18 mm E1.L

E1.S

M.2

Add-in card formats

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