Flash Memory Summit

Challenges to CXL Device Test and Qualification

Justin Treon
Advantest America
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Agenda

1. Brief CXL Overview
2. Type 3 Device Progression
3. Challenges
    i. Device Isolation
        i. Call to action
    ii. Real World Testing
        i. Call to action
4. Conclusion

CXL – Compute Express Link

- Protocol types
  - CXL.cache – Adding cache to the system
  - CXL.io – Basic command protocol for functional equivalence to PCIe Gen. 5
  - CXL.mem – To adding **persistent** and **volatile** memory to the system
- Device types
  - Type 1: .cache and .io
    - Hard to implement
  - Type 2: .cache, .io, and .mem
    - Really hard to implement
  - Type 3: .io and .mem
    - Current market focus

CXL Type 3 Progression in the Industry

- CXL 1.1 is a steppingstone
  - No hot plug support
  - Limited production, investigative
- CXL 2.0 is usable, but only viable for CXL type 3 device (.mem)
  - Managed hot pluggable memory expanders
  - CXL switches
    - Memory pooling
  - Still limited production, investigative
  - No link down support
- CXL 3.0 is the first feature complete version
  - Supports link down

Challenge 1: Device Isolation (1)

- System stability are paramount to an SSD tester
  - Server response to RAM failure is to reboot
- DUT isolation is need for repeatable results
  - If a Type 3 devices is added to system memory than it will be used by the system

Challenge 1: Device Isolation (2)

- Manage Faults
  - CXL 2.0 devices are managed hot pluggable, but are likely to take down a server
    - Bad device
    - Poor insertion
  - CXL testers must keep the system up despite bad devices

Compute Express Link, Revision 2.0, October 2020

12.3 CXL Link Down Handling

There is no expectation of a graceful Link Down. A Link Down condition will most likely result in a timeout in the Host since it is quite possible that there are transactions headed to or from the CXL device that will end up not making progress.

Call to Action 1: Manage Faults

- To BIOS Developers
  - BIOS cannot just treat CXL Type 3 devices as RAM
    - Fault tolerance is needed
- To CPU/Switch Vendors
  - Features beyond CXL 2.0 specification are needed to implement CXL 2.0 in the real world
    - Bad or poorly inserted devices needs to be handled gracefully
  - Design to be tested, not just simulated
- To Driver Developers
  - Isolate and be fault tolerant

Challenge 2: Real World Testing

- CXL Type 3 devices need to be tested like RAM for volatile devices
  - Devices are byte addressed rather than by LBA
  - Assume multiple threads and data patterns
  - RAM test method need to be applied

Call to Action: New tools

- To CXL Developers and Testers
  - New performance and stability tools are needed
- To CXL Controllers
  - Allow for RAM testing similar to a RAM tester

Conclusion

- Beware limitations of CXL 1.1 and CXL 2.0
  - Fault tolerance is needed
- Beware the CXL 3.0 band wagon
  - Focus on CXL 2.0+ Type 3 devices

Q&A