

# What Exactly are SSD Low Power States and How Can They Be Tested and Measured?

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# Overview

- Understand the L1 state of the LTSSM
- Understand the L1.1 and L1.2 PM states
- Case Study 1- Measuring Power with Quarch and SerialTek
- Case Study 2- Testing Low Power with SANBlaze and SerialTek

# Understanding L1 LTSSM

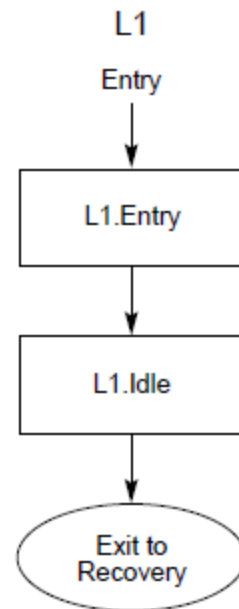
- From Section 4.2.6.8 of the PCIe 6.0 Spec it says:

“L1 is intended as a power savings state.

The L1 state allows an additional power savings over L0s at the cost of additional resume latency.

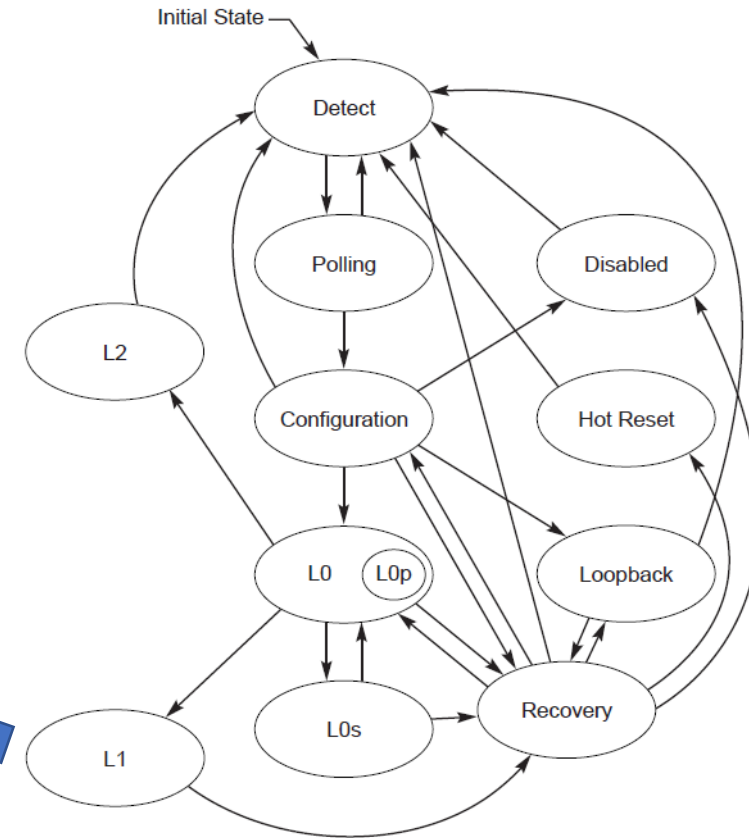
The entry to L1 occurs after being directed by the Data Link Layer and receiving an EIOS.”

- L1 only has 2 substates, L1.Entry and L1.Idle, it does **not** have L1.0/L1.1/L1.2 substates



OM13805A

Figure 4-54 L1 Substate Machine



OM13800F

Figure 4-48 Main State Diagram for Link Training and Status State Machine

# Understanding L1 LTSSM- Entry

Events	All Channels	Search...	Speed	Width	Down 0	Down LTSSM 0	Up 0	Up LTSSM 0
M...	Timestamp							
	005.543.414.878.500	Gen 4	x4					DLLP Ack (0xc67)
	005.640.793.652.000	---	---					
	005.642.394.131.125	Gen 4	x4					TLP Msg_Local (0xc43)
	005.642.394.250.375	Gen 4	x4					DLLP Ack (0xc43)
	005.642.409.966.625	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.409.972.750	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.409.978.875	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.409.984.875	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.003.250	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.009.250	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.015.375	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.021.500	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.027.625	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.033.625	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.039.750	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.045.875	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.052.000	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.058.000	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.064.125	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.070.250	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.076.375	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.082.375	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.088.500	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.094.625	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.097.625	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.097.625	Gen 4	x4					DLLP PM_Request_Ack

1. Device sends PM DLLP Requesting L1

2. Host responds with PM DLLP Acknowledging the request

Events	All Channels	Search...	Speed	Width	Down 0	Down LTSSM 0	Up 0	Up LTSSM 0
M...	Timestamp							
	005.642.410.201.250	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.204.250	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.210.375	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.210.375	Gen 4	x4					DLLP PM_Active_State_Request_L1
	005.642.410.211.375	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.212.375	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.213.375	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.214.500	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.215.500	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.216.500	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.217.500	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.226.625	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.227.625	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.228.625	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.229.625	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.230.000	---	---					1 x EIOS
	005.642.410.230.000	---	---					Electrical Idle Start
	005.642.410.230.000	---	---					LTSSM L1.Entry from L0
	005.642.410.230.000	---	---					LTSSM L1.0 from PowerManagementInitialState
	005.642.410.230.750	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.231.750	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.232.750	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.233.750	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.242.875	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.243.875	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.244.875	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.245.875	Gen 4	x4					DLLP PM_Request_Ack
	005.642.410.247.000	Gen 4	x4					DLLP PM_Request_Ack

3. EIOS Ordered Set to transition into L1 sent by the device

4. Device is now sending Electrical Idle as part of L1

# Understanding L1 LTSSM- Exit

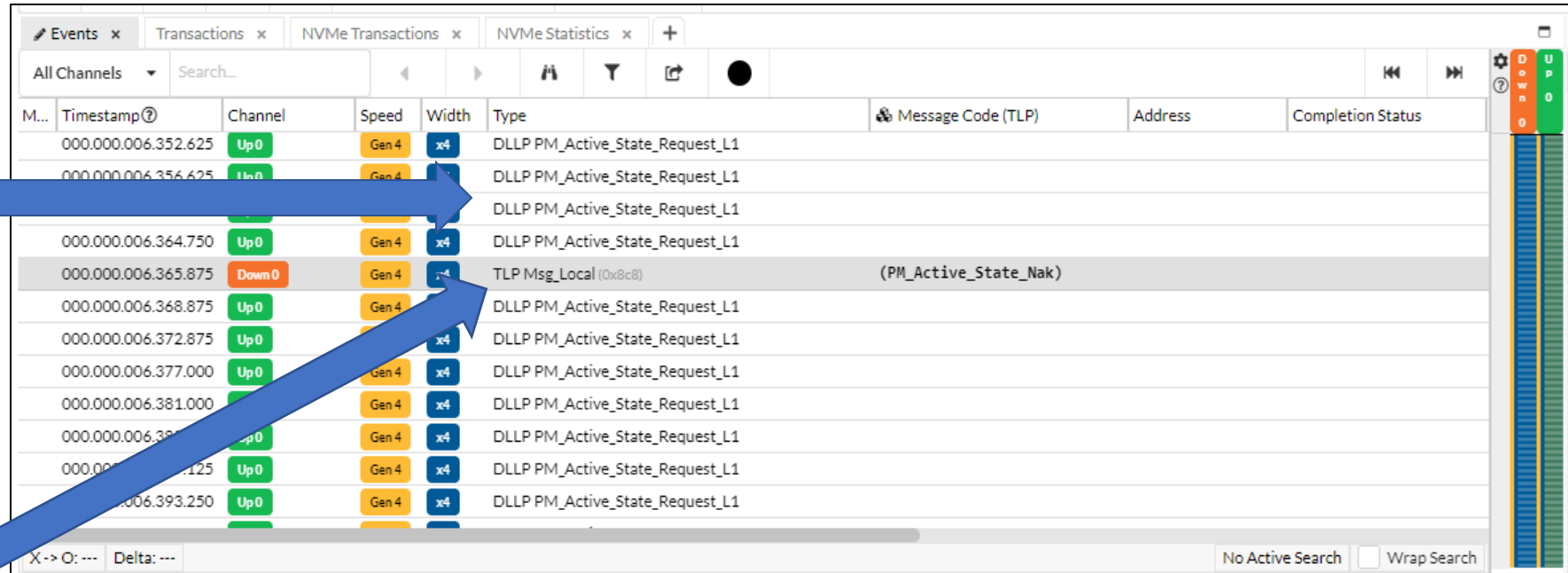
Events x Transactions x NVMe Transactions x NVMe Statistics x +									
All Channels		Search...							
M...	Timestamp?	Speed	Width	Down 0	Down LTSSM 0	Up 0	Up LTSSM 0	Completion Status	
	006.099.245.076.125	Gen 4	x4					DLLP PM_Request_Ack	
	006.099.245.077.250	Gen 4	x4					DLLP PM_Request_Ack	
	006.099.245.078.250	Gen 4	x4					DLLP PM_Request_Ack	
	006.099.245.079.250	Gen 4	x4					DLLP PM_Request_Ack	
	006.099.245.080.250	Gen 4	x4					DLLP PM_Request_Ack	
	006.099.245.174.750	Gen 4	x4					1 x EIOS	
	006.099.245.183.000	Gen 4	x4					Electrical Idle Start	
	006.099.245.183.000	---	---					LTSSM L1.Entry from L0	
	006.099.245.183.000	---	---					LTSSM L1.0 from PowerManagementInitia	
	006.099.245.203.000	---	---					LTSSM L1.Idle from L1.Entry	
	006.103.689.958.000	Gen 4	x4					Electrical Idle End	
	006.103.689.958.000	---	---					LTSSM Recovery.RcvrLock from Recove	
	006.103.689.966.125	Gen 4	x4					644 x TS1	
	006.103.690.031.000	---	---					LTSSM Recovery.RcvrCfg from Recover	
	006.103.695.365.000	Gen 4	x4					1950 x TS1	
	006.103.711.749.500	Gen 4	x4					1951 x TS1	
	006.103.728.139.500	Gen 4	x4					1951 x TS1	
	006.103.744.531.625	Gen 4	x4					1949 x TS1	
	006.103.760.001.500	Gen 4	x4					1950 x TS1	

Device leaves  
Electrical Idle  
and starts  
Sending TS1  
Ordered Sets.

# Understanding L1 LTSSM-Nak

PM DLLP  
Requesting L1

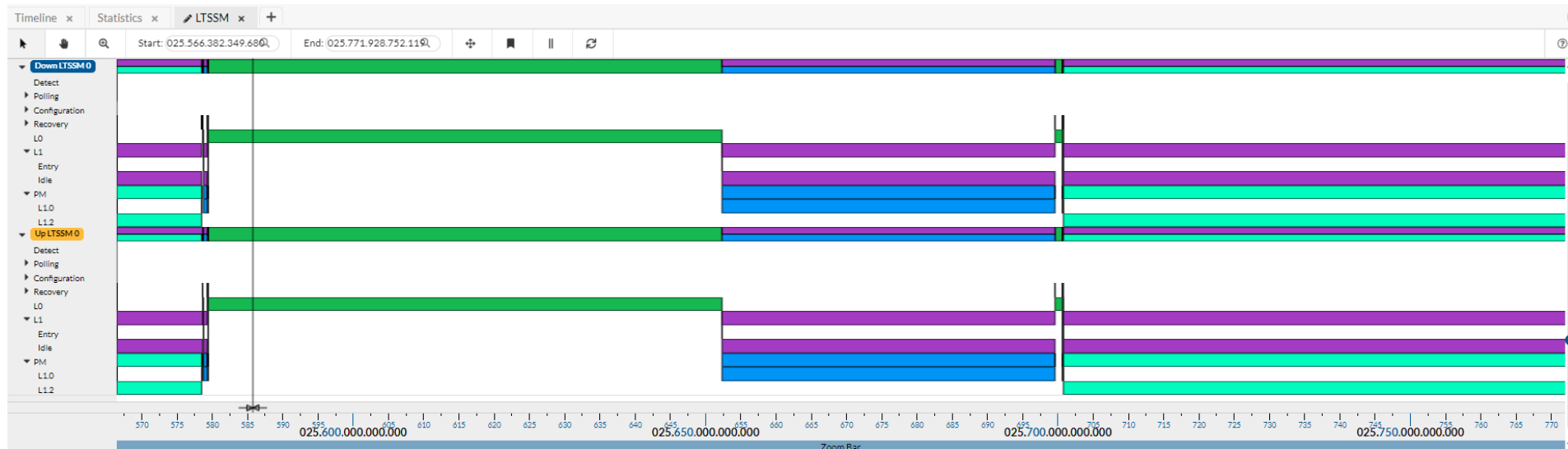
Message TLP Nak  
to reject the  
request



M...	Timestamp	Channel	Speed	Width	Type	Message Code (TLP)	Address	Completion Status
	000.000.006.352.625	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			
	000.000.006.356.625	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			
					DLLP PM_Active_State_Request_L1			
	000.000.006.364.750	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			
	000.000.006.365.875	Down0	Gen 4	x4	TLP Msg_Local (0x8c8)	(PM_Active_State_Nak)		
	000.000.006.368.875	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			
	000.000.006.372.875	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			
	000.000.006.377.000	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			
	000.000.006.381.000	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			
	000.000.006.381.125	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			
	000.000.006.393.250	Up0	Gen 4	x4	DLLP PM_Active_State_Request_L1			

# Understanding L1.1/L1.2 PM States

- Section 5.1 explains about Power Management (PM) states.
  - D states are associated with a particular Function
  - L states are associated with a particular Link
- L states contain the following states
  - L0 is the operational state
  - L0p is a reduced power sub-state of L0
  - L0s, L1, L1.0, L1.1 and L1.2 are various low power states



# Understanding L1.1/L1.2 PM States

- **L1.0** substate
  - The L1.0 substate corresponds to the conventional L1 Link state. This substate is entered whenever the Link enters L1. The L1 PM Substate mechanism defines transitions from this substate to and from the L1.1 and L1.2 substates.
  - The Upstream and Downstream Ports must be enabled to detect Electrical Idle exit as required in § Section 4.2.7.7.2 .
- **L1.1** substate
  - Link common mode voltages are maintained.
  - Uses a bidirectional open-drain clock request (CLKREQ#) signal for entry to and exit from this state.
  - The Upstream and Downstream Ports are not required to be enabled to detect Electrical Idle exit.
- **L1.2** substate
  - Link common mode voltages are not required to be maintained.
  - Uses a bidirectional open-drain clock request (CLKREQ#) signal for entry to and exit from this state.
  - The Upstream and Downstream Ports are not required to be enabled to detect Electrical Idle exit.

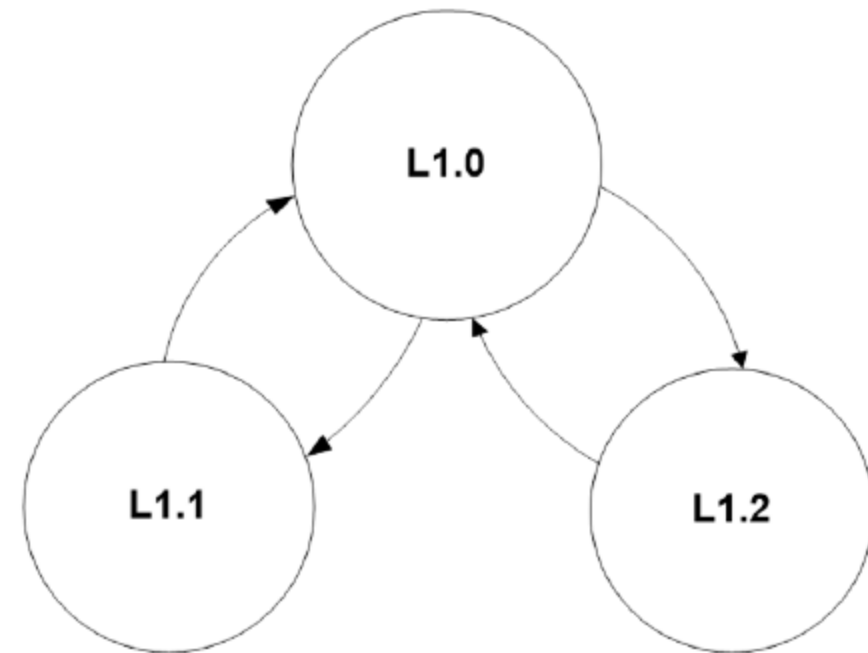


Figure 5-9 State Diagram for L1 PM Substates



# Understanding L1 PM Register Example

L1 PM Substate Extended Capability register is used when enabling the PM substate.

Details

Config Space

Memory Space

Bookmarks

Find All

+

Display

23:00.0

◀

▶

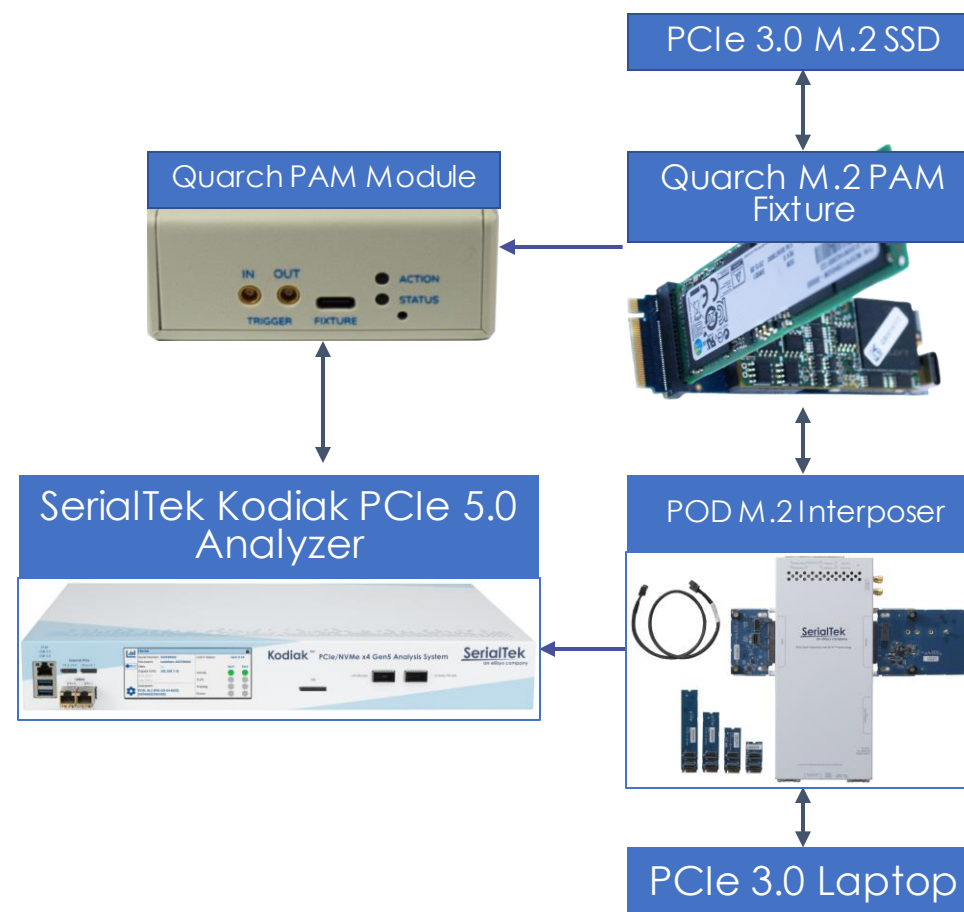
061.034.856.814.000

– L1 PM Substates v1 (ID: 30) @ 0x0110

Hex	7	6	5	4	3	2	1	0
0	Capability ID 001e							
1								
2	Next Capability Offset 128				Capability Version 1			
3								
4	Reserved 0	Link Activation Supported 0	L1 PM Substates Supported 1	ASPM L1.1 Supported 1	ASPM L1.2 Supported 1	PCI-PM L1.1 Supported 1	PCI-PM L1.2 Supported 1	
5	Port Common_Mode_Restore_Time 0a							
6	Port T_POWER_ON Value 03				Reserved 0	Port T_POWER_ON Scale 2 (100 us)		
7	Reserved 00							
8	Reserved 0	Link Activation Control 0	Link Activation Interrupt Enable 0	ASPM L1.1 Enable 0	ASPM L1.2 Enable 0	PCI-PM L1.1 Enable 0	PCI-PM L1.2 Enable 0	
9	Common_Mode_Restore_Time 00							
10	LTR_L1.2_THRESHOLD Value 001							
11	LTR_L1.2_THRESHOLD Scale 3			Reserved 0				
12	T_POWER_ON Value 03				Reserved 0	T_POWER_ON Scale 2 (100 us)		
13	Reserved 000000							
15								
16	Reserved ---							Link Activation Status ---
19								

# Case Study 1

- Goal
  - Understand the Power savings in a laptop environment
- Tools Used
  - PCIe 3.0 Laptop
  - PCIe 3.0 M.2 SSD
  - Quarch Power Analysis Module with PCIe4.0 M.2 PAM Fixture
  - SerialTek Kodiak PCIe Analyzer
- Software
  - lspci & setpci
  - Quarch Power Studio
  - SerialTek BusXpert

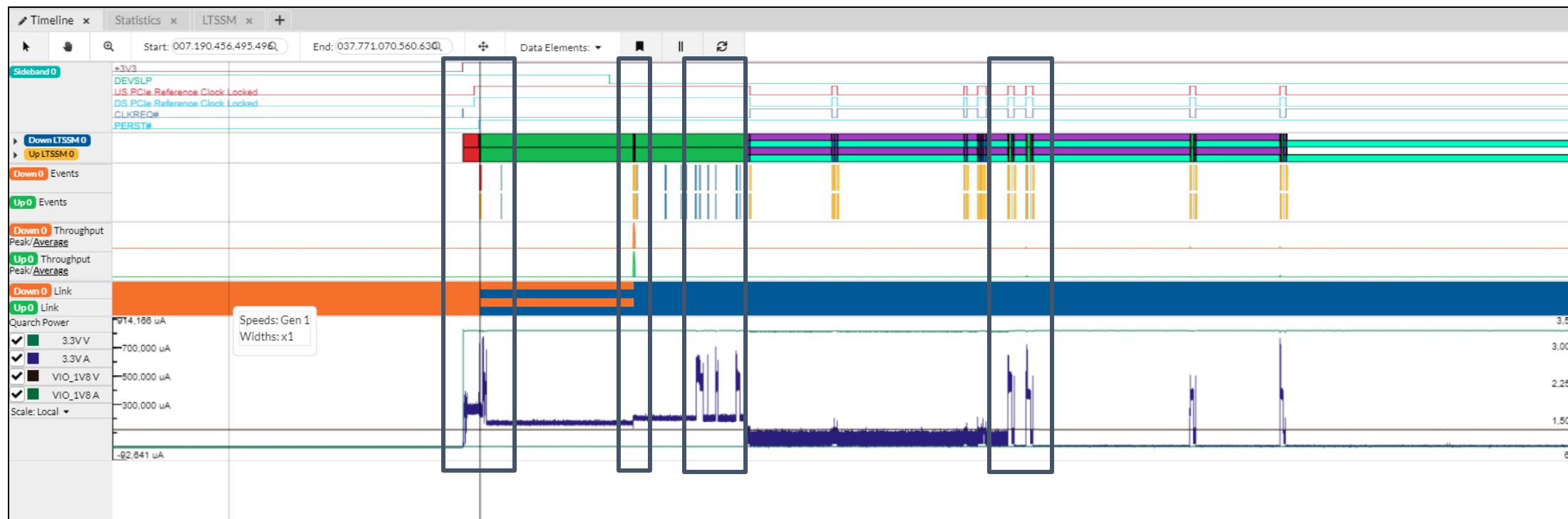


# Case Study 1

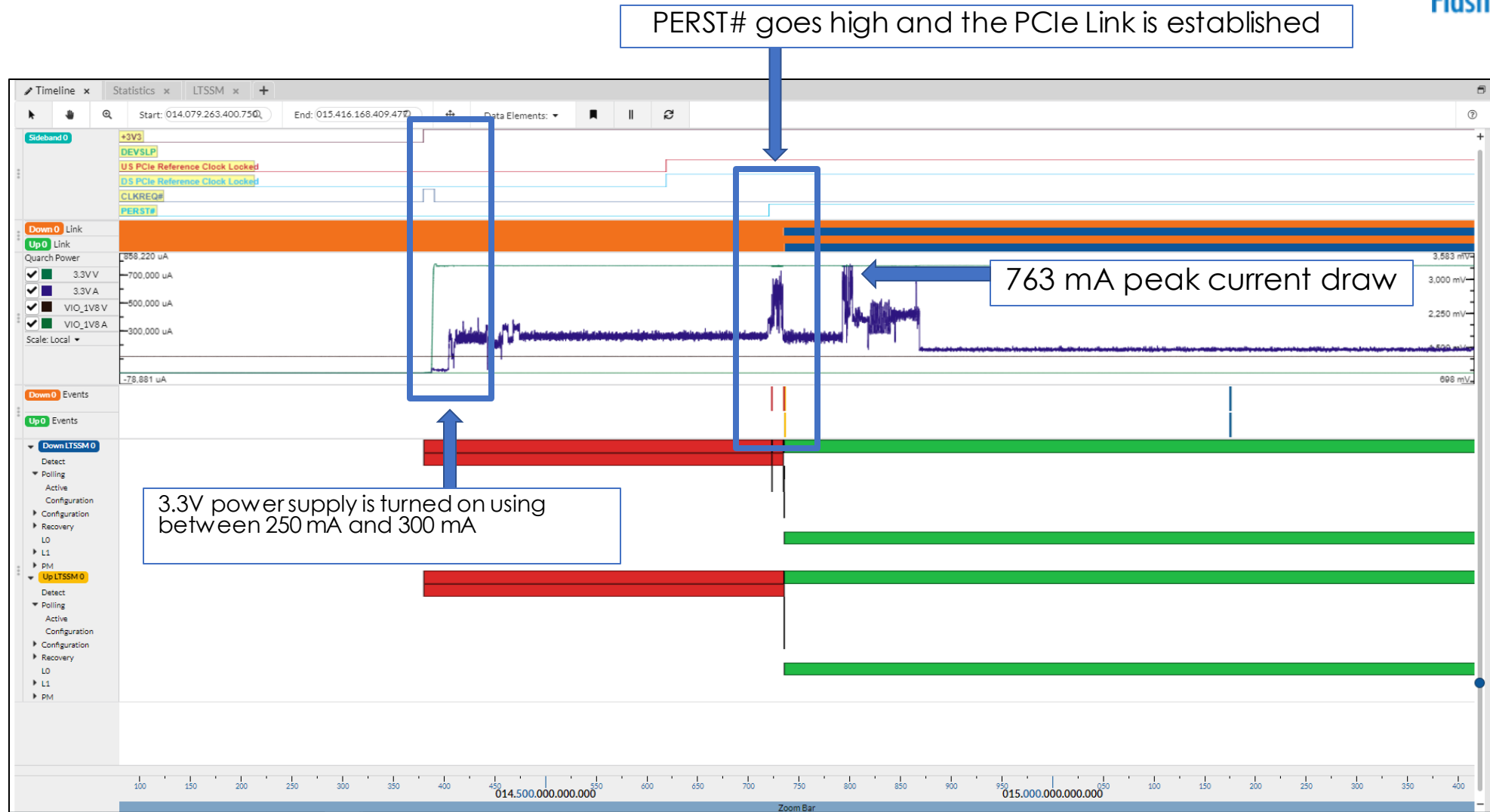
Capture a bootup of the laptop until the OS fully loads.

Let's look closer at the following:

- When 3.3V is first applied
- Speed change
- At some of the current spikes
- L1 Transitions



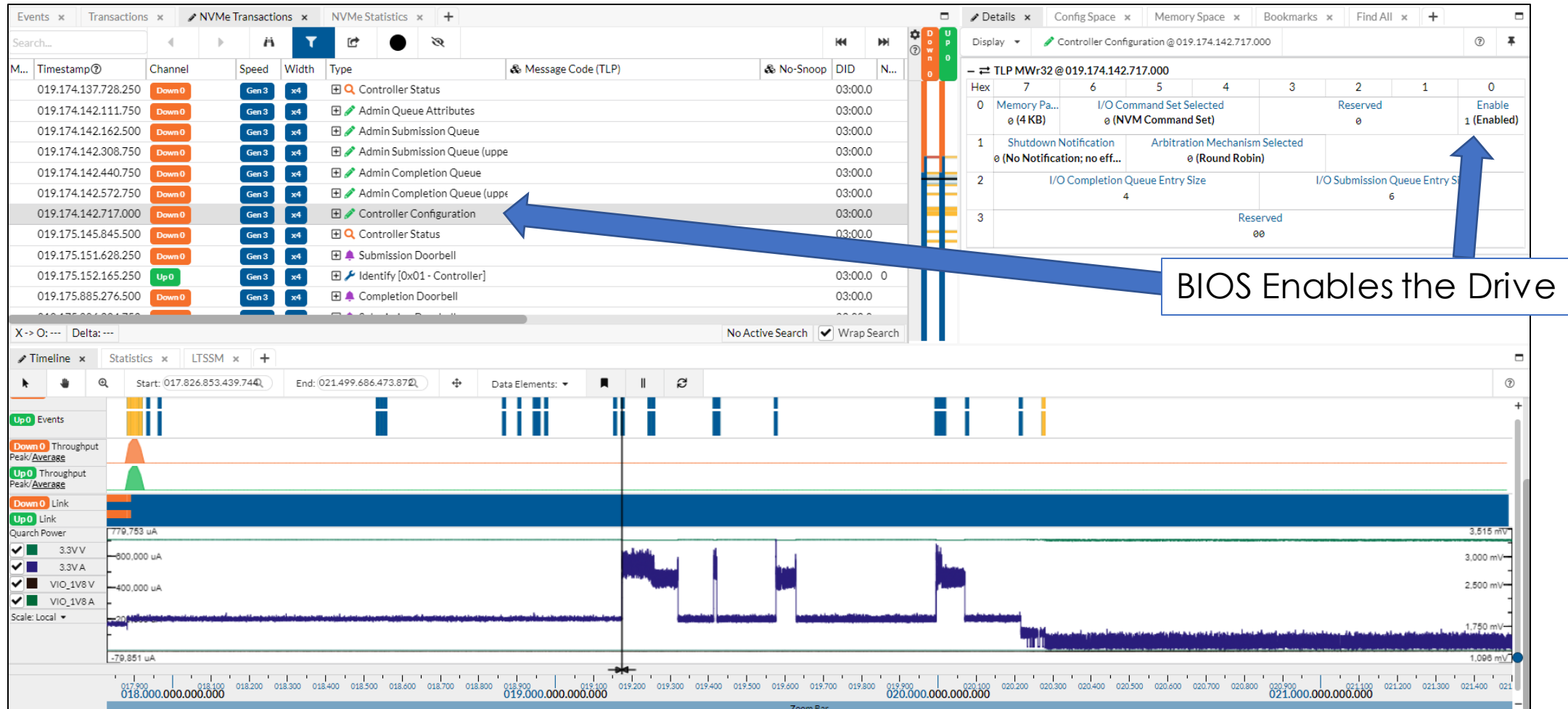
# Case Study 1- Power On



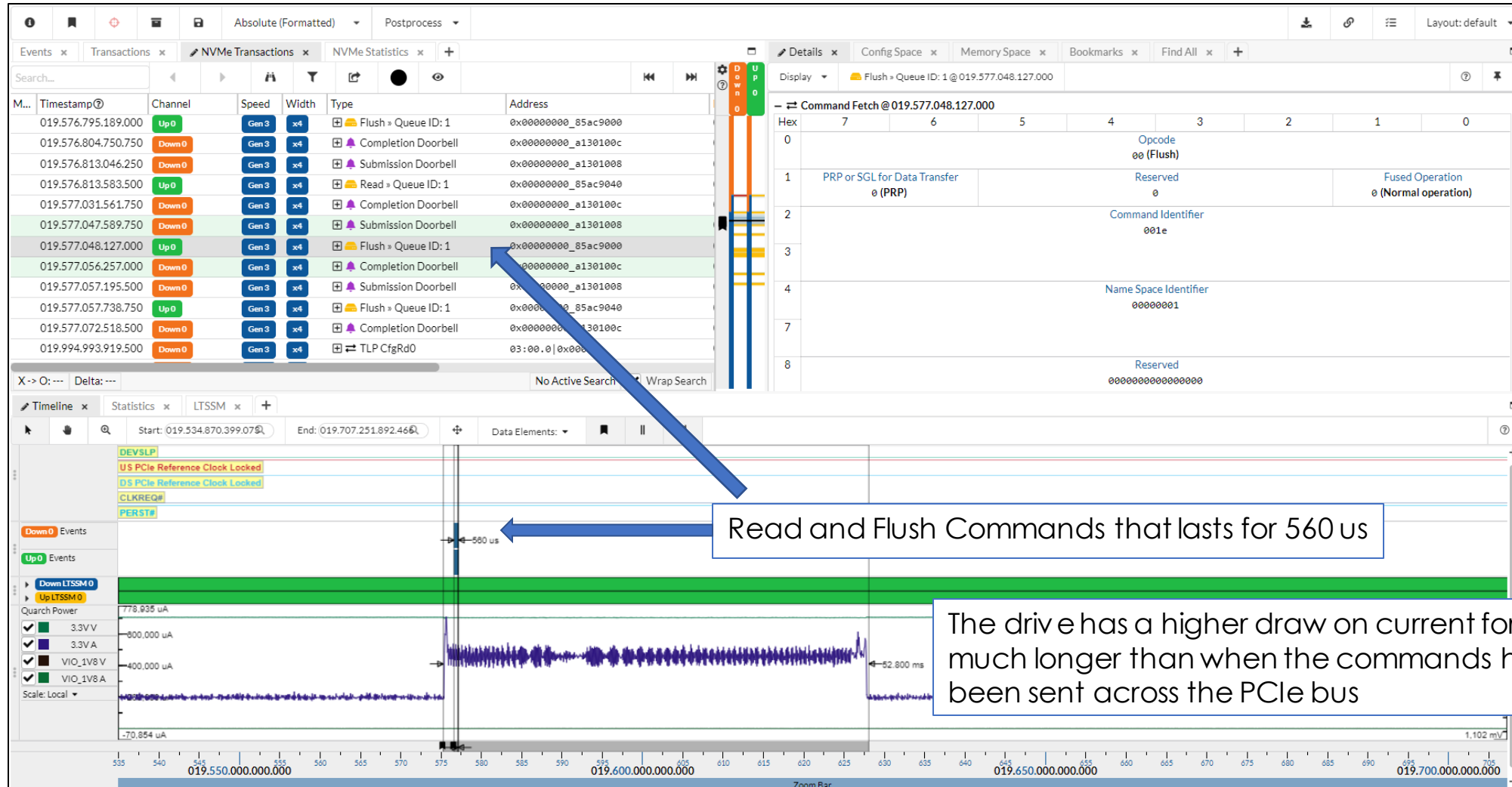
# Case Study 1- Speed Change to Gen3



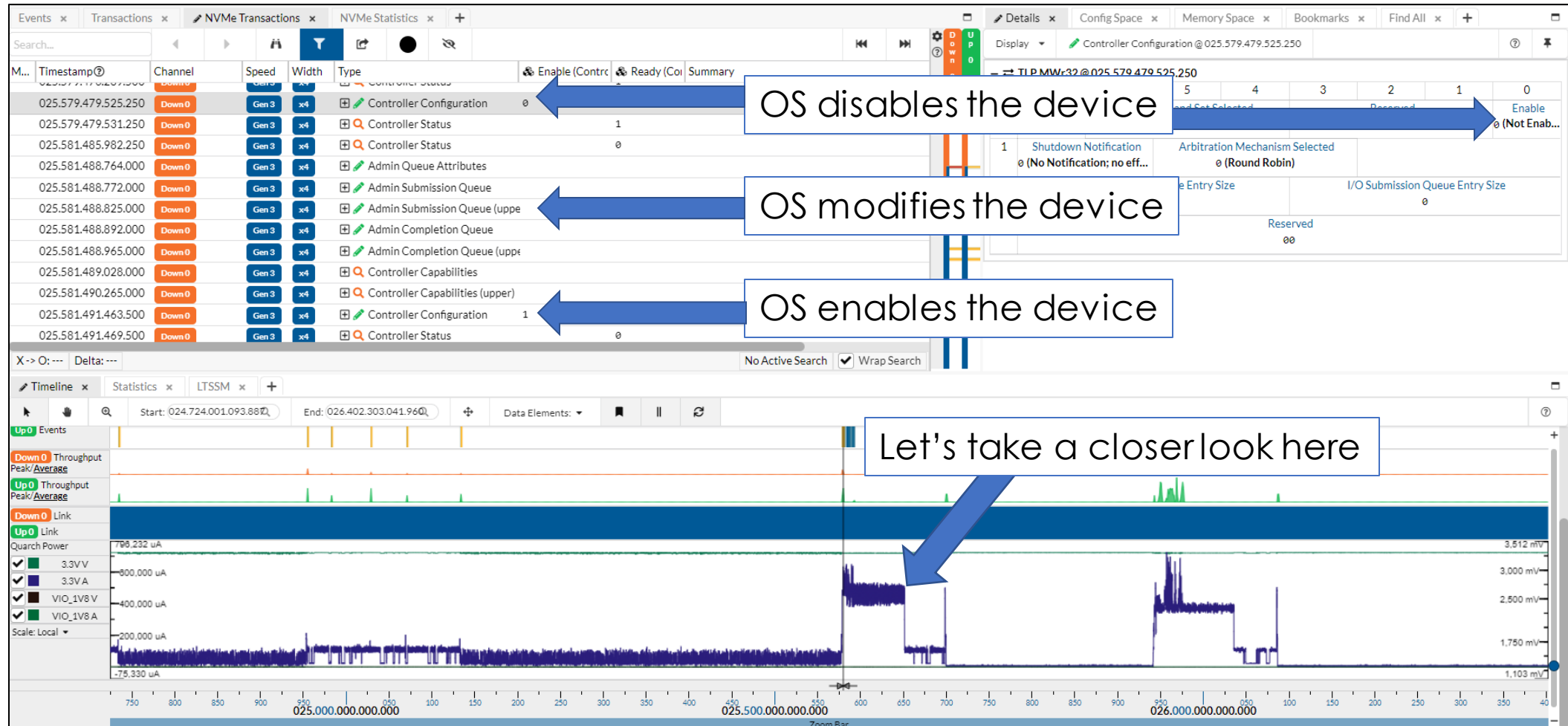
# Case Study 1- Analyzing Spike



# Case Study 1

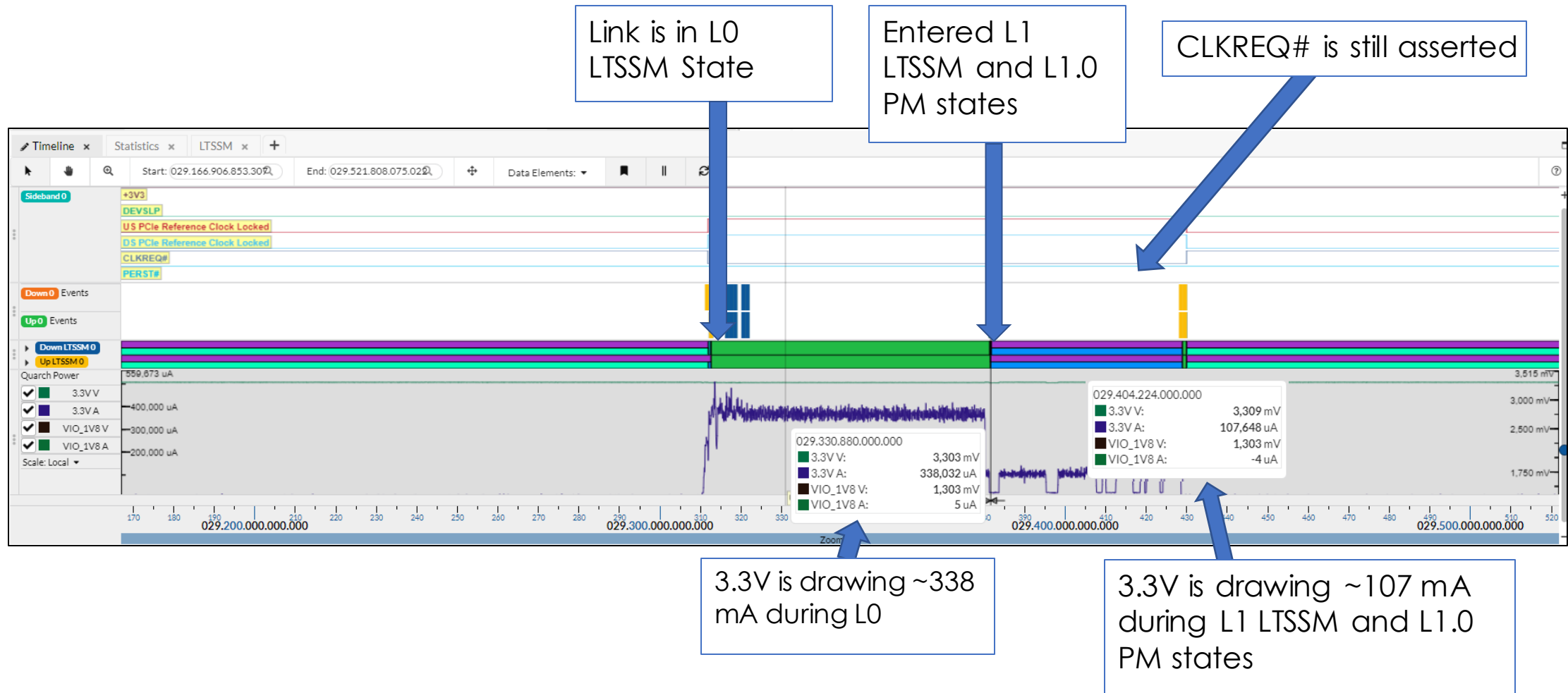


# Case Study 1- OS Configures the Device





# Case Study 1- Closer Look



# Case Study 1- Understanding LTR

- Why is CLKREQ# still asserted?
- From section “5.5.1 Entry Conditions for L1 PM Substates and L1.0 Requirements”
  - “When in ASPM L1.0 and the ASPM L1.2 Enable bit is Set, the L1.2 substate must be entered when CLKREQ# is deasserted and all of the following conditions are true:”
    - “The reported snooped LTR value last sent or received by this Port is greater than or equal to the value set by the LTR\_L1.2\_THRESHOLD Value and Scale fields, or there is no snoop service latency requirement.”
    - “The reported non-snooped LTR last sent or received by this Port value is greater than or equal to the value set by the LTR\_L1.2\_THRESHOLD Value and Scale fields, or there is no non-snoop service latency requirement.”

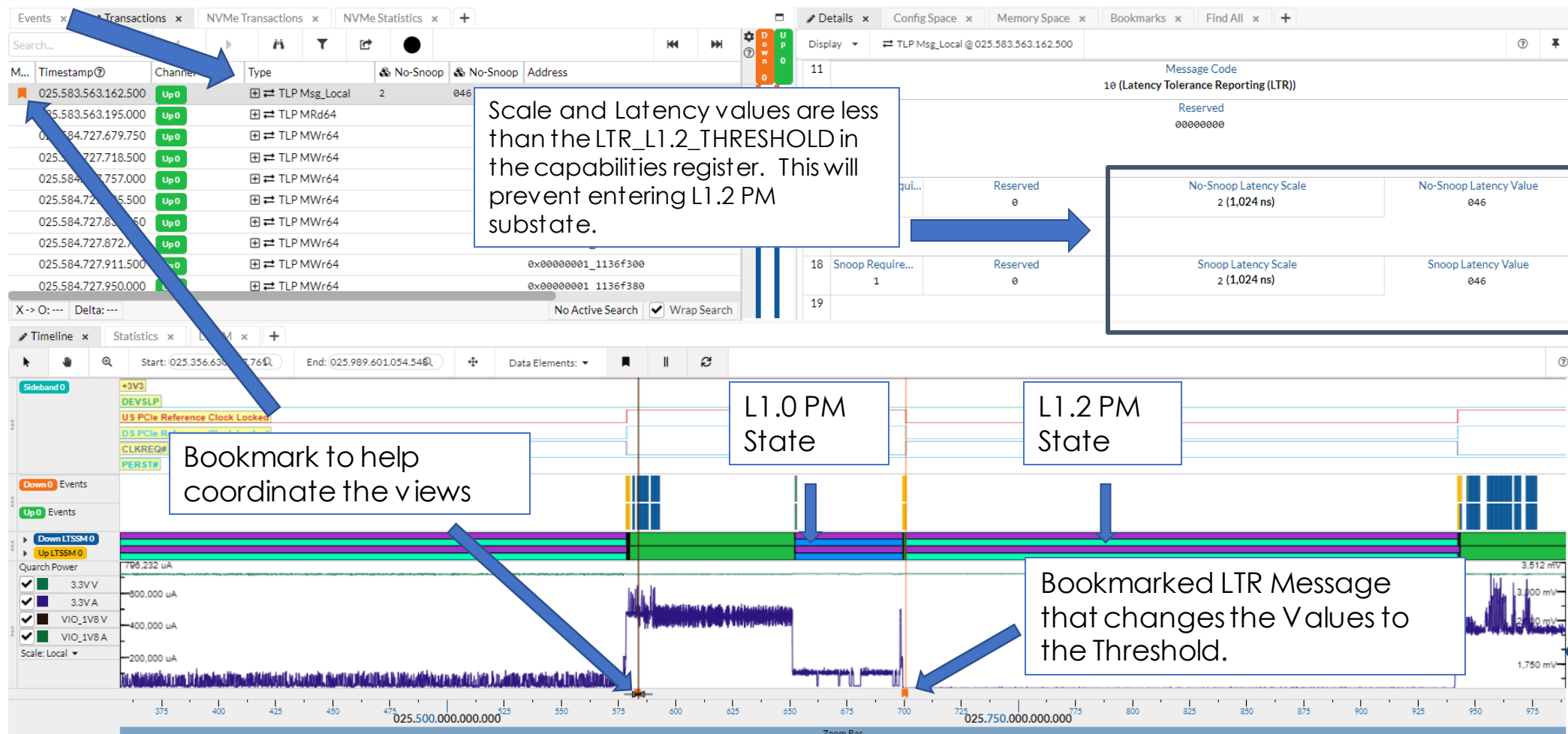
# Case Study 1- LTR Message TLPs Decoded

11			<div>Message Code 10 (Latency Tolerance Reporting (LTR))</div>		<div>Used to determine how the rest of the data is decoded. In this case it is a LTR message as shown below.</div>
12			<div>Reserved 00000000</div>		
15					
16	No-Snoop Requi... 1	Reserved 0	<div>No-Snoop Latency Scale 2 (1,024 ns)</div> <div>No-Snoop Latency Value 046</div>		
17			<div>Compared to the LTR_L1.2_THRESHOLD_Scale for L1.2</div>		
18	Snoop Require... 1	Reserved 0	<div>Snoop Latency Scale 2 (1,024 ns)</div> <div>Snoop Latency Value 046</div>		
19					

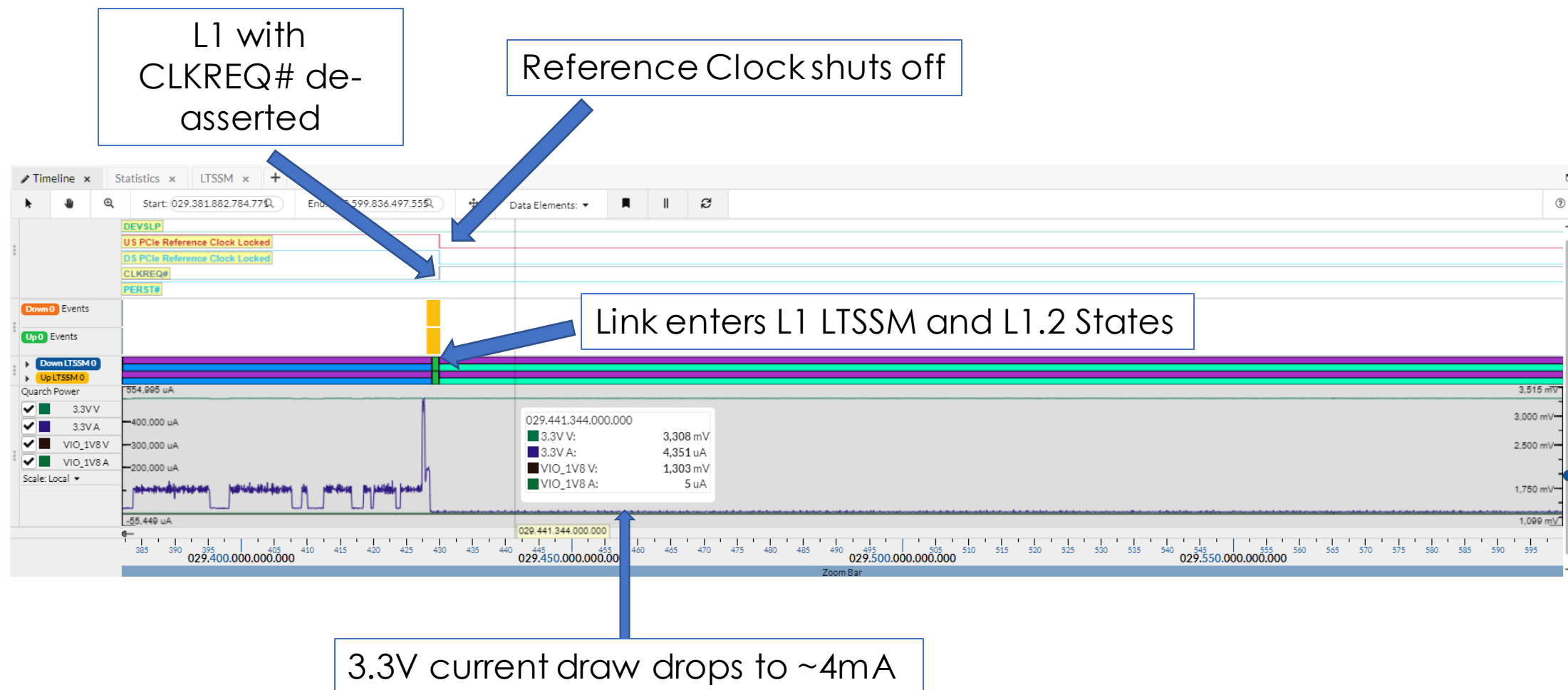


# Case Study 1- LTR and L1.2

## LTR Message TLP



# Case Study 1- Closer Look at L1.2



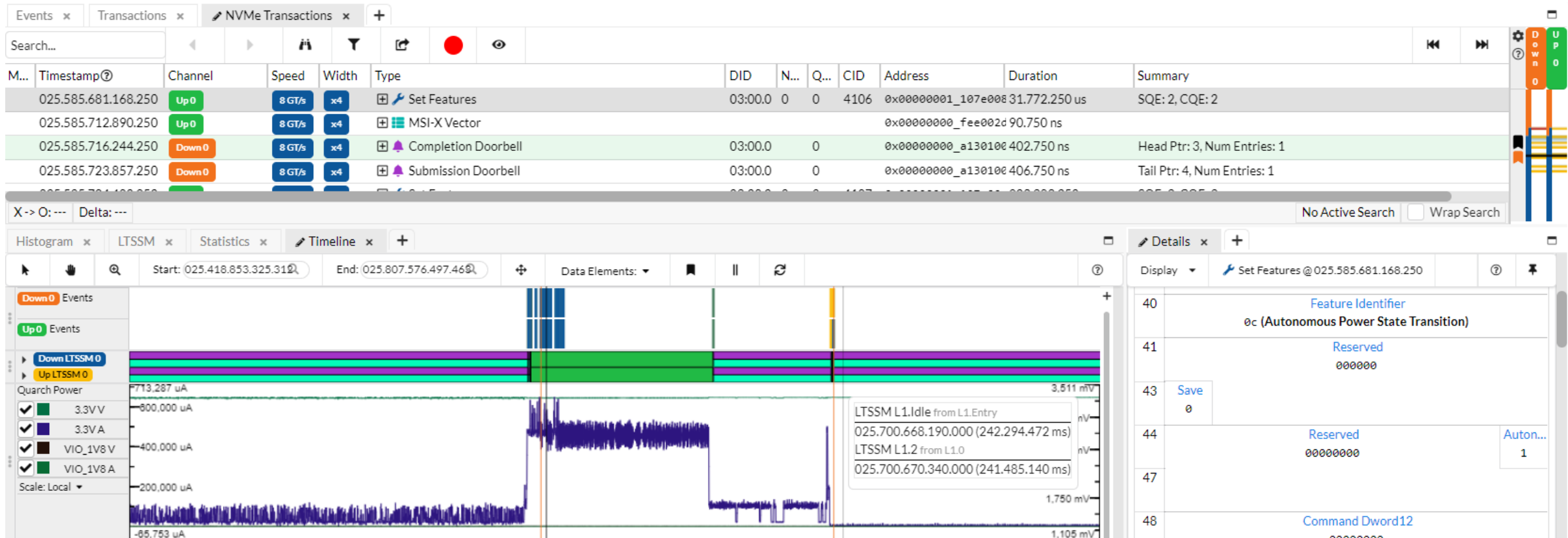
# Case Study 1- Power Observations

LTSSM and PM State	Average 3.3V Current draw
L0 LTSSM	380 mA
L1 LTSSM and L1.0 PM State	107 mA
L1 LTSSM and L1.2 PM State	4 mA

- Observation 1: By turning on ASPM L1, the drive can reduce its current draw by 71.8%.
- Observation 2: going into L1.2 PM substate the drive can reduce its current draw by almost 98.9% versus when operating at the L0 state

# Case Study 1- Power Observations

- Observation: The host used the Set Features command to tell the device to enable Autonomous Power State Transition. Once the device returned to L1.2 the power draw was lower and more consistent.



L1.2 with inconsistent power draw

L1.2 with lower consistent power draw

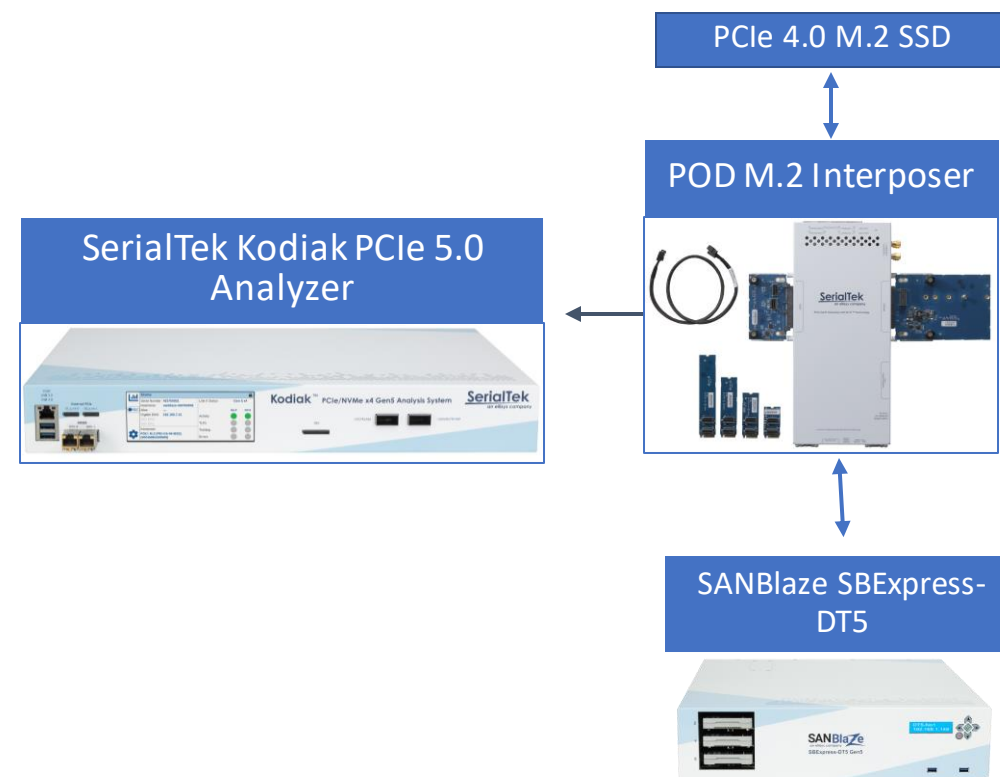


# Case Study 1- Other Observations

- When changing speeds that the link operates, the device uses more current.
- By enabling features, this also creates temporary demands on the amount of power the drive consumes.
- Different types of drive operations (i.e. flush command) can also impact the power the drive consumes even when the link activity of the PCIe bus is inactive (sending idle data, flow control DLLPs and skip OS)
- Latency Tolerance Reporting can impact if the device can enter L1.2 PM state which can reduce the power savings of the device.

# Case Study 2

- Goal
  - **Test a design to verify that they properly enter lower power states**
- Tools Used
  - SerialTek Kodiak PCIe 5.0 Analyzer + POD interposer configured for M.2
  - SANBlaze SBExpress-DT5
  - PCIe 4.0 M.2 SSD
- Software
  - SerialTek BusXpert
  - SANBlaze



# Case Study 2- Test Scripts

The following scripts are available in the SANBlaze V10.5 software package.

- PM\_L1\_Substate\_Verify.sh
- PM\_L0\_Enable.sh
- PM\_L1.1\_Enable.sh
- PM\_L1.2\_Enable.sh
- PM\_L1\_Enable.sh

All scripts are variations of the first script PM\_L1\_Substate\_Verify.sh, which walks the DUT from L0.Active to L1.Idle to L1.1 and L1.2. The variations are as follows:

- PM\_PM\_L0\_Enable.sh - Restores the device to L0.Active state
- L1.1\_Enable.sh - Leaves the device in L1.1 state
- PM\_L1.2\_Enable.sh - Leaves the device in L1.2 state
- PM\_L1\_Enable.sh - Leaves the device in L1 (L1.0) state

# Case Study 2- Test Setup

Certified by SANBlaze [ShowTestManager](#)

IOL OCP SANBlaze **User** TestMgr

ExampleScripts/PCIE\_Common\_Clock\_With\_SSC.sh  
ExampleScripts/PM\_CLKREQ\_L\_Toggle.sh  
ExampleScripts/PM\_L0\_Enable.sh  
ExampleScripts/PM\_L1.1\_Enable.sh  
ExampleScripts/PM\_L1.1\_Verify.sh  
ExampleScripts/PM\_L1.2\_Enable.sh  
ExampleScripts/PM\_L1.2\_Verify.sh  
ExampleScripts/PM\_L1\_Enable.sh  
☒ ExampleScripts/PM\_L1\_Substate\_Verify.sh

**Selected Certification Tests**

ExampleScripts  
◦ ExampleScripts/PM\_L1\_Substate\_Verify.sh

System Index	NVMe Initiator	Controller	Namespace	# of Passes	Pass Time	Action	Restore Suite
<input checked="" type="radio"/> 1 <input type="radio"/> All	<input checked="" type="radio"/> 0 <input type="radio"/> All	<input checked="" type="radio"/> 101 <input type="radio"/> All	<input checked="" type="radio"/> 1 <input type="radio"/> All	1	0	<input checked="" type="checkbox"/> Level1 <input type="checkbox"/> Level2 <input type="checkbox"/> Level3 <a href="#">AddSBCert</a>	SBCert Express Suites

Select the PM\_L1\_Substate\_Verify.sh test.

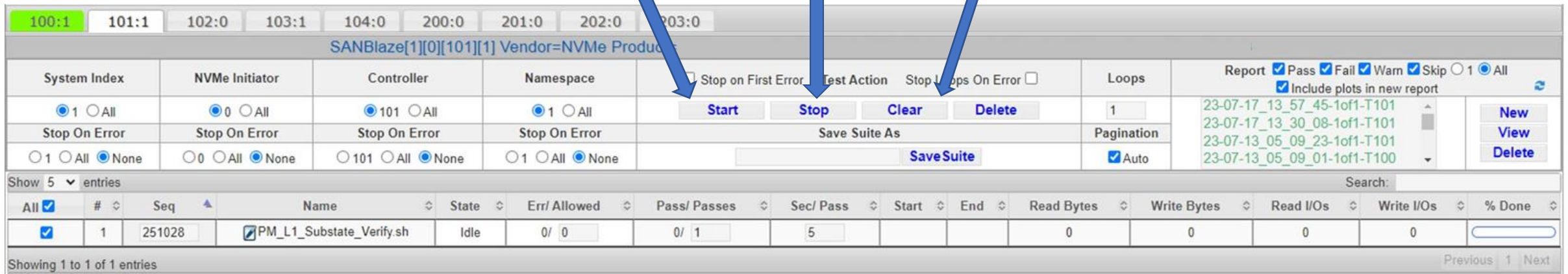
Add the test to the SBCert

# Case Study 2- Test Setup

Start the test run

Stop a test run

Reset a test run



The screenshot shows the SerialTek test setup interface. At the top, there are tabs for different test configurations: 100:1 (selected), 101:1, 102:0, 103:1, 104:0, 200:0, 201:0, 202:0, and 203:0. Below the tabs, the selected configuration is SANBlaze[1][0][101][1] Vendor=NVMe Product=.

The main configuration area includes a table with columns: System Index, NVMe Initiator, Controller, Namespace, Stop on First Error, Test Action, Stop On Error, Loops, and Report. The Test Action column contains buttons: Start, Stop, Clear, and Delete. The Stop On Error column contains checkboxes for Stop On Error and Save Suite As. The Loops column contains a text input field with the value 1. The Report column contains checkboxes for Pass, Fail, Warn, Skip, and All, and a checkbox for Include plots in new report.

Below the configuration area, there is a table showing the list of tests to run. The table has columns: #, Seq, Name, State, Err/ Allowed, Pass/ Passes, Sec/ Pass, Start, End, Read Bytes, Write Bytes, Read I/Os, Write I/Os, and % Done. The first entry is a test named PM\_L1\_Substate\_Verify.sh, which is currently in the Idle state.

#	Seq	Name	State	Err/ Allowed	Pass/ Passes	Sec/ Pass	Start	End	Read Bytes	Write Bytes	Read I/Os	Write I/Os	% Done
1	251028	PM_L1_Substate_Verify.sh	Idle	0/ 0	0/ 1	5			0	0	0	0	

List of tests to run

The PM\_L1\_Substate\_Verify.sh test the DUT for the expected power state transition by inspecting the PCIe bus link state and the current state of the CLKREQ# signal.

# Case Study 2- Examining the Test



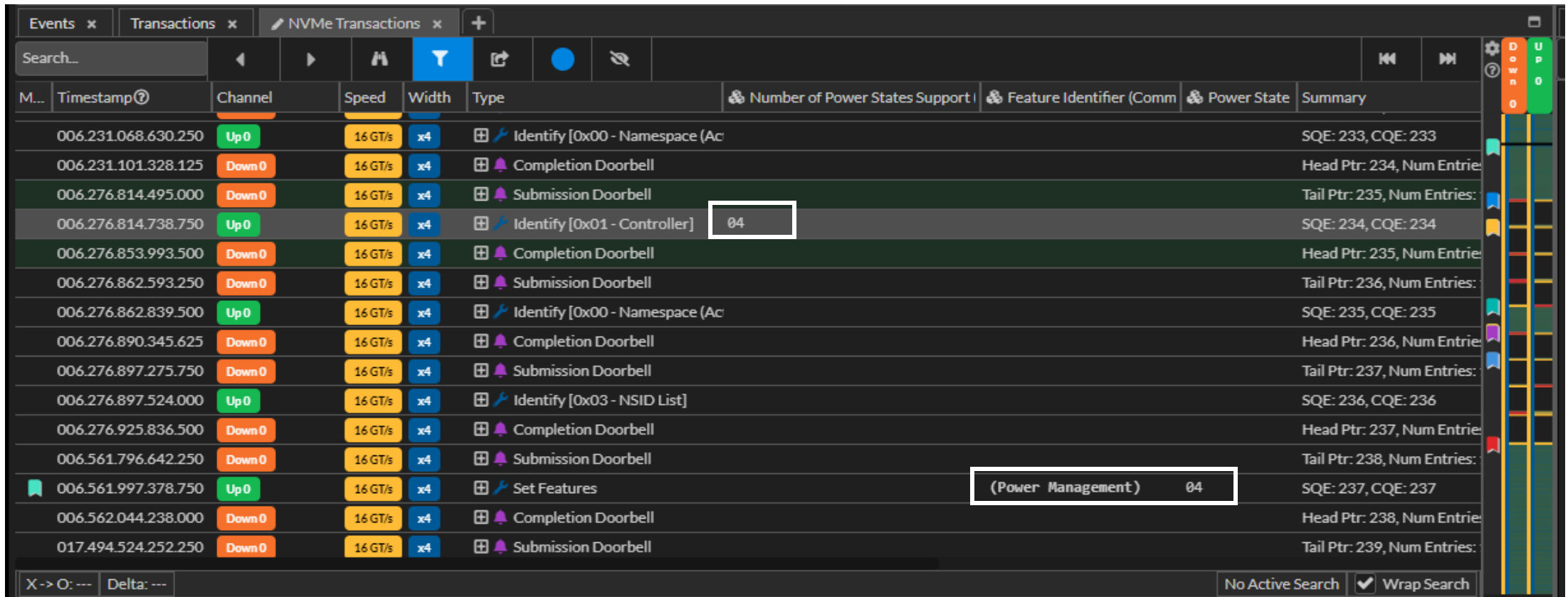
# Case Study 2- Enabling Lowest Power State

Get the number of power states supported from the Identify command

- `cat /iport0/target100 | grep ^NPSS`  
**NPSS=4**

Issue Set Features command

- `io /iport0/target103 SetFeatures -fid 2 -d 4 -w`

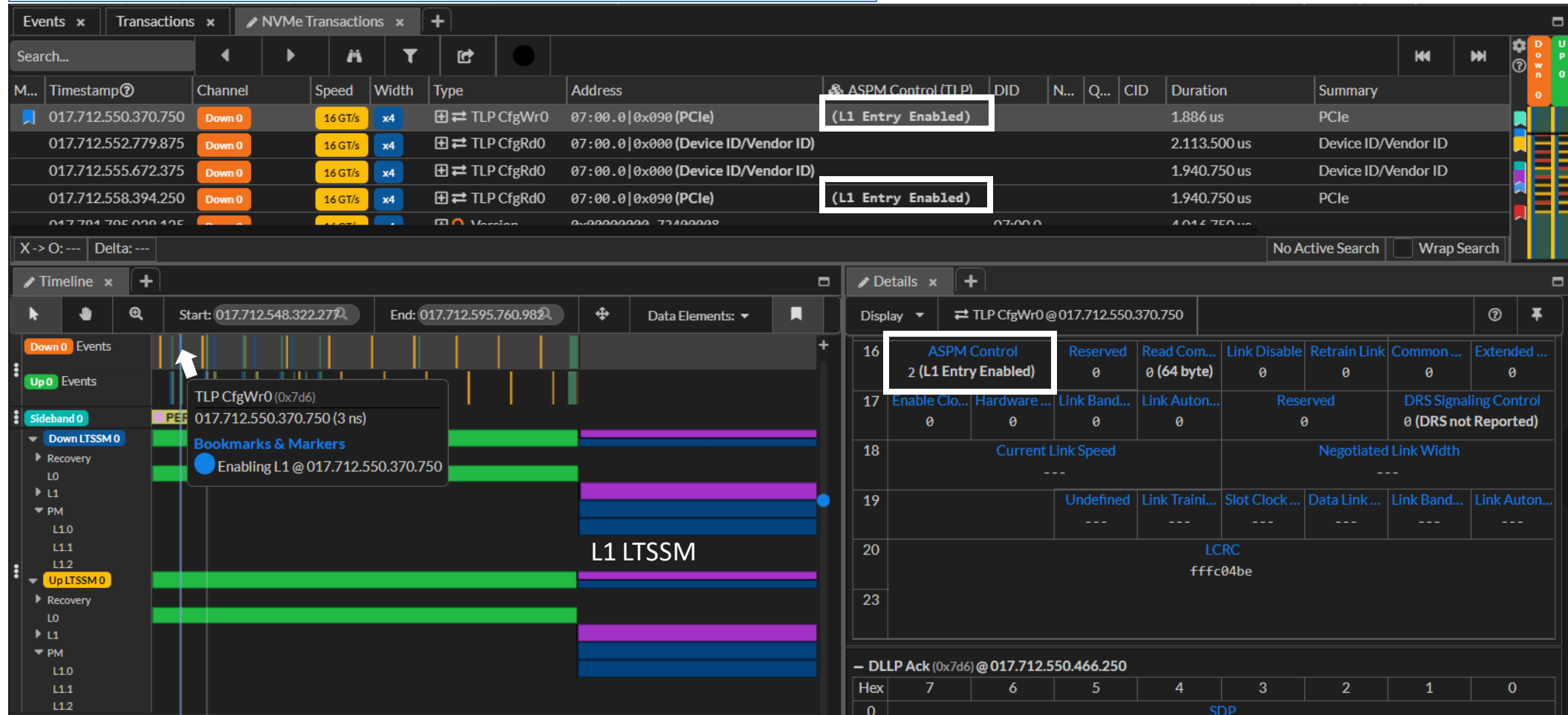


M...	Timestamp	Channel	Speed	Width	Type	Number of Power States Support	Feature Identifier (Command)	Power State	Summary
	006.231.068.630.250	Up 0	16 GT/s	x4	Identify [0x00 - Namespace (Ac				SQE: 233, CQE: 233
	006.231.101.328.125	Down 0	16 GT/s	x4	Completion Doorbell				Head Ptr: 234, Num Entries:
	006.276.814.495.000	Down 0	16 GT/s	x4	Submission Doorbell				Tail Ptr: 235, Num Entries:
	006.276.814.738.750	Up 0	16 GT/s	x4	Identify [0x01 - Controller]	04			SQE: 234, CQE: 234
	006.276.853.993.500	Down 0	16 GT/s	x4	Completion Doorbell				Head Ptr: 235, Num Entries:
	006.276.862.593.250	Down 0	16 GT/s	x4	Submission Doorbell				Tail Ptr: 236, Num Entries:
	006.276.862.839.500	Up 0	16 GT/s	x4	Identify [0x00 - Namespace (Ac				SQE: 235, CQE: 235
	006.276.890.345.625	Down 0	16 GT/s	x4	Completion Doorbell				Head Ptr: 236, Num Entries:
	006.276.897.275.750	Down 0	16 GT/s	x4	Submission Doorbell				Tail Ptr: 237, Num Entries:
	006.276.897.524.000	Up 0	16 GT/s	x4	Identify [0x03 - NSID List]				SQE: 236, CQE: 236
	006.276.925.836.500	Down 0	16 GT/s	x4	Completion Doorbell				Head Ptr: 237, Num Entries:
	006.561.796.642.250	Down 0	16 GT/s	x4	Submission Doorbell				Tail Ptr: 238, Num Entries:
	006.561.997.378.750	Up 0	16 GT/s	x4	Set Features		(Power Management)	04	SQE: 237, CQE: 237
	006.562.044.238.000	Down 0	16 GT/s	x4	Completion Doorbell				Head Ptr: 238, Num Entries:
	017.494.524.252.250	Down 0	16 GT/s	x4	Submission Doorbell				Tail Ptr: 239, Num Entries:

# Case Study 2- Turn on ASPM

Enable ASPM L1 on the DT5 with the following command

- **sbecho ASPMControl=2 > /iport0/target100**

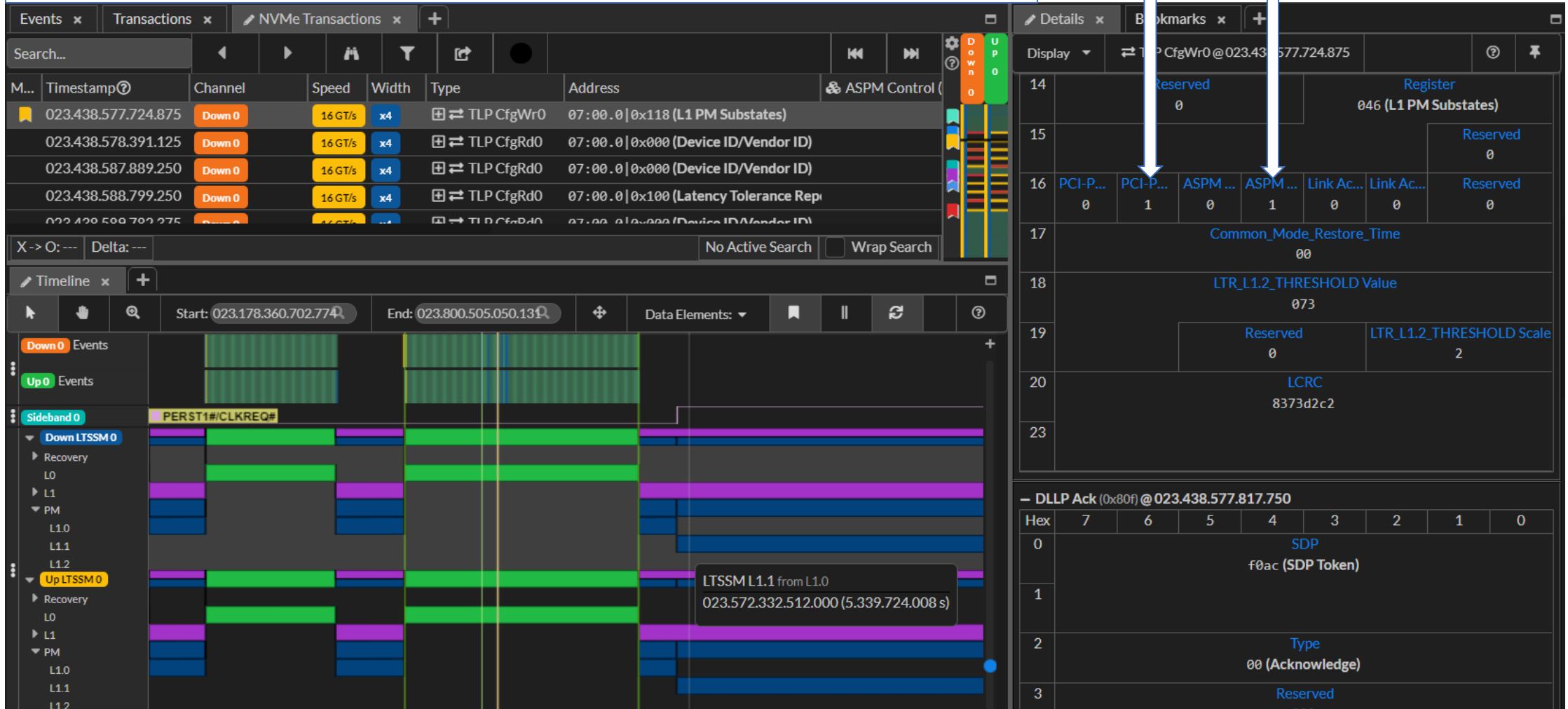




# Case Study 2- Turn on L1.1

Command to enable L1.1 in the LP Control register

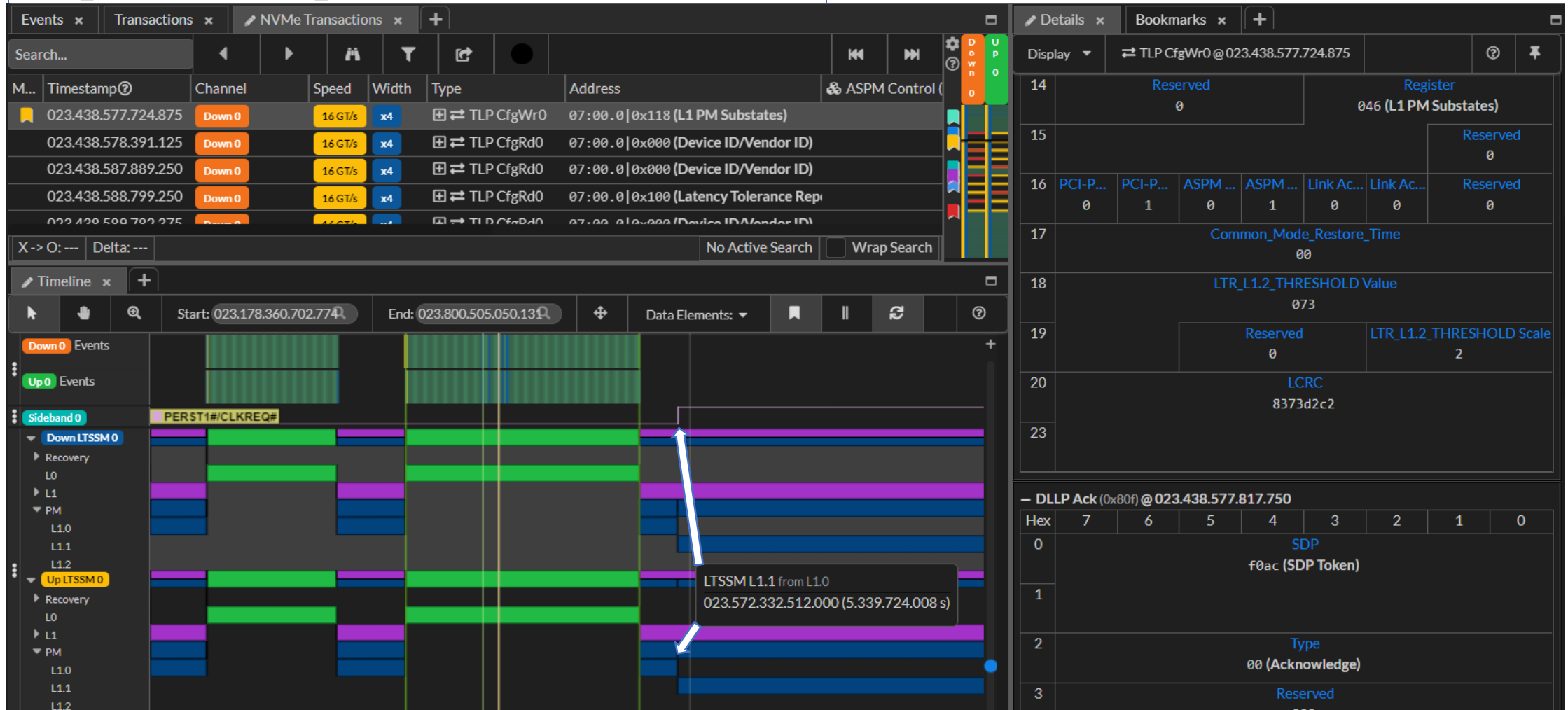
- `sbecho L1PMControl=4 > /iport0/target100`



# Case Study 2- De-assert CLKREQ#

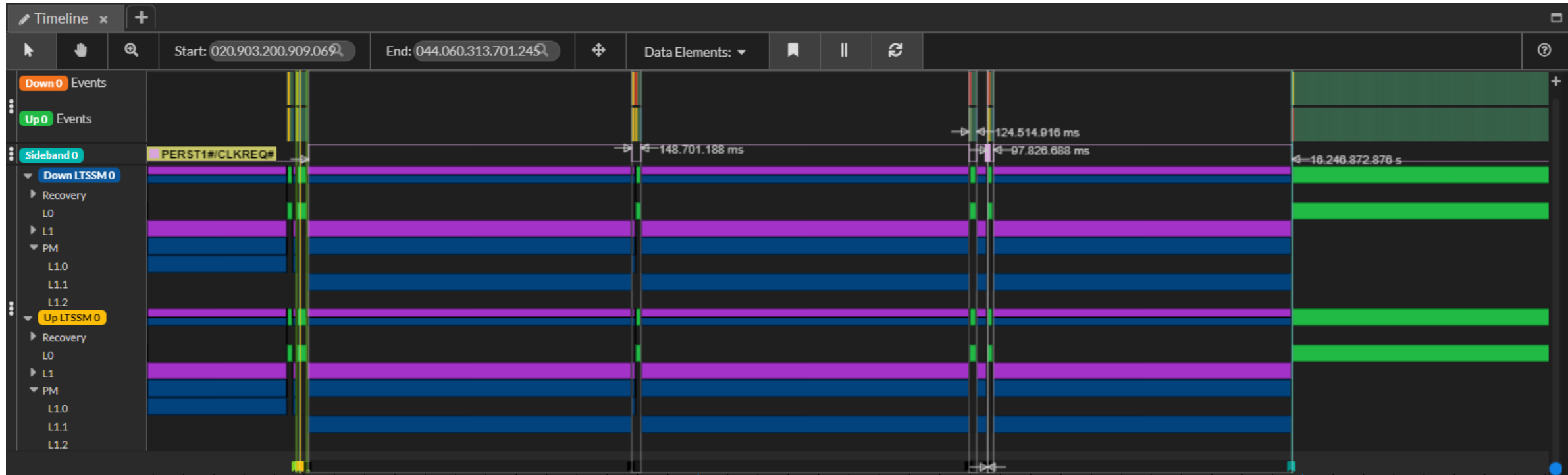
De-assert CLKREQ# by running the following command

- `sb_12x2 -d 0 -f CLKREQ_L -w 1`



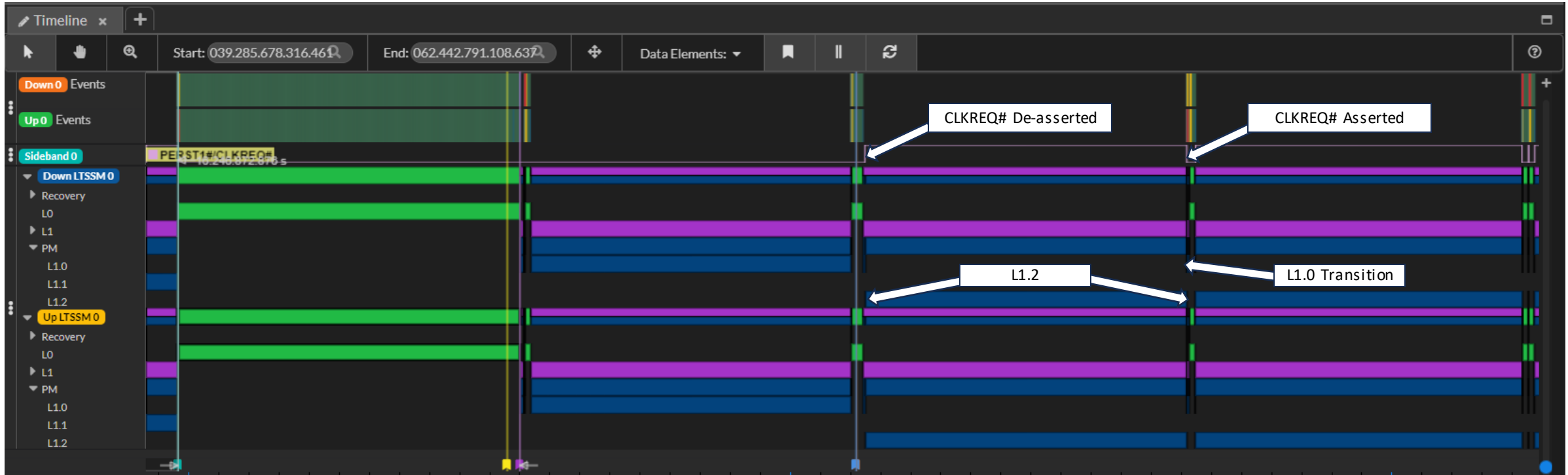
# Case Study 2- Verify CLKREQ#

We can now verify that CLKREQ# has been asserted and de-asserted various times as it transitions back and forth from L1 -> L0 -> L1 along with the timings



# Case Study 2- Setup Test for L1.2

For L1.2 we change the config space to use L1.2 and then repeat the steps for L1.1 and de-assert CLKREQ# to transition to L1.2.



# Case Study 2 Summary

- SANBlaze software allows for easy way to test your devices for support of L1 LTSSM substate and L1 PM substates
- Paired with a SerialTek Kodiak Analyzer, the Sanblaze tool allows you verify that link is properly entering/exiting L1.
- Manually testing L1 LTSSM substates can be difficult, but using a tool such as the SANBlaze SBExpress-DT5 can simplify this testing.

# Summary

- There appears a contradiction in L1.Idle/L1.Entry vs L1.0/L1.1/L1.2 substates due to the misunderstanding of the specification
- L1.0/L1.1/L1.2 or Power Management Substates, not LTSSM L1 substates.
- When combined with L1.1 and L1.2 Power management states, devices can achieve significant power savings.
- Using the Quarch PAM and SerialTek Kodiak Analysis system, users can help validate power management changes.
- Using the SANBlaze SBExpress-DT5 and SerialTek Kodiak Analysis system, users can test their devices to verify that the device conforms to the specifications when performing Power Management Substates.