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Design of Low Voltage Power Loss Protection IC

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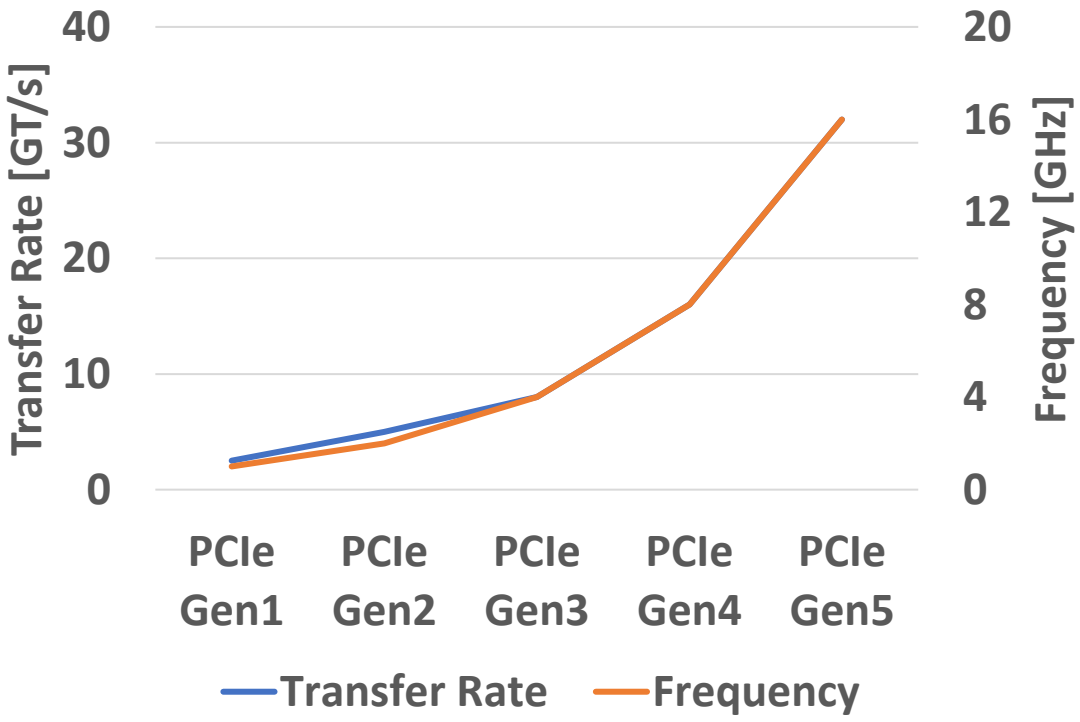
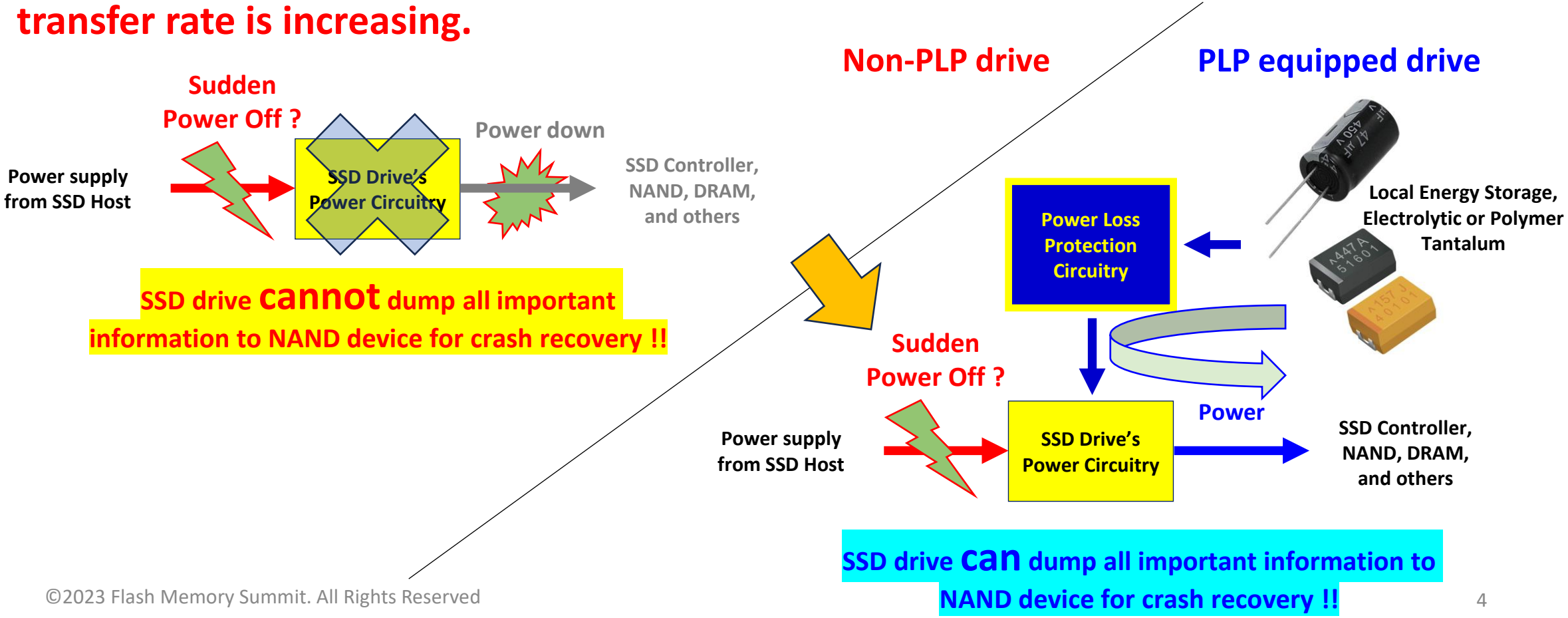
Increasing SSD power consumption

- Increasing two times the transfer rate and drive capacity compared to the previous eSSD generation.
- The power consumption of SSDs is now very high, up to 24W or more.



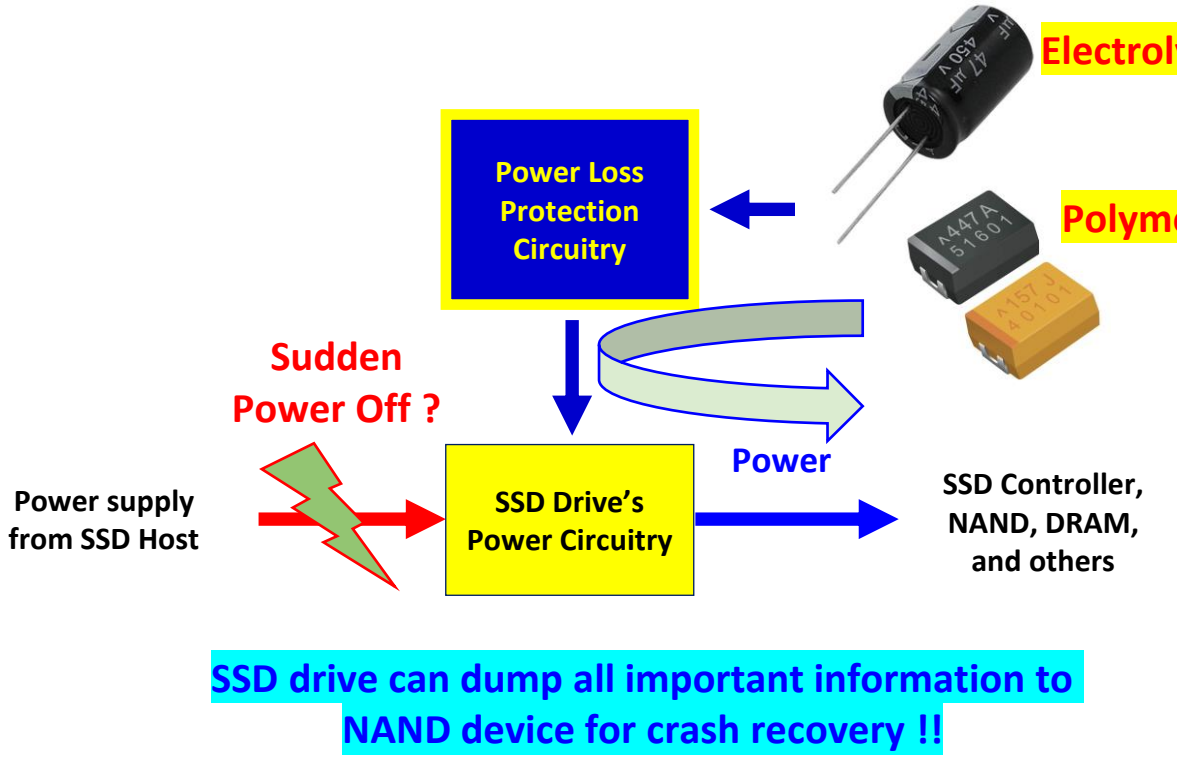
What if sudden power off occurs?

- **PLP (Power Loss Protection), an on-board emergency backup power system, prevents this disaster.**
- **More and more emergency backup energy is needed because drive capacity and transfer rate is increasing.**



Traditional High Voltage PLP System

- An emergency storage capacitor system for backup power uses high voltage charging structures.
- Stored energy is proportional to the square of the charging voltage, the use of high voltage is an easy way to achieve energy density.

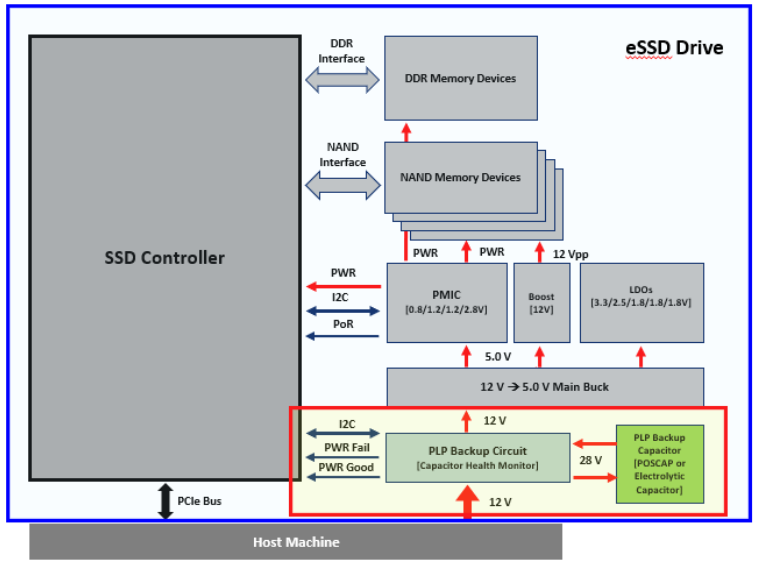


Electrolytic capacitors up to 35 V !

Polymer Tantalum capacitors up to 28 V !

$$Energy \propto \frac{1}{2} C_{total} V^2$$

- Enterprise SSD Drive structure



So, what's the problem with a high voltage PLP system? : Motivation

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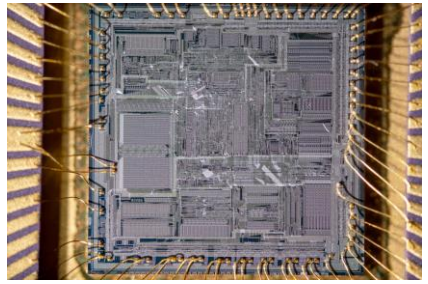
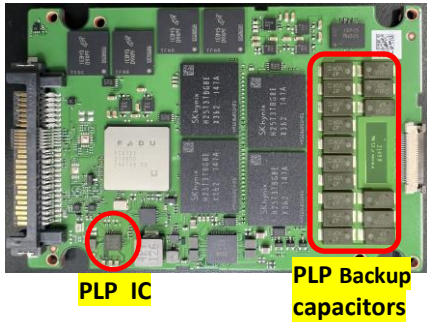
High Voltage PLP IC perspectives :



28~35V Level High Voltage PLP System

- Must use high voltage 45~60V BCD process
  - Relatively expensive design cost
  - Relatively expensive mask cost
  - Relatively expensive package cost
- Transistor size must be larger → larger die size
- Current leakage problems at high voltage mode
- Long term reliability problems
- And so on…

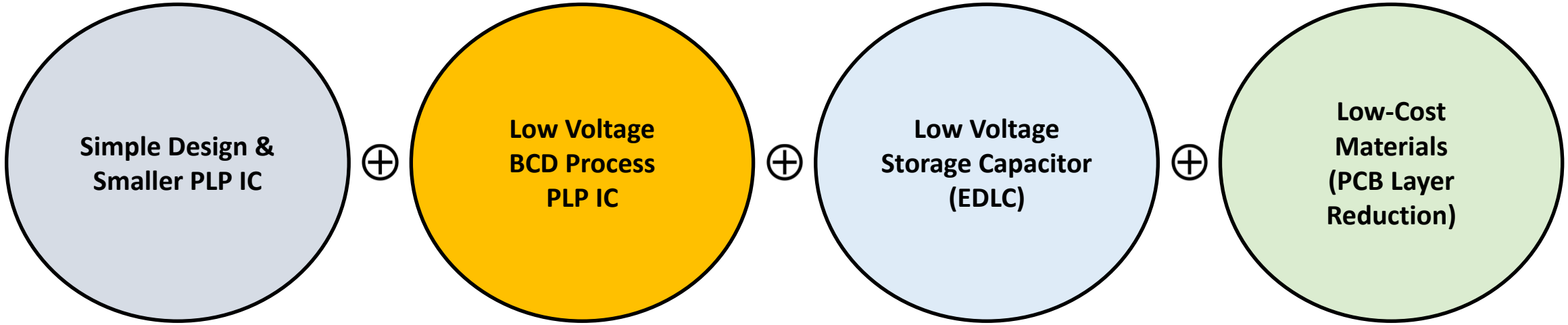
SSD Module perspectives :



- Must use separate layer for high voltage node
- High voltage switching noise injection into sensitive high-speed signals
- Relatively expensive capacitor cost :
  - especially Polymer Tantalum capacitor
- Long term reliability problems :
  - Metal corrosion from highly accelerated E-field
- And so on…

This is not cost effective at all !!

Design Approach



- IC Verification, valid cost 60% down
- 45~60V BCD → 12V BCD (Cost Down)
- Reduced manufacture cost
- Longer lifetime
- Smaller mounting area
- Die size 60% Down
- Package cost 80% down

Highly Stable, Reliable, and Cost Effective PLP System

High vs Low Voltage PLP System

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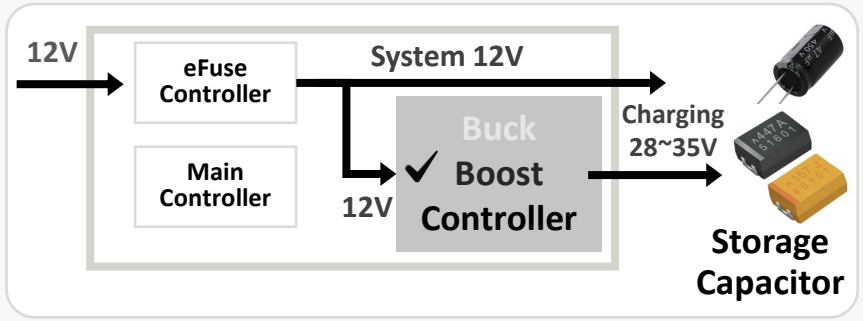
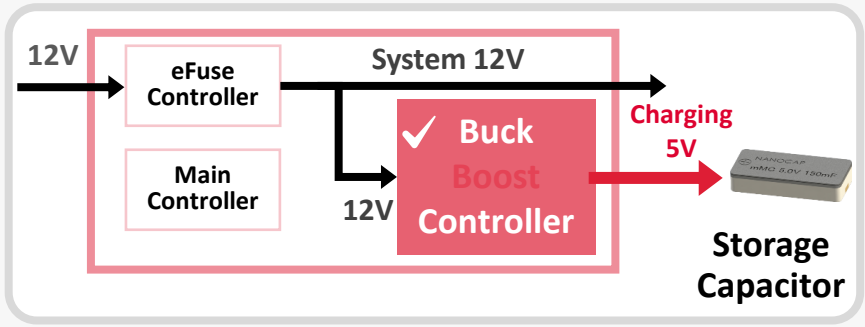
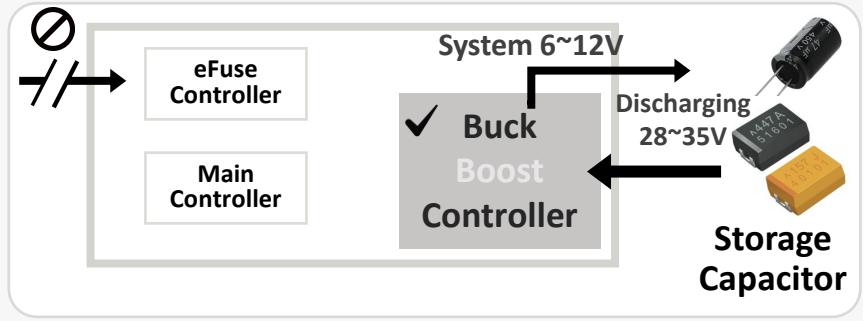
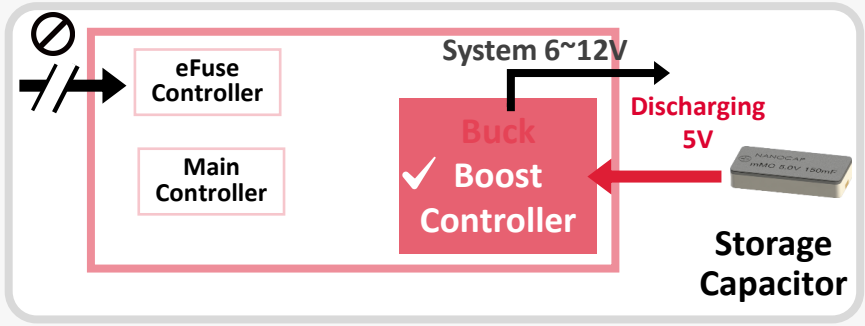
	High Voltage PLP System	Low Voltage PLP System
01 Normal Condition		
02 Power Loss Condition		

Electrolytic or Polymer Tantalum

ELDC (Electrolytic Double-Layer Capacitor)

- Charging: Boost, Discharging: Buck
- High voltage 45~60V BCD process
- High voltage charging capacitors (28~35V)

- Charging: Buck, Discharging: Boost
- Low voltage 12V BCD process
- Low voltage charging capacitors (5V)

High vs Low Voltage PLP System

Items	High Voltage PLP System	Low Voltage PLP System
PLP IC Fabrication Process	45 ~ 60 V BCD	12V BCD (Cost Down)
PLP IC Die Area	100%	~60% ↓
PLP IC Design & Verification Cost	100%	~60% ↓
PLP IC Validation Cost	100%	~80% ↓
PLP IC Package Cost	100%	~80% ↓
PLP IC Level Long-term Reliability	Normal	Good
Storage Capacitor Cost	High	Low
SSD Module Cost	Normal	Low
SSD Module Level Switching Noise	High	Low
SSD Module Level Long-term Reliability	Low	High

Highly Stable, Reliable,
and Cost Effective PLP System

EDLC, PLP Backup Storage Capacitor for Low Voltage PLP

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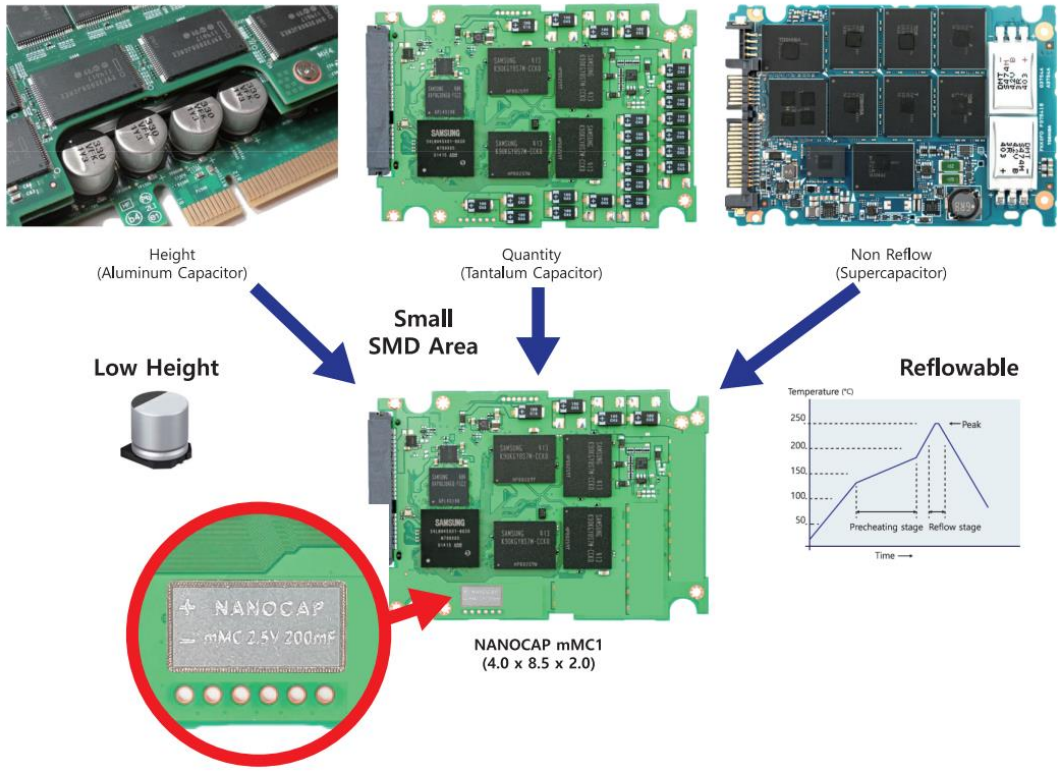
- **FADU adopted 5V (Unit Cell) high power, high temperature lifetime Supercapacitor for SSD PLP**

Advantage of EDLC



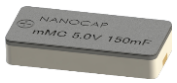
Specification

NANOCAP
www.nanocap.kr

Item	Unit	Specification		
Working Voltage(WV)	V	2.5	8.0	5.0
Capacitance(CAP)	m F	200	100	150
Internal Resistance(ESR)	Ω	0.2	0.4	0.30
Operating Temperature	℃	-40 ~ +85		
Dimension	WxDxH(mm)	8.0 x 15.7 x 2.0	8.0 x 12.0 x 3.7	4.0 x 8.5 x 2.0
Endurance LifeTime	Hrs	2,000		
Reflowable	Number	3		

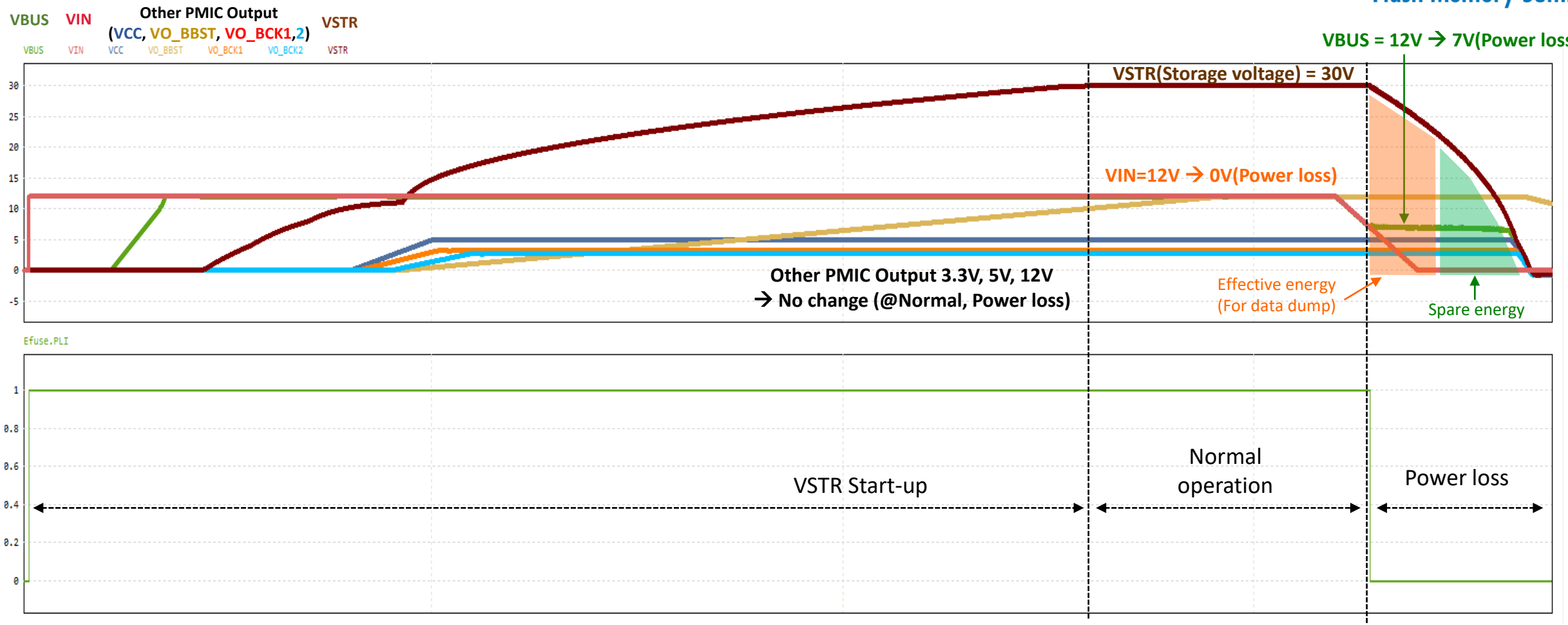
[2.5V 200mF]

[8.0V 100mF]



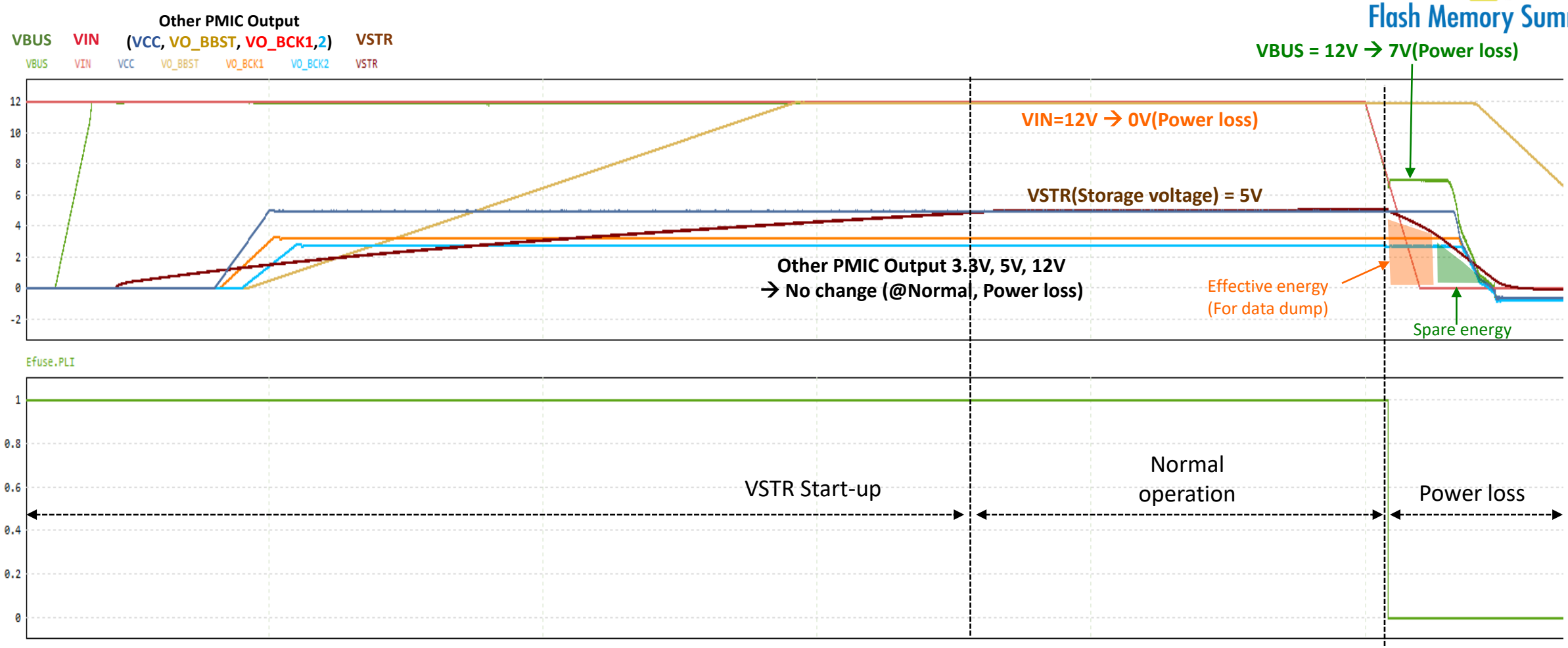
[5.0V 150mF]

Simulation : High Voltage PLP PSIM Simulation Results



- **Consumed energy by PLP dump operation**
  = ½ x Total capacitance x (Max. voltage^2 – Min. voltage^2) = ½ x (100uF) x (30^2 – 20^2 V) = 25 mJ

Simulation : Low Voltage PLP PSIM Simulation Results



- **Consumed energy by PLP dump operation**
  = ½ x Total capacitance x (Max. voltage^2 – Min. voltage^2) = ½ x (5000uF) x (5^2 – 3^2 V) = 40 mJ
  → Sufficient energy for PLP dump

Conclusion

- **Improved System Stability and Reliability**

  The LV-PLP circuit improves the stability of the overall system, ensuring reliable power supply even during power loss situations.

- **Cost Efficient**

  Low voltage charging capacitors are typically more cost-effective compared to high-voltage capacitors, resulting in potential cost savings for the PLP integrated circuit.

- **Reduced Size**

  The LV-PLP circuit offers a smaller module and chip size compared to circuits using HV-PLP.

A Highly Stable, Reliable, and Cost Effective PLP System can be secured with a low voltage PLP.

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Thank you

FADU

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