

UCIe™ (Universal Chiplet Interconnect Express™)

*Building an open ecosystem of chiplets
for on-package innovations*

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Chairman of UCIe Consortium



Agenda

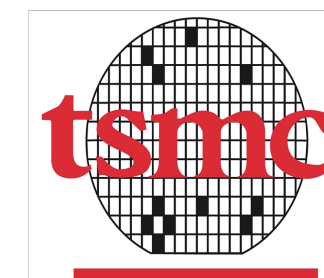
- UCIE Overview
- On-Package Interconnects: Opportunities and Challenges
- Universal Chiplet Interconnect Express (UCIE): An Open Standard for Chiplets
- Introducing UCIE 1.1 ²
- UCIE – Usage Models
- Future Directions and Conclusions

120+ Member Companies and growing!

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive The open chiplet ecosystem.

JOIN US!



UCIe Consortium is Open for Membership

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level.**
- **UCIe** was founded in March 2022, incorporated in June 2022. Two levels of memberships: Contributor and Adopter
- **Contributor Membership**
 - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
 - Implement with the IP protections as outlined in the Agreements
 - Right to attend Corporation trade shows or other industry events as determined by the Board
 - Participate in the technical working groups
 - Influence the direction of the technology
 - Access the intermediate (dot level) specifications
 - Election to get to the Promoter Class/ Board every year when the term of half the board completes
- **Adopter Membership**
 - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
 - Implement with the IP protections as outlined in the Agreements
 - Right to attend Corporation trade shows or other industry events as determined by the Board

On-Package Interconnects: Opportunities and Challenges

Moore Predicted “Day of Reckoning”

*“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”**

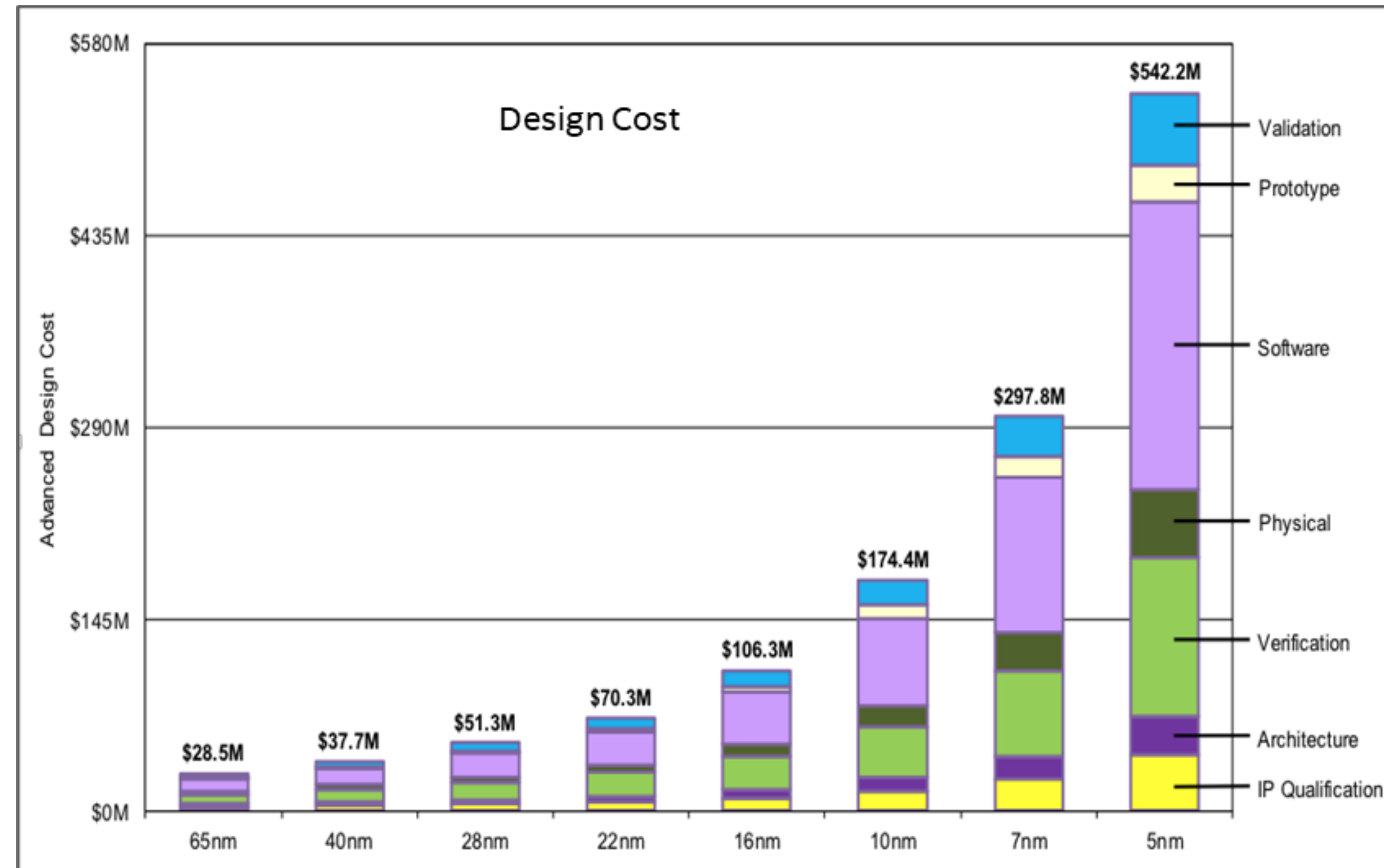
- Gordon E. Moore



*[“Cramming more components onto integrated circuits,”](#) Electronics, Volume 38, Number 8, April 19, 1965

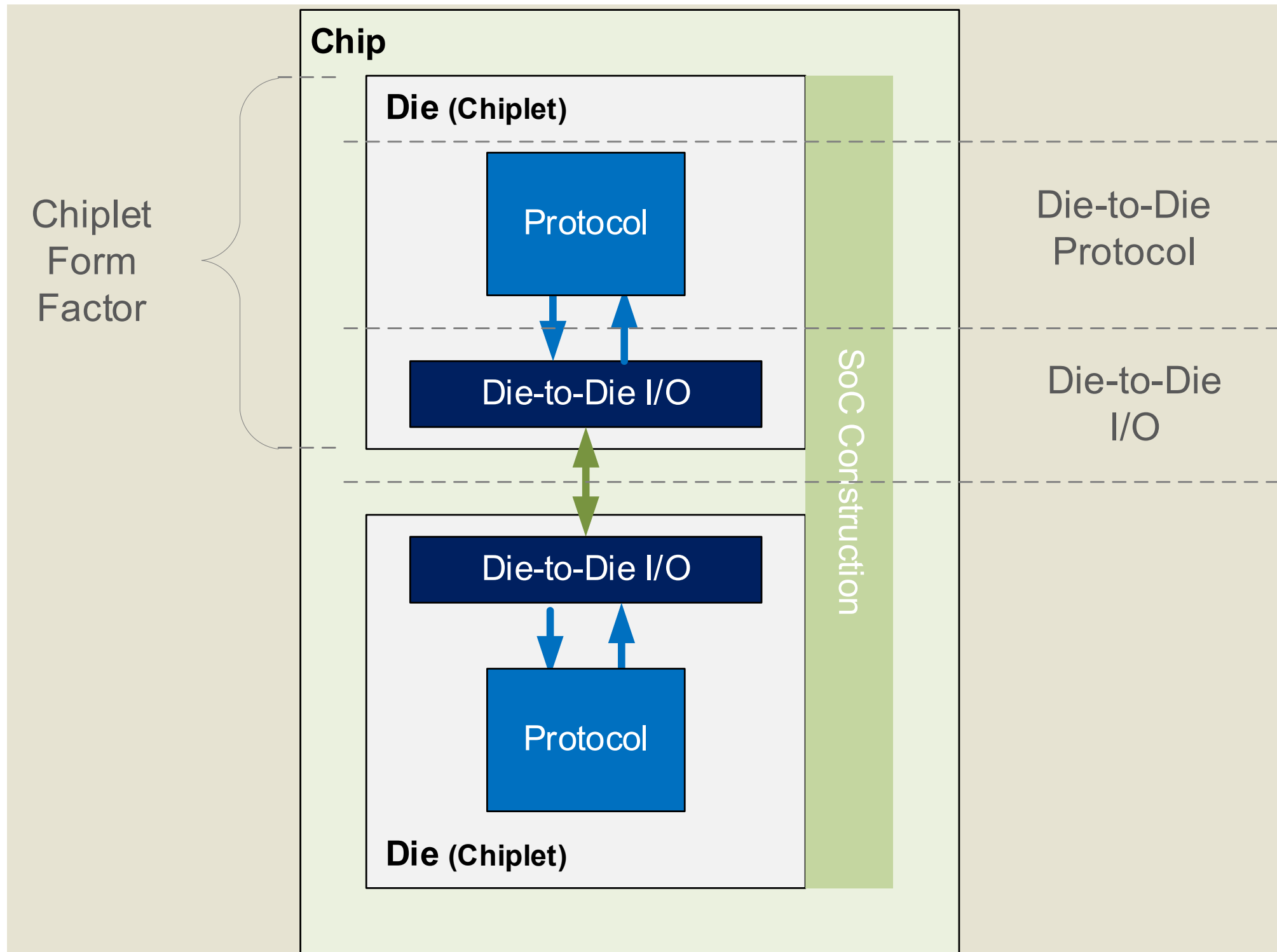
Drivers for On-Package Chiplets

- Reticle Limit, yield optimization, scalable performance
 - Same dies on package (Scale-up)
- Increasing design costs at leading edge process nodes
 - Disaggregate dies across different nodes
 - Deploy latest process node for advanced functionality
- Time to Market (Late binding)
- Easily enables Custom silicon for different customers leveraging a common base product
 - E.g., Different acceleration functions with common compute
- Different process nodes optimized for different functions
 - E.g., Memory, logic, analog, co-packaged optics
- Enables high, power-efficient bandwidth with low-latency access (e.g., HBM memory)



Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)

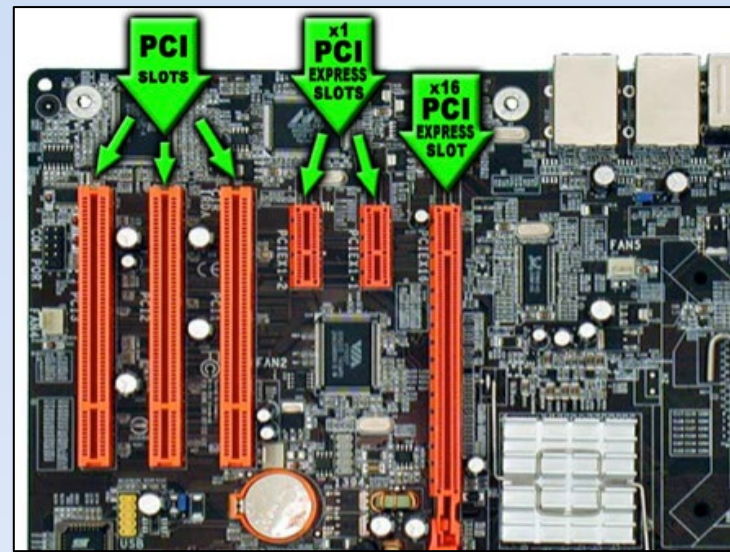
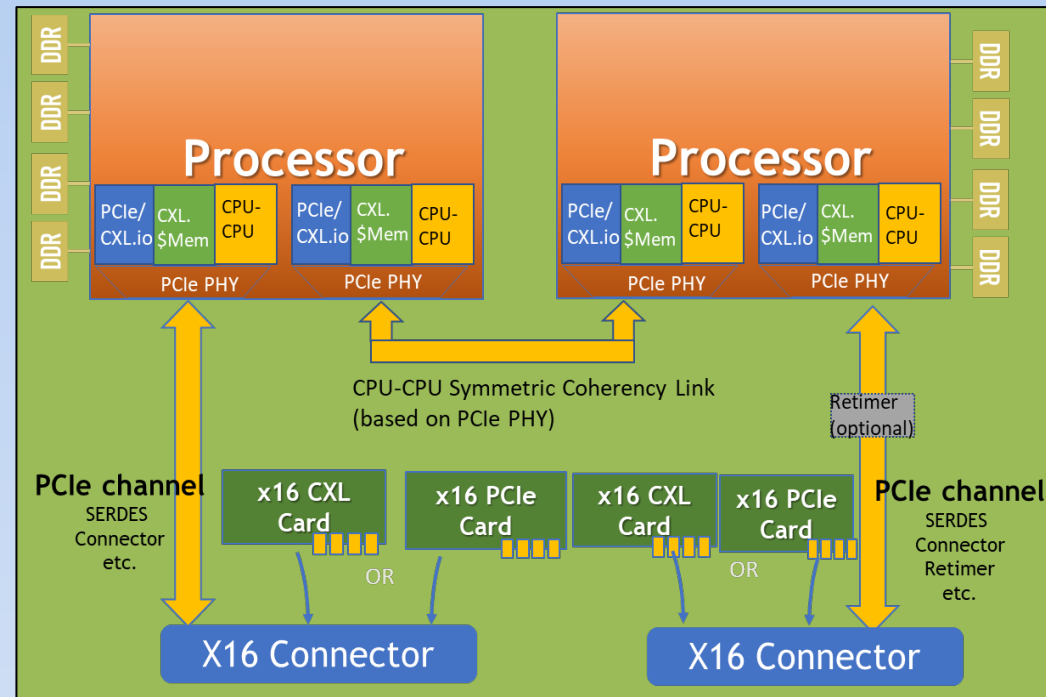
Components of Chiplet Interoperability



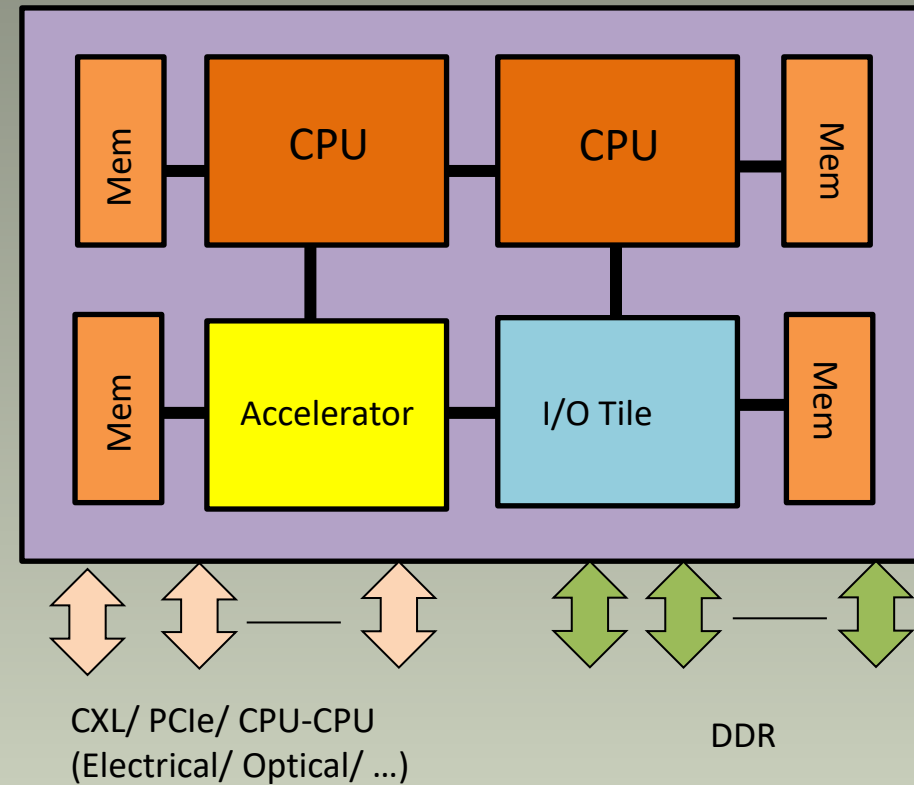
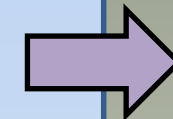
(Example SoC showing two chiplets only)

- **Chiplet Form Factor**
 - Die Size / bump location
 - Power delivery
- **SoC Construction** (Application Layer)
 - Reset and Initialization
 - Register access
 - Security
- **Die-to-Die Protocols** (Data Link to Transaction Layer)
 - PCIe/ CXL/ Streaming
 - Plug and play IPs
- **Die-to-Die I/O** (Physical Layer)
 - Electrical, bump arrangement, channel, reset, initialization, power, latency, test repair, technology transition

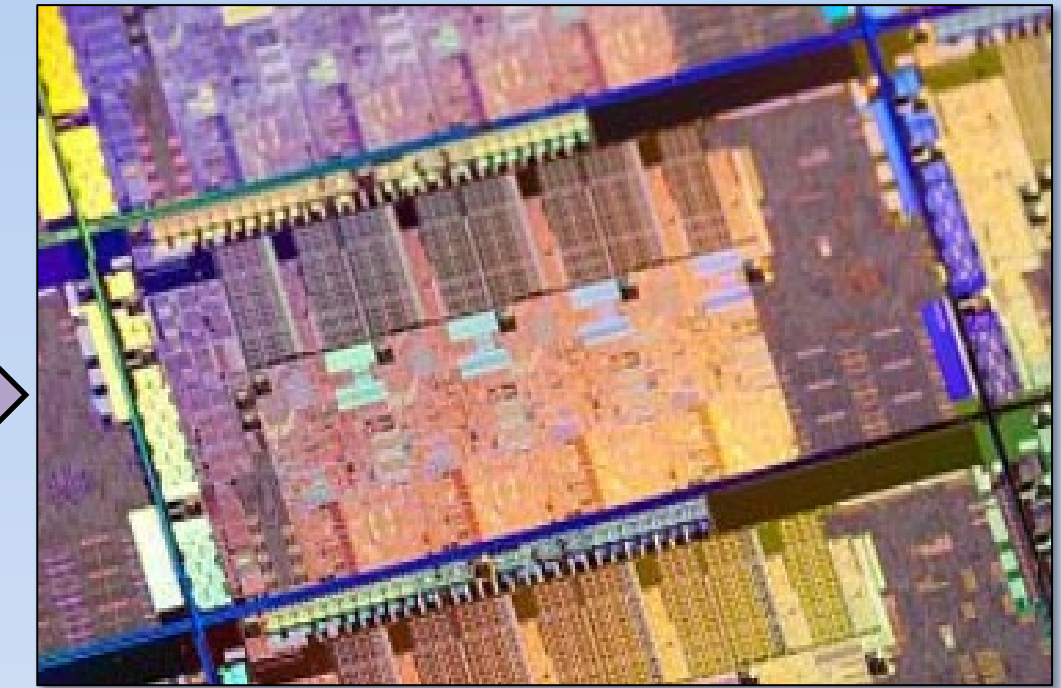
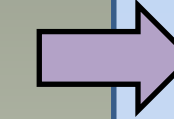
Design Choice: Seamless Integration from Node → Package → On-die Enables Reuse, Better User Experience



Node / Board Level
Integration



Package Level Integration
(with on-package interconnects)



On-die Integration

Same Software, IP, and Subsystem to build scalable solutions offers economies of scale , time to market advantage, and seamless user experience. Innovations at the open slot in board level needs to migrate to package level for multiple usages!

Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplets

Guiding principles of UCIe

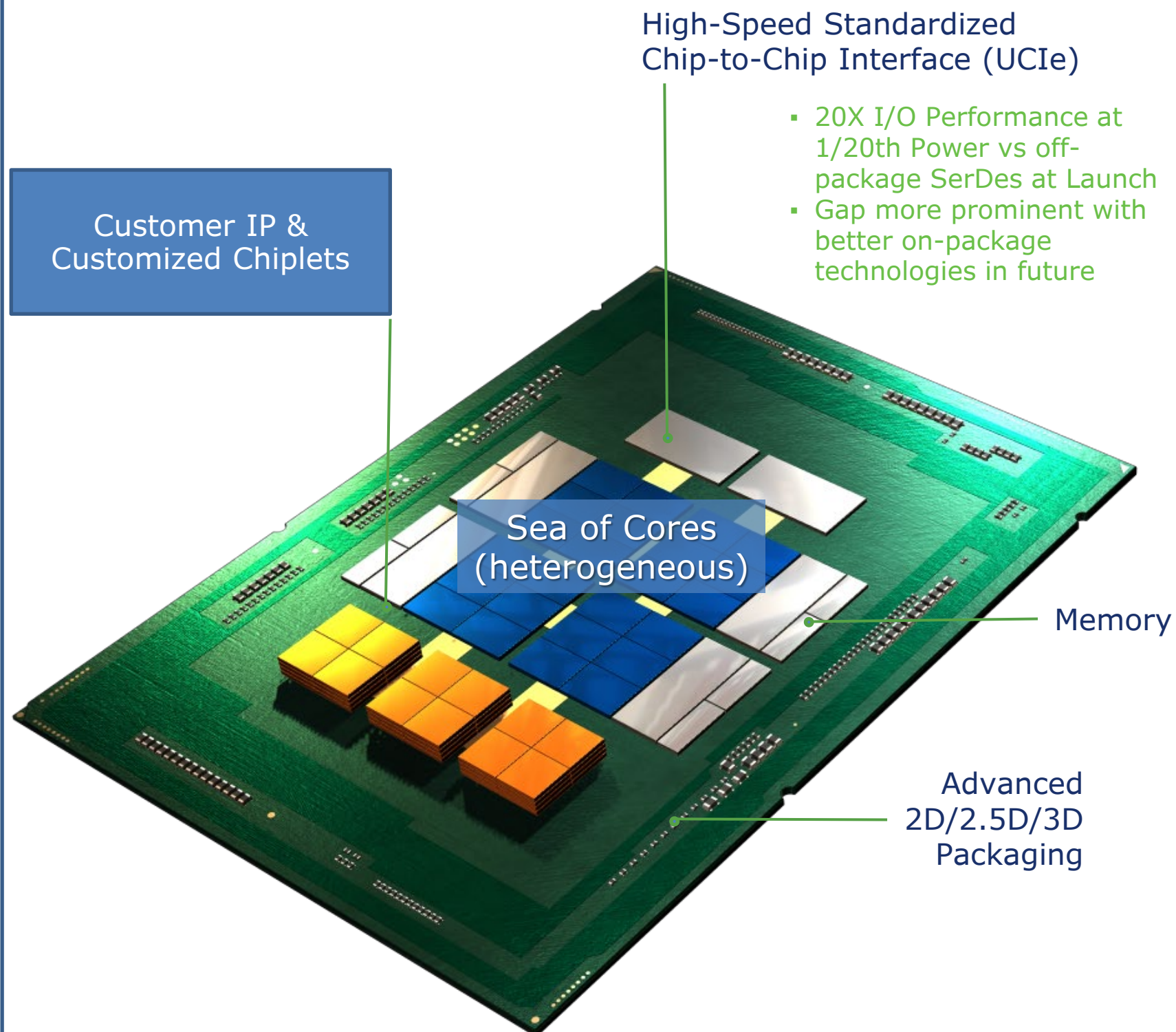
1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)



Motivation

OPEN CHIPLET: PLATFORM ON A PACKAGE



Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
 - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
 - Enables optimal process technologies
 - Smaller (better yield)
 - Reduces IP porting costs
 - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing/ process locked IPs)

Key Metrics and Adoption Criteria

Key Technology Metrics

- Bandwidth density (linear & area)
 - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
 - Scalable energy consumption
 - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
- Technology, frequency, & BER
- Reliability & Availability
- Cost (Standard vs advanced packaging)

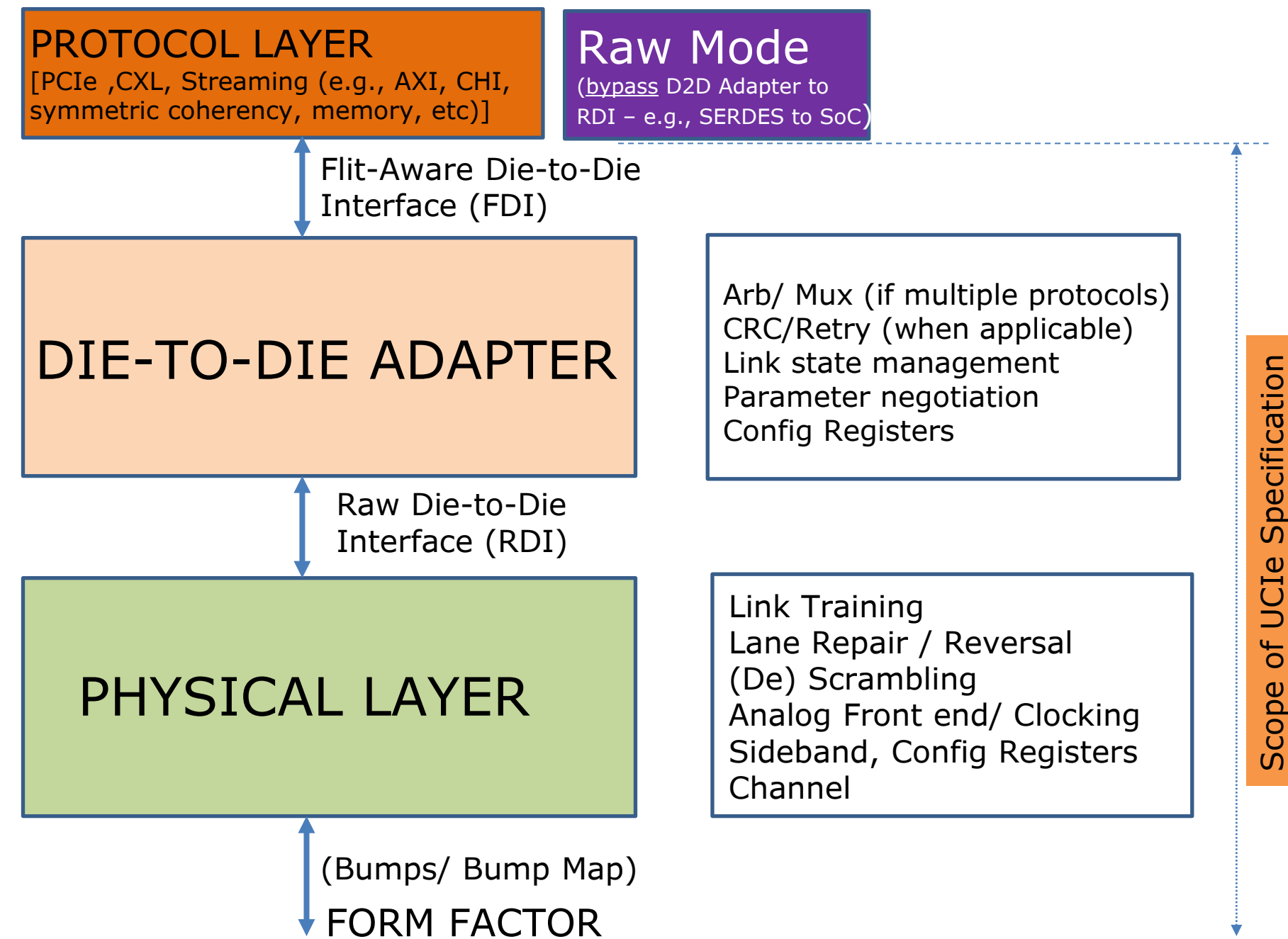
Factors Affecting Wide Adoption

- Interoperability
- Full-stack, plug-and-play with existing s/w is+
- Different usages/segments
- Technology
 - Across process nodes & packaging options
 - Power delivery & cooling
 - Repair strategy (failure/yield improvement)
 - Debug – controllability & observability
- Broad industry support / Open ecosystem
 - Learnings from other standards efforts

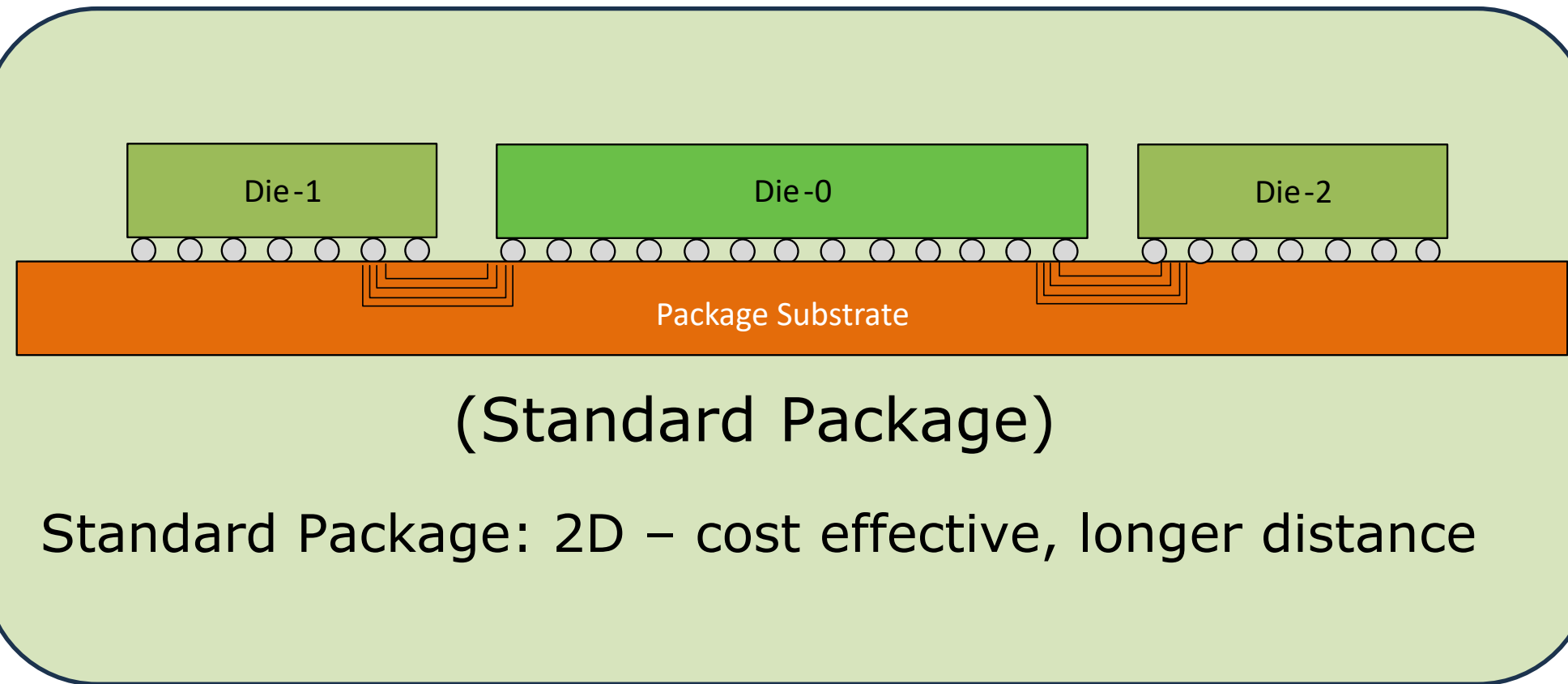
UCIe - Architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria to drive innovations at package level

UCIe 1.0 Specification

- **Layered Approach with industry-leading KPIs**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:** Reliable delivery
 - Support for multiple protocols: bypassed in raw mode
- **Protocol:** CXL/PCIe and Streaming
 - **CXL™/PCIe® for volume attach and plug-and-play**
 - SoC construction issues are addressed w/ CXL/PCIe
 - CXL/PCIe addresses common use cases
 - I/O attach, Memory, Accelerator
 - **Streaming for other protocols**
 - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
 - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/ etc)
 - Raw Mode only
- **Well defined specification:** interoperability and future evolution
 - Configuration register for discovery and run-time
 - control and status reporting in each layer
 - transparent to existing drivers
 - Form-factor and Management
 - Compliance for interoperability
 - Plug-and-play IPs with RDI/ FDI interface

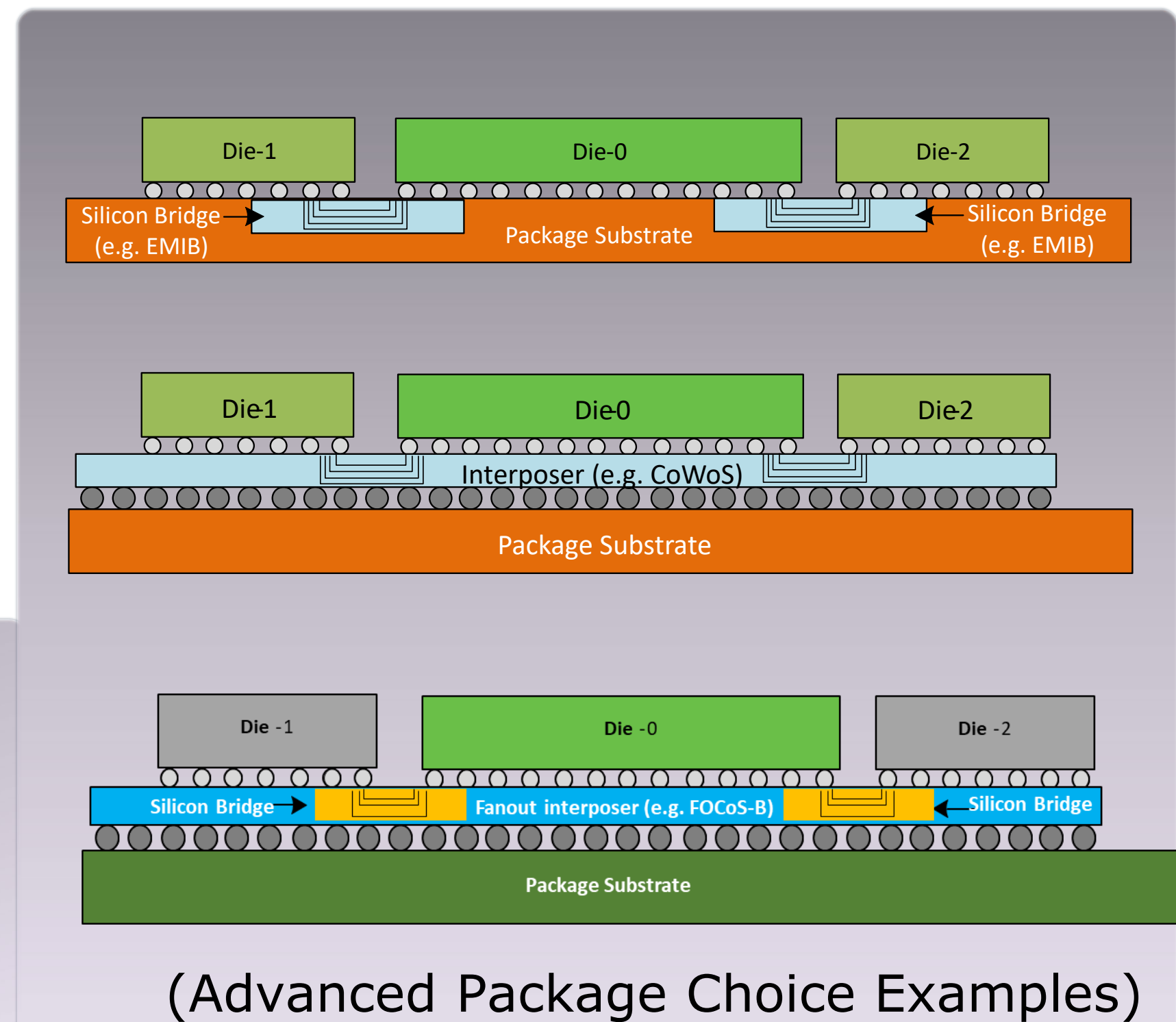


UCIe 1.0: Supports Standard and Advanced Packages



Advanced Packages: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer



One UCIe 1.0 spec supports **different flavors** of packaging options to build an open ecosystem

UCIe PHY: Bump-out for Interoperability

- UCIE architected with process portability in mind
 - Circuit components can be built with common digital/ analog structures
- Bump-out specified in the specification for interoperability even with future bump-pitch reductions
 - Die rotation and mirroring supported

	txdatasb		txcksb		vccaon		vccaon		rxcksb		rxdatasb
vccio		vccio		vccio		vccio		vccio		vccio	
	vss		vss		vccio		vss		vss		vss
vss		txdata7		txdata9		vss		rxdata8		rxdata6	
	txdata5		txckn		txdata11		rxdata10		rxckp		rxdata4
vss		txdata6		txdata8		vss		rxdata9		rxdata7	
	txdata4		txckp		txdata10		rxdata11		rxckn		rxdata5
vccio		vss		vss		vccio		vss		vss	
	txdata1		txvld		txdata15		rxdata14		rxtrk		rxdata0
vccio		txdata3		txdata13		vccio		rxdata12		rxdata2	
	txdata0		txtrk		txdata14		rxdata15		rxvld		rxdata1
vss		txdata2		txdata12		vss		rxdata13		rxdata3	

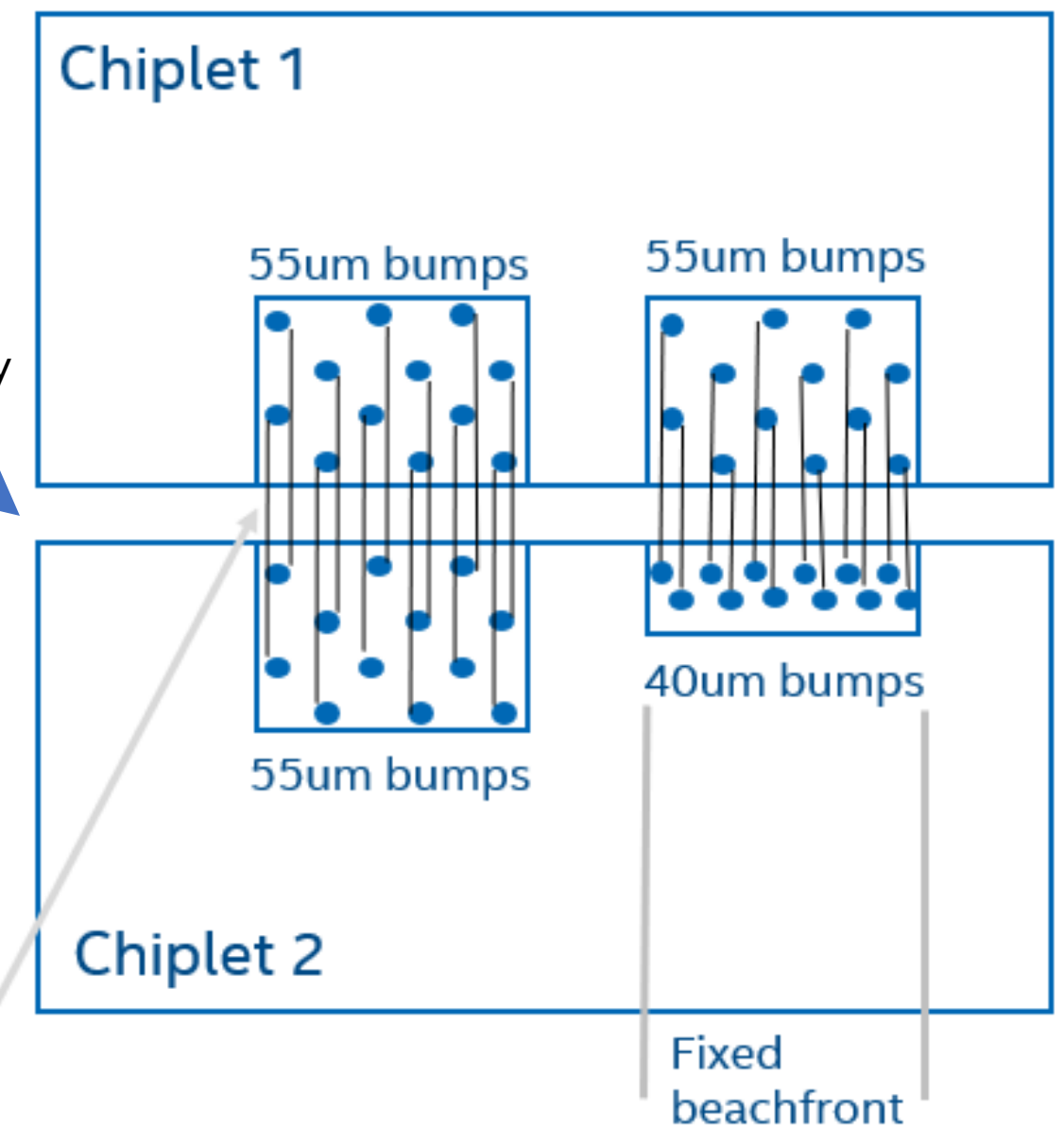
(UCIe-S Unstacked Bump-out)

	m2rxdatasb		m2rxcksb		vccaon		m2txcksb		m2txdatasb		vccaon
m1txdatasb		m1txcksb		vccaon		vccaon		m1rxcksb		m1rxdatasb	
	vccio		vccio		vccio		vccio		vccio		vccio
vss		vss		vss		vss		vss		vss	
m2rxdata4	m2rxdata6	m2rxckp	m2rxdata8	m2rxdata10	vss	m2txdata11	m2txdata9	m2txckn	m2txdata7	m2txdata5	vss
m2rxdata5	m2rxdata7	m2rxckn	m2rxdata9	m2rxdata11	vss	m2txdata10	m2txdata8	m2txckp	m2txdata6	m2txdata4	vss
m2rxdata0	vss	m2rxtrk	vss	m2rxdata14	vss	m2txdata15	vss	m2txckp	vss	m2txdata1	vss
m2rxdata1	m2rxdata2	m2rxvld	m2rxdata12	m2rxdata15	vss	m2txdata13	m2txdata15	m2txvld	m2txdata3	m2txdata0	vss
	m2rxdata3		m2rxdata13	m2rxdata15	vccio	m2txdata14	m2txdata12	m2txtrk	m2txdata2	m2txdata0	vccio
vccio		vccio		vccio		vccio		vccio		vccio	
	vss		vss		vccio		vss		vss		vccio
vss	m1txdata5	m1txdata7	m1txckn	m1txdata9	m1txdata11	vss	m1rxdata10	m1rxdata8	m1rxckp	m1rxdata6	m1rxdata4
vss	m1txdata4	m1txdata6	m1txckp	m1txdata8	m1txdata10	vss	m1rxdata11	m1rxdata9	m1rxckn	m1rxdata7	m1rxdata5
vccio	m1txdata1	vss	m1txvld	vss	m1txdata15	vccio	m1rxdata14	vss	m1rxckn	vss	m1rxdata0
vccio	m1txdata0	m1txdata3		m1txdata13	m1txdata14	vccio	m1rxdata12	m1rxdata15	m1rxtrk	m1rxdata2	m1rxdata1
vss		m1txdata2	m1txtrk	m1txdata12	m1txdata14	vss	m1rxdata13	m1rxvld	m1rxdata3	m1rxdata1	

(UCIe-S Stacked Bump-out)

	rxckb8R0		rxckb3		vc00		rxckb6	rxckb8R0		rxckb10		rxckb12		rxckb14		rxckb16		rxckb18		rxckb20		rxckb22		rxckb24		rxckb26		rxckb28		rxckb30		rxckb32		rxckb34		rxckb36		rxckb38		rxckb40		rxckb42		rxckb44		rxckb46		rxckb48		rxckb50		rxckb52		rxckb54		rxckb56		rxckb58		rxckb60		rxckb62		rxckb64		rxckb66		rxckb68		rxckb70		rxckb72		rxckb74		rxckb76		rxckb78		rxckb80		rxckb82		rxckb84		rxckb86		rxckb88		rxckb90		rxckb92		rxckb94		rxckb96		rxckb98		rxckb100		rxckb102		rxckb104		rxckb106		rxckb108		rxckb110		rxckb112		rxckb114		rxckb116		rxckb118		rxckb120		rxckb122		rxckb124		rxckb126		rxckb128		rxckb130		rxckb132		rxckb134		rxckb136		rxckb138		rxckb140		rxckb142		rxckb144		rxckb146		rxckb148		rxckb150		rxckb152		rxckb154		rxckb156		rxckb158		rxckb160		rxckb162		rxckb164		rxckb166		rxckb168		rxckb170		rxckb172		rxckb174		rxckb176		rxckb178		rxckb180		rxckb182		rxckb184		rxckb186		rxckb188		rxckb190		rxckb192		rxckb194		rxckb196		rxckb198		rxckb200		rxckb202		rxckb204		rxckb206		rxckb208		rxckb210		rxckb212		rxckb214		rxckb216		rxckb218		rxckb220		rxckb222		rxckb224		rxckb226		rxckb228		rxckb230		rxckb232		rxckb234		rxckb236		rxckb238		rxckb240		rxckb242		rxckb244		rxckb246		rxckb248		rxckb250		rxckb252		rxckb254		rxckb256		rxckb258		rxckb260		rxckb262		rxckb264		rxckb266		rxckb268		rxckb270		rxckb272		rxckb274		rxckb276		rxckb278		rxckb280		rxckb282		rxckb284		rxckb286		rxckb288		rxckb290		rxckb292		rxckb294		rxckb296		rxckb298		rxckb300		rxckb302		rxckb304		rxckb306		rxckb308		rxckb310		rxckb312		rxckb314		rxckb316		rxckb318		rxckb320		rxckb322		rxckb324		rxckb326		rxckb328		rxckb330		rxckb332		rxckb334		rxckb336		rxckb338		rxckb340		rxckb342		rxckb344		rxckb346		rxckb348		rxckb350		rxckb352		rxckb354		rxckb356		rxckb358		rxckb360		rxckb362		rxckb364		rxckb366		rxckb368		rxckb370		rxckb372		rxckb374		rxckb376		rxckb378		rxckb380		rxckb382		rxckb384		rxckb386		rxckb388		rxckb390		rxckb392		rxckb394		rxckb396		rxckb398		rxckb400		rxckb402		rxckb404		rxckb406		rxckb408		rxckb410		rxckb412		rxckb414		rxckb416		rxckb418		rxckb420		rxckb422		rxckb424		rxckb426		rxckb428		rxckb430		rxckb432		rxckb434		rxckb436		rxckb438		rxckb440		rxckb442		rxckb444		rxckb446		rxckb448		rxckb450		rxckb452		rxckb454		rxckb456		rxckb458		rxckb460		rxckb462		rxckb464		rxckb466		rxckb468		rxckb470		rxckb472		rxckb474		rxckb476		rxckb478		rxckb480		rxckb482		rxckb484		rxckb486		rxckb488		rxckb490		rxckb492		rxckb494		rxckb496		rxckb498		rxckb500		rxckb502		rxckb504		rxckb506		rxckb508		rxckb510		rxckb512		rxckb514		rxckb516		rxckb518		rxckb520		rxckb522		rxckb524		rxckb526		rxckb528		rxckb530		rxckb532		rxckb534		rxckb536		rxckb538		rxckb540		rxckb542		rxckb544		rxckb546		rxckb548		rxckb550		rxckb552		rxckb554		rxckb556		rxckb558		rxckb560		rxckb562		rxckb564		rxckb566		rxckb568		rxckb570		rxckb572		rxckb574		rxckb576		rxckb578		rxckb580		rxckb582		rxckb584		rxckb586		rxckb588		rxckb590		rxckb592		rxckb594		rxckb596		rxckb598		rxckb600		rxckb602		rxckb604		rxckb606		rxckb608		rxckb610		rxckb612		rxckb614		rxckb616		rxckb618		rxckb620		rxckb622		rxckb624		rxckb626		rxckb628		rxckb630		rxckb632		rxckb634		rxckb636		rxckb638		rxckb640		rxckb642		rxckb644		rxckb646		rxckb648		rxckb650		rxckb652		rxckb654		rxckb656		rxckb658		rxckb660		rxckb662		rxckb664		rxckb666		rxckb668		rxckb670		rxckb672		rxckb674		rxckb676		rxckb678		rxckb680		rxckb682		rxckb684		rxckb686		rxckb688		rxckb690		rxckb692		rxckb694		rxckb696		rxckb698		rxckb700		rxckb702		rxckb704		rxckb706		rxckb708		rxckb710		rxckb712		rxckb714		rxckb716		rxckb718		rxckb720		rxckb722		rxckb724		rxckb726		rxckb728		rxckb730		rxckb732		rxckb734		rxckb736		rxckb738		rxckb740		rxckb742		rxckb744		rxckb746		rxckb748		rxckb750		rxckb752		rxckb754		rxckb756		rxckb758		rxckb760		rxckb762		rxckb764		rxckb766		rxckb768		rxckb770		rxckb772		rxckb774		rxckb776		rxckb778		rxckb780		rxckb782		rxckb784		rxckb786		rxckb788		rxckb790		rxckb792		rxckb794		rxckb796		rxckb798		rxckb800		rxckb802		rxckb804		rxckb806		rxckb808		rxckb810		rxckb812		rxckb814		rxckb816		rxckb818		rxckb820		rxckb822		rxckb824		rxckb826		rxckb828		rxckb830		rxckb832		rxckb834		rxckb836		rxckb838		rxckb840		rxckb842		rxckb844		rxckb846		rxckb848		rxckb850		rxckb852		rxckb854		rxckb856		rxckb858		rxckb860		rxckb862		rxckb864		rxckb866		rxckb868		rxckb870		rxckb872		rxckb874		rxckb876		rxckb878		rxckb880		rxckb882		rxckb884		rxckb886		rxckb888		rxckb890		rxckb892		rxckb894		rxckb896		rxckb898		rxckb900		rxckb902		rxckb904		rxckb906		rxckb908		rxckb910		rxckb912		rxckb914		rxckb916		rxckb918		rxckb920		rxckb922		rxckb924		rxckb926		rxckb928		rxckb930		rxckb932		rxckb934		rxckb936		rxckb938		rxckb940		rxckb942		rxckb944		rxckb946		rxckb948		rxckb950		rxckb952		rxckb954		rxckb956		rxckb958		rxckb960		rxckb962		rxckb964		rxckb966		rxckb968		rxckb970		rxckb972		rxckb974		rxckb976		rxckb978		rxckb980		rxckb982		rxckb984		rxckb986		rxckb988		rxckb990		rxckb992		rxckb994		rxckb996		rxckb998		rxckb1000		rxckb1002		rxckb1004		rxckb1006		rxckb1008		rxckb1010		rxckb1012		rxckb1014		rxckb1016		rxckb1018		rxckb1020		rxckb1022		rxckb1024		rxckb1026		rxckb1028		rxckb1030		rxckb1032		rxckb1034		rxckb1036		rxckb1038		rxckb1040		rxckb1042		rxckb1044		rxckb1046		rxckb1048		rxckb1050		rxckb1052		rxckb1054		rxckb1056		rxckb1058		rxckb1060		rxckb1062		rxckb1064		rxckb1066		rxckb1068		rxckb1070		rxckb1072		rxckb1074		rxckb1076		rxckb1078		rxckb1080		rxckb1082		rxckb1084		rxckb1086		rxckb1088		rxckb1090		rxckb1092		rxckb1094		rxckb1096		rxckb1098		rxckb1100		rxckb1102		rxckb1104		rxckb1106		rxckb1108		rxckb1110		rxckb1112		rxckb1114		rxckb1116		rxckb1118		rxckb1120		rxckb1122		rxckb1124		rxckb1126		rxckb1128		rxckb1130		rxckb1132		rxckb1134		rxckb1136		rxckb1138		rxckb1140		rxckb1142		rxckb1144		rxckb1146		rxckb1148		rxckb1150		rxckb1152		rxckb1154		rxckb1156		rxckb1158		rxckb1160		rxckb1162		rxckb1164		rxckb1166		rxckb1168		rxckb1170		rxckb1172		rxckb1174		rxckb1176		rxckb1178		rxckb1180		rxckb1182		rxckb1184		rxckb1186		rxckb1188		rxckb1190		rxckb1192		rxckb1194		rxckb1196		rxckb1198		rxckb1200		rxckb1202		rxckb1204		rxckb1206		rxckb1208		rxckb1210		rxckb1212		rxckb1214		rxckb1216		rxckb1218		rxckb1220		rxckb1222		rxckb1224		rxckb1226		rxckb1228		rxckb1230		rxckb1232		rxckb1234		rxckb1236		rxckb1238		rxckb1240		rxckb1242		rxckb1244		rxckb1246		rxckb1248		rxckb1250		rxckb1252		rxckb1254		rxckb1256		rxckb1258		rxckb1260		rxckb1262		rxckb1264		rxckb1266		rxckb1268		rxckb1270		rxckb1272		rxckb1274		rxckb1276		rxckb1278		rxckb1280		rxckb1282		rxckb1284		rxckb1286		rxckb1288		rxckb1290		rxckb1292		rxckb1294		rxckb1296		rxckb1298		rxckb1300		rxckb1302		rxckb1304		rxckb1306		rxckb1308		rxckb1310		rxckb1312		rxckb1314		rxckb1316		rxckb1318		rxckb1320		rxckb1322		rxckb1324		rxckb1326		rxckb1328		rxckb1330		rxckb1332		rxckb1334		rxckb1336		rxckb1338		rxckb1340		rxckb1342		rxckb1344		rxckb1346		rxckb1348		rxckb1350		rxckb1352		rxckb1354		rxckb1356		rxckb1358		rxckb1360		rxckb1362		rxckb1364		rxckb1366		rxckb1368		rxckb1370		rxckb1372		rxckb1374		rxckb1376		rxckb1378		rxckb1380		rxckb1382		rxckb1384		rxckb1386		rxckb1388		rxckb1390		rxckb1392		rxckb1394		rxckb1396		rxckb1398		rxckb1400		rxckb1402		rxckb1404		rxckb1406		rxckb1408		rxckb1410		rxckb1412		rxckb1414		rxckb1416		rxckb1418		rxckb1420		rxckb1422		rxckb1424		rxckb1426		rxckb1428		rxckb1430		rxckb1432		rxckb1434		rxckb1436		rxckb1438		rxckb1440		rxckb1442		rxckb1444		rxckb1446		rxckb1448		rxckb1450		rxckb1452		rxckb1454		rxckb1456		rxckb1458		rxckb1460		rxckb1462		rxckb1464		rxckb1466		rxckb1468		rxckb1470		rxckb1472		rxckb1474		rxckb1476		rxckb1478		rxckb1480		rxckb1482		rxckb1484		rxckb1486		rxckb1488		rxckb1490		rxckb1492		rxckb1494		rxckb1496		rxckb1498		rxckb1500		rxckb1502		rxckb1504		rxckb1506		rxckb1508		rxckb1510		rxckb1512		rxckb1514		rxckb1516		rxckb1518		rxckb1520		rxckb1522		rxckb1524		rxckb1526		rxckb1528		rxckb1530		rxckb1532		rxckb1534		rxckb1536		rxckb1538		rxckb1540		rxckb1542		rxckb1544		rxckb1546		rxckb1548		rxckb1550		rxckb1552		rxckb1554		rxckb1556		rxckb1558		rxckb1560		rxckb1562		rxckb1564		rxckb1566		rxckb1568		rxckb1570		rxckb1572		rxckb1574		rxckb1576		rxckb1578		rxckb1580		rxckb1582		rxckb1584		rxckb1586		rxckb1588		rxckb1590		rxckb1592		rxckb1594		rxckb1596		rxckb1598		rxckb1600		rxckb1602		rxckb1604		rxckb1606		rxckb1608		rxckb1610		rxckb1612		rxckb1614		rxck
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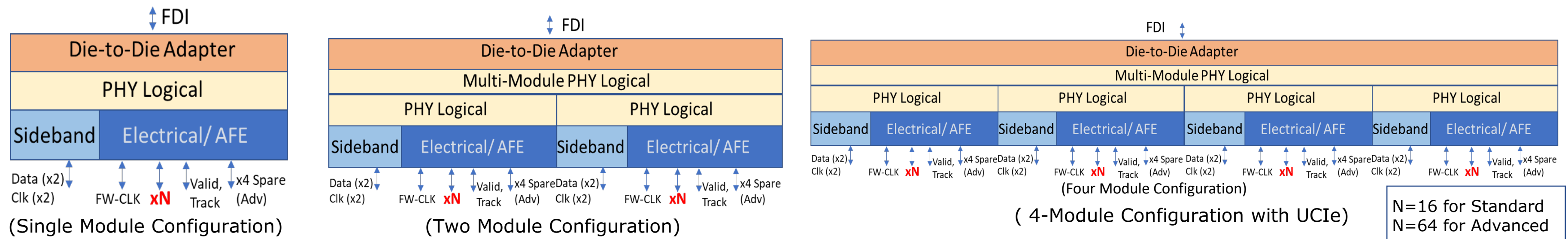
(UCIe-A Bump-out)



CoWoS or EMIB or FoCoS or
similar tight-pitch tech

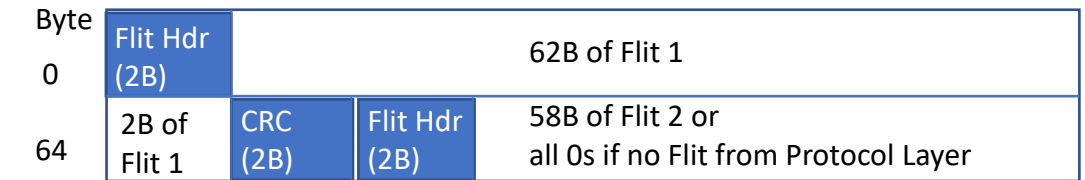
Physical Layer

- Unit is One Module: uni-directional: 1, 2, or 4 modules form a Link
 - 16 (64) SE Lanes for Std (Adv)
 - 1 SE Lane of valid
 - 1 differential pair of forwarded clock
 - 1 lane (SE) calibration - Track
 - Lane reversal on Transmit side
 - Reliability: Spare Lanes in Adv; degradation in Std
 - Supported frequencies: 4, 8, 12, 16, 24, 32 GHz
 - A component must support all data rates up to its advertised maximum data rate for interoperability
 - B/W per module/ dir: 64 GB/s Std, 256 GB/s Adv: Two module gets 2X, 4-module gets 4X
- Sideband: always on; 2 Lanes/ direction @ 800 MHz – data and clock
 - Used for training, debug, management, etc; Leverages depopulated bumps to ensure no extra shore-line
- Valid used for effective dynamic power management

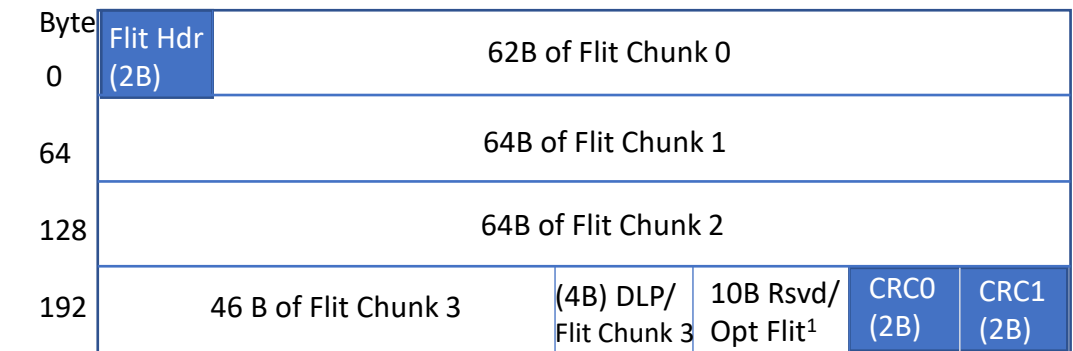


D2D Adapter and Flit Mapping through FDI

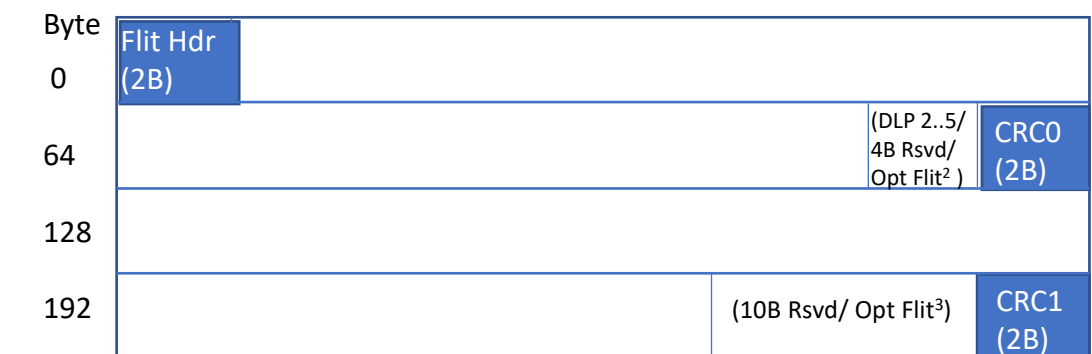
- Responsible for packetization
 - Adds Flit Header (2B) and CRC (2B)
- Supported Flit Sizes: 68B and two flavors of 256B
 - Decided at negotiation
- Flit Hdr (2B): Protocol ID (3b), Credit (1b), Flit Ack/Nak management (2b command + 8b sequence number), Rsvd (2b)
- CRC: Covers 128B payload (smaller payloads are 0-extended)
 - Triple bit flip detection guarantee with 16 bits
 - Replay if CRC fails
 - Sample RTL code for CRC provided in the spec



(a. 68-Byte Flit – usage CXL 2.0/ PCIe Non-Flit Mode/ Streaming)



(b. 256-Byte Flit – usage CXL 3.0/ PCIe 6.0)



(c. 256-Byte Latency-Optimized Flit – usage CXL 3.0/ Streaming)

(Opt Flit is for better link efficiency to use the unused CRC/ FEC bytes in PCIe/ CXL)

Introducing UCIE 1.1

Enhancements for **Automotive Segment** Usage

New Usages: Streaming Protocols with Full Stack

Cost Optimization for **Advanced Packaging**

Enhancements for **Compliance Testing**

UCIE 1.1 is fully Backward compatible with UCIE 1.0

UCIe 1.1: Automotive Enhancements

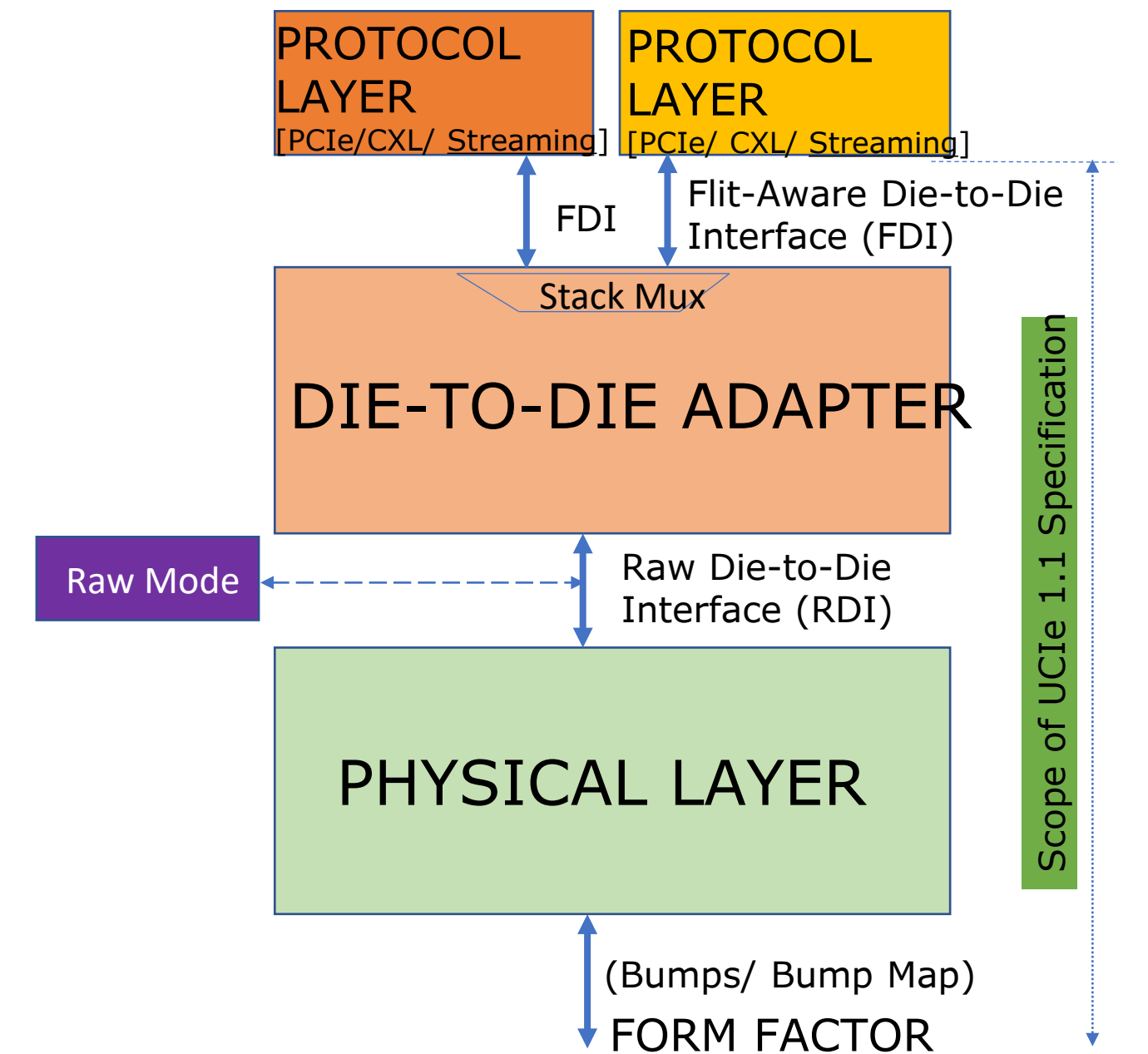
- Automotive is an important segment of the compute continuum – Announcing the formation of an Automotive WG to explore enhancing UCIe for automotive usages
- Automotive moving towards UCIe based chiplets to leverage the broad ecosystem
- UCIe is a compelling technology for automotive compute needs. UCIe 1.1 has the following enhancements building on UCIe 1.0:
 - Preventive Monitoring for link health
 - Run-time testability of failure rate of the link
 - Field repairability to get around faults

UCIe 1.1: Automotive Enhancements

- Preventive Monitoring:
 - Added new registers to capture Eye Margin (eye width and eye height, if applicable) information in a standard format from training
 - SW can trigger periodic retrain of the link to get eye margin info using existing UCIe 1.0 mechanism
- Run-time Testability of Link Health
 - Existing mechanism in UCIe 1.0: Periodic parity Flit injection and checking for monitoring health of each Lane in mission mode
 - Enhancements in UCIe 1.1: Per-Lane error Log/ counter with ability to send interrupt
 - Usage: Software can inject periodic parity Flit and monitor the UCIe 1.1 error log register to assess the health of each Lane to assess the Link health and repair if needed
- Field Repairability
 - Already present with UCIe 1.0 (mask Lane, retrain, etc) – so no changes in this area
- We will continue to monitor and meet the automotive needs

UCIe 1.1: Streaming Protocols on Full Stack

- UCIe 1.0 supports Streaming Protocol (e.g., AXI, CHI, SMP coherency protocols, SFI, CPI) only in Raw Mode
- Two enhancements with UCIe 1.1 (raw mode still supported)
 1. Streaming Protocols can use the D2D adapter
 - Enables them to reuse the CRC, Retry etc.
 - Mechanism: map streaming to existing Flit Formats at FDI interface
 2. Streaming Protocols can multiplex with other protocols with on-demand interleaving
 - Enables co-existence of multiple protocols (e.g., streaming for processing, PCIe for discovery, DMA, TLB, error reporting, interrupt, etc.) for different use cases
 - Mechanism: Protocol muxing for Streaming protocol with existing Flit Formats at FDI interface



UCIe 1.1: Streaming Protocol Flit Formats

Format Number	Flit Format Name	PCIe Non-Flit Mode	PCIe Flit Mode	CXL 68B Flit Mode	CXL 256B Flit Mode	Streaming	
						UCIe 1.0	UCIe 1.1
1	Raw	Optional	Optional	Optional	Optional	Mandatory	
2	68B	Mandatory	N/A	Mandatory	N/A	N/A	Supported
3	Standard 256B End Header	N/A	Mandatory	N/A	N/A	N/A	Supported
4	Standard 256B Start Header	N/A	Optional	N/A	Mandatory	N/A	Supported
5	Latency Optimized 256B without optional bytes	N/A	N/A	N/A	Optional	N/A	Supported
6	Latency Optimized 256B with optional bytes	N/A	Strongly Recommended	N/A	Strongly Recommended	N/A	Supported

- Two newly introduced bumpout configurations for maintaining optimized BW/mm² across allowable bump pitch range
 - Existing bumpout : 10-column
 - New: 8-column, 16-column
 - Suggested usage guideline:

BP	Max Data Rate by Spec	Columns within 388.8 shoreline
25-30	12	16
31-37	16	
38-44	24	10
45-50	32	
51-55	32	8

[illegible]

16Col
Recommended for
25-37um bump pitch

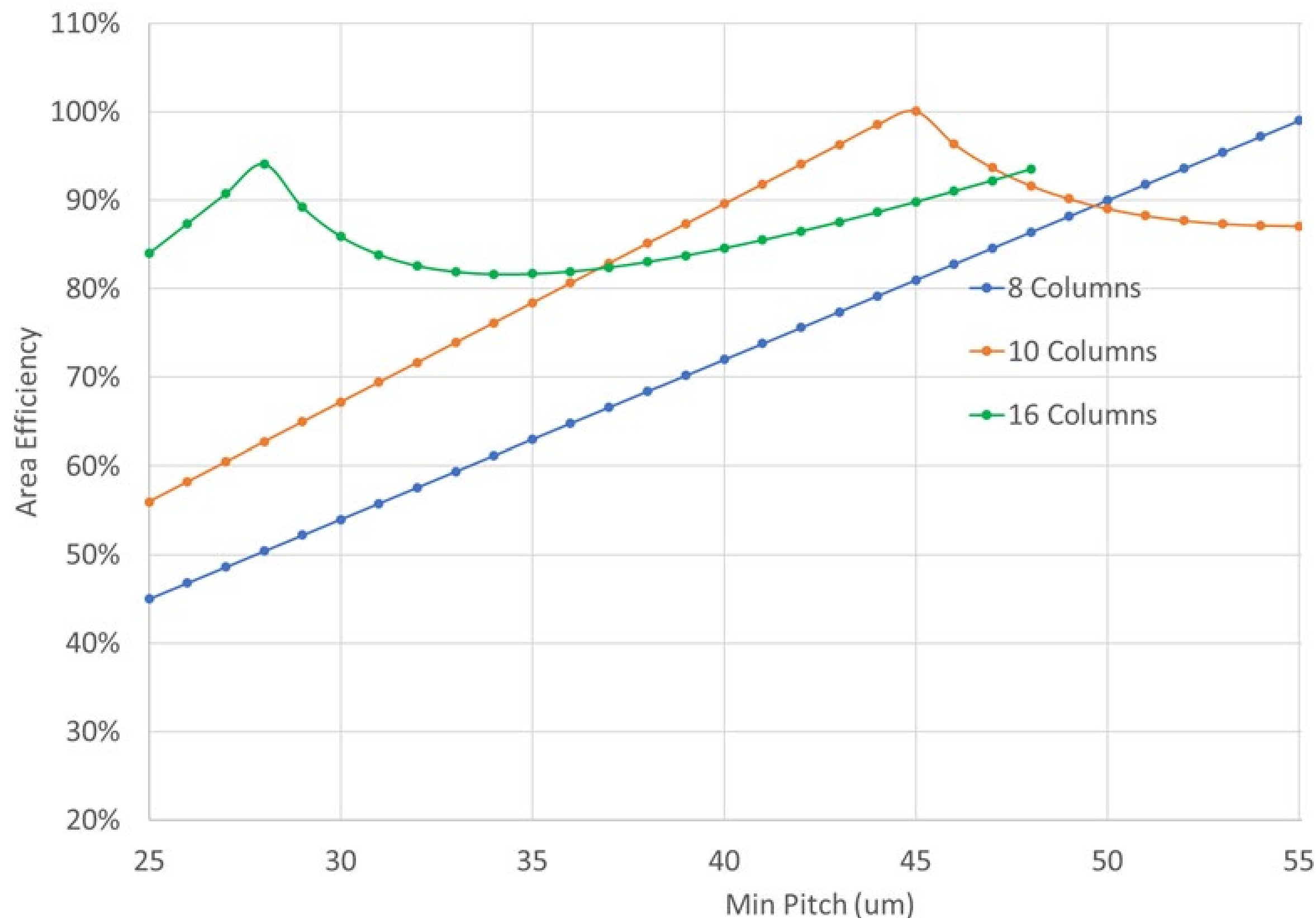
	1	2	3	4	5	6	7	8	9	10
45	vss		vss		vccio		vccio		vss	
44		vss		vccio		vccio		vss		vss
43	vss		vss		vccio		vccio		vss	
42		rxcksbRD		rxcksb		vccio		rxdatasb		rxdatasBR
41	xdatasBRD		txdatasb		vccio		txcksb		txcksbRD	
40		rxdata50		rxdata35		rxdata29		rxdata14		rxdataRD
39	rxdataRD3		rxdata49		rxdata34		rxdata28		rxdata13	
38		rxdata51		rxdata36		rxdata30		rxdata15		vss
37	rxdata63		vccio		rxdata33		vccio		rxdata12	
36		rxdata52		vss		rxdata31		vss		rxdata0
35	vss		rxdata48		rxdata32		rxdata27		rxdata11	
34		rxdata53		rxdata37		rxdataRD1		rxdata16		rxdata1
33	rxdata62		rxdata47		rxdataRD2		rxdata26		rxdata10	
32		rxdata54		rxdata38		vss		rxdata17		vss
31	rxdata61		rxdata46		vccio		rxdata25		rxdata9	
30		rxdata55		rxdata39		rxckRD		rxdata18		rxdata2
29	vss		rxdata45		rxvldRD		rxdata24		rxdata8	
28		rxdata56		vss		rxckn		rxdata19		rxdata3
27	rxdata60		rxdata44		rxvld		vss		rxdata7	
26		rxdata57		rxdata40		rxckp		rxdata20		vss
25	rxdata59		rxdata43		rxtrk		rxdata23		rxdata6	
24		rxdata58		rxdata41		vss		rxdata21		rxdata4
23	vss		rxdata42		vccio		rxdata22		rxdata5	
22		vccfwdio		vccfwdio		vccfwdio		vccfwdio		vccfwdio
21	vccio		txdata21		vccio		txdata41		txdata58	
20		txdata5		txdata22		vss		txdata42		vss
19	txdata4		txdata20		txckp		txdata40		txdata57	
18		txdata6		txdata23		txtrk		txdata43		txdata59
17	vss		txdata19		txckn		vss		txdata56	
16		txdata7		vss		txvld		txdata44		txdata60
15	txdata3		txdata18		txckRD		txdata39		txdata55	
14		txdata8		txdata24		txvldRD		txdata45		vss
13	txdata2		txdata17		vccio		txdata38		txdata54	
12		txdata9		txdata25		vss		txdata46		txdata61
11	vccio		vccio		vccio		vccio		vccio	
10		txdata10		txdata26		txdataRD2		txdata47		txdata62
9	txdata1		txdata16		txdataRD1		txdata37		txdata53	
8		txdata11		txdata27		txdata32		txdata48		vss
7	txdata0		vss		txdata31		vss		txdata52	
6		txdata12		vss		txdata33		vss		txdata63
5	vss		txdata15		txdata30		txdata36		txdata51	
4		txdata13		txdata28		txdata34		txdata49		txdataRD3
3	txdataRD0		txdata14		txdata29		txdata35		txdata50	
2		vccio		vccio		vccio		vccio		vccio
1	vccio		vccio		vccio		vccio		vccio	

10Col (in spec 1.0)
Recommended for
38-50um bump pitch

[illegible]

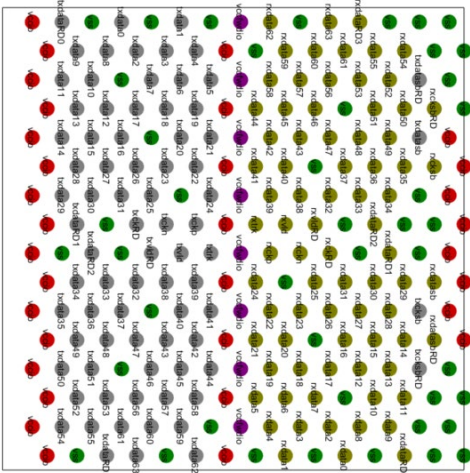
8Col
Recommended for
51-55um bump pitch

UCIe-A Area/Column Type Efficiency Plots

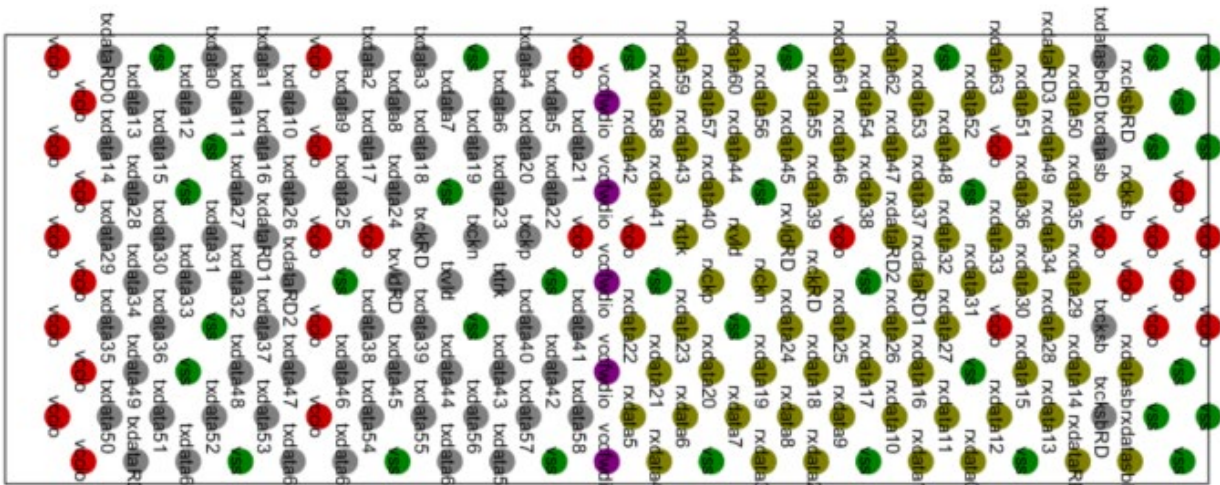


- Points of overlap are the optimal cross-over points between recommended 8/10/16-column bump maps
- At the lower bump pitch range, >80% area efficiency is acceptable given overall magnitude of PHY depth is lower
- As bump pitch increases, >90% area efficiency is desired due to the much bigger PHY depth (um)
 - Example: 10% of 1000um is greater than 20% of 400um

Physical Illustration x64 Bump Maps

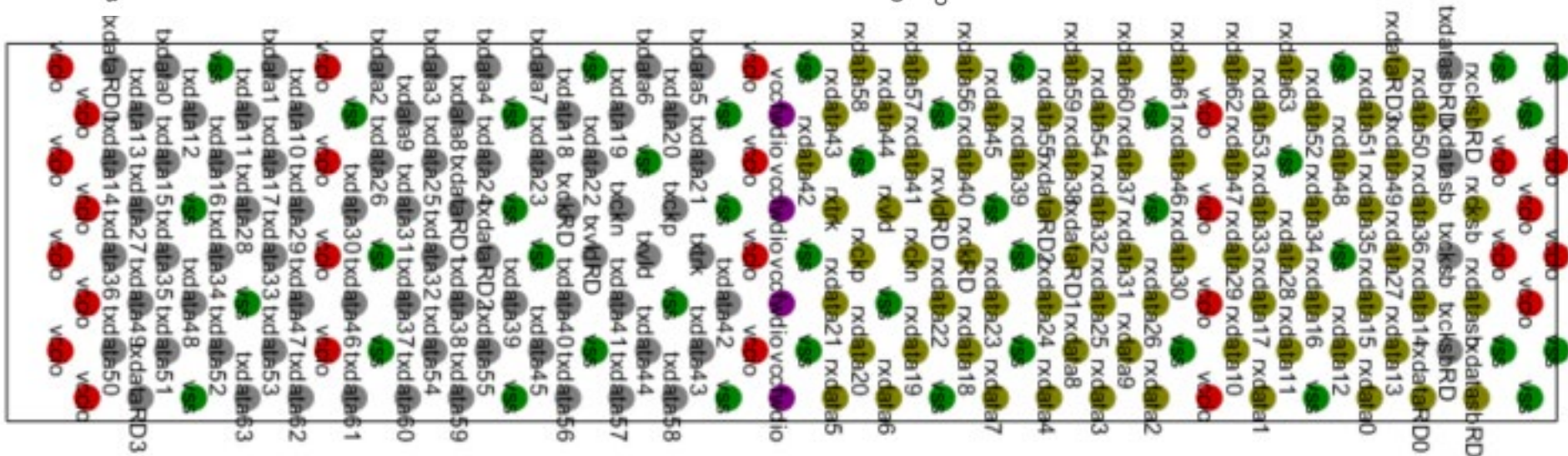


16-Col at 25 μm pitch
388.8 μm shoreline
 \sim 388 μm depth



10-Col at 45 μm pitch
388.8 μm shoreline
 \sim 1043 μm depth

In UCIE 1.0 spec: No change

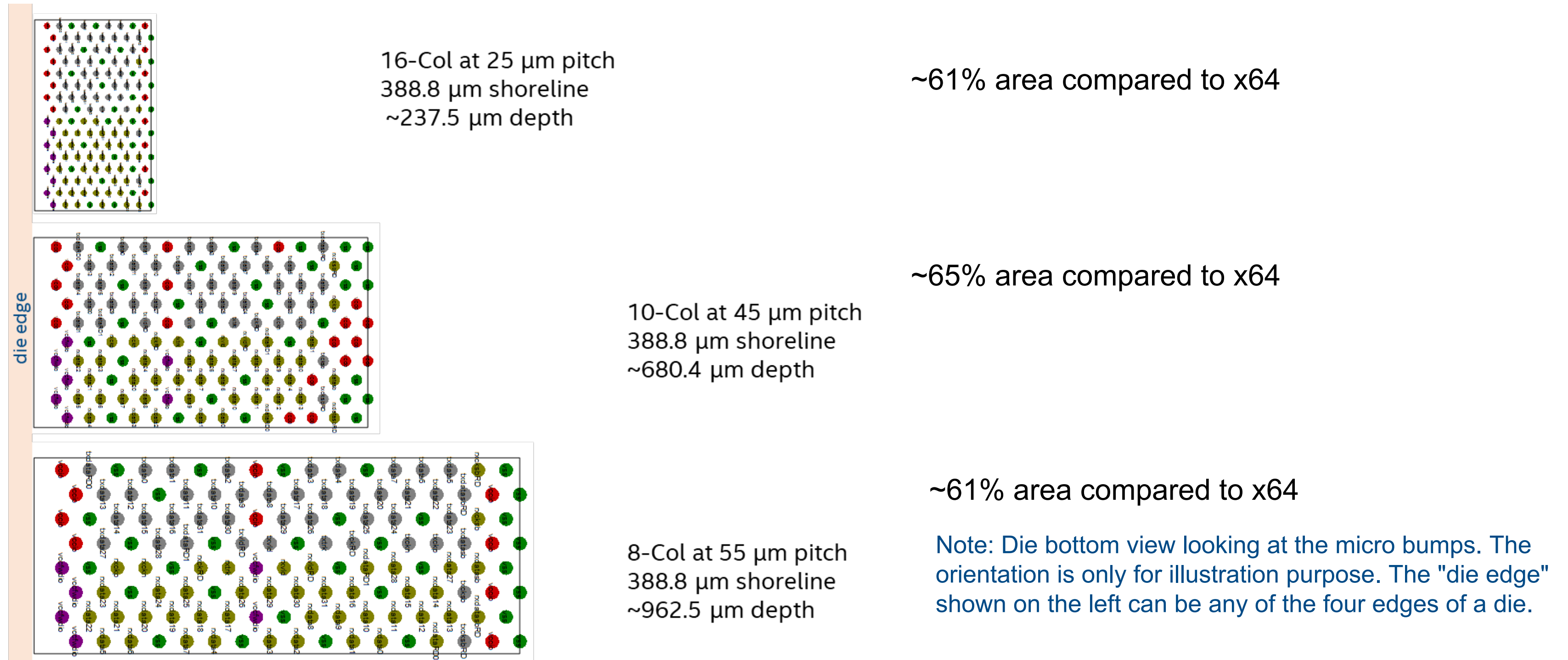


8-Col at 55 μm pitch
388.8 μm shoreline
 \sim 1585 μm depth

Note: Die bottom view looking at the micro bumps. The orientation is only for illustration purpose. The "die edge" shown on the left can be any of the four edges of a die.

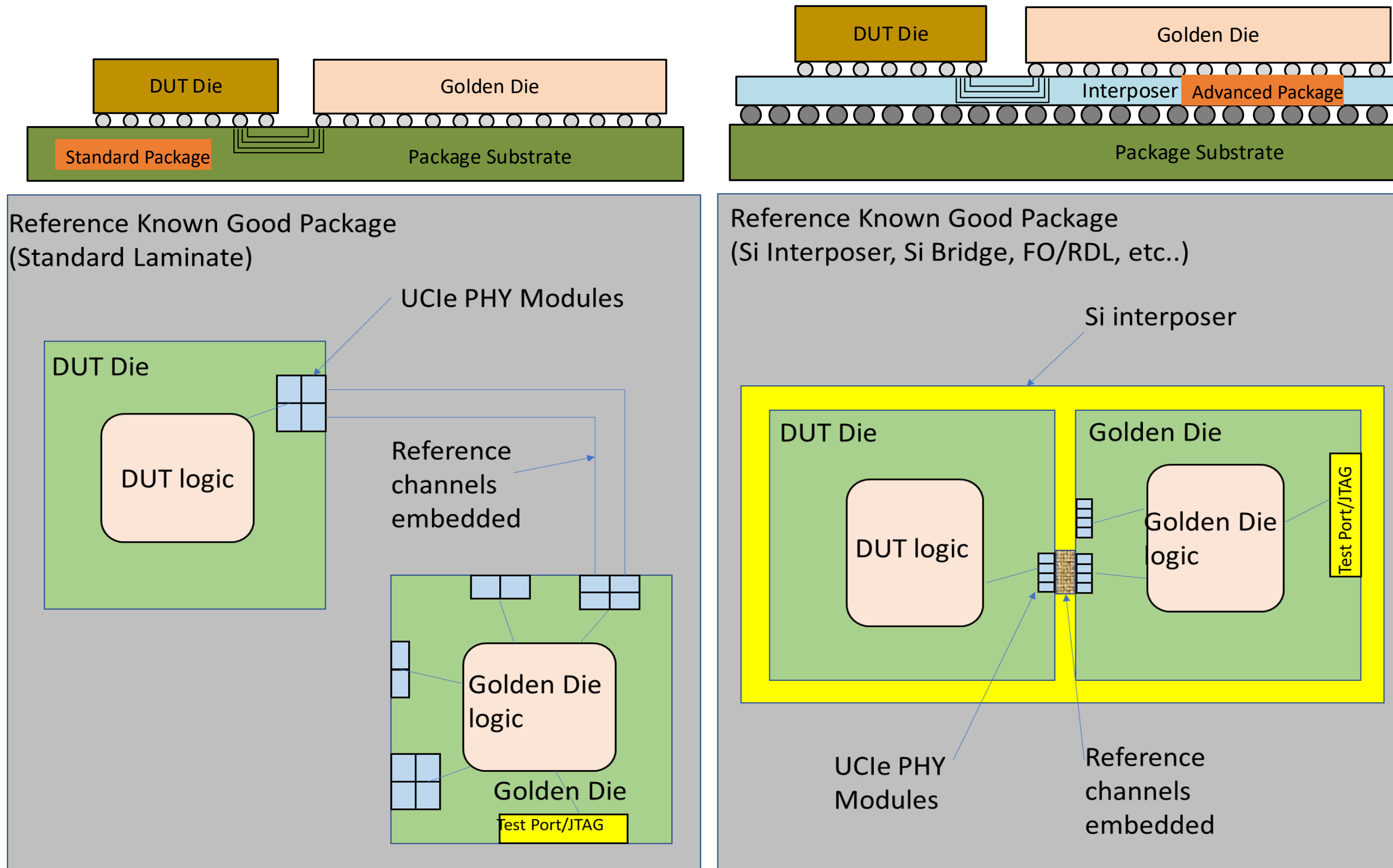
UCIe 1.1: Reduced Width for Cost Optimization

- Some usages need x32 width native width in addition to x64 (e.g., FPGAs with lots of parallel narrower widths consistent with processing capability). One can not gang-up these x32s though (that would be x64s)
- x64 can interoperate with a x32 by utilizing only the lower 32 lanes per module



X32 enables lower-cost advanced packaging by allowing single layer routing in addition silicon area reduction by ~40%

UCIe Compliance: Setup



Ingredients: Reference known good package with Reference Channels, Golden Die, DUT

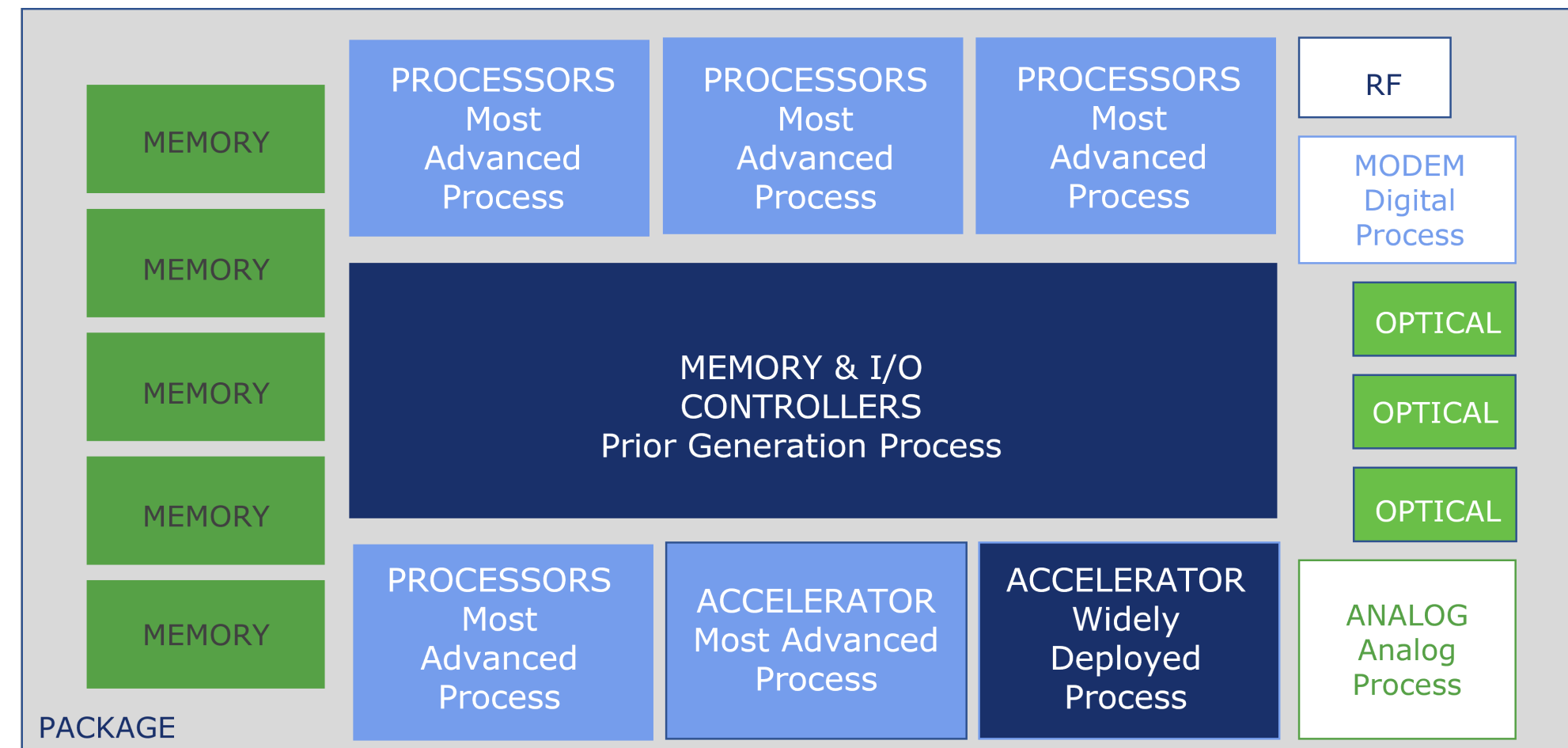
UCIe 1.1 Enhancements: Compliance

- PHY level Compliance:
 - Timing/ Voltage margin, BER measurement, Lane to lane skew, Even/Odd eye asymmetry, Tx EQ – register based control
 - Golden die: all above plus ability to inject errors/ cause timeouts in various phases of training
- D2D Adapter Compliance:
 - DUT: Register based injection of NOP/Test Flit, Replay etc.
 - Golden Die: Support all formats, ability to inject the above, error in sideband, etc
- Protocol Compliance: Expected to be orchestrated through an FPGA / dedicated silicon connected to the golden die
 - Leverage PCIe and CXL protocol compliance as defined by those specifications
 - Streaming Protocols: Use their respective compliance

UCIe Usage Models

Usage Models for UCIE: SoC at Package level

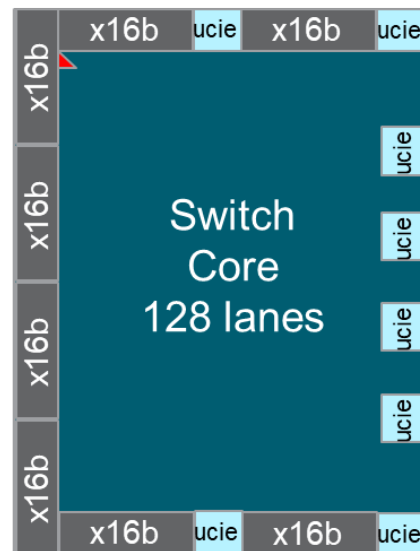
- SoC as a Package level construct
 - Standard and/ or Advanced package
 - Homogeneous and/or heterogeneous chiplets
 - Mix and match chiplets from multiple suppliers
- Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, Automotive, IoT, etc
- UCIE PHY and D2D adapter common
 - PCIe/CXL protocol for plug-and-play
 - Streaming for others (similar to board level connectivity today where scale-up systems are on PCIe PHY)
 - Similar to PCIe/ CXL at board level



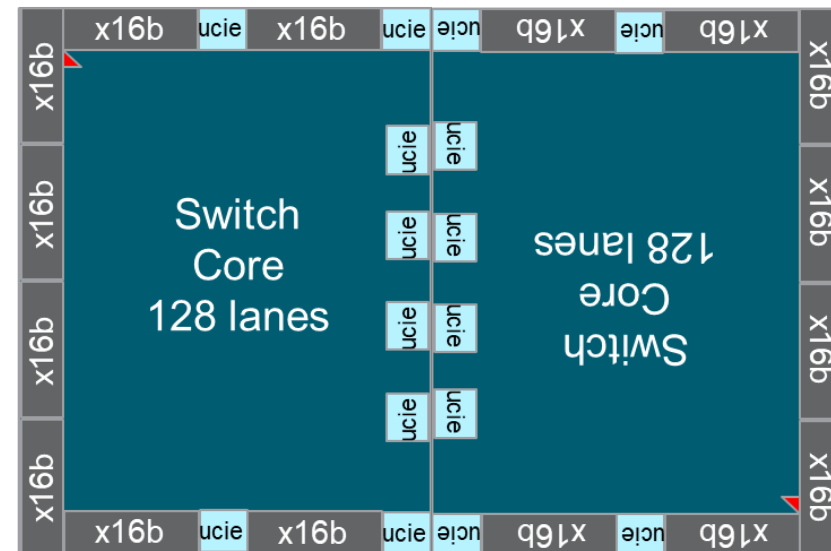
Processors: symmetric coherency protocol mapped on UCIE through FDI
 Memory: CXL.Mem mapped on UCIE through FDI
 Accelerators: PCIe/ CXL mapped on UCIE through FDI
 Modem/ RF/ Optical: Raw mode on UCIE

Example Scale-up SoC from Homogeneous Dies: Large Switch with On-Die Protocol as Streaming Over UCIE

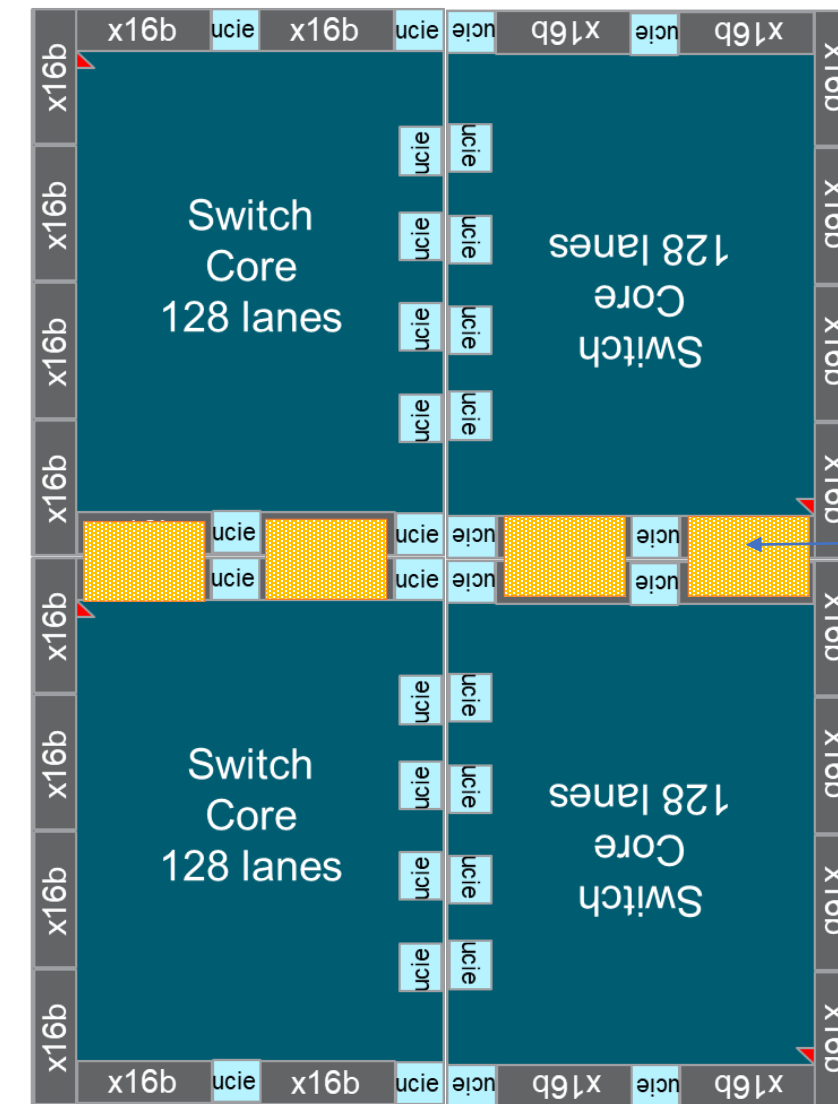
- Need large radix CXL switches – challenges: reticle limit, cost, etc.
- UCIE based Chiplets should help with scalable products
- 64G Gen6 x16b CXL links
- UCIE as d2d interconnect – while this is a scale-up CXL switch, a switch vendor may prefer to have their on-die interconnect protocol be transported over UCIE rather than create a hierarchy of switches which will not work for CXL 2.0 tree-based topology



Small CXL Switch (128 lanes)



Medium-sized CXL Switch (256 lanes)

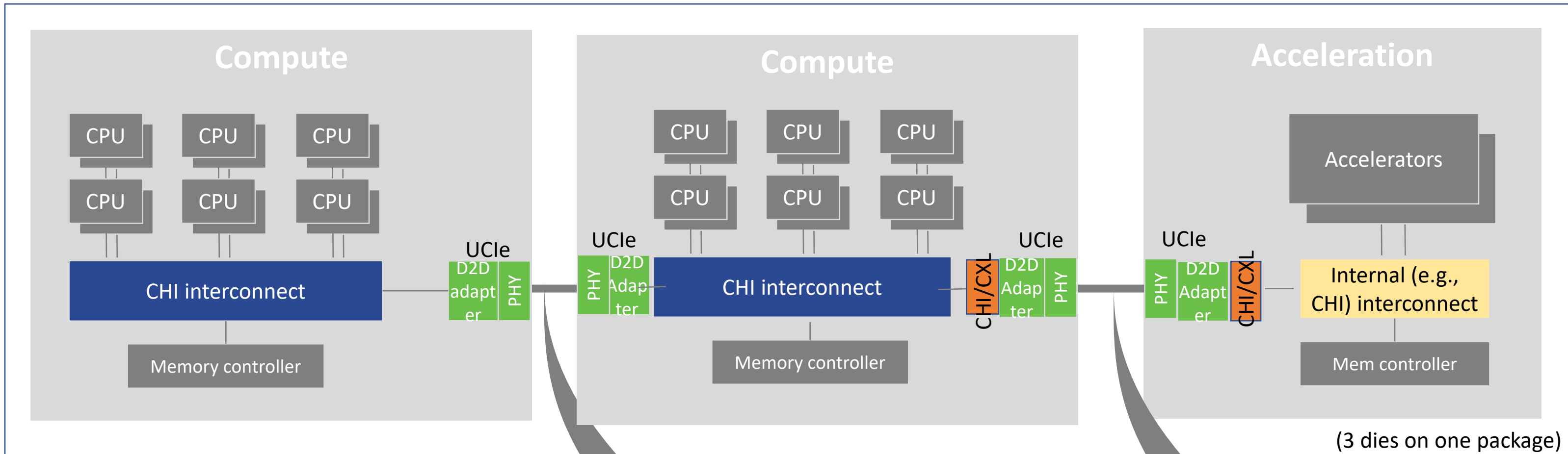


Large CXL switch (512 lanes)

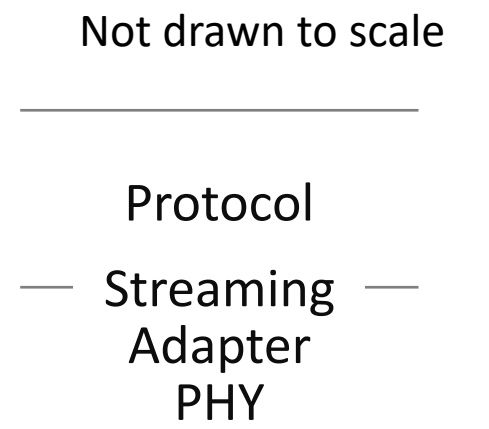
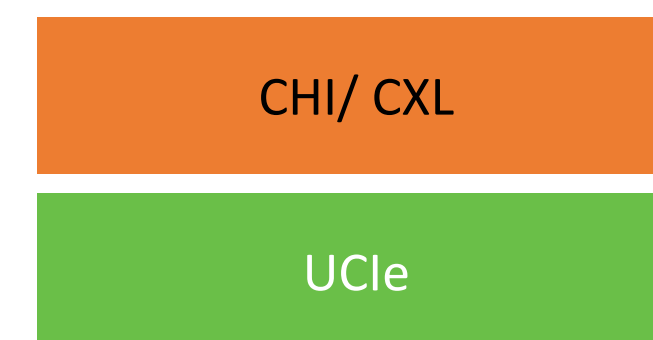
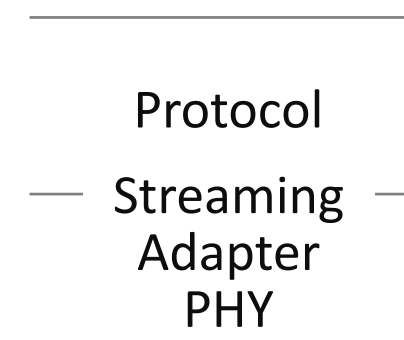
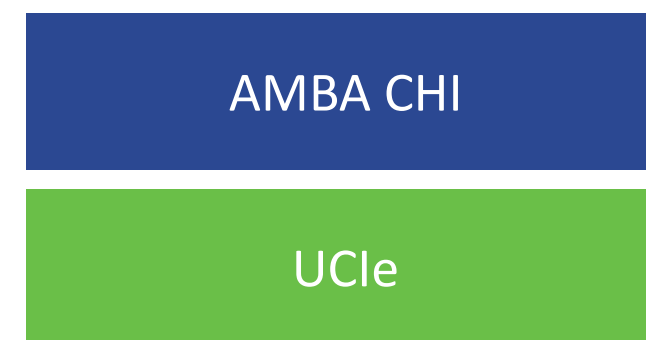
Unused x16 ports
(2 per die)

One can construct CPUs (low, medium, large core-count CPUs) from smaller dies connected through UCIE using the same principle
Here the UCIE PHY and D2D adapter will carry the packetized version of internal CPU interconnect fabric

Example Scale-up Package using Streaming and Open-Plug-In using PCIe/ CXL

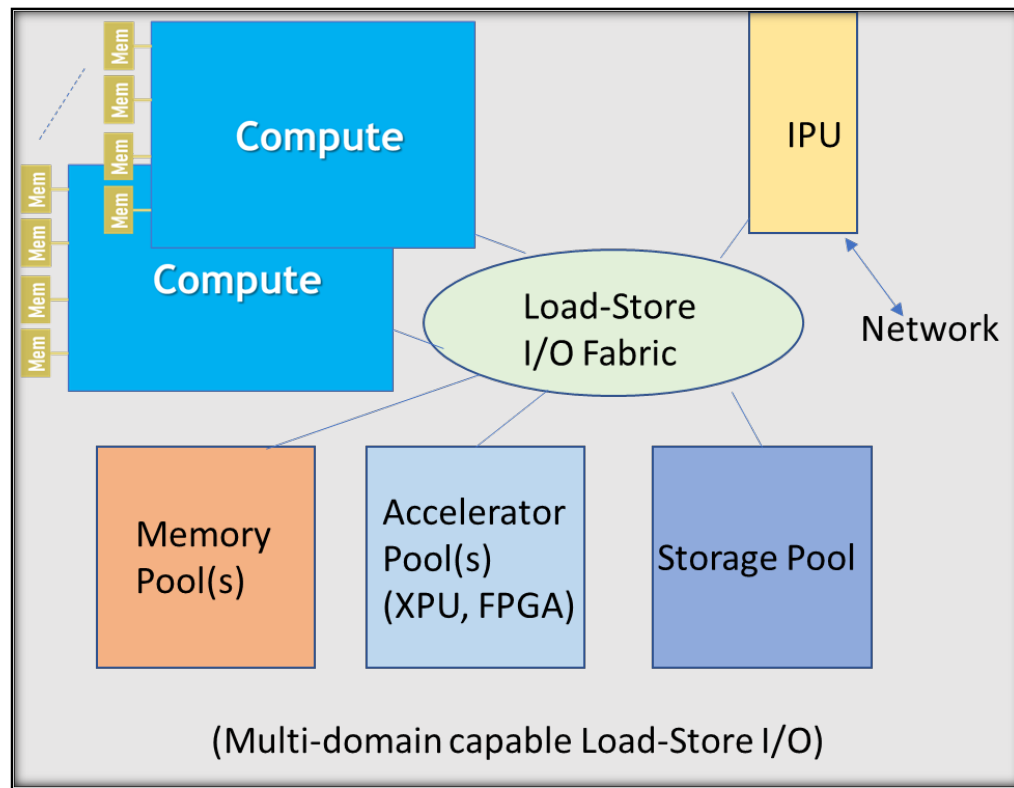


- Transporting the same on-chip protocol allows seamless use of architecture specific features without protocol conversion
- Streaming interface with additional flit formats provide link robustness using UCle defined data-link CRC and retry



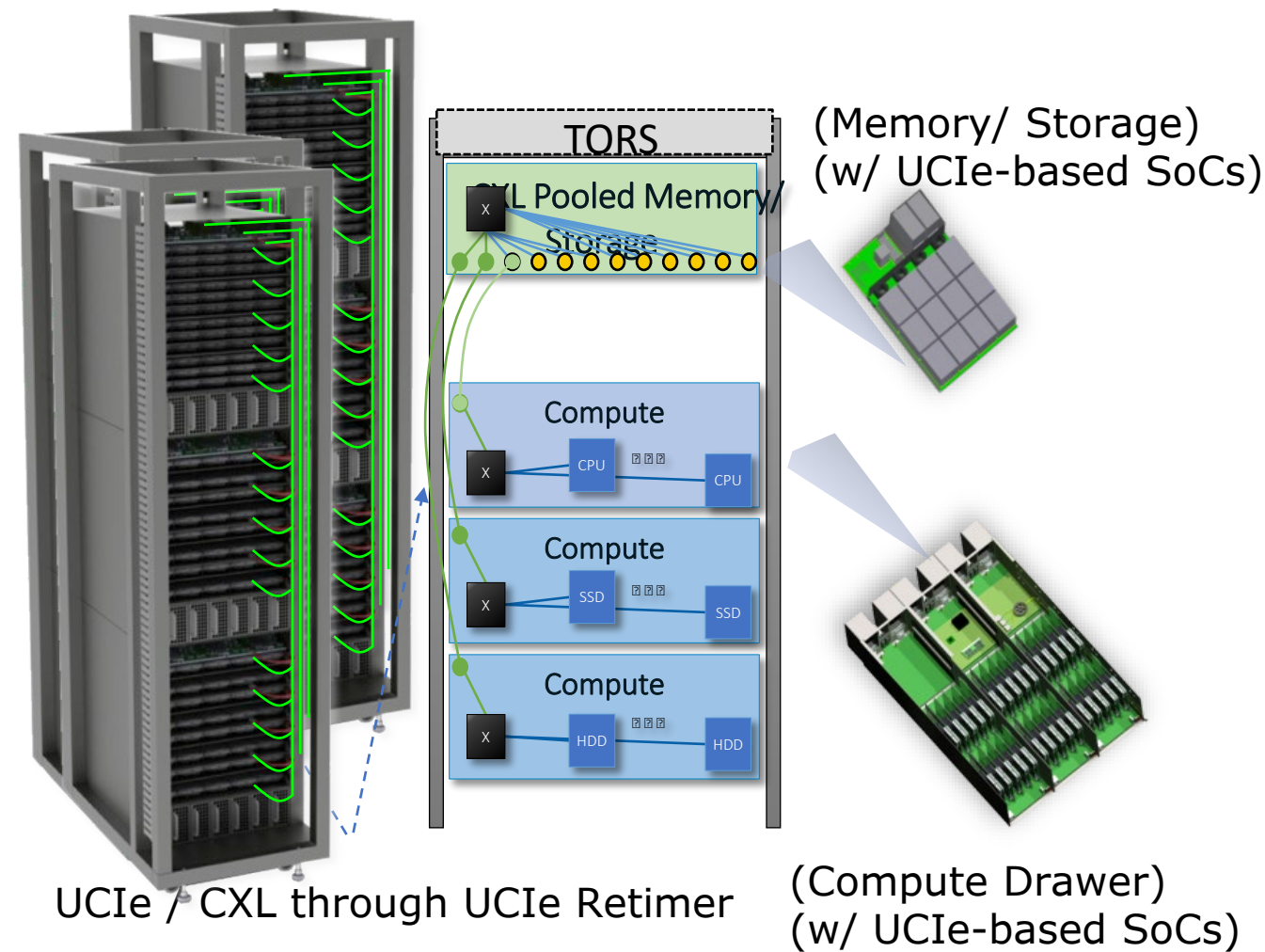
- Any device type in this open plug-in slot with CXL (or CHI if both support it)

UCIe Usage: Off-package Connectivity w/ Retimers



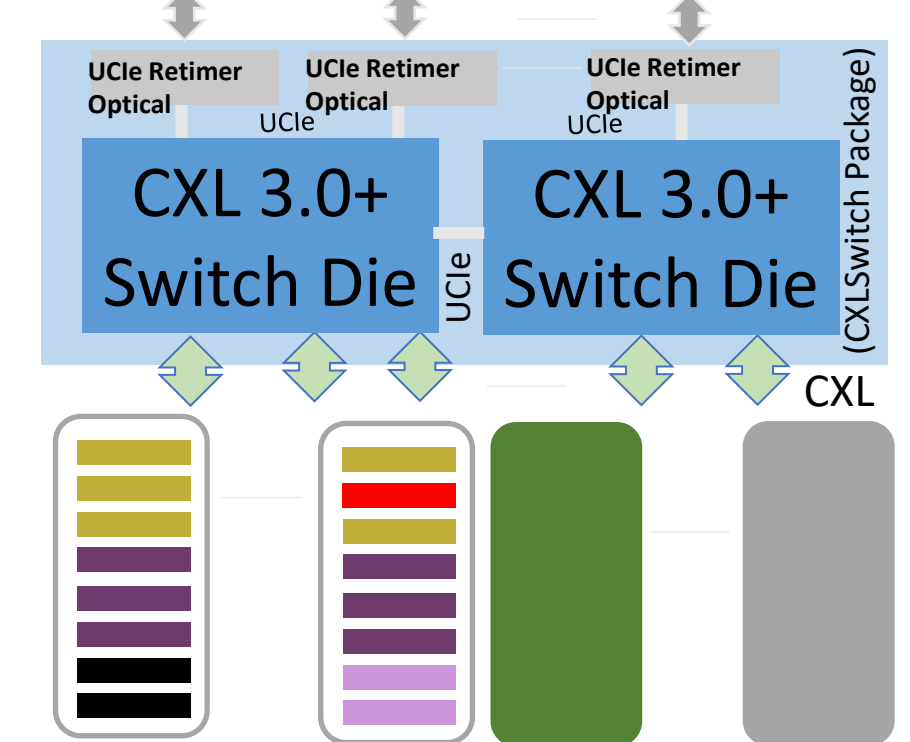
(Use Case: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/ sharing as well as message passing)

(Another example can be multi-terabit networking switches Constructed from UCIe-based co-packaged optics and partitionable networking switch dies connected through UCIe on package)



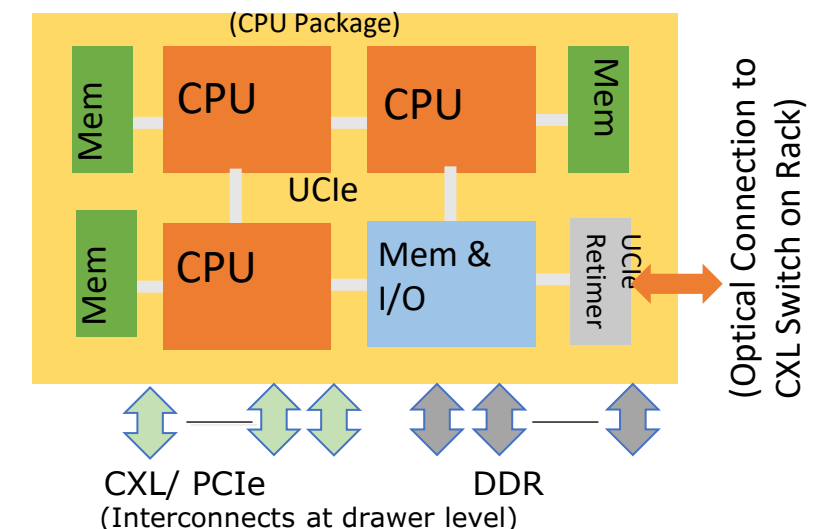
Provision to extend off-package with UCIe Retimers connecting to other media (e.g., optics)

(Optical connections: Intra-Rack and Pod)



(Pooled/ Shared Memory) (Pooled Accelerator)

(Switch dies connected through UCIe PHY + Adapter Running a proprietary switch internal protocol)



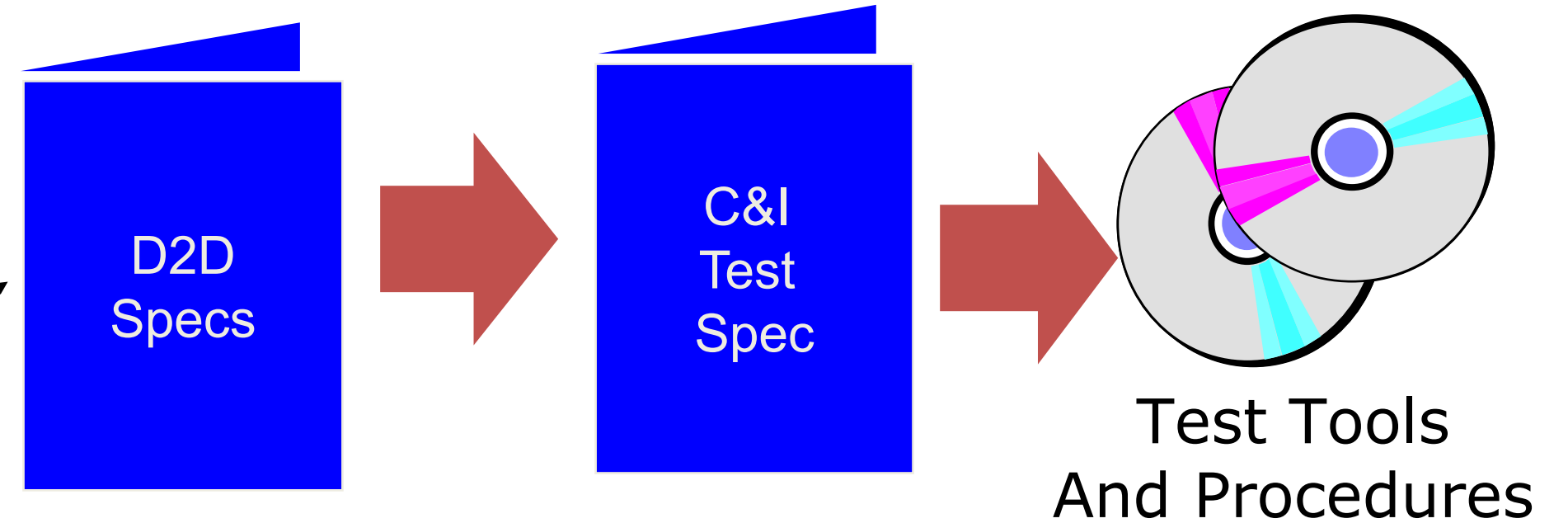
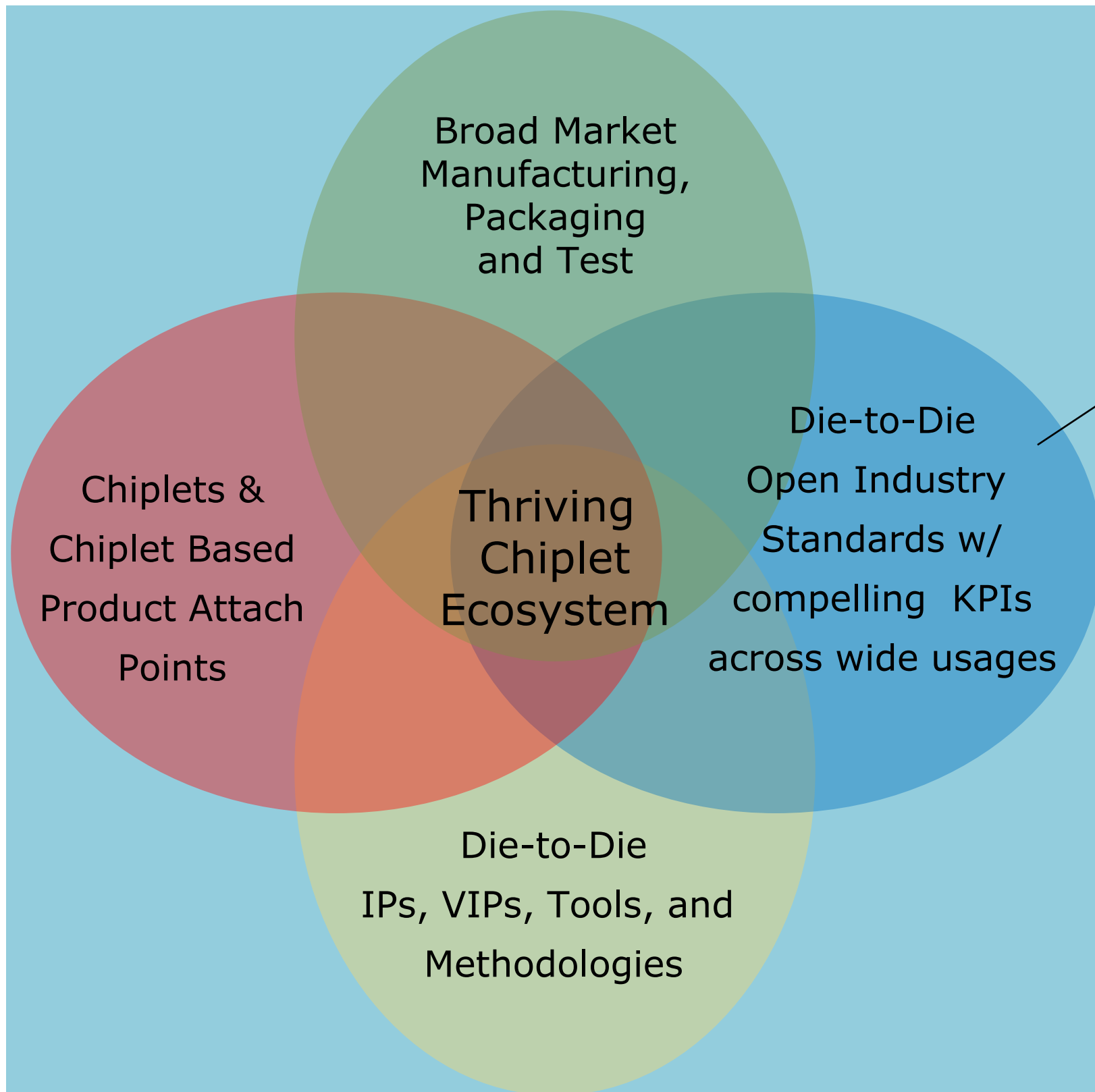
UCIe 1.0/ 1.1: Characteristics and Key Metrics

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm ²)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

UCIe 1.0/1.1 delivers the best KPIs while meeting the projected needs for the next 5-6 years across the compute continuum.

Ingredients for a Broad Inter-operable Chiplet Ecosystem



Well-defined Specs

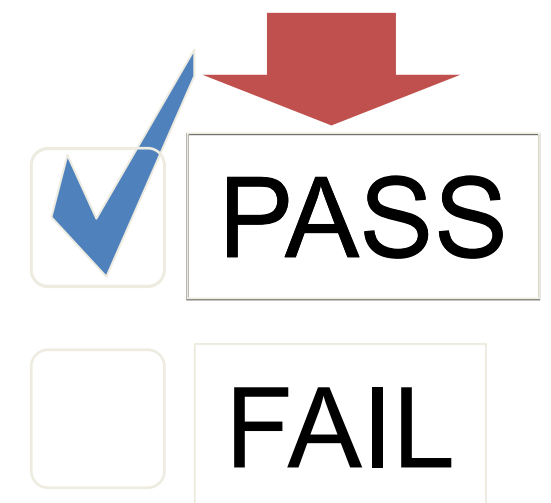
(Electrical, Logical, Protocol (e.g., PCIe/CXL) Software, Form-Factor, Management)

Test criteria based on Specs

(Test Definitions, Pass/Fail Criteria: Electrical, Logical, Protocol, Software)

Test H/W & S/W
Validates

- Test criteria
- Compliance
 - Interoperability



Predictable path to design compliance with UCIE

Summary

- **UCIe Consortium continues to evolve the UCIe Technology in a backward-compatible manner comprehending new usage models, additional cost optimization, and a robust compliance mechanism**
- **UCIe is an open industry standard that establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.**
 - Tremendous support across the industry with several companies announcing IP/VIP availability
 - Evolving as the interconnect of SoCs the same way PCIe and CXL did at the board level
 - UCIe 1.1 Specification is available to the public <https://www.uciexpress.org/specification>
- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor or Adopter level.**
- **6 Technical Working Groups** (Electrical, Protocol, Form Factor/Compliance, Manageability / Security, Systems and Software, Automotive) and **Marketing Working Group** driving the technology forward
 - Plenty of innovations happening in the consortium
- **Join us if you have not done so! Learn more by visiting www.UCIexpress.org**

Thank You

www.UCIexpress.org

