

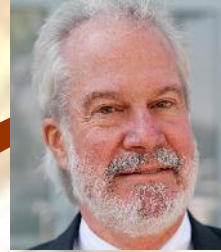


Moving DRAM to 3D

Jim Handy

OBJECTIVE ANALYSIS

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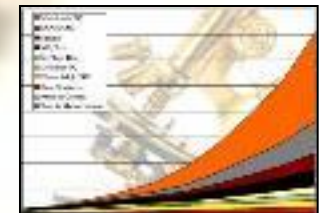
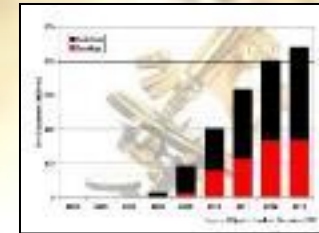


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OBJECTIVE ANALYSIS

Semiconductor Forecast Accuracy

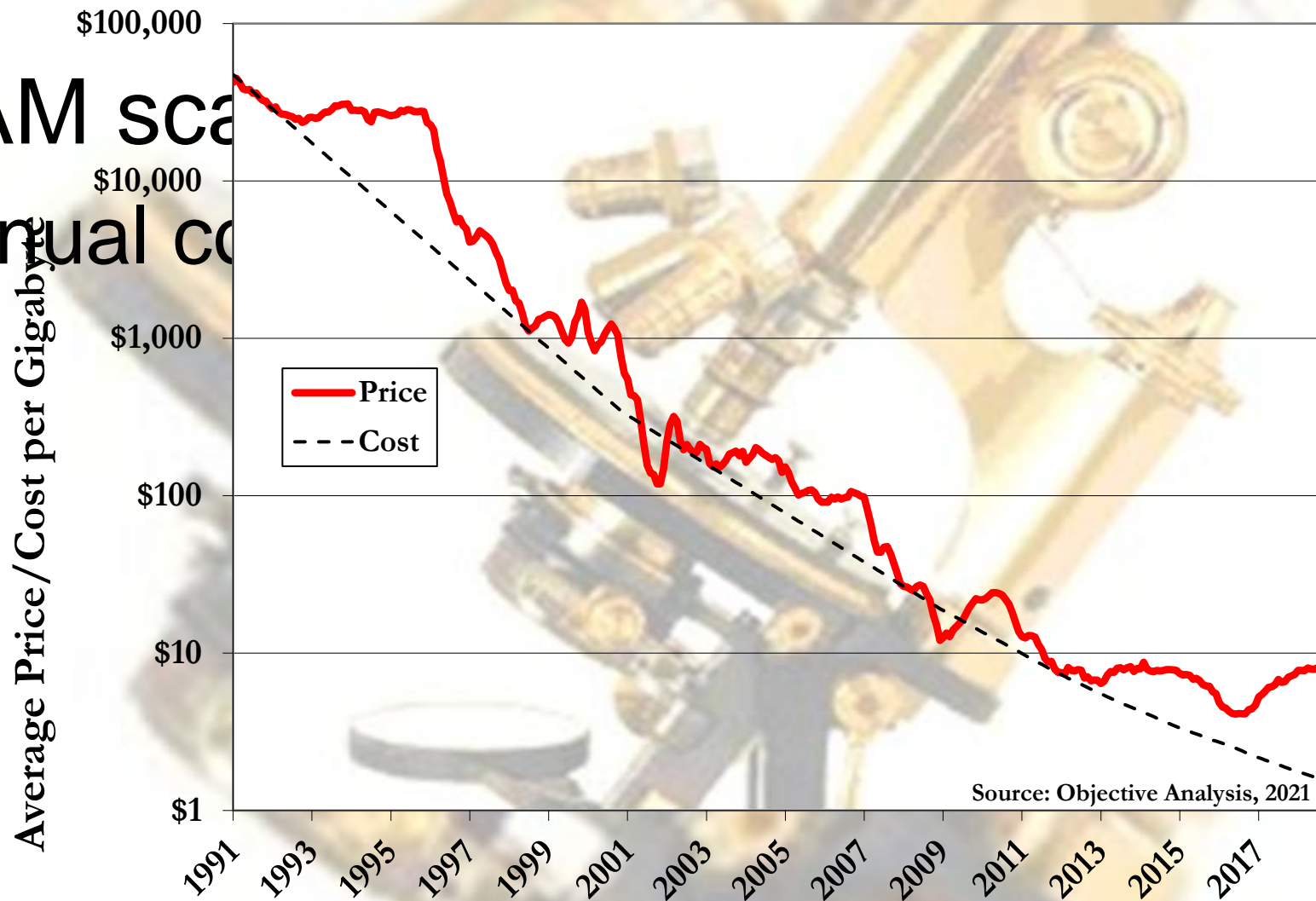
Year	Forecast	Actual
<u>2008</u>	Zero growth at best	-3%
<u>2009</u>	Growth in the mid teens	-9%
<u>2010</u>	Should approach 30%	32%
<u>2011</u>	Muted revenue growth: 5%	0%
<u>2012</u>	Revenues drop as much as -5%	-2.7%
<u>2013</u>	Revenues increase nearly 10%	4.9%
<u>2014</u>	Revenues up 20%+	9.9%
<u>2015</u>	Revenues up ~10%	-0.2%
<u>2016</u>	Revenues up ~10%	1.1%
<u>2017</u>	Revenues up ~20%	22%
<u>2018</u>	Strong start supports 10+% growth	14%
<u>2019</u>	Semiconductors down -5%	-12.5%
<u>2020</u>	Zero growth at best	6.8%
<u>2021</u>	Revenues grow 6% by remaining flat	26.2%
<u>2022</u>	Total semi still grows 6%	TBD



Let's Talk About DRAM!

The Problem

- DRAM scaling – Annual cost



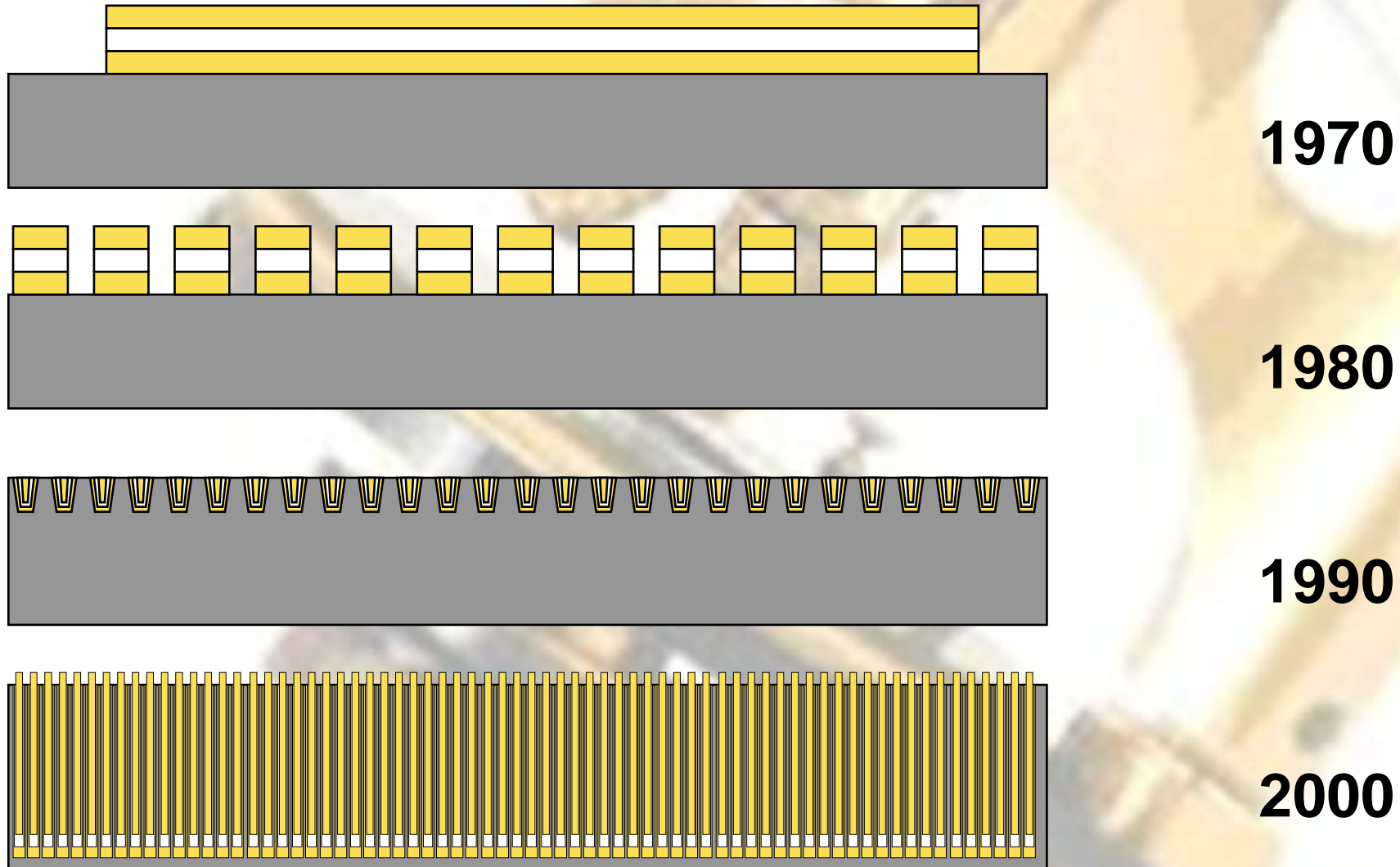
Source: Objective Analysis, 2021

The Problem

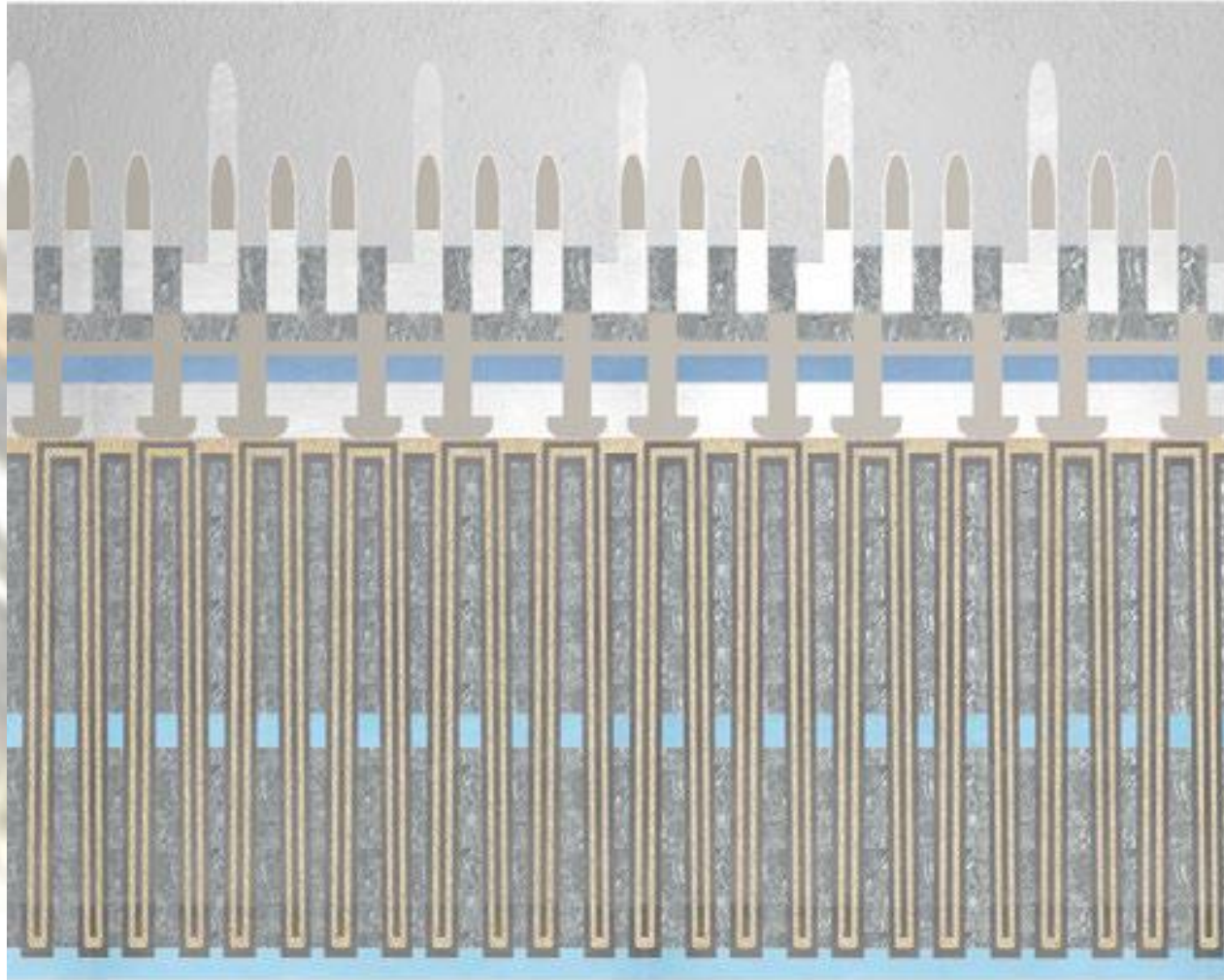
- DRAM scaling is slowing down
 - Annual cost declines are getting smaller
- Industry is hitting physical limits
 - NAND successfully overcame this by going 3D

Can DRAM go 3D too?

DRAM Is Already 3D



DRAM Is Already 3D



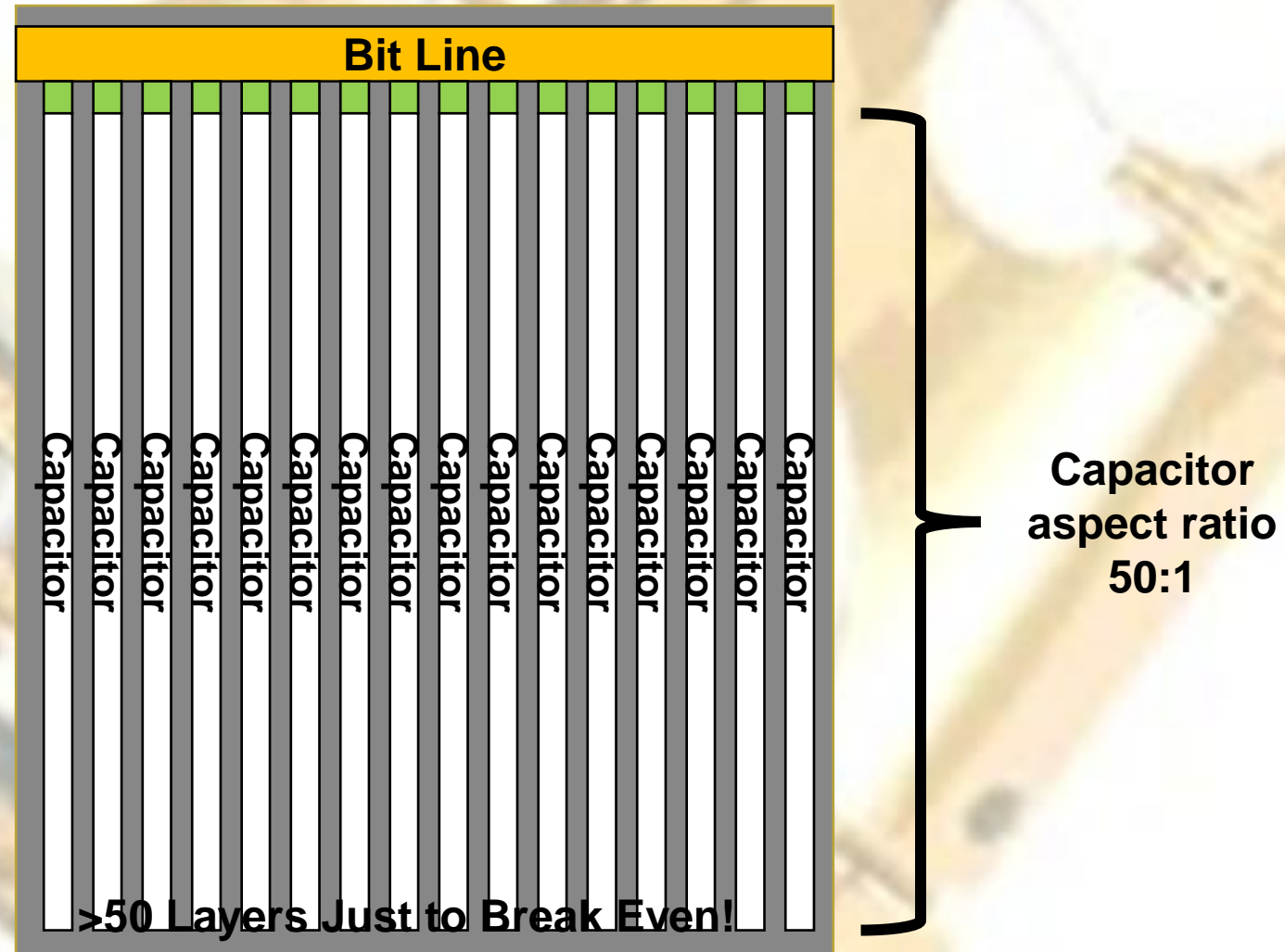
So What's The Problem?

- Deep & Narrow trenches are hard to etch well
- The standard way to follow Moore's Law is to shrink the cell, which means:
 - Smaller width & length
 - Deeper trench
- The alternative is to use new dielectrics
 - Not well understood in a production environment

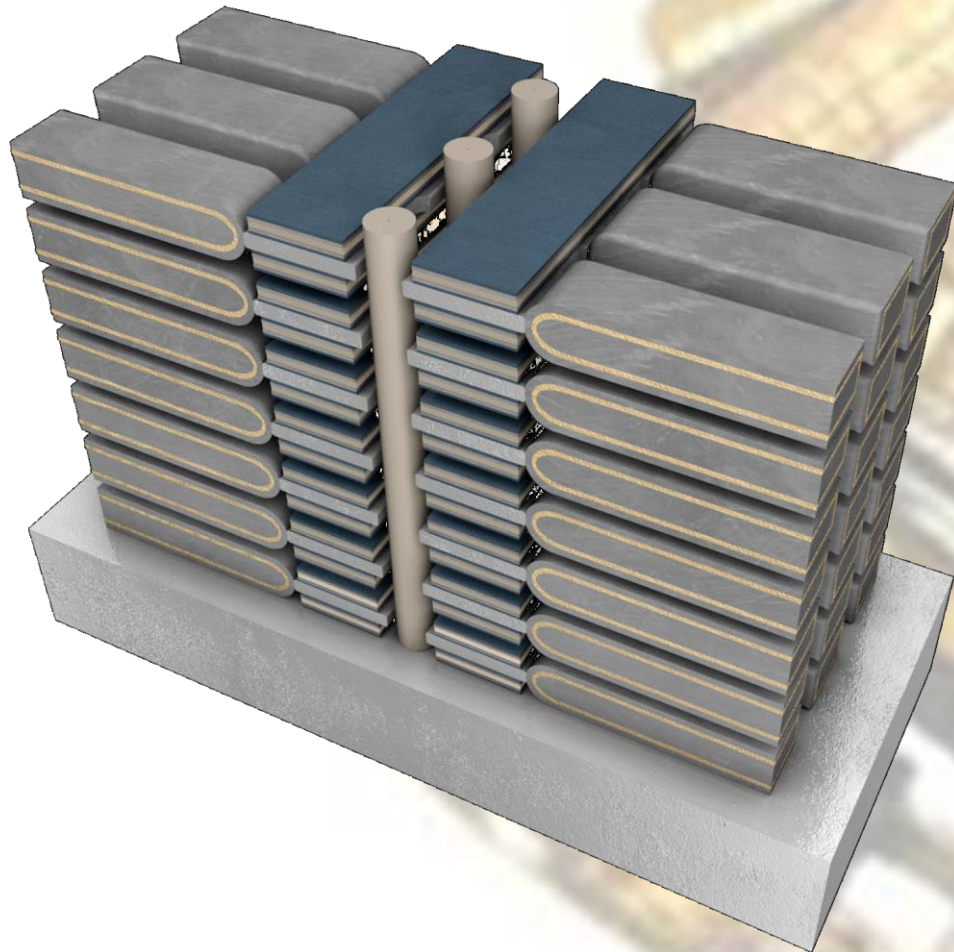
How NAND Flash Went 3D



The Problem with 3D DRAM



Applied Materials Approach



- Turn everything sideways
 - Simplifies capacitor etch
 - Complicates high-speed signals
- Should stack as high as NAND

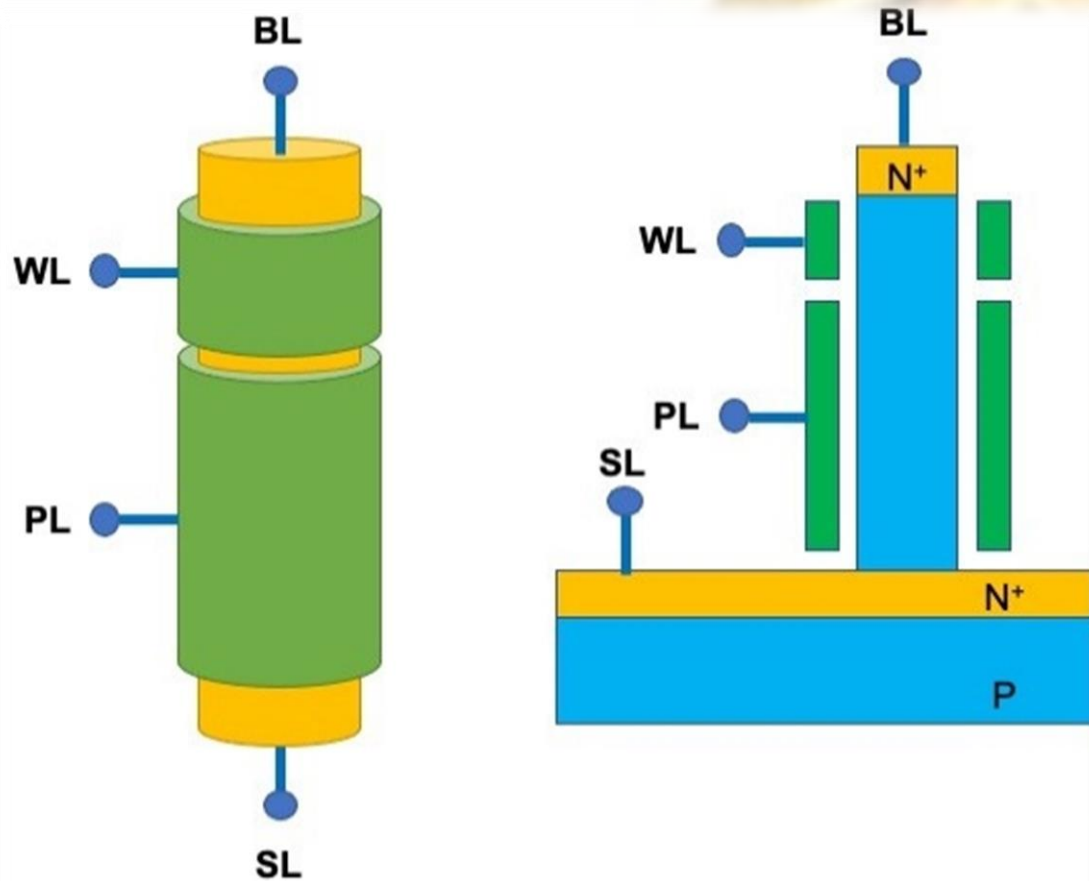
No Shortage of Alternatives

- Z-RAM
- Dynamic Flash Memory
- Short-retention flash
- Monolithic3D
- Vertical select transistor
- HfO dielectric on 3D NAND-like structure
- Gain cell
- IGZO
- Vertical Layered Thyristor (VLT)

Z-RAM

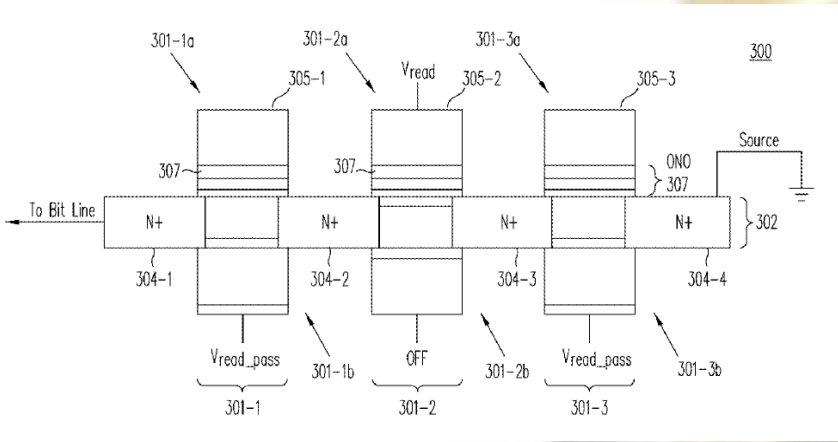
- The original floating body DRAM
 - No capacitor
- Made a big splash in 2007
 - Company still exists, but no website today

DFM: Dynamic Flash Memory



- Stabilized floating body concept
- Highly promoted
- Potentially stackable
- Not yet prototyped

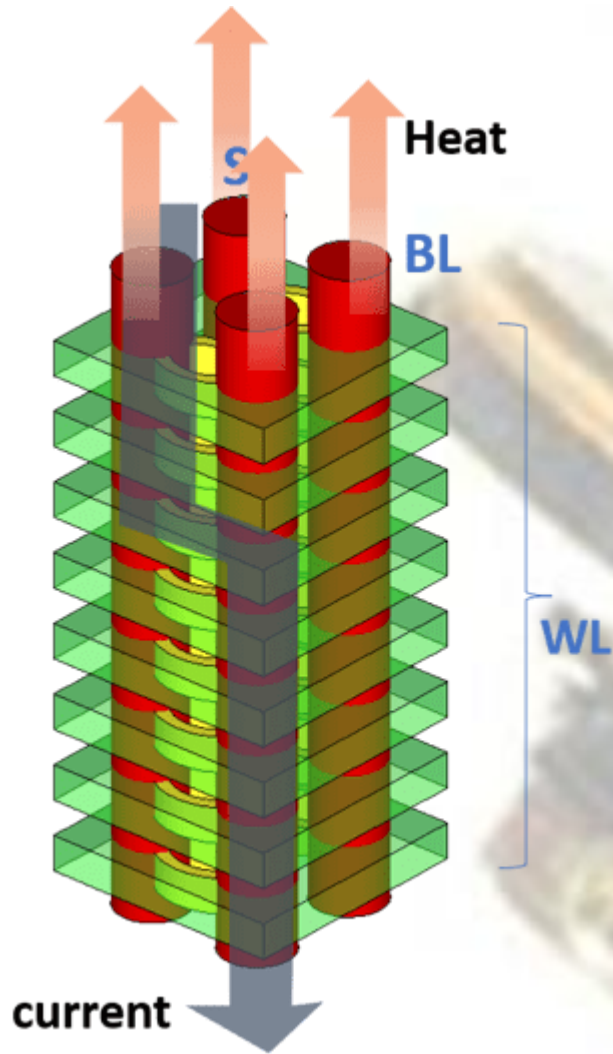
Short-Retention NAND Flash



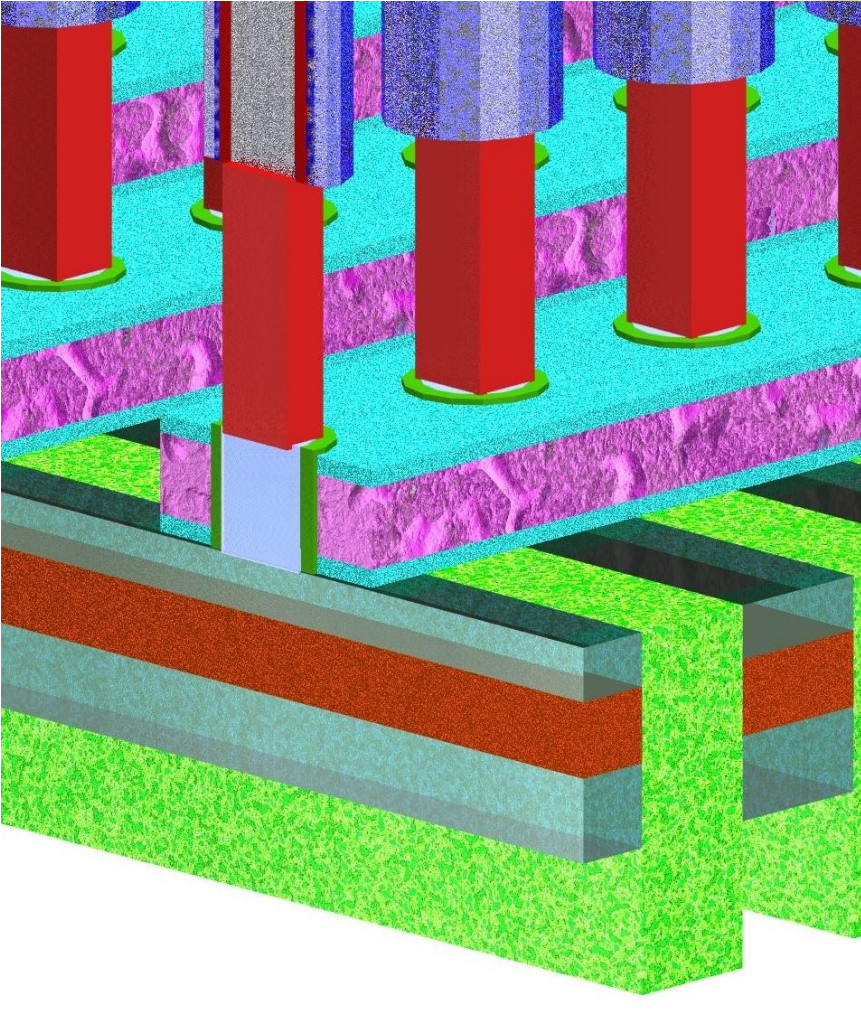
- It's a tweaked 3D NAND chip
 - Built using existing 3D NAND chip designs
- Trades off fast write against short retention
 - Like DRAM it needs refreshing
- Patent applied for, then abandoned

Monolithic3D

- Similar to 3D NAND topology
- Metal pillars instead of polysilicon
- 3 holes for every bit line
- Not yet prototyped

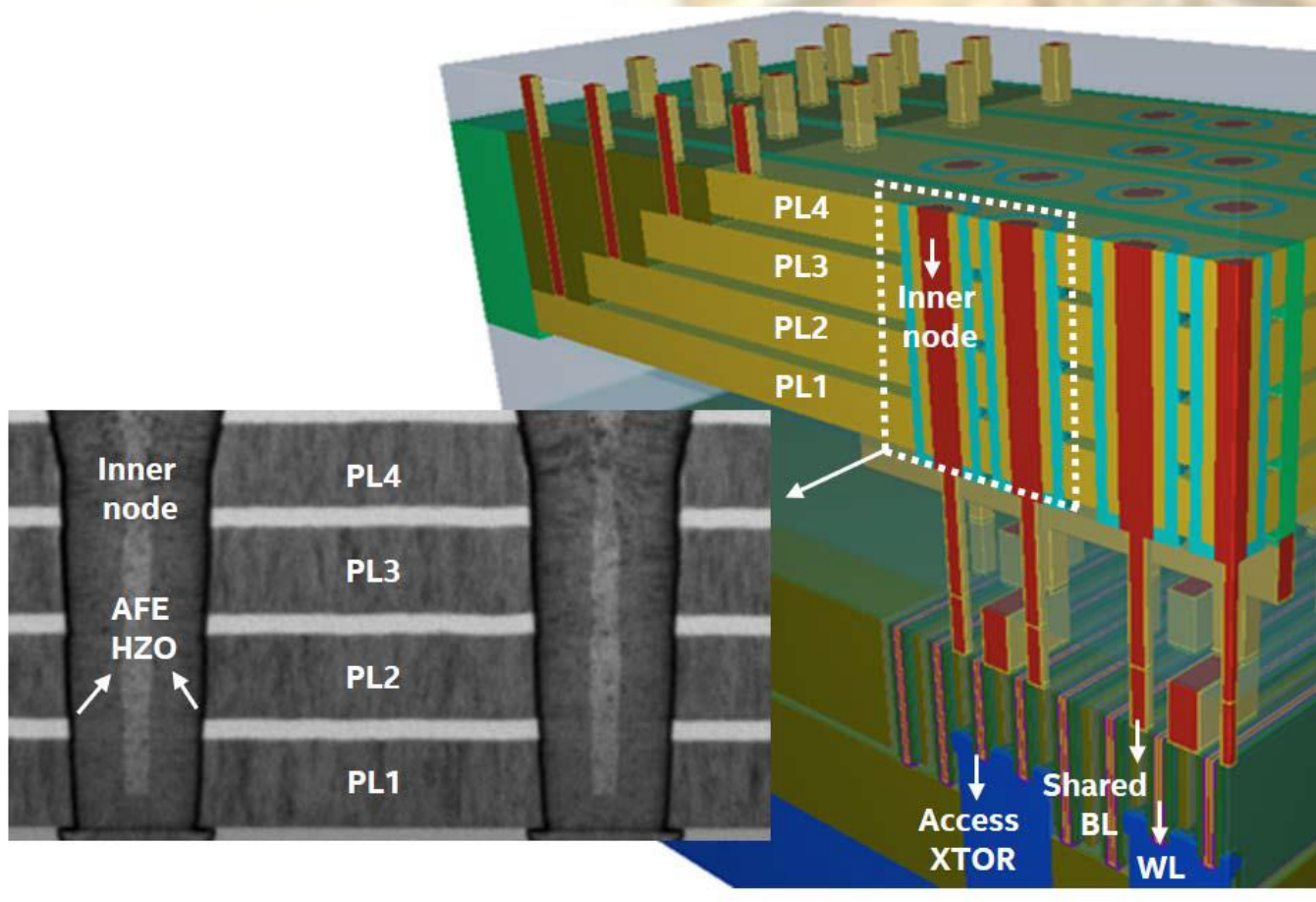


Spin Memory's Vertical Selector



- Borrows 3D NAND techniques
- Supports smaller cells
 - Potentially stackable
- Company liquidated

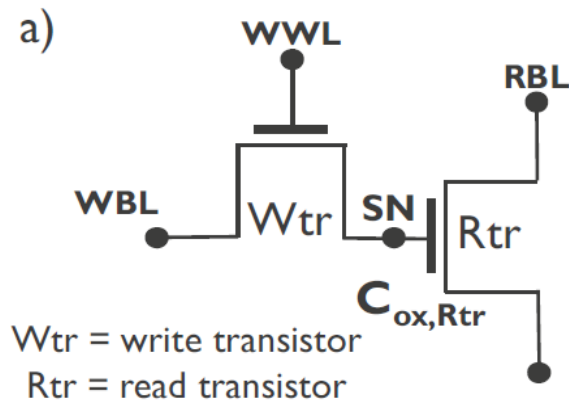
Intel's HfO Dielectric 3D DRAM



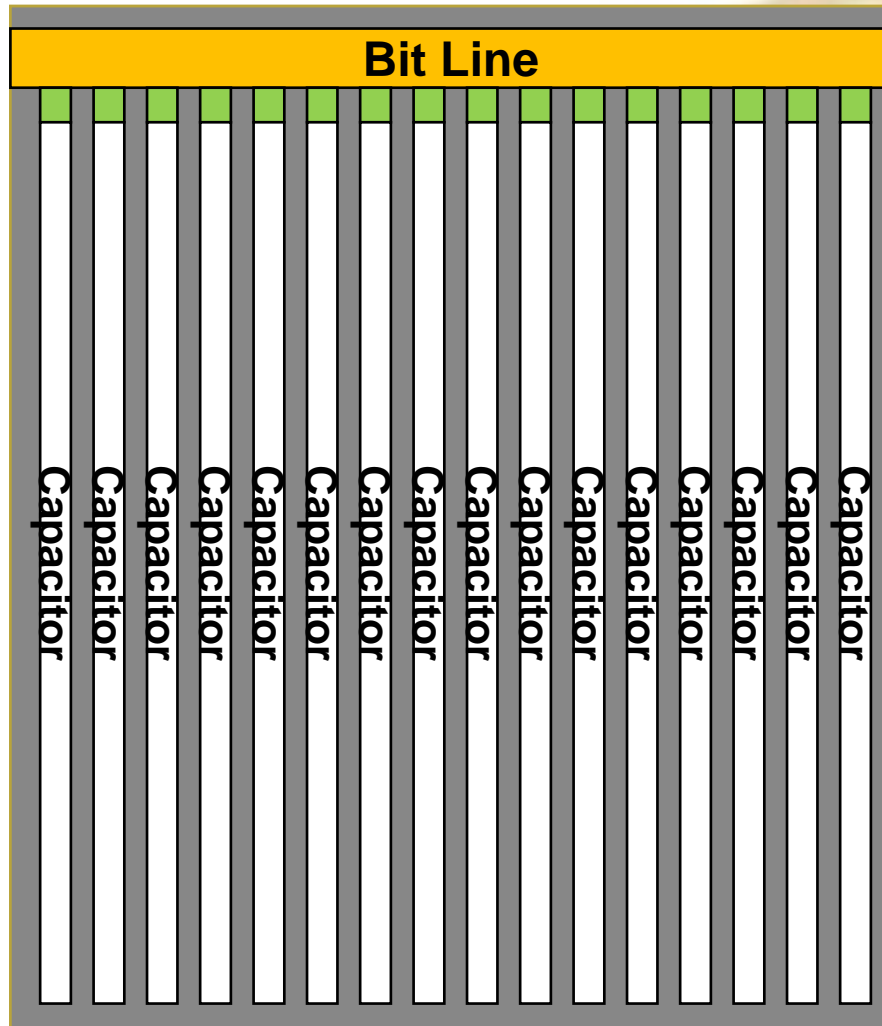
- Presented at IEDM '20
- Working prototypes
- 3D NAND topology
- Antiferroelectric HfO dielectric
 - Not well understood

Gain Cell

- 2-transistor-0-capacitor (2T0C) DRAM cell
- May not have economies of 3D NAND
 - Current designs use more costly topology

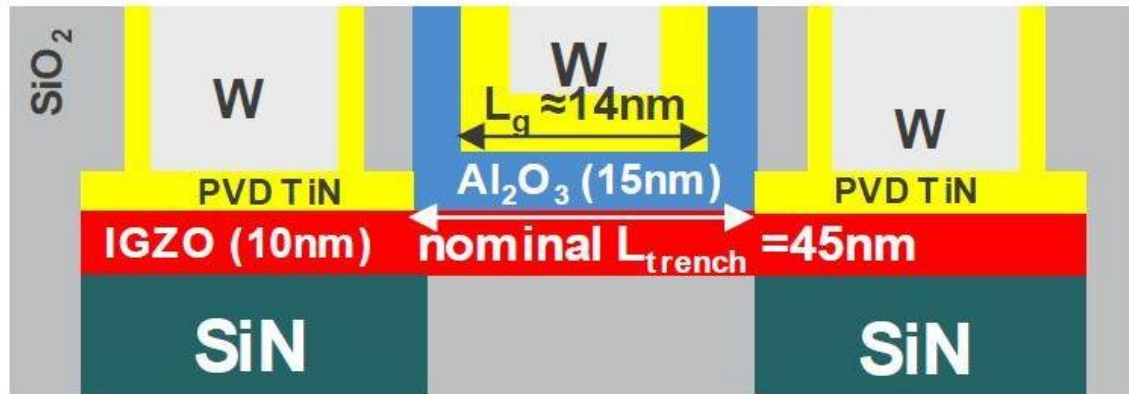


Gain Cell Pluses and Minuses

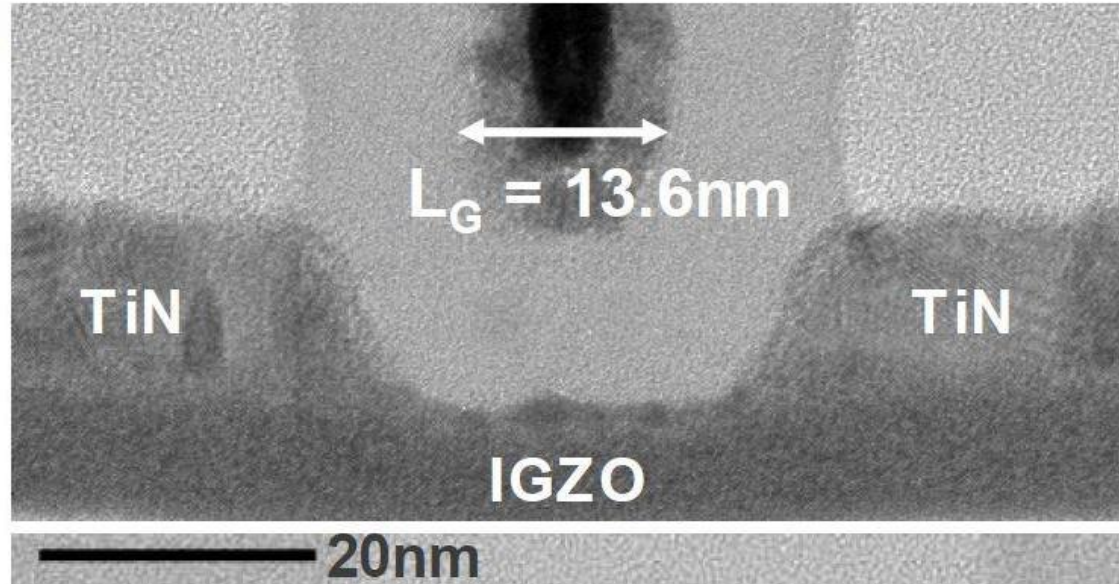


- Remove half of the capacitors
- Shrink the other half
- Suddenly it's like a NAND string!

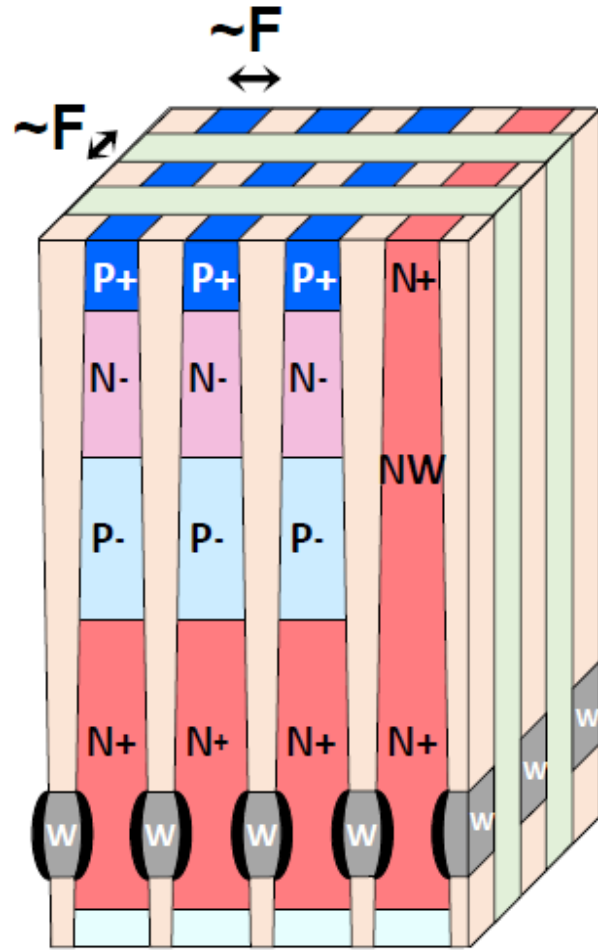
IGZO: Indium Gallium Zinc Oxide



- Gain cell with low-leakage read transistor
- Shown at IEDM 2020
- Lab prototypes at 45nm (imec)
- IGZO is not well understood



VLT: Vertical Layered Thyristor



- Announced in 2016
- Capacitor-less $4f^2$ cell
 - Prototyped at 55nm
 - Scales $<10\text{nm}$
- Never got any traction



The Short Answer?

We're not even close yet!

Moving to 3D

Lessons Learned from NAND Flash

- Toolset changes are extremely expensive
- New processes are hard to master
 - Toshiba announced BiCS in 2007
 - First 3D NAND shipments 2013
 - Production stalled until 2016
 - Shortages in the interim
- All vendors must pull together



My Expectation?

It's about a decade out.

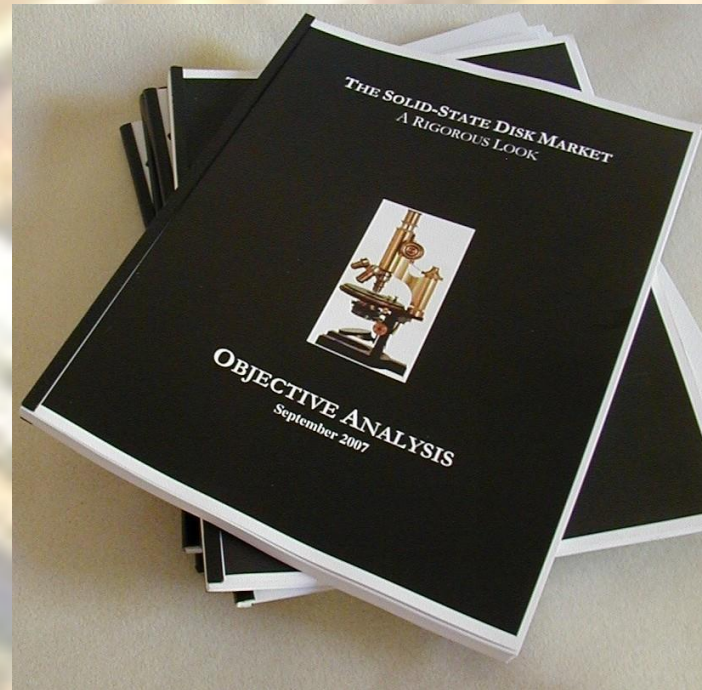
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QUESTIONS?