Flash Memory Summit

Persistent xSPI STT-MRAM Memory Device enabled with both Serial SRAM and NOR Flash Protocol

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Safe Harbor Statement

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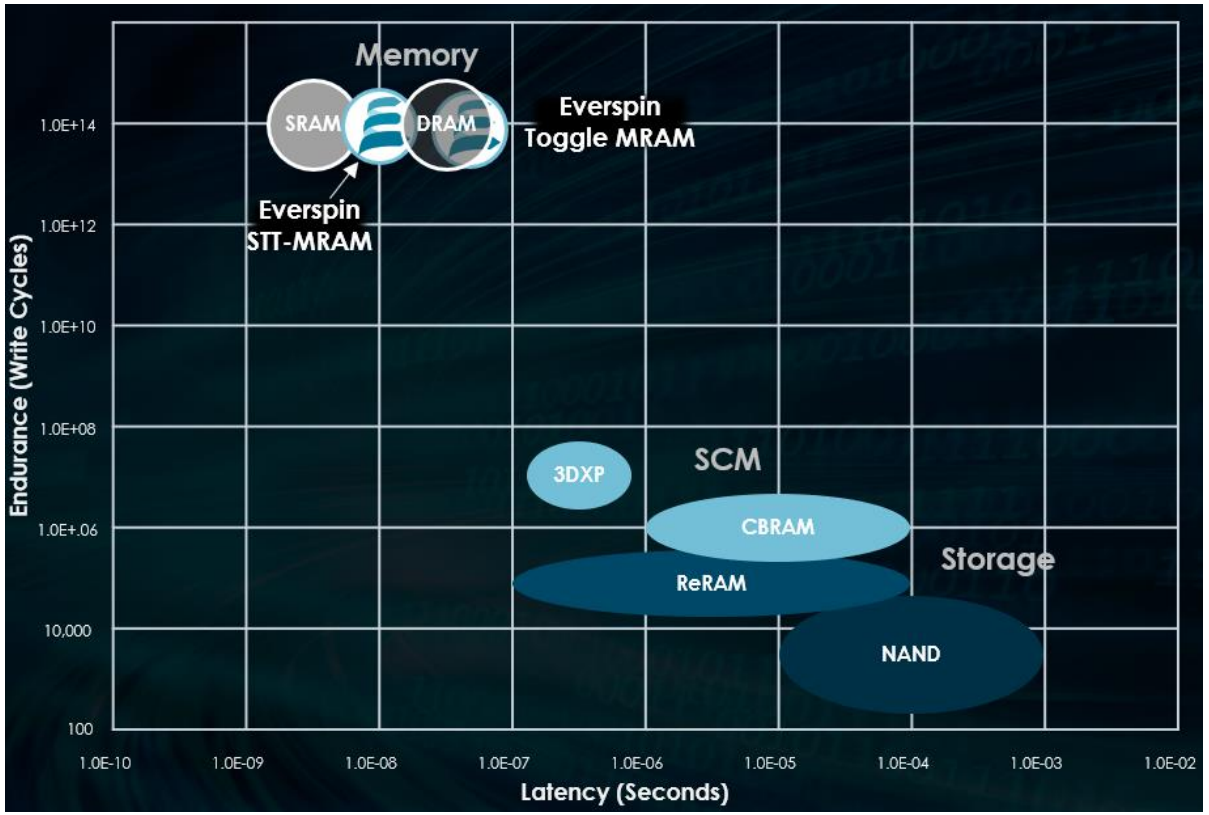
Outline

- MRAM introduction
  - Advantages and Applications
- Introducing the fastest xSPI STT-MRAM
  - Design and Technology Advances
- Write Speed and Energy Advantages
- Conclusion

MRAM for Persistence in Working Memory



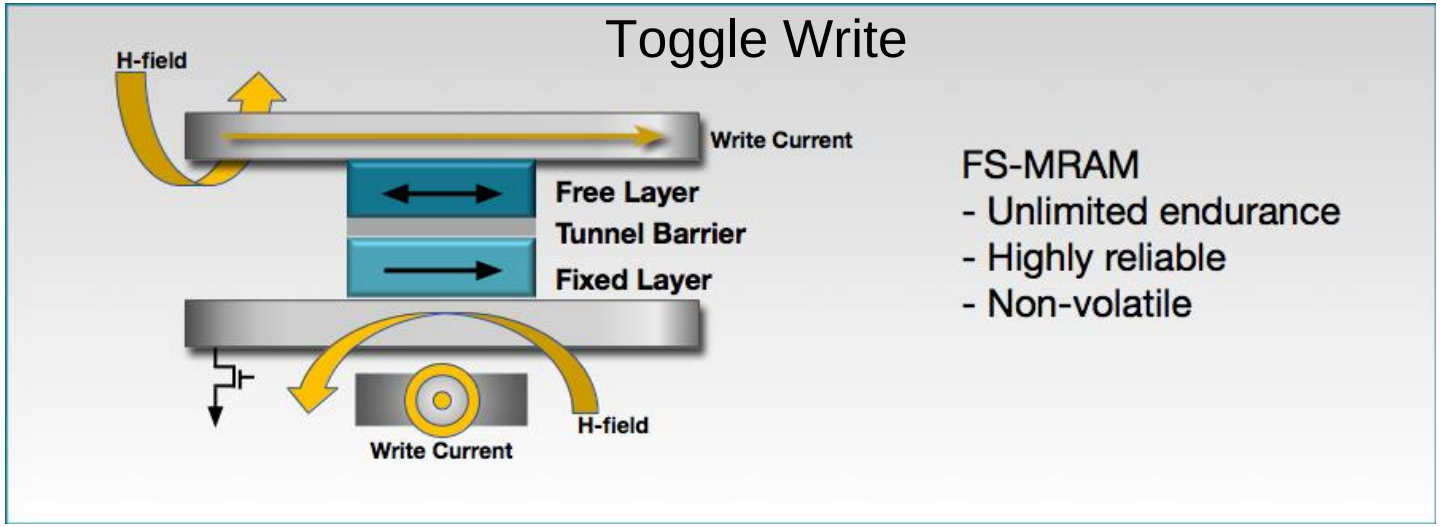
MRAM COMBINES PERFORMANCE OF MEMORY WITH PERSISTENCE OF STORAGE

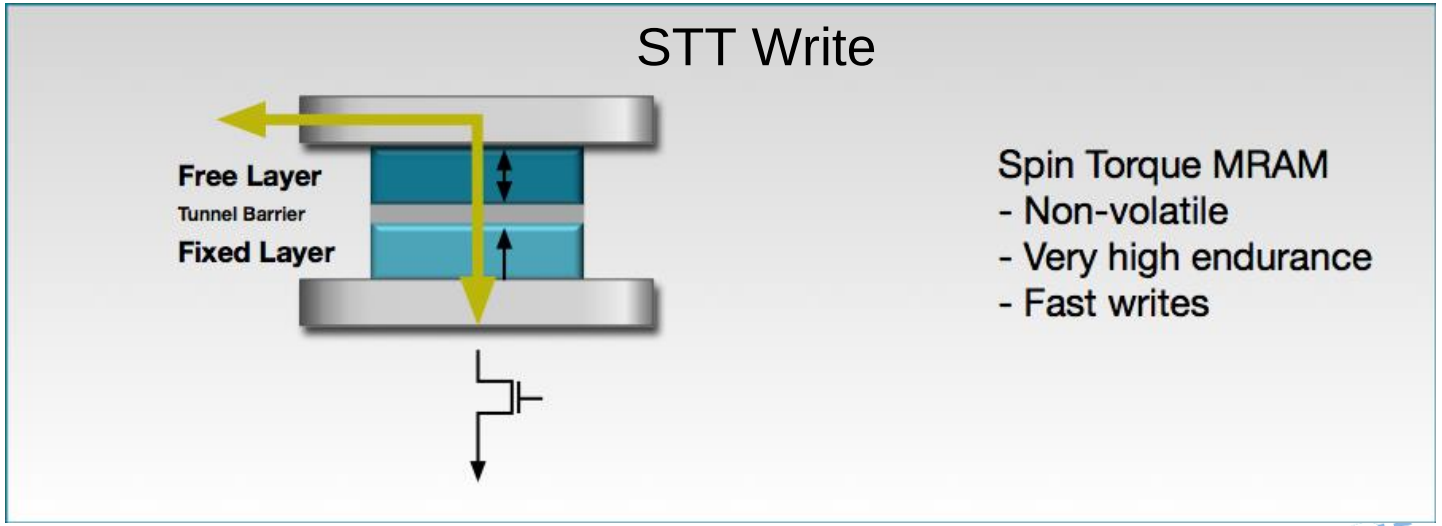
- **Non-Volatile:** Maintains data without power or refresh
- **Fast:** Read/write similar to DRAM
- **Endurance:** Handles memory workloads

MRAM Generations

- Toggle MRAM uses a magnetic field for switching
  - *Limits scaling due to constant magnetic field*

- Spin-transfer torque (STT) MRAM enables scaling to Gb densities





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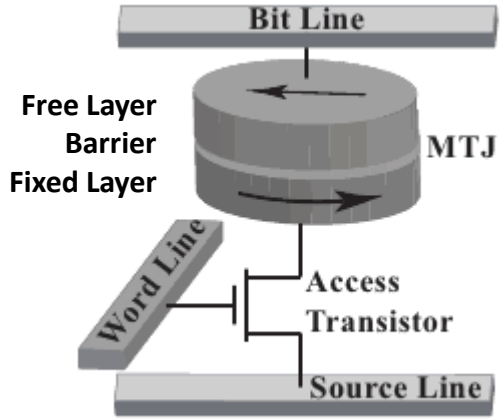
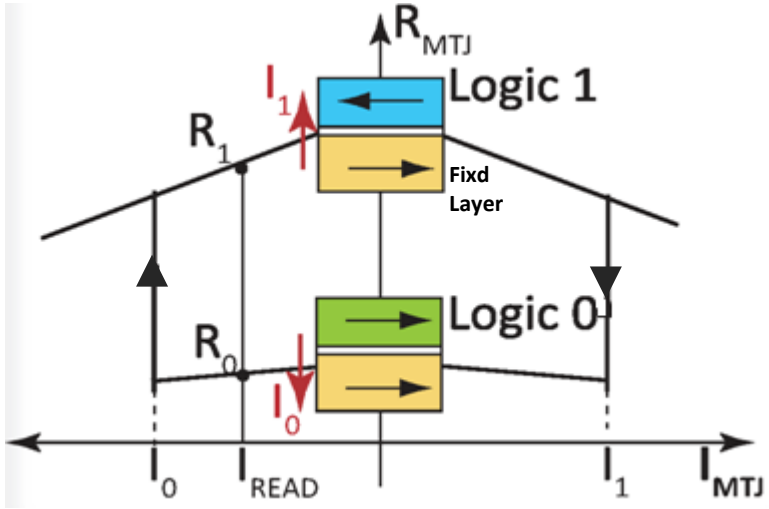
STT-MRAM Bitcell



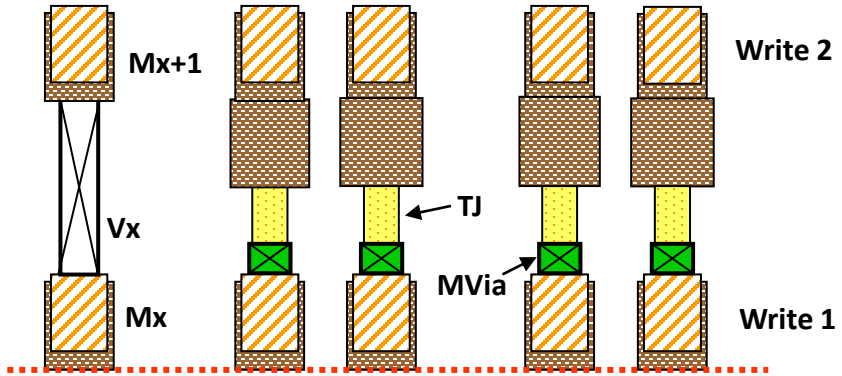


- Magnetic Tunnel Junction (MTJ) with
  - Logic 1 – high resistance state
  - Logic 0 – Low resistance state
- Spin-transfer Torque (STT) current based switching between logic states
  - Direct torque transfer (Logic 1 to 0 switch)
  - Reflective torque transfer (Logic 0 to 1)
- MR (magnetoresistance) based read

$$MR = \frac{R_1 - R_0}{R_0}$$

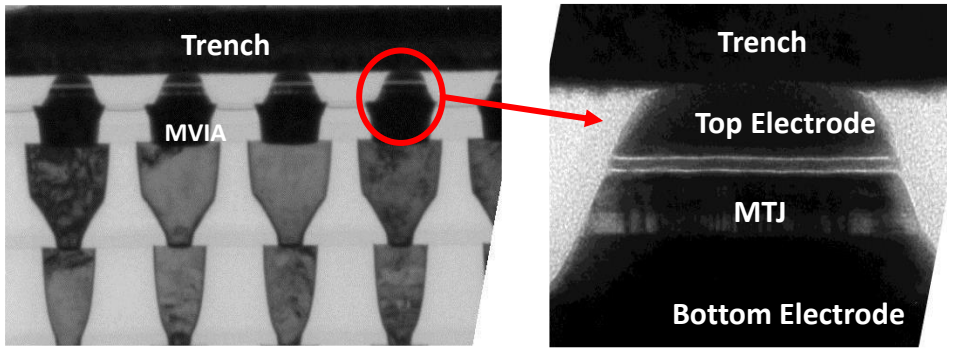
STT-MRAM – Easy Integration with CMOS

On Axis Integration, 1Gb STT-MRAM



MRAM Layer Additions

MVia	TJ	Trench
Msk1	Msk2	Msk3



STT-MRAM in
GlobalFoundries' 28nm CMOS technology

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Comparison of MRAM with Other Memories

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				Emerging NVM w/ Production Proven Quality				In Development	
	SRAM	DRAM	3D NAND Flash	**Toggle-MRAM**	**STT-MRAM**	ReRAM	PCRAM	FeFET	NRAM (CNT)
Nonvolatility	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Endurance (cycles)	Unlimited	Unlimited	$10^3 – 10^5$	Unlimited	$10^9 – 10^{15}$ Unlimited	10^5 - 10^9	$10^6 – 10^9$	10^4 - 10^5	10^{15}
Write speed (ns)	< 1	1 – 10	$10^5 – 10^6$	1-10	1 – 100	10 - 10^5	100 - 10^4	10	10
Memory capacity	Small – Medium	Large	Large	Small	Medium	Small – Large (demo 32Gb)	Medium – Large	Small (demo 32Mb)	Small (demo 16Mb)

- Among new memories: MRAM, ReRAM, and PCRAM,
  MRAM has longer cycling endurance and faster write → SRAM or DRAM like usage

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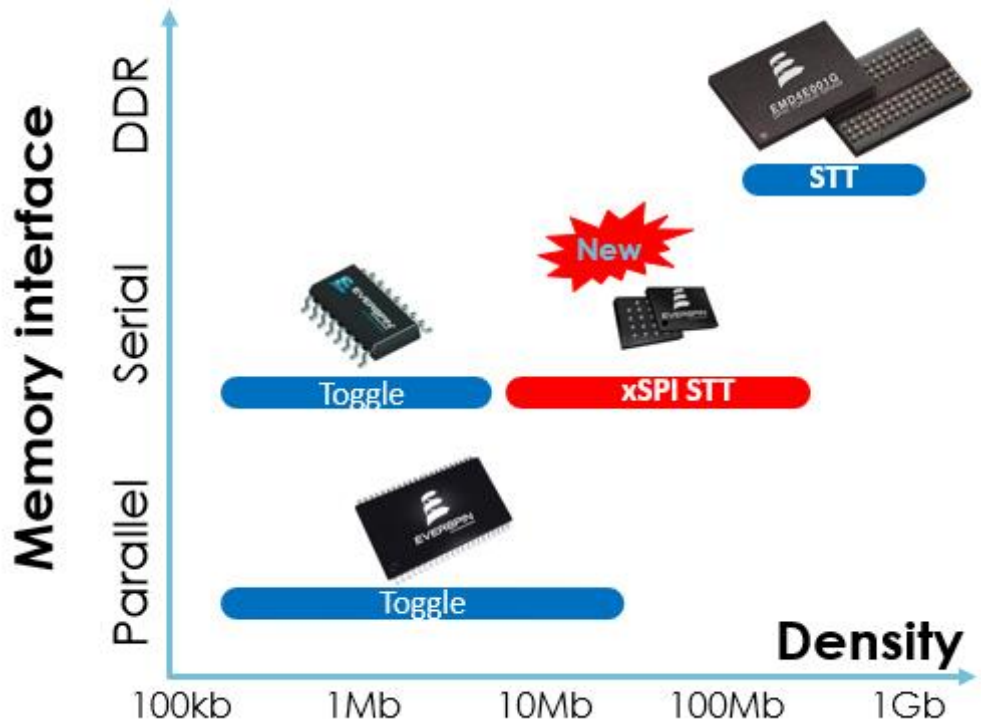
Everspin MRAM Products and Market



Multiple products by optimizing Technology and Design Architecture

Specifications for Newest STT-MRAM

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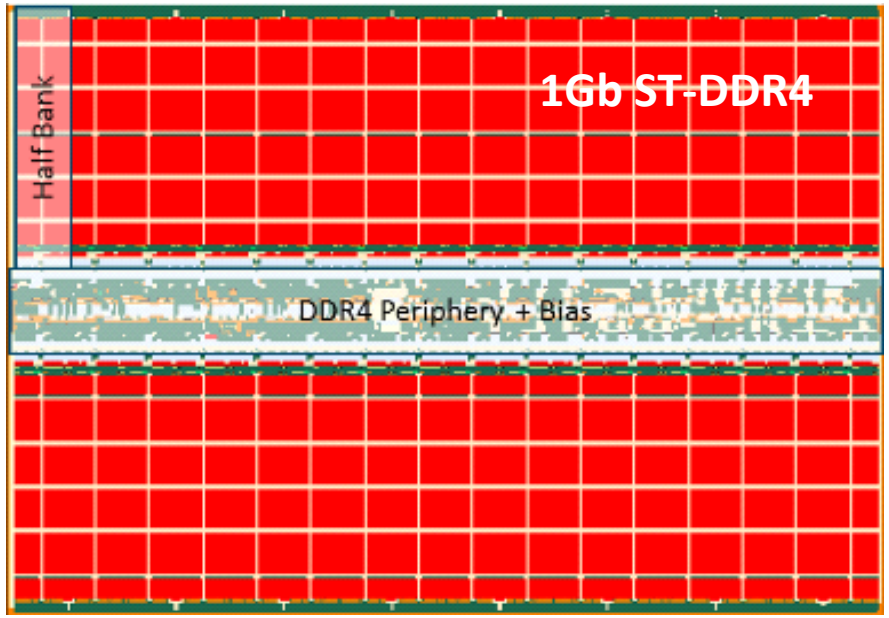
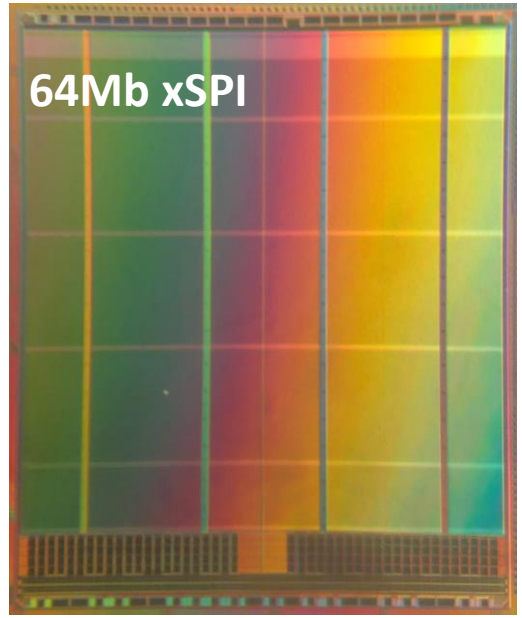
	ST-DDR4	xSPI
Supply voltage	1.2V	1.8V
Density	1Gb	64Mb base, 8-256Mb option
Package	10x13	6x8
Clock frequency	667 MHz	Up to 200 MHz
Number of IOs	16	1,2,4,8
Bandwidth	2.6 GB/s	Up to 400 MB/s
Temperature range	0°C to +85°C	-40°C to +85°C
Data retention	70°C 3mo	85°C 10yr
Endurance	>1e10 cycles	>1e15 cycles
Bit Error rate	<1e-11	<1e-15





Not drawn to scale. Both products on GlobalFoundries 28nm CMOS

New

xSPI STT-MRAM

- **Standard interface and meets reliability for industrial market**
- **Larger density vs current standard; both SRAM and NOR protocol enabled**

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MTJ Fast Write enables Bus Speed Non-Volatile Write

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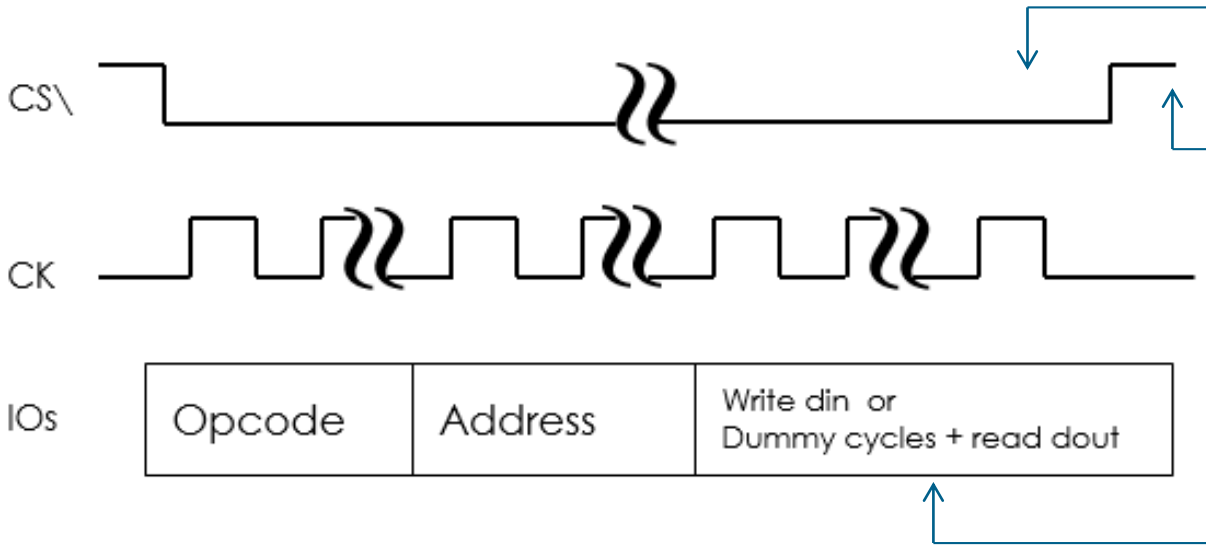
Serial interface signal protocol for read and write commands



IO modes: 1, 2, 4 or 8
STR: Single transfer rate – bits transfer at clock rising edge
DTR: Dual transfer rate – bits transfer at both clock edges

NOR/NAND Flash approach

- Page buffer is written while chip is selected (CS/ low)
- Actual non-volatile write occurs after CS/ high with busy flag for 100s of µs

Everspin xSPI STT-MRAM approach

- Non-volatile write occurs while chip is selected (CS/ low) at data bus speed
- 200MHz clock (CK) in Octal DTR enables 400MB/s write bandwidth

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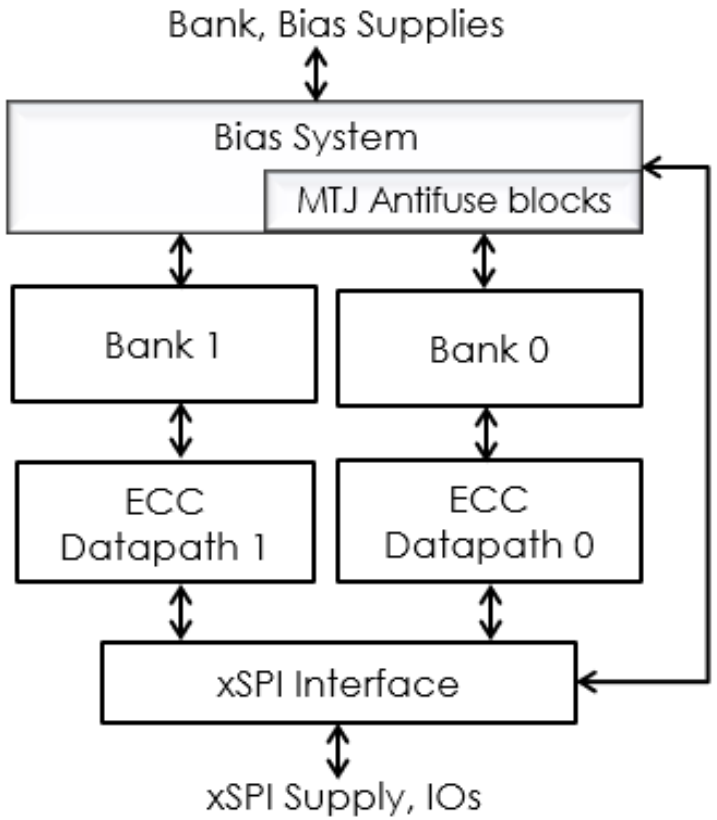
Architecture for Both SRAM and Flash like Interface

64Mb xSPI functional block diagram



- Two bank architecture with independent datapath and timing control
- xSPI Interface block controls bank overlap timing for different IO modes
  - Single, dual, quad, and octal w/ STR or DTR

Protocol Feature	Serial SRAM-like (baseline)	Serial NOR-like (additional)
Program	Byte program with write 0 and 1	+ 2kbit page emulation
Erase	Not needed	Optional Erase commands
Read / Write speed	Symmetric with clocked data rate	+ busy flag for only 10s of ns

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MTJ Technology Improvements

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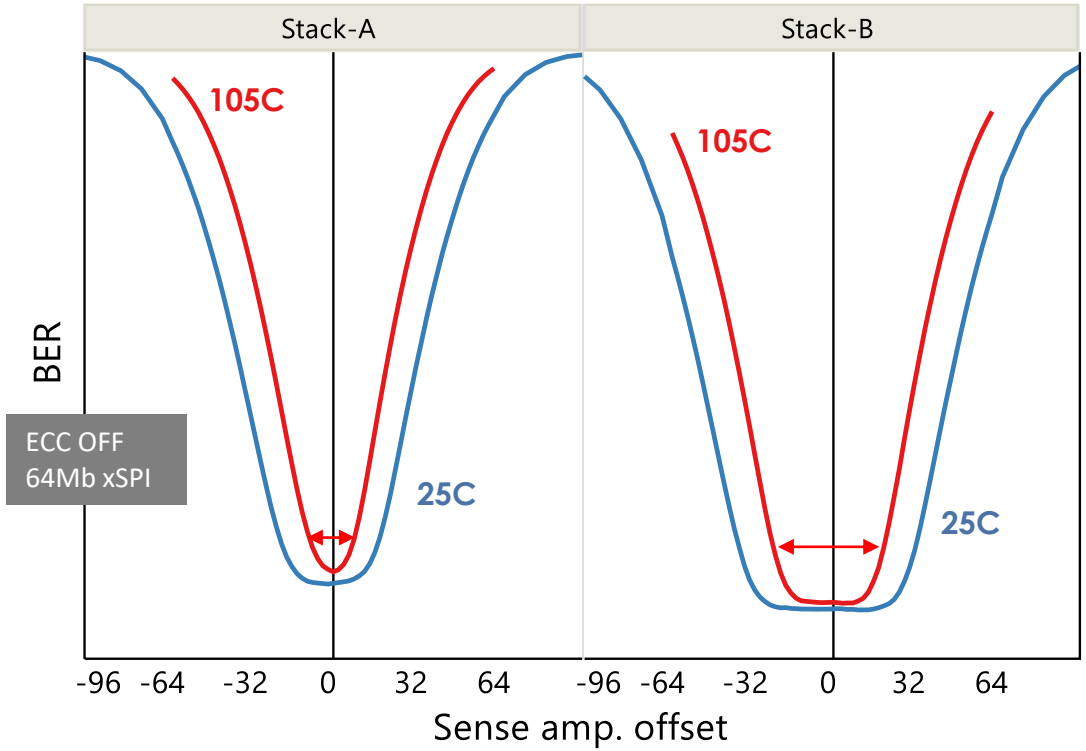
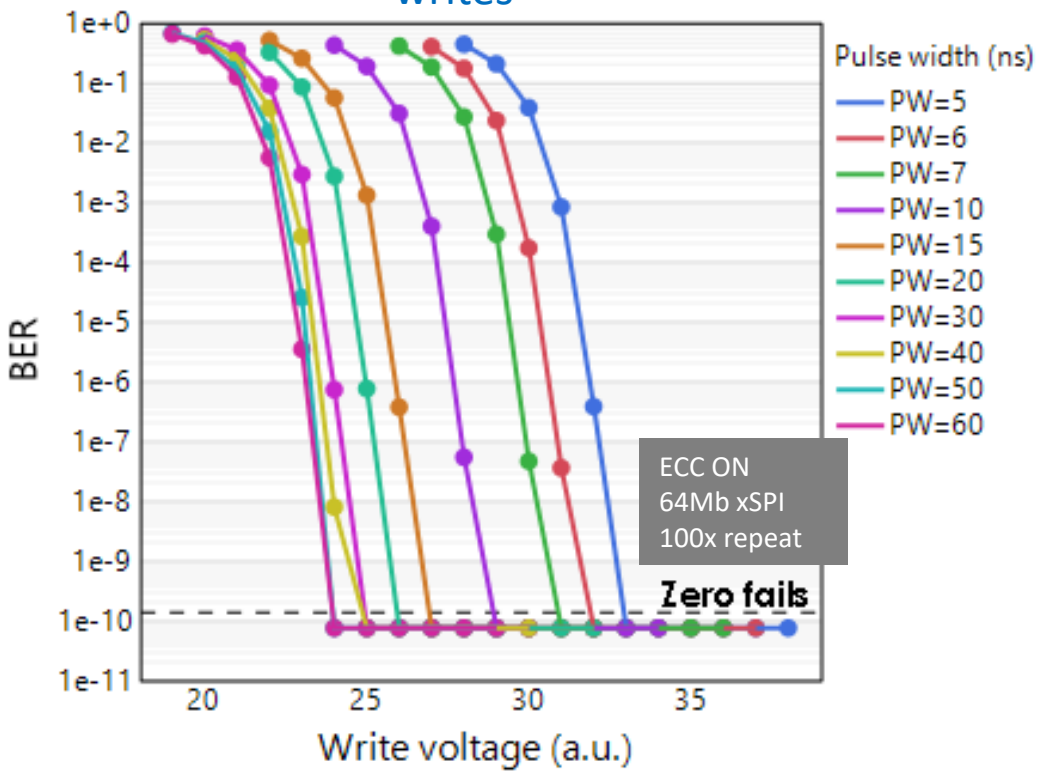
32% higher MR with new Stack



- Faster read timing
- Low read BER at hot temperature

Critical switching Vc is unaffected to enable fast writes



- Good switching distribution *down to 5ns* write pulse
- Zero fails line show BER floor in 100x repeat full 64Mb test

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Write Time and Energy Advantage

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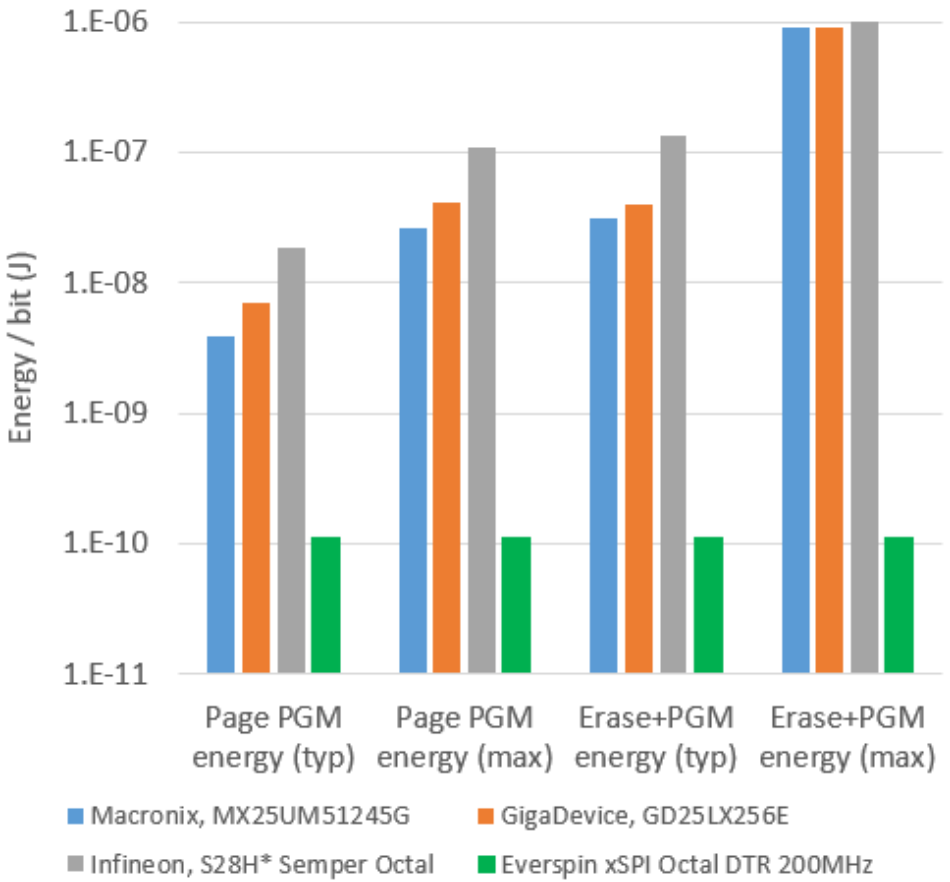
xSPI STT-MRAM is fast and write energy efficient

- Up to 20ns write pulse with concurrent write 0, 1
- No write-verify
- No Erase needed

Write time comparison with selected NOR Octal SPI products

	Macronix MX25* [7]	GigaDevice GD25LX* [8]	Infineon S28H*[9]	xSPI STT-MRAM
Page buffer size (bytes)	256	256	256	256
PGM time typ / max (us)	150 / 750	400 / 1200	430 / 2175	0.64 / 0.64
Erase sector size (bytes)	4k	4k	4k	Erase not necessary
Erase time typ / max (ms)	25 / 400	30 / 400	42 / 335	

Up to 4 orders less write energy/bit in xSPI STT-MRAM



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Application Use Cases Example

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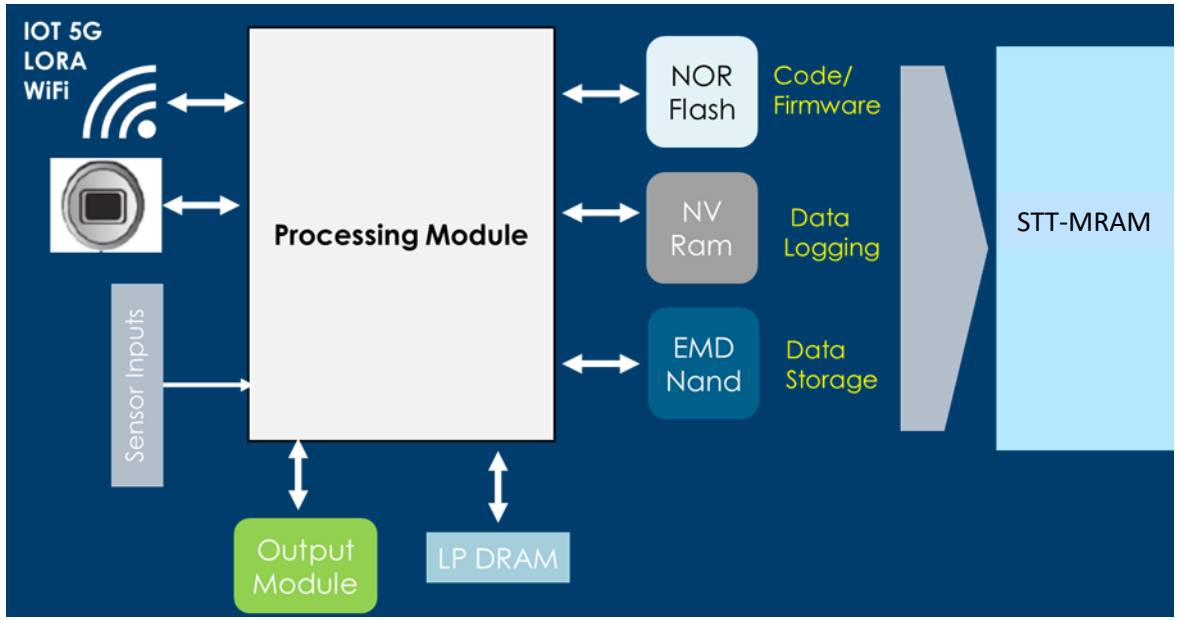
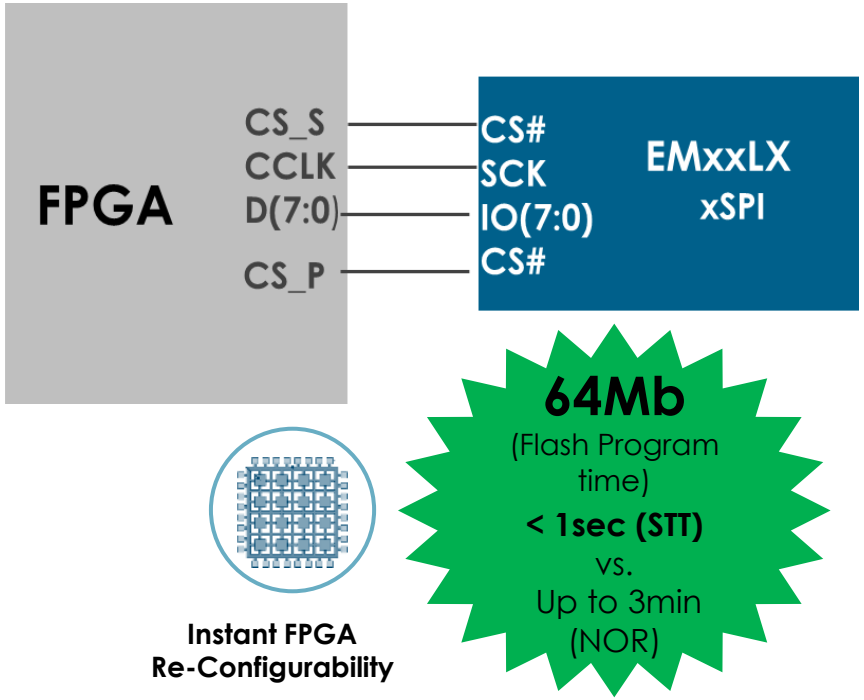
Unified NV Memory supporting high speed read & writes



Fast OTA FPGA configurations



The xSPI product family, with 400MB/s write performance, can easily support very fast downloads, saving power and simplifying the software management.

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Conclusion

- Everspin continues to innovate and expand successful commercialization of MRAM with this introduction of xSPI STT-MRAM product

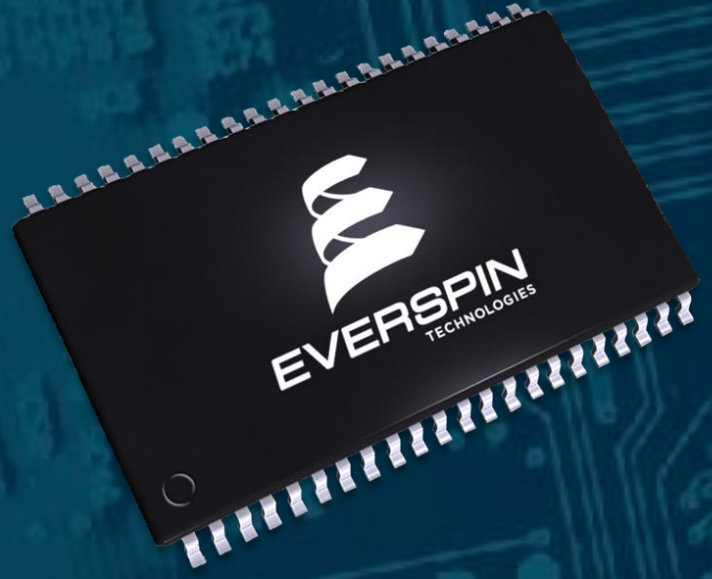
- JEDEC compliant with both Serial SRAM and NOR Flash-like protocol in xSPI STT-MRAM
  - Up to 400MB/s symmetric read and write bandwidth
  - Industry standard 24-BGA and 8-DFN packages
  - Ease of adoption in industrial, embedded, and FPGA applications

- STT-MRAM technology and design advances enable:
  - No erase commands needed
  - Fast write without write-verify
  - Up to 4 orders of write energy advantage over Serial NOR products

Acknowledgements

- Everspin Technologies, Inc.:
  - Design, Technology R&D, Product, and Marketing groups

- Partners for STT-MRAM Manufacturing & Development



Thank you.

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