



Flash Memory Summit

# Solving Memory Bottlenecks in Compute Systems with CXL<sup>TM</sup>- Based Memory Controllers

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# Agenda

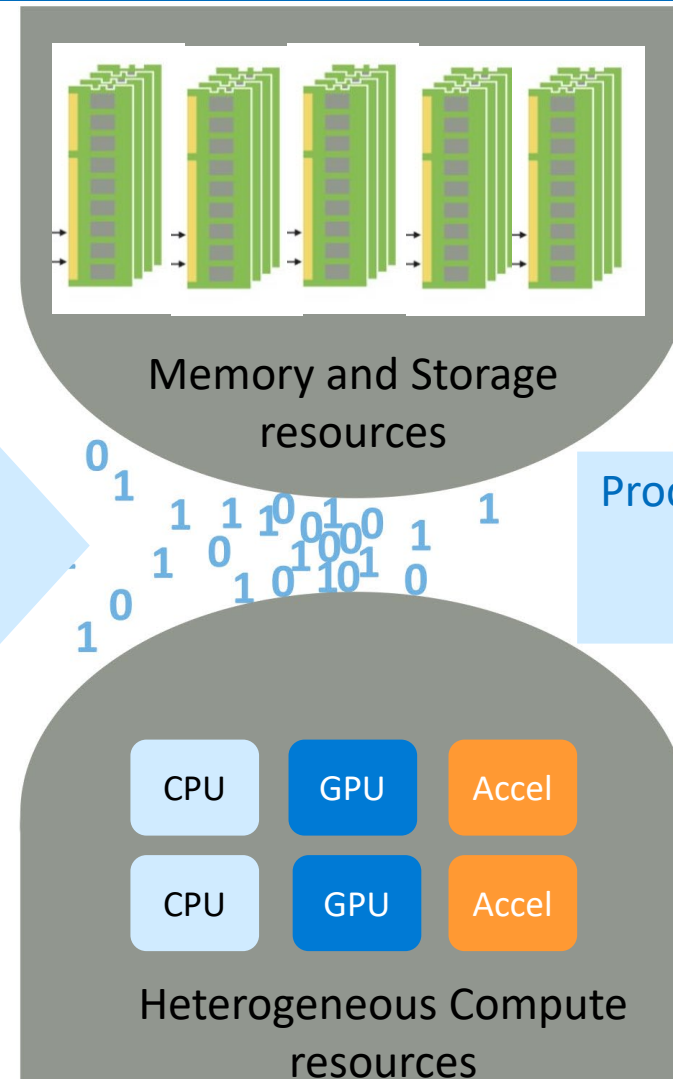
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- What problem is being solved by CXL™ and how
- Resource management
- Sharing and efficient data exchange
- First instantiations of CXL™
- Resilience, security and performance

# What Problem is Being Solved by CXL™



Global data generation



Process and extract  
meaningful  
information

Time critical data

- Stock market decisions

Analysis extraction

- Medical modelling

- Self driving machines

Filtered and sorting

- Data analytics

- Cat photos

Task Prioritization

Augmented reality

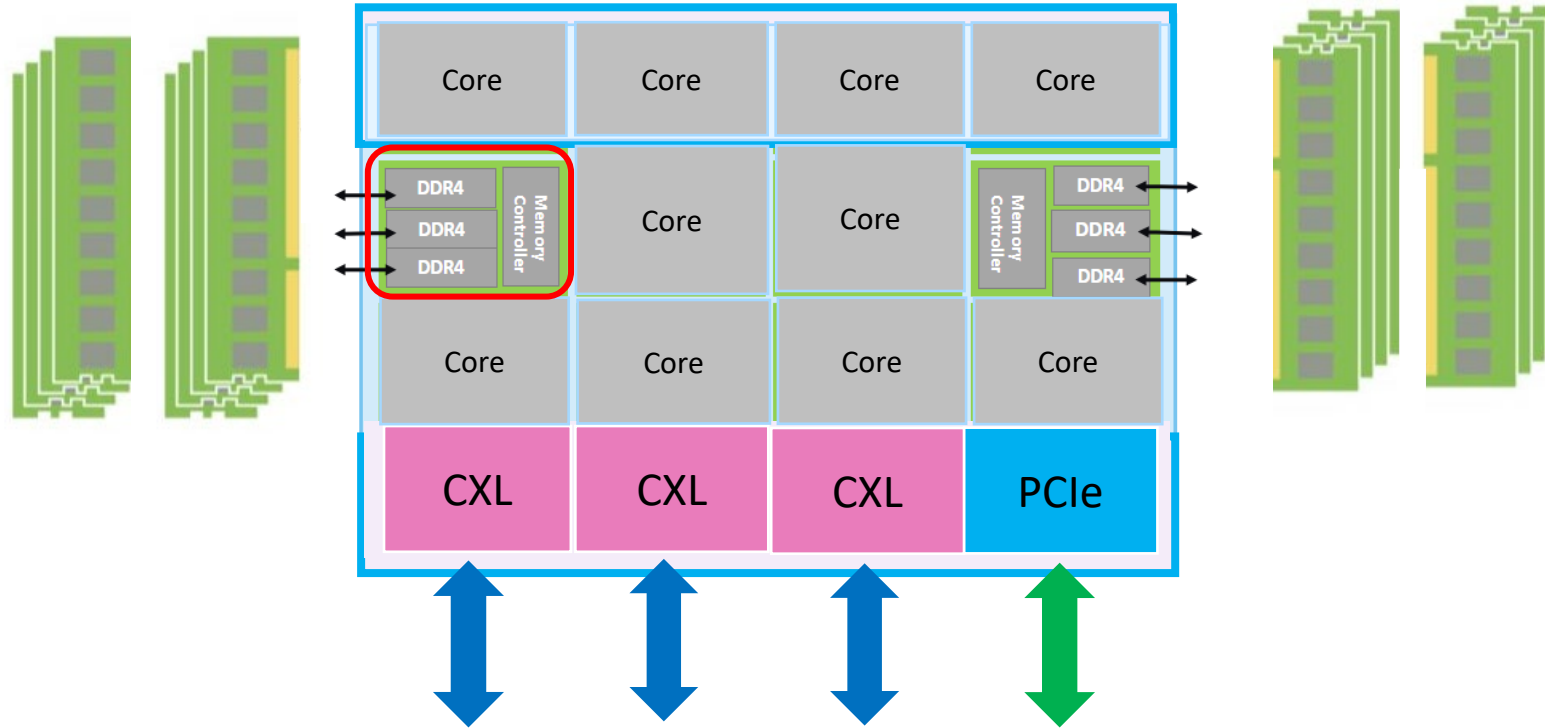
Advertising

Catastrophe avoidance

Tomorrows weather forecast

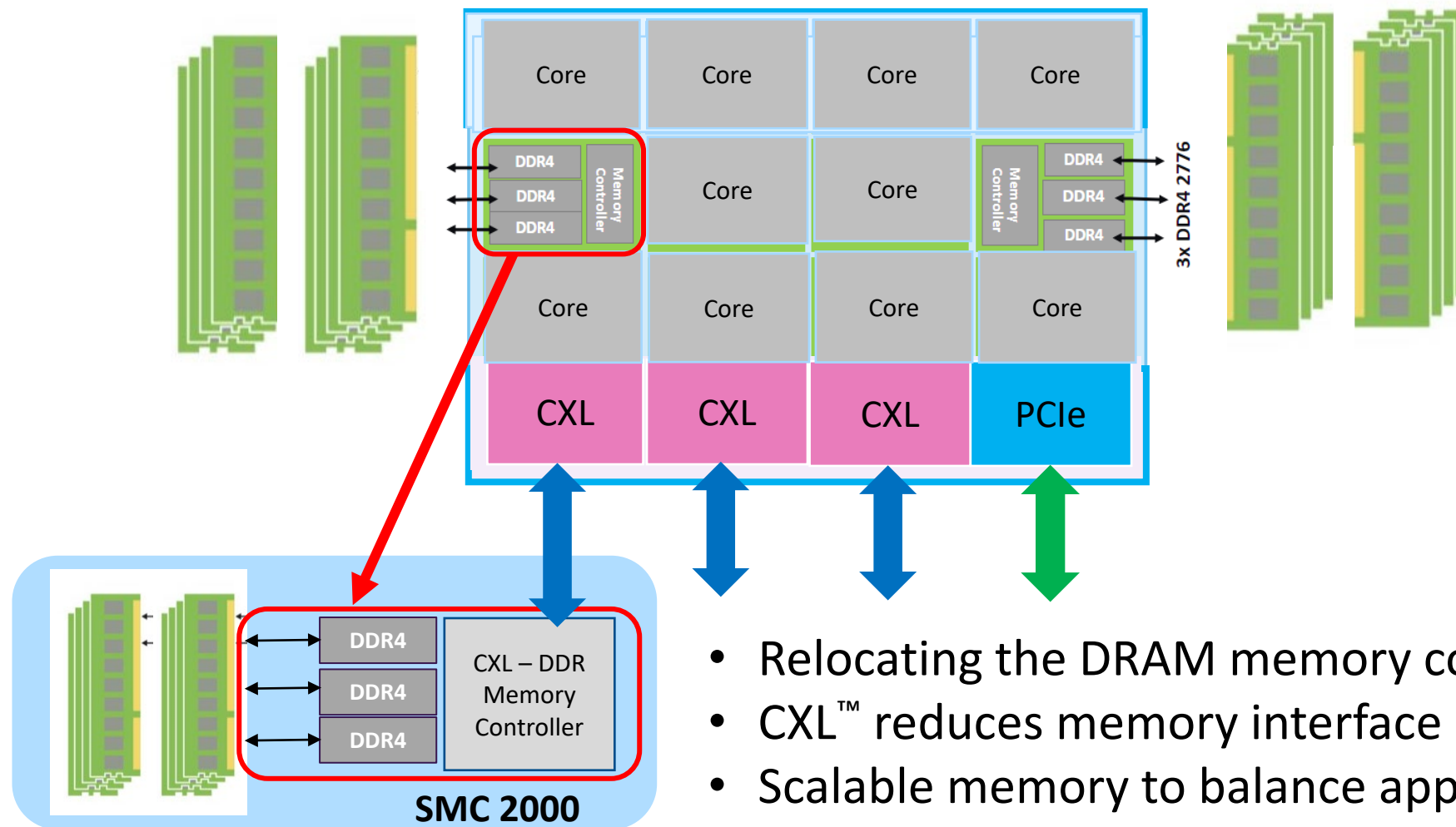
Meaningful data, Time  
critical results

# Resource Management



- CXL ports enables expansion of memory access by the processor cores
- CXL support 3 protocols:
  - CXL.mem
  - CXL.cache and
  - CXL.io

# Resource Management

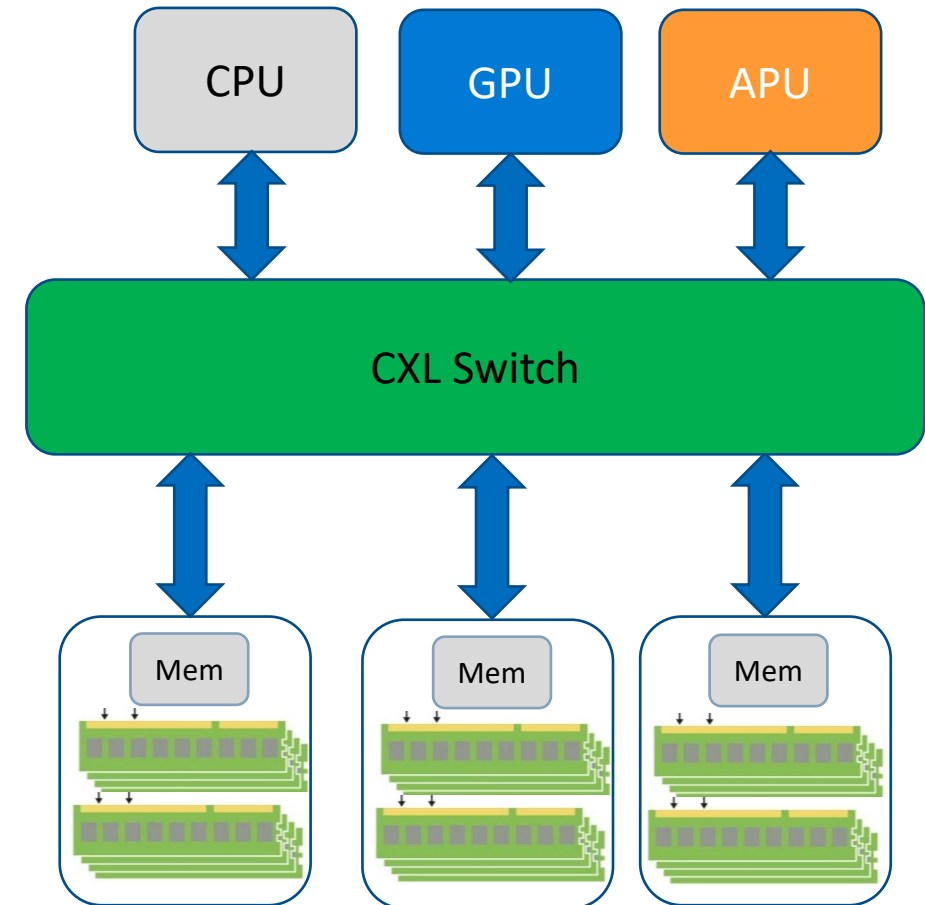


Disaggregated CXL – DDR memory controller

- Relocating the DRAM memory controller outside the core
- CXL™ reduces memory interface pin-count
- Scalable memory to balance application needs
- Re-balance ratio of processor cores to memory

# Sharing and Efficient Data Exchange

- CXL™ 2.0 adds support for switching topologies
- Switching enables resources to be allocated, managed and reconfigured in response to application needs
- Provisioning is much more flexible to avoid underutilized or stranded resources



# First Instantiations of CXL™ – Memory Controllers



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## EDSFF formats

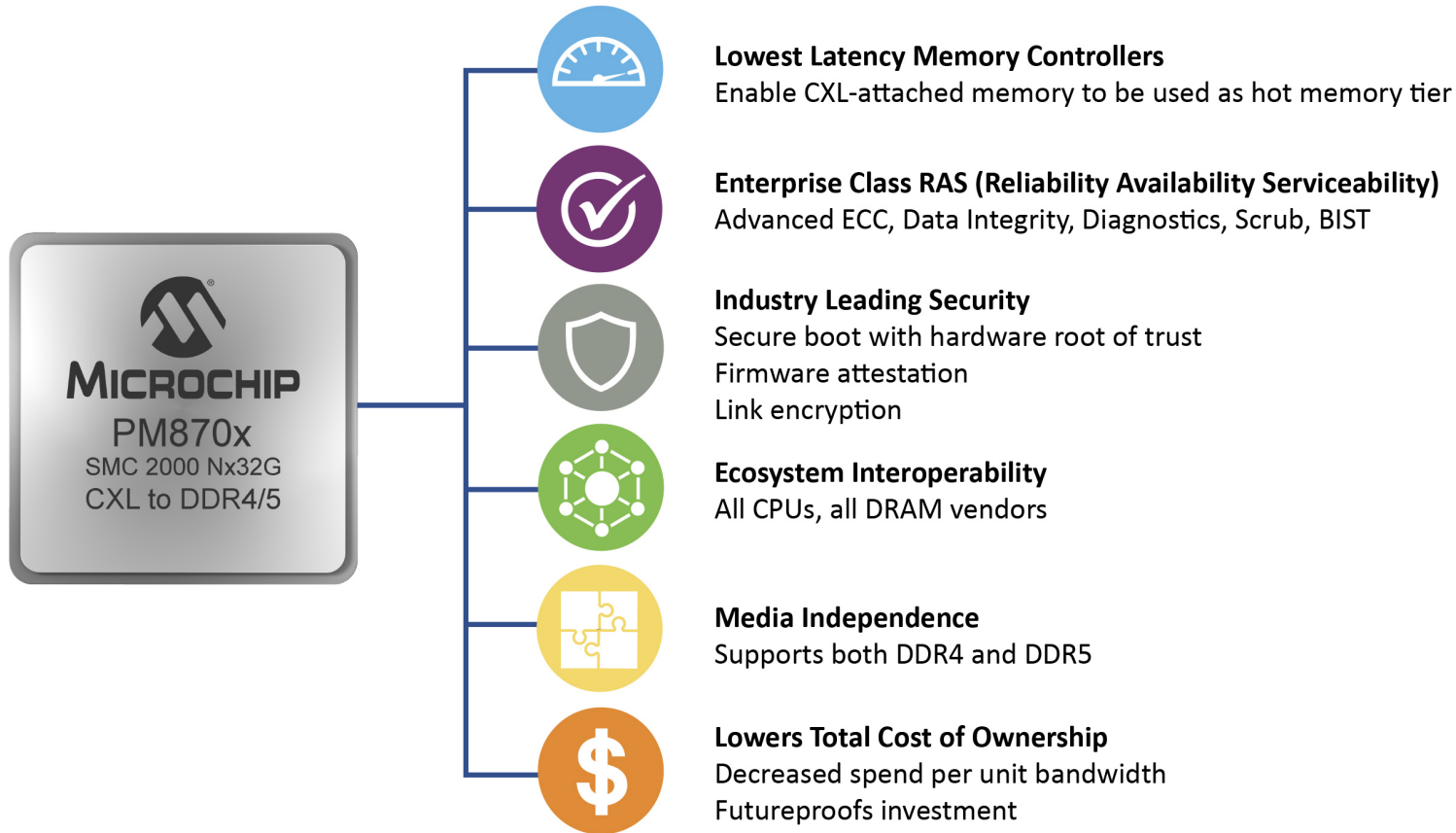


## Add-in card formats





# Resilience, Security and Performance







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