2022 Flash Memory Summit

Tech Insights

OMEM-201-2: NDRAM, Part 2

# Recent DRAM Technology Overview

## Trends & Challenges


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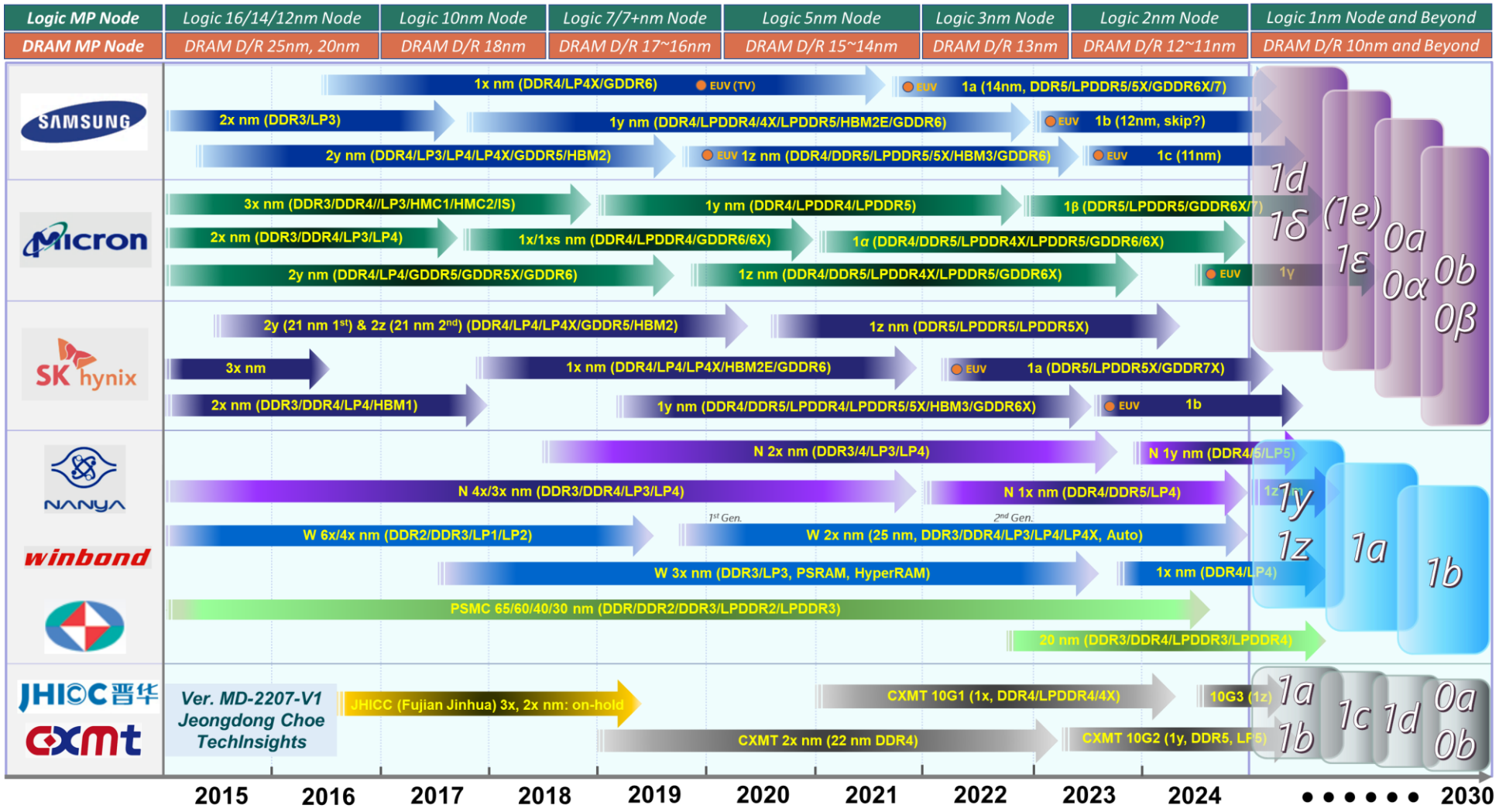
# DRAM Technology Roadmap (Expected)





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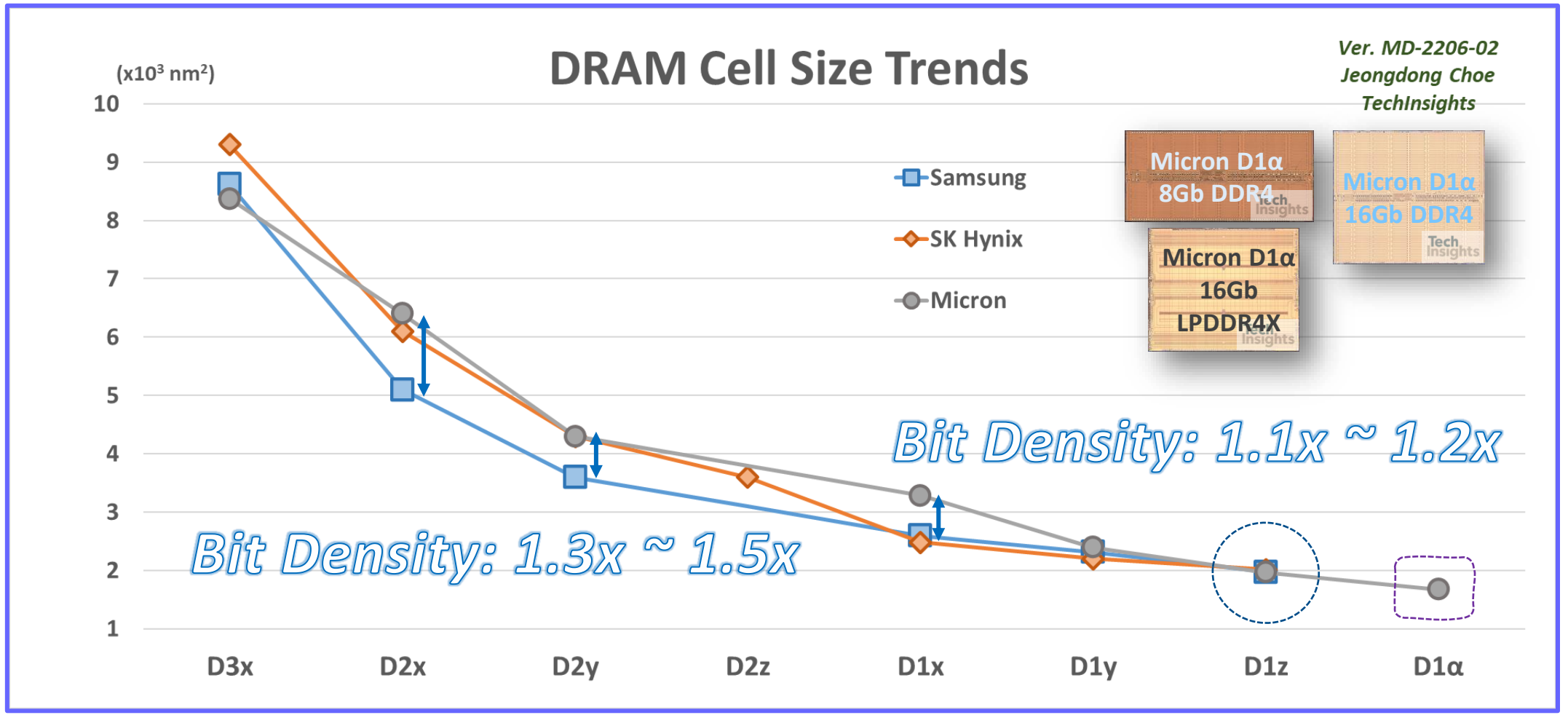
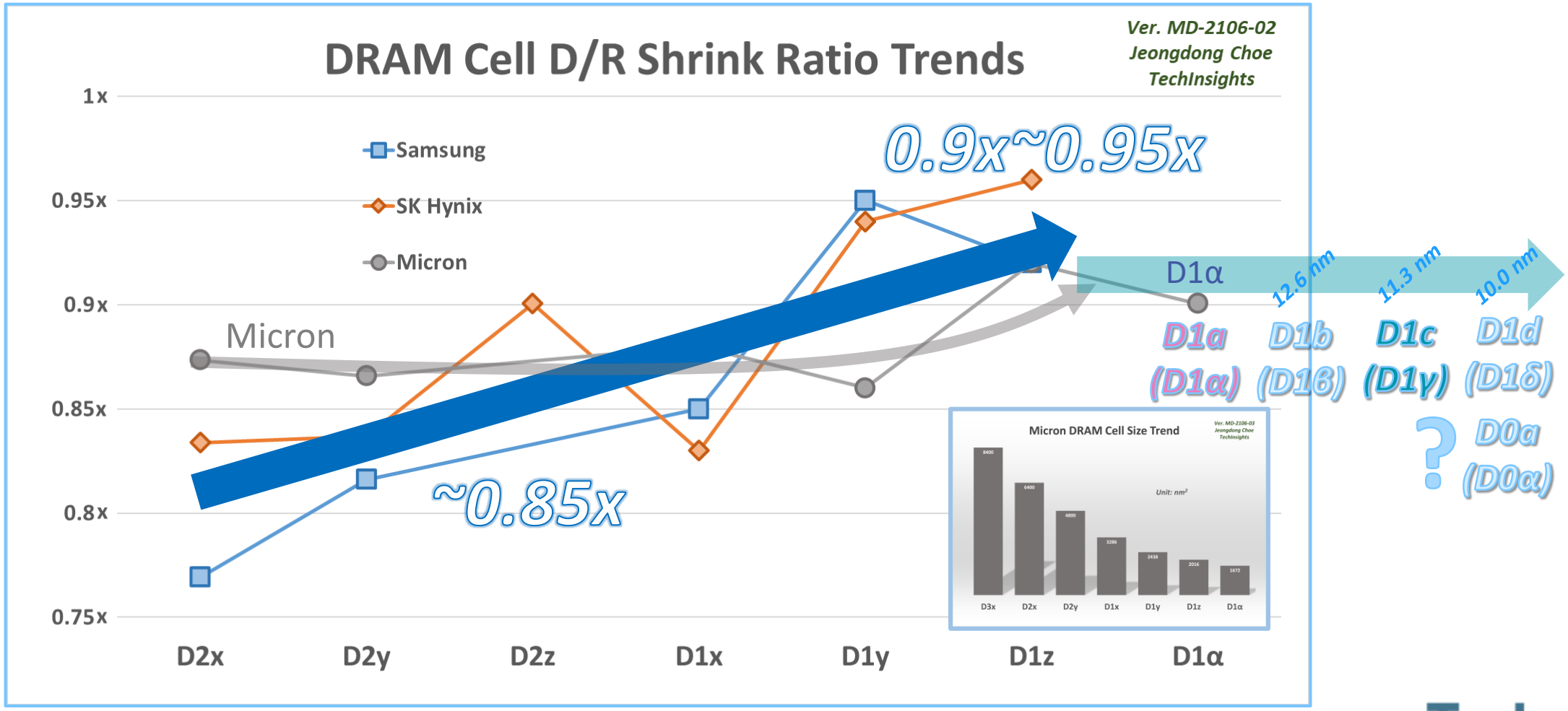
# DRAM Cell Size Trend





# DRAM Cell D/R Shrink Ratio Trend

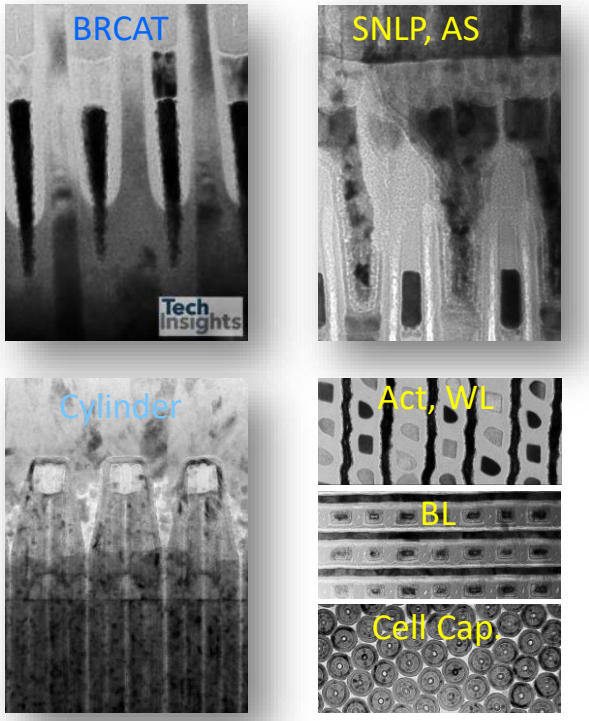


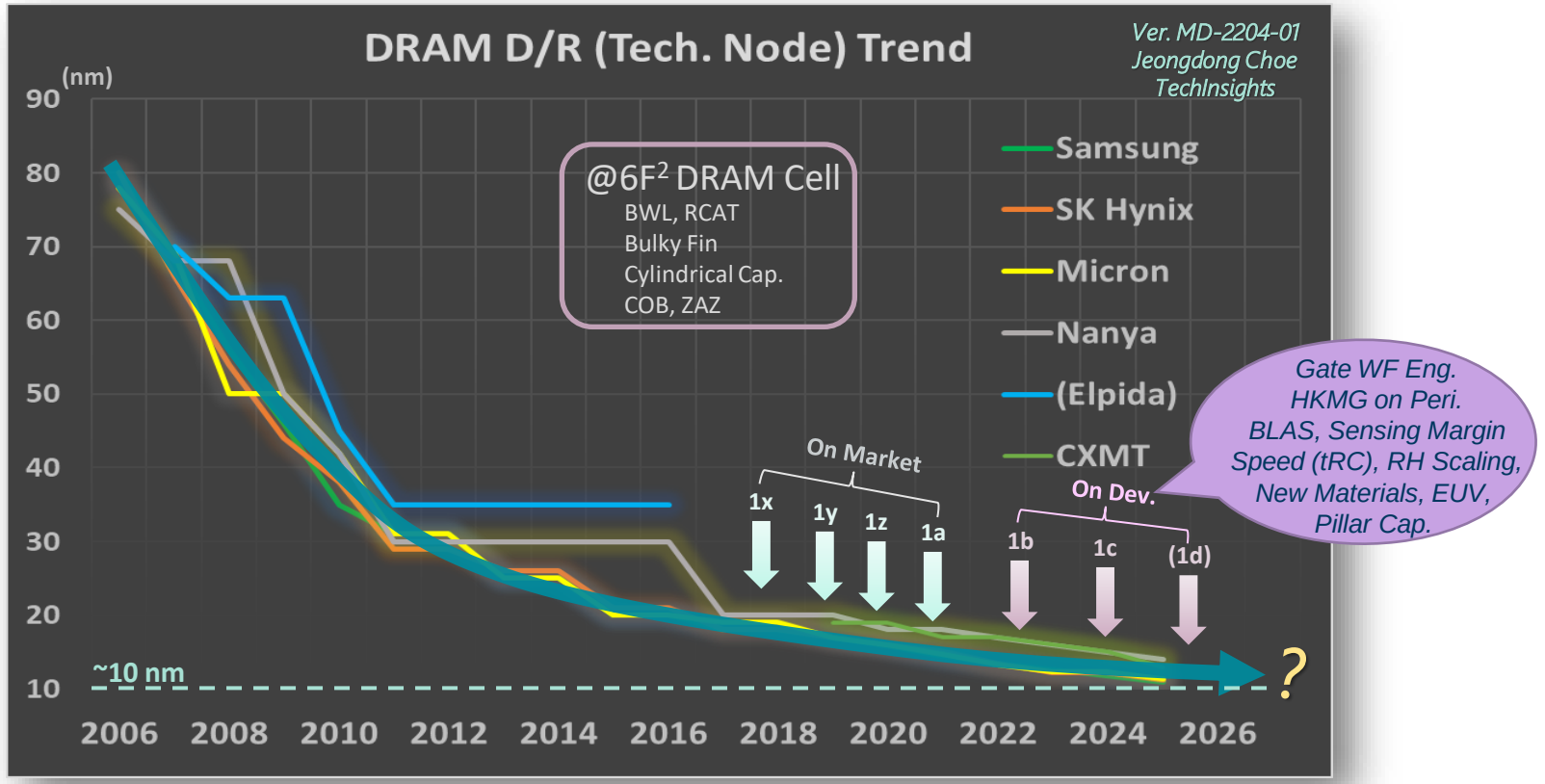

 

# DRAM Scaling



## 6F² DRAM Process




*2027 ~ 2028*
*3D? 4F²?*

# Cell & Periphery Scaling: Examples



| | 2019 | 2020 | 2021~2022 |
|---|---|---|---|
| **Items** | **Micron D1y 16 Gb DDR4** | **Micron D1z 16 Gb DDR4** | **Micron D1α 8 Gb DDR4** |
| Die Size | 81.30 $mm^2$ (8.54 mm x 9.52 mm) | 64.75 $mm^2$ (8.27 mm x 7.83 mm) | 25.41 $mm^2$ (7.28 mm x 3.49 mm) |
| Bit Density | 0.197 $Gb/mm^2$ | 0.247 $Gb/mm^2$ | 0.315 $Gb/mm^2$ |
| Cell size | 0.00239 $\mu m^2$ | 0.00204 $\mu m^2$ | 0.00163 $\mu m^2$ |
| WL (Cell Gate) Materials | Poly-Si/W/TiN | Poly-Si/TiN | Poly-Si/TiN |
| Active Island Pattern Length | 120 nm | 110 nm | 98 nm |
| Pitch (Act/WL/BL) | 32 nm / 46 nm / 52 nm | 30 nm / 41 nm / 48 nm | 28 nm / 37 nm / 44 nm |
| BL Spacer | ONON | ON | ON |
| Peripheral Gate Pitch | 200 nm | 160 nm | 160 nm |
| Cell SNLP Shape | Mushroom | Square | Square |
| SNC Etch | Conventional | Likely, SAC | Likely, SAC |
| Top Plate Materials | W 100 nm / Si 90 nm / SiGe 40 nm on TiN | W 57 nm / Si 43 nm / SiGe 88 nm on TiN | W 110 nm / SiGe 75 nm on TiN |
| Cap. Dielectrics, Height | ZrNbO on both side, 1.27 µm | ZrNbO on outer surface, 1.00 µm | Quasi-Cylinder, ZrNbO on outer surface, 0.89 µm |
| Cap. MESH Pattern | Triangle | Rhombus | Triangular |
| M2 & M3 Top Layer | Cu | CuMn on Cu | CuMn on Cu |
| | | TT/ZrNbO/ZrAlO/ZrHfO/ZrAlO/ZrHfO/BT | TT/HfO/ZrO/ZrAlO/ZrNbO/BT (BE-sided ZrNbO) |

# DRAM Capacitor MESH Patterning



| Player | D1x | D1y | D1z | D1a (D1α) |
|---|---|---|---|---|
| SAMSUNG | Elongated | | Square | |
| SK hynix | Rectangular | Quasi-Pillar Triangular (1-sided Cap.) | | Triangular |
| Micron | | | Rhombus | |

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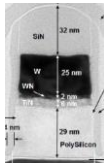
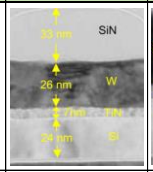
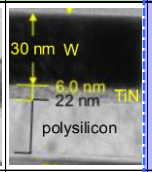
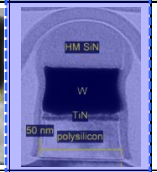
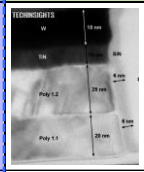
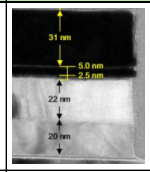
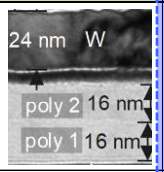
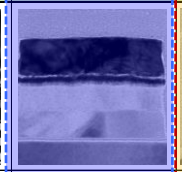
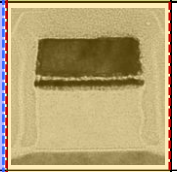
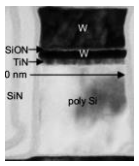
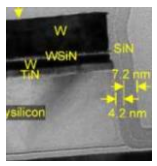
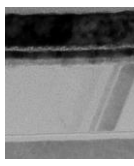
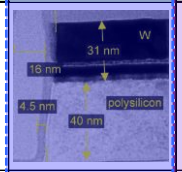
# DRAM Peripheral Transistor



| Manufacturer | Samsung | | | | Micron | | | | | SK Hynix | | | | CXMT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Tech Node | D2y | D1x | D1y | D1z | D2y | D1x | D1y | D1z | D1α | D2z | D1x | D1y | D1z | D2x (22nm) |
| Gate Image (x-section TEM) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Gate Layer 1 | Poly-Si | Poly-Si | Poly-Si | Poly-Si | Poly-Si 1 | Poly-Si 1 | Poly-Si 1 | Poly-Si 1 | Poly-Si 1 | Poly-Si | Poly-Si | Poly-Si | Poly-Si | Poly-Si |
| Gate Layer 2 | TiN | TiN | TiN | TiN | Poly-Si 2 | Poly-Si 2 | Poly-Si 2 | Poly-Si 2 | Poly-Si 2 | TiN | TiN | TiN | TiN | TiN |
| Gate Layer 3 | WN | W | W | W | TiN | TiN | TiN | TiN | TiN | W | W | W | W | W |
| Gate Layer 4 | W | | | | W | WN | WN | W | W | SiON | WSiN | WSiN | WSiN | |
| Gate Layer 5 | | | | | | W | WSiN | WSiN | WSiN | W | W | W | W | |
| Gate Layer 6 | | | | | | | W | W | W | | | | | |
| Gate Height | 62 nm | 57 nm | 58 nm | 55 nm | 73 nm | 80.5 nm | 63 nm | 56 nm | 50 nm | 98 nm | 71 nm | 71 nm | 71 nm | 78 nm |
| Gox Structure | SiO/SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO | SiON/SiO |
| LV Gox Thickness | 2.3 nm | 3.0 nm | 2.5 nm | 1.9 nm | 2.7 nm | 2.3 nm | 2.0 nm | 2.0 nm | 2.0 nm | 2.2 nm | 1.8 nm | 1.8 nm | 1.8 nm | 2.8 nm |
| HV Gox Thickness | 6.0 nm | 5.8 nm | 5.0 nm | 4.6 nm | 6.4 nm | 5.6 nm | 5.0 nm | 5.2 nm | 5.3 nm | 5.2 nm | 5.4 nm | 4.2 nm | 4.2 nm | 5.2 nm |
| Gate Spacer | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO SW | SiN liner / SiO Buffer / SiN | SiN liner / SiO Buffer / SiN | SiN liner / SiO Buffer / SiN | SiN liner / SiO SW | SiN double liners / SiO SW | SiN double liners / SiO SW | SiN/SiO/SiN | SiN liner / SiO SW |
| CONT Materials | CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi | W/TiN/CoSi |
| Report ID | 0315-39040-O-5DM-100 | AME-1701-805 | AME-1902-802 | AME-2102-801 | 0716-43012-O-5DM-100 | AME-1804-803 | AME-1905-801 | AME-2007-801 | AME-2106-801 | AME-1703-801 | AME-1811-801 | AME-1911-801 | AME-2104-801 | AME-2006-802 |

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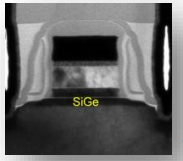
HKMG GDDR6 | HKMG DDR5 | HKMG GDDR6

➢ *HKMG Peripheral Gates beyond D1b?*

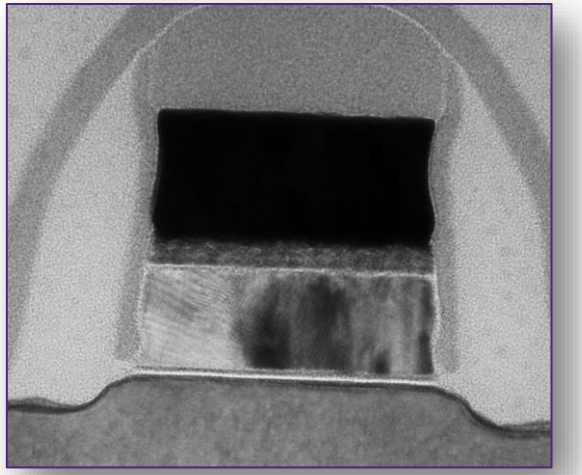



*Samsung DDR5 HKMG*

# HKMG on DRAM

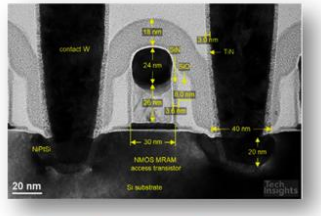


## ■ Conventional TR (DDR4, D1y)



W/TiN/Poly-Si/SiON/SiO

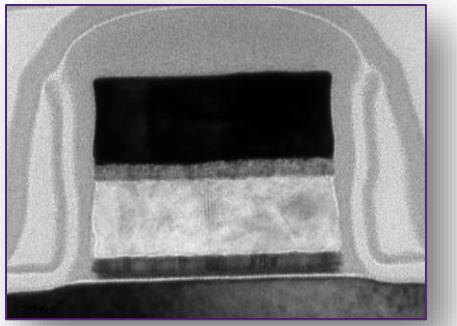
**Everspin 28nm** *Ref.*




- Gate-First, HKMG
- NiPtSi/Poly-Si/TiAl/TiN Gate
- La-doped HfON/SiO GOx
- Lg=30nm

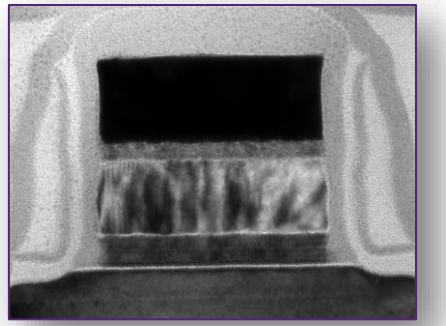
*Ref. PMOS: HfON/SiO/SiGe*

## ■ HKMG TR (DDR5, D1y, Gate-First)



**LV NMOS**

- La-doped HfSiON
- Thinner TiN WF
- W/TiN/poly-Si



**LV PMOS**

- Al-doped HfSiON
- La-doped TiN1/TiN2 Interface
- Thicker TiN WF
- SiGe Epi-Channel
- W/TiN/poly-Si

| Manufacturer/Device | Samsung D1y DDR5 | | Everspin/GF 28nm STT-MRAM | |
|---|---|---|---|---|
| HKMG Transistors | LVN | LVP | LVN | LVP |
| Layers, bulk | W/TiN/poly-Si | W/TiN/poly-Si | NiPtSi/poly-Si | NiPtSi/poly-Si |
| WF Layer | TiN2 | TiN2/TiN1 | TiAl/TiN | TiAl/TiN |
| Gox. | HfSiON/SiO | HfSiON/SiO | HfON/SiO | HfON/SiO |
| Channel | Si | SiGe/Si-Epi | Si | SiGe/Si-Epi |
| WF/Gox. Interface | La-doped (Likely $La_2O_3$) | TiAl | La-doped (Likely $La_2O_3$) | Nothing |

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# Industry Needs: More DRAM



## ❑ Higher Density (Chip/PKG), Higher Bandwidth, Higher Speed, Low Power (Energy)

- Higher Density (Chip)
  - ✓ 2D Device Scaling
  - ✓ $4F^2$ Cell Design
  - ✓ 3D DRAM, GAA
  - ✓ 3-MESH, 4-MESH
  - ✓ EUV, high NA EUV
  - ✓ Hardmask Engineering
  - ✓ ALD, ALE, Defect Control
  - ✓ Capacitorless (2T, 1T)
  - ✓ IGZO-based Cell, CuA
- Higher Density & Bandwidth (PKG)
  - ✓ HBM-TSV (HBM3, HBM4, …)
  - ✓ DRAM-TSV
  - ✓ MCP
  - ✓ Chiplet (Intel, TSMC, AMD, …)
  - ✓ SoIC
  - ✓ H-Bonding, FO-SiP
  - ✓ Thermal Engineering, Cryo-DRAM
- Higher Speed, Low Power
  - ✓ PIM, FIM-DRAM*
  - ✓ HBM-PIM*
  - ✓ GDDR6-AiM*
  - ✓ LPDDR6, 7
  - ✓ DDR6, 7

*Data-intensive high performance computing applications*

- *FIM: Function - in - Memory*
- *PIM: Processing - in - Memory*
- *AiM: Accelerator in Memory*

 