Flash Memory Summit

YOLE SystemPlus

Future of Wafer-to-Wafer Bonding to overcome NVM Density Limitations

Presented By: Belinda L Dube

35 YEARS OF NAND FLASH MEMORY INNOVATION

Biography

Belinda Dube, Technology & Cost Analyst

Belinda Dube serves as a Technology & Cost Analyst at Yole SystemPlus, part of Yole Group.

Belinda's core expertise is memory technology, especially DRAM and 3D NAND flash memory. At the same time, she also investigates IC technologies as well as advanced packaging.

Belinda's mission is to develop reverse engineering & costing reports. She also works on custom projects, where she works closely with the laboratory team to set up significant physical & chemical analyses of innovative memory chips. Based on the results, Belinda identifies and analyzes the overall manufacturing process and all technical choices made by the memory makers.

In addition, a significant portion of her mission is dedicated to a strategic technology watch, where her aim is to identify innovative memory chips and manufacturing processes. Based on her expertise, Belinda updates internal simulation tools and runs custom training sessions and demos with industrials.

She regularly has an opportunity to reveal pertinent results during key onsite presentations and webcasts.

Prior to System Plus Consulting, Belinda had the opportunity to work on several R&D projects dedicated to MEMS technologies and new substrates at INSA (Lyon, France).

Belinda holds a master's degree in Instrumentation & Nanotechnology Engineering from INSA (France).

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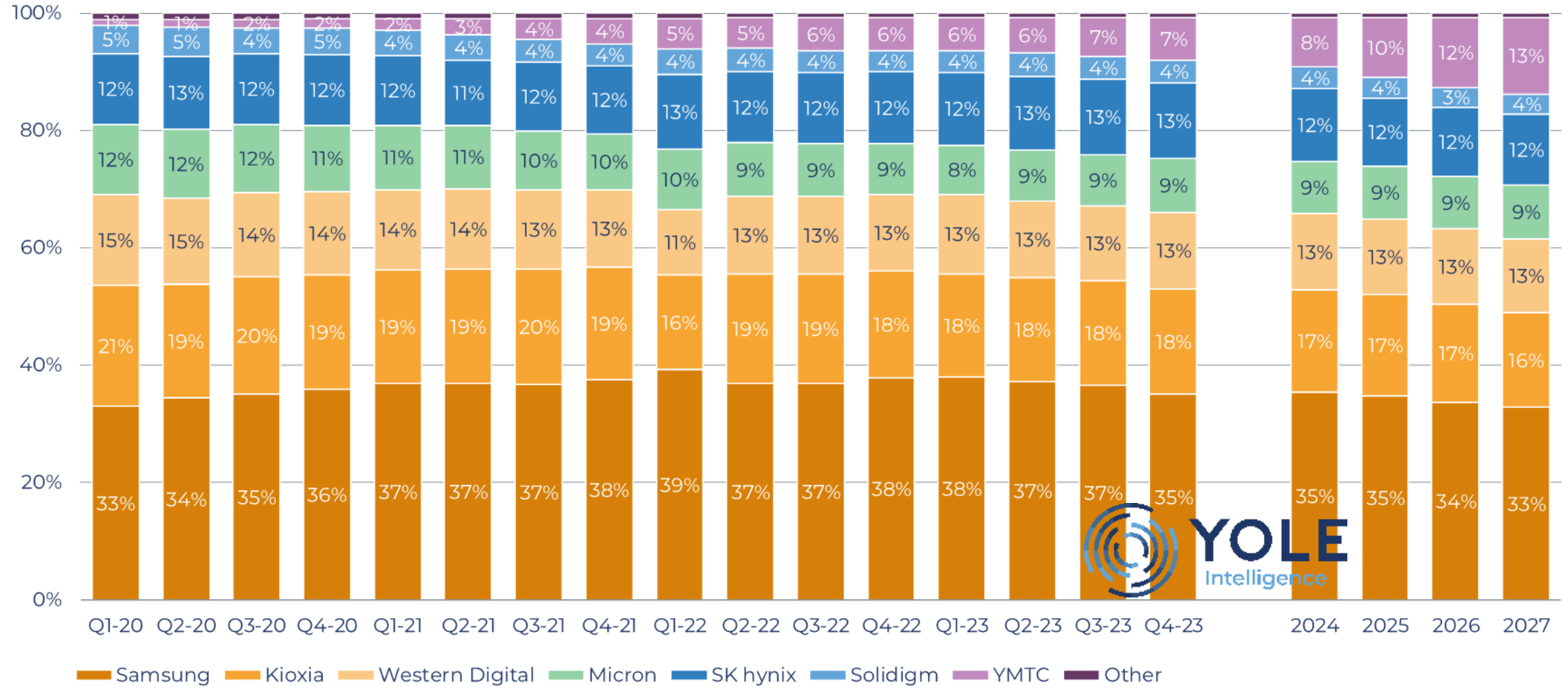
NAND WAFER MARKET SHARE



NAND Market Monitor Q2 2022

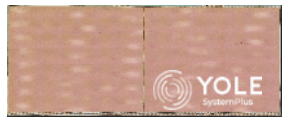
NAND Memory Technology

NAND Density 64 layer vs 128 layer

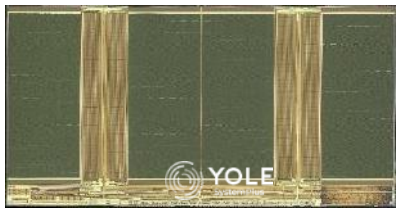
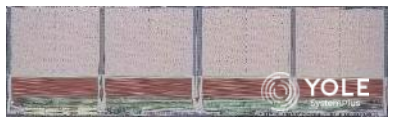
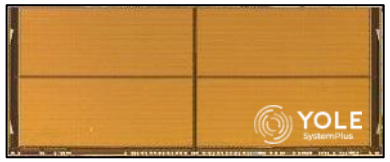
TOSHIBA	SAMSUNG	SK hynix	Micron	YMTC
32GB	32GB	32GB	32GB	32GB
74.7 mm²	*93.6 mm²*	*71.0 mm²*	*57.7 mm²*	*50 mm²*







KIOXIA	SAMSUNG	SK hynix	Micron	YMTC
64GB	32GB	64GB	32GB	64GB
81.9 mm²	*45.3 mm²*	*65.2 mm²*	*49.7 mm²*	*60.16 mm²*

Density Increase

2D

- Planar Manufacturing to 3D Stacking Wordline Layers

Wordlines

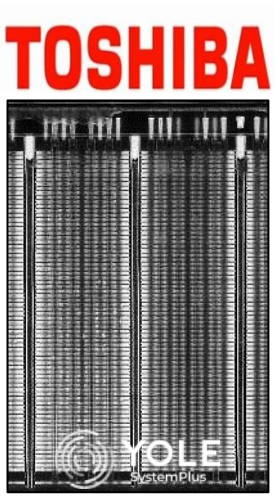
- Wordline Increase
- Continual Vertical increase currently at 176 -layers

CMOS Logic Placement

- CMOS under Array (CuA)
- Periphery under Cell (PuC)
- **Seperate NAND & CMOS Wafer**

Cell Storage

- Increase of number of bits stored per cell
- MLC/TLC/QLC/PLC



Toshiba/SanDisk 64 –layer 3D NAND
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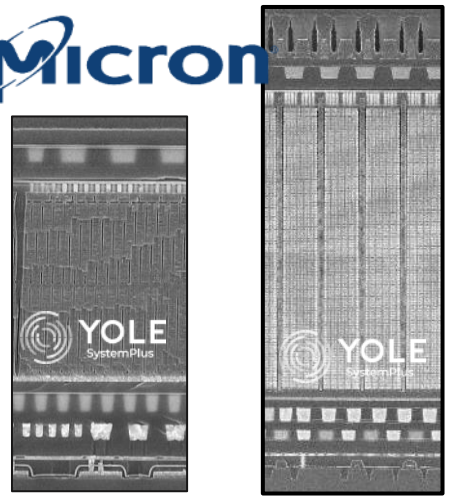

Micron 64–layer
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Micron 176–layer
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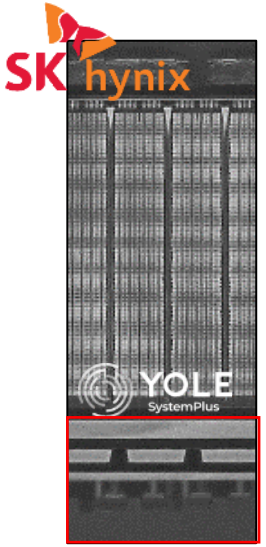

SK hynix 128–layer
Periphery under Cell
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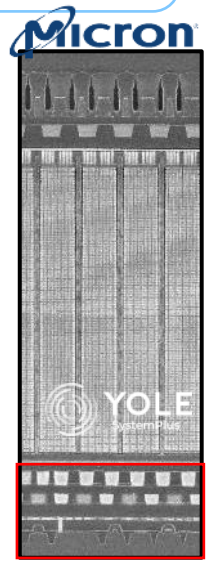

Micron 176–layer
CMOS under Array
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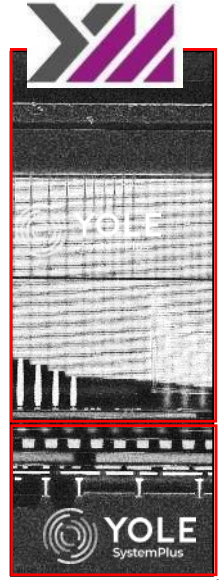

YMTC 128–layer
CMOS on separate wafer
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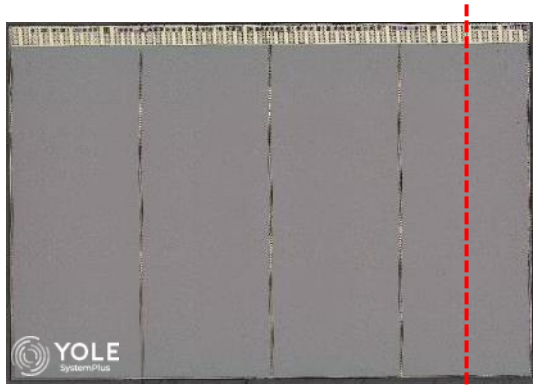
YMTC NAND Wafer

- YMTC's 3D NAND memory uses two silicon wafers, CMOS transistors and NAND array are manufactured on a separate wafers.



YMTC 128–layer 3D NAND Die
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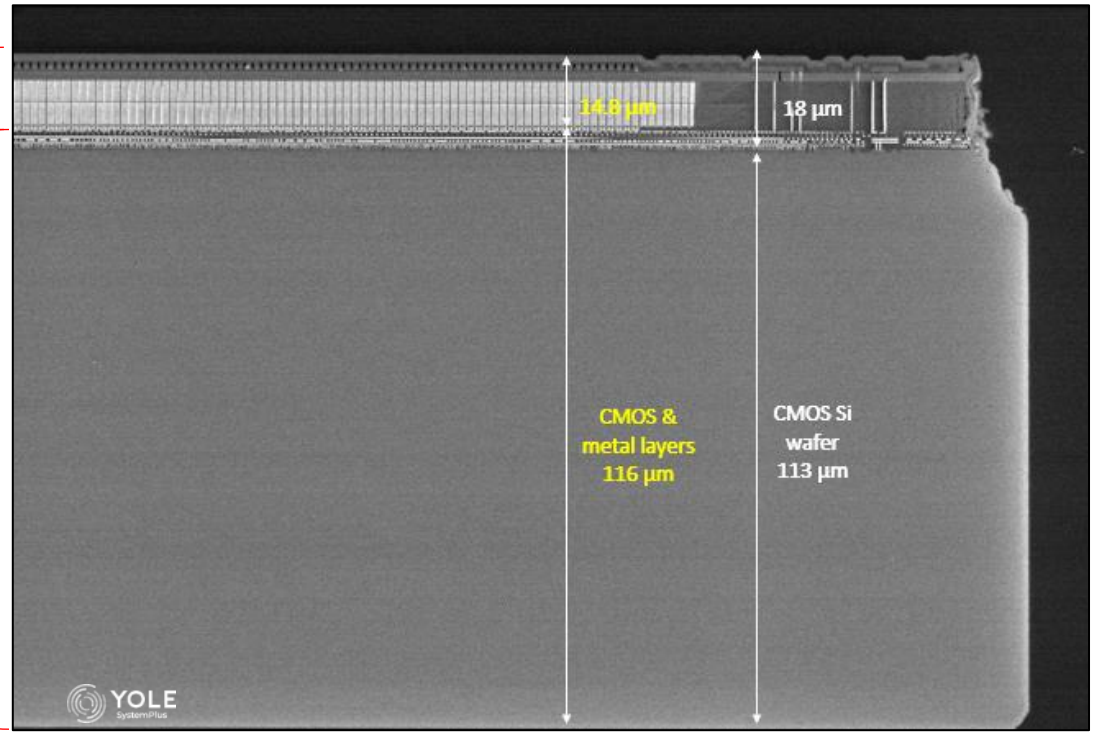
NAND Array wafer& top metal 14.8 µm

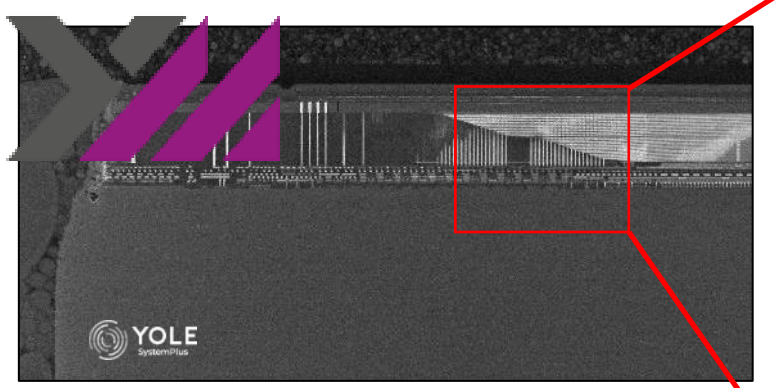
CMOS Periphery wafer



YMTC 128–layer 3D NAND Die
©2022 by System Plus Consulting

Wafer to Wafer Bonding

- Direct Bond Interconnect(DBI) technology uses Cu - Cu hybrid direct bonding technique.
- The last copper metal layer are used as the bonding on CMOS wafer to the NAND array wafer.
- Metal pads on CMOS wafer and NAND wafer are aligned.



YMTC 128–layer 3D NAND Cross Section
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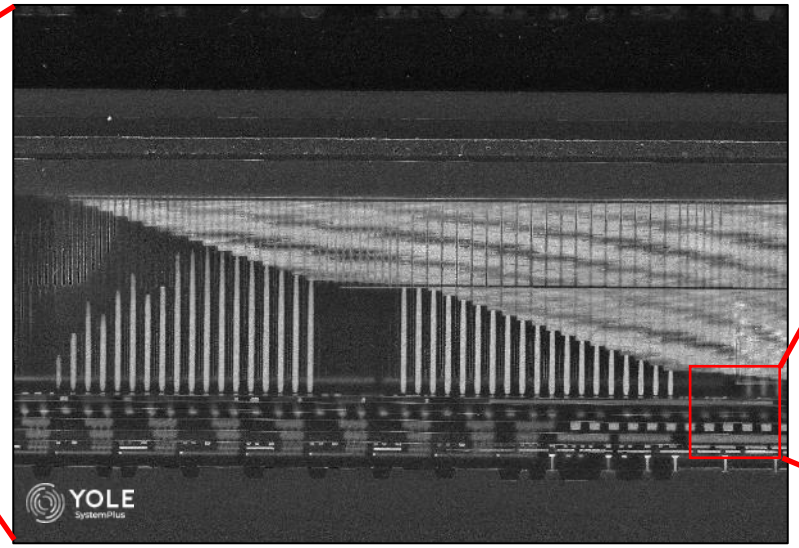

YMTC 128–layer 3D NAND Cross Section
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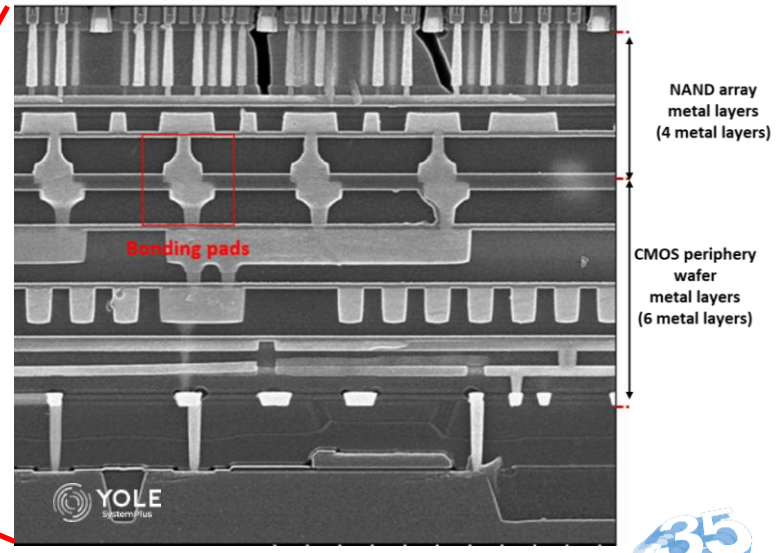

YMTC 128–layer 3D NAND Cross Section
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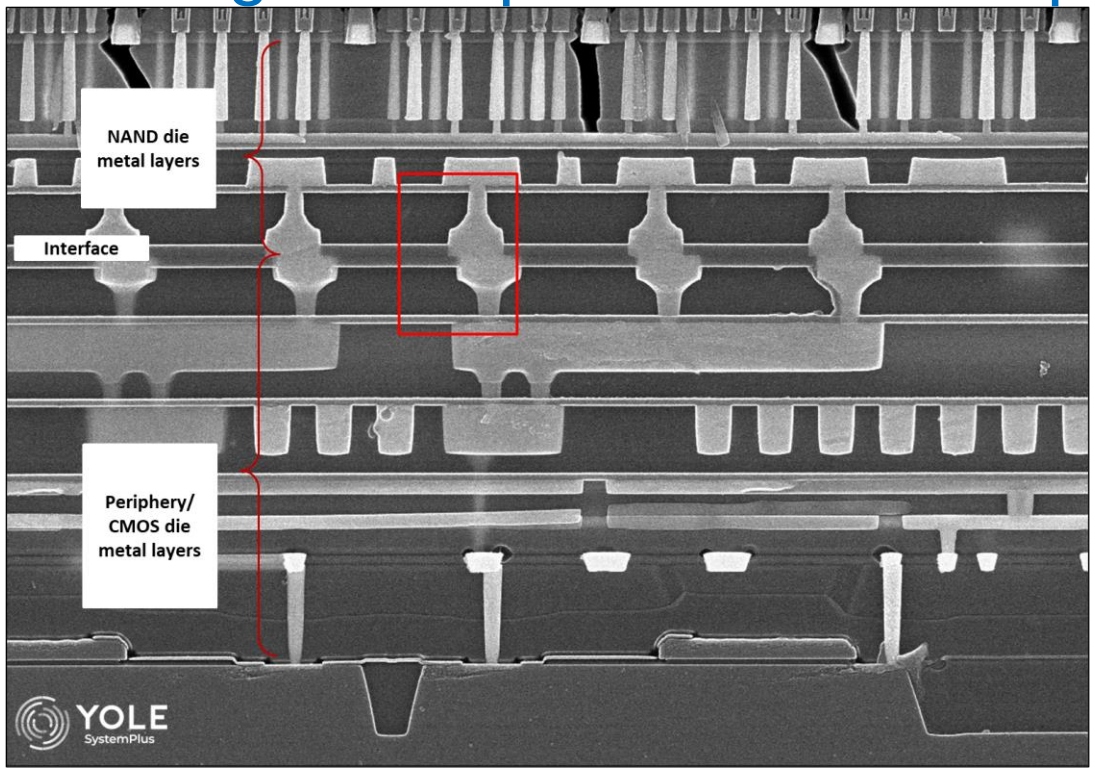
Wafer to Wafer Bonding

- Alignment accuracy is crucial, misalignment could result in electrical disfunctionalities.
- Scaling of the pads remains important in producing good yields.



YMTC 128–layer 3D NAND Cross Section
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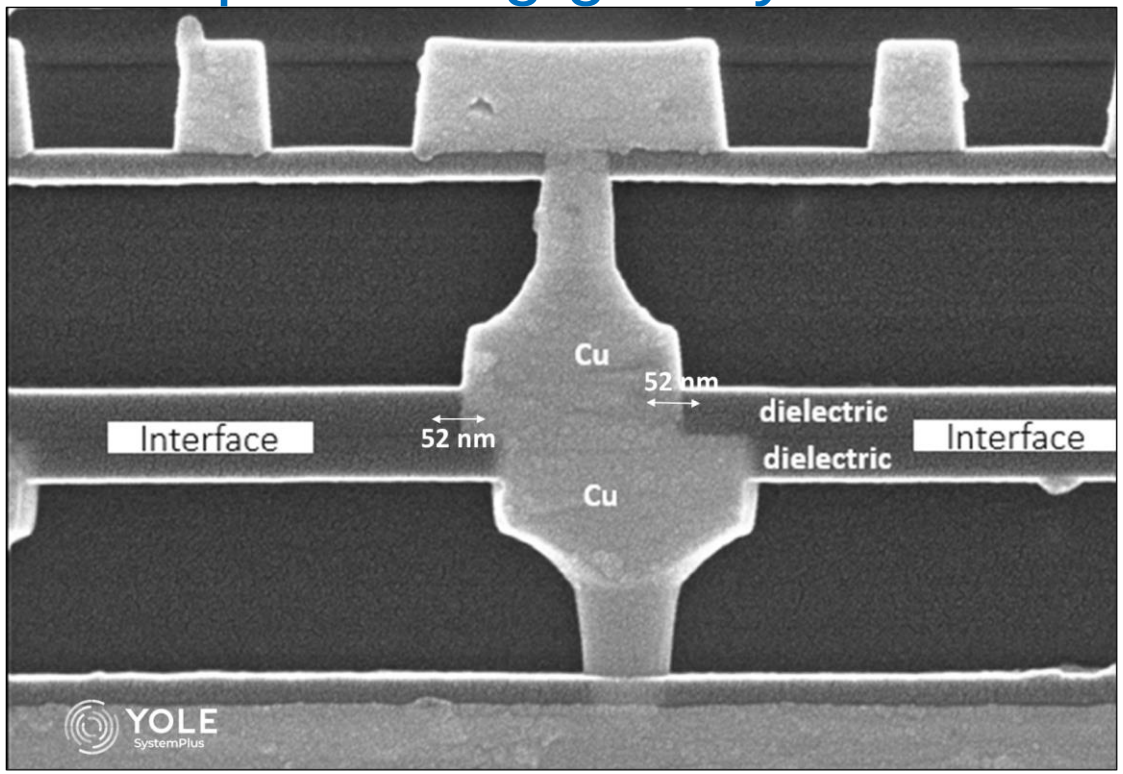

YMTC 128–layer 3D NAND Cross Section
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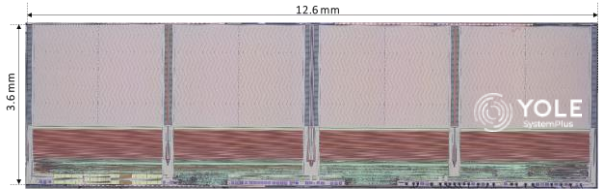
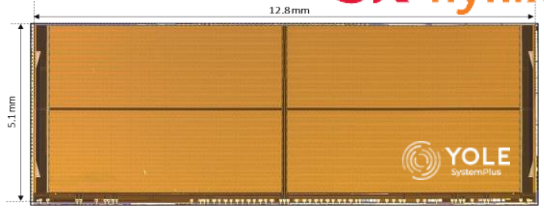
Wafer to wafer Bonding Advantages

SAMSUNG

CMOS on Side



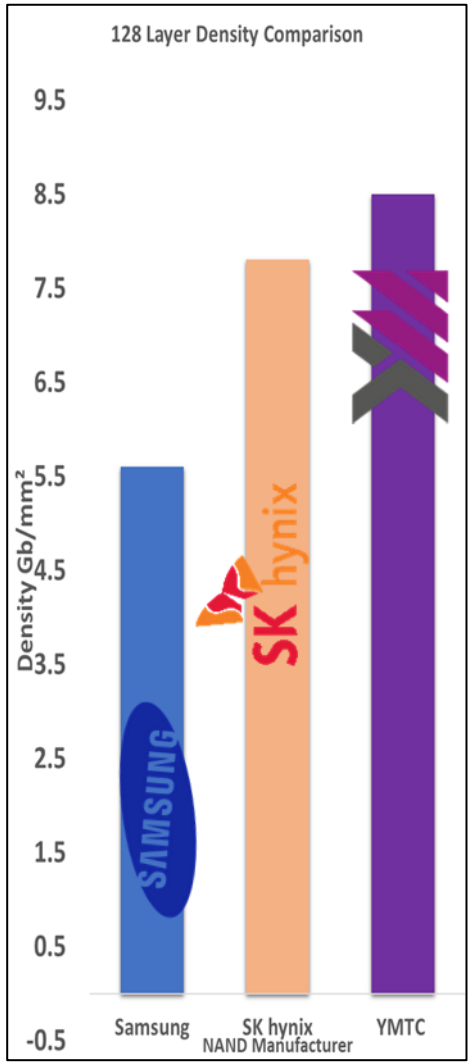
Periphery under Cell SK hynix



Wafer to Wafer Bonding

	Samsung 128-layer NAND	SK hynix 128-layer NAND	YMTC 128-layer NAND
Die Capacity	32GB	64 GB	64 GB
Die Area	45.36 mm²	65.28 mm²	60.16 mm²
Die Density	5.64 Gb/mm²	7.84 Gb/mm²	8.5 Gb/mm²
Die Active Area	25.85 mm²	55.56 mm²	60.16 mm²
Effective Die Area %	**57 %**	**85 %**	**92 %**
Potential Dies/ Wafer	1,392	960	1,048
Potential GB per Wafer	44,544 GB/ 300mm wafer	61,440 GB/300mm wafer	67,072 GB/300mm wafer

Wafer to wafer Bonding Advantages



BENEFITS

- High NAND density increase
- Higher throughput
- Improved Bandwidth
- Different technology wafers could be bonded together

SETBACKS

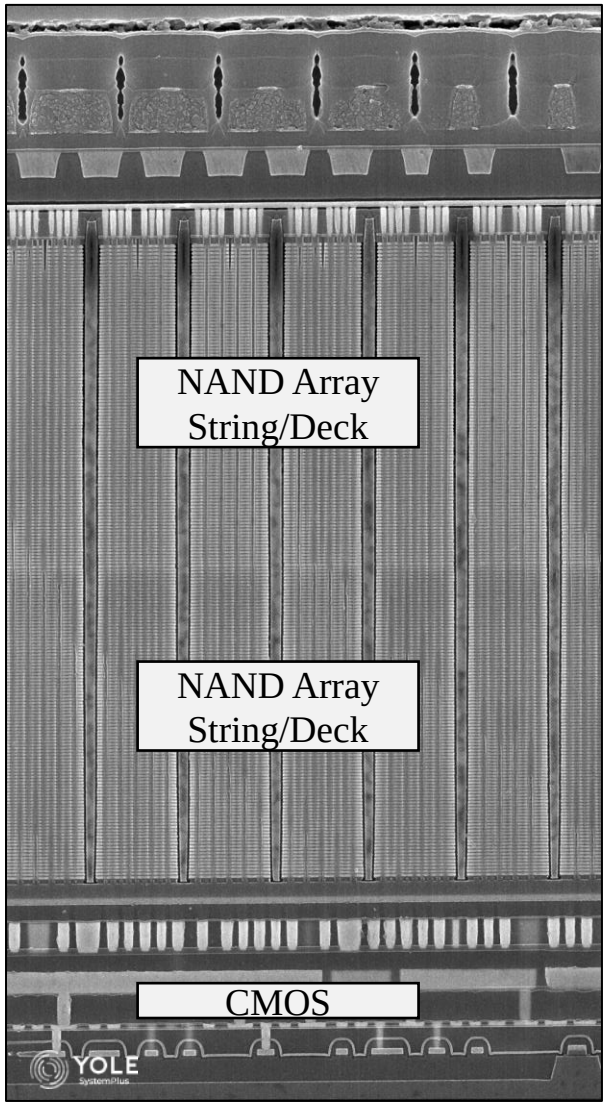
- Precise polishing on both wafers
- High alignment accuracy
- Sensitive to defects
- Low bonding yields

Future of Wafer To Wafer Bonding

Several NAND Decks Wafer

Several wafers could be used to:

- Reduce HAR etch and deposition therefore improving yields
- Increase memory density
- Increase throughput



SK hynix 128–layer Memory Die Cross Section

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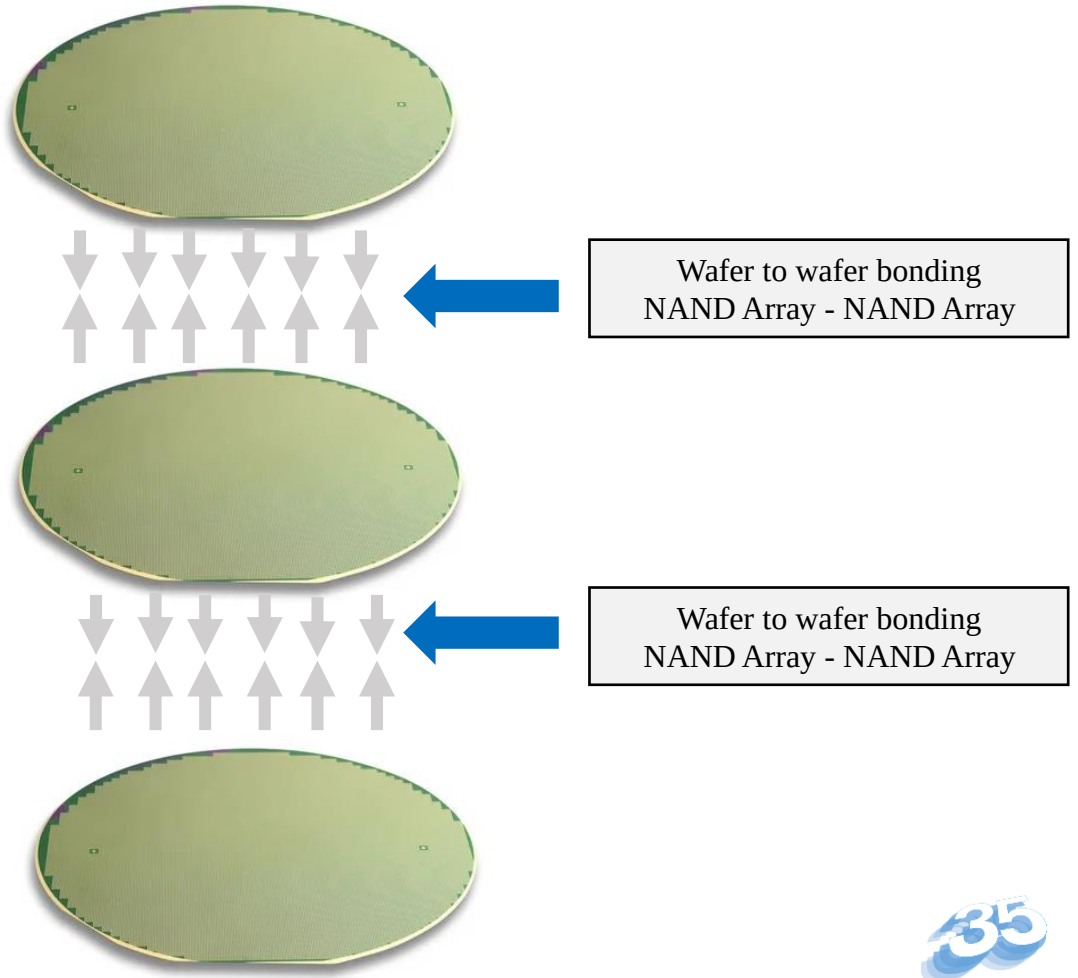
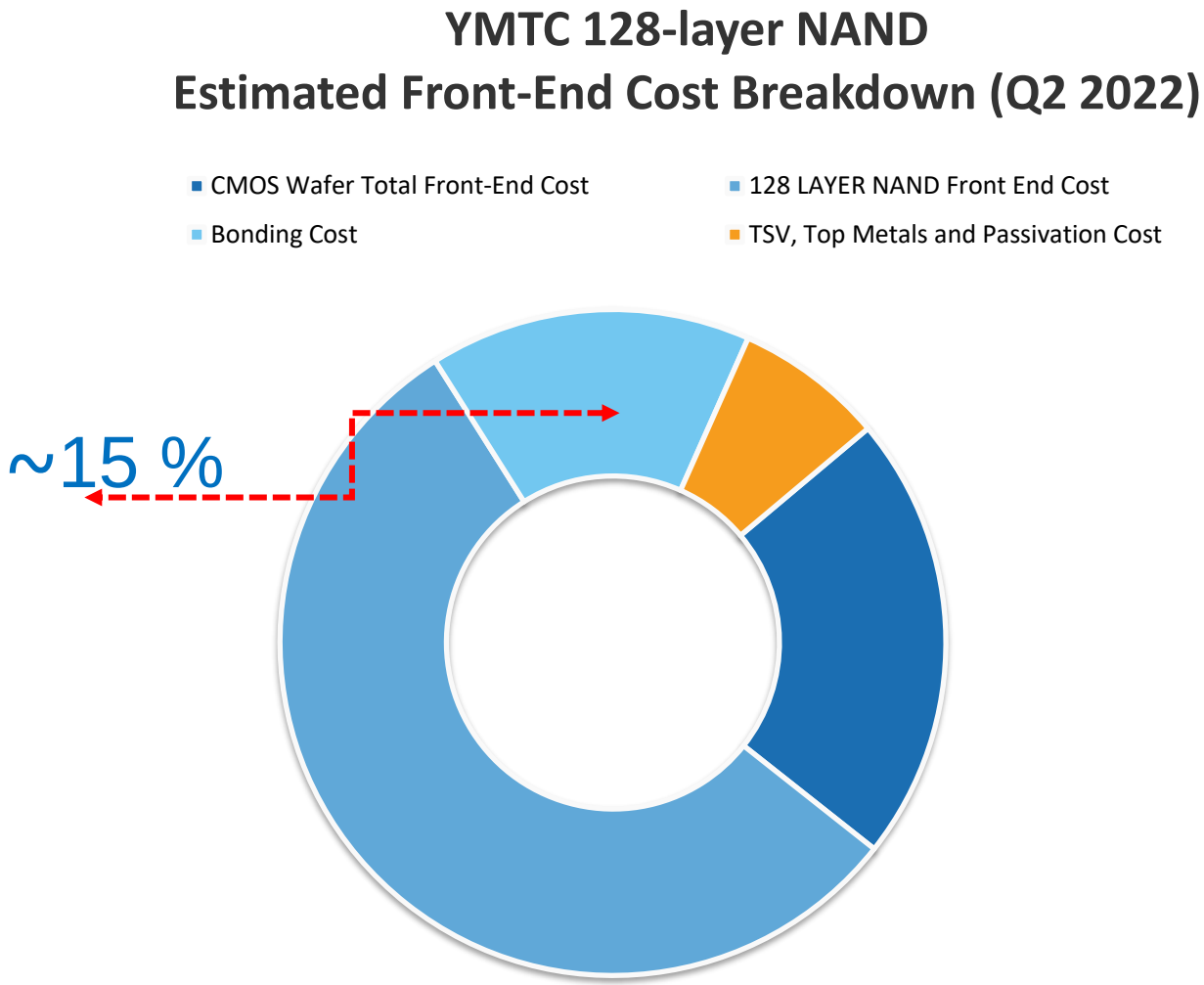


Wafer to Wafer Bonding Cost



Other semiconductor components to also adopt hybrid bonding

- Hybrid Bonding is an enabling technology not only in memory but other semiconductor components like CMOS Images Sensors and High Perfomance Computing.

Galaxy S21 Ultra

Pixel Wafer + Logic Wafer

Ryzen 7 5800X3D

Memory Wafer + SoC Processor Wafer

Conclusion

Conclusion

POTENTIAL IS HUGE

- Potential of Wafer-to-wafer bonding in the memory industry will eliminate some of the NVM manufacturing challenges.
- Density increase is significant,
- Increased throughput will cater for the high memory demand.
- Potential adoption by other manufacturers is huge.
- Potential use as an advanced packaging technology.
- Maturity of the technology will result in improved bonding yields.
- Benefits outweigh the challenges of this technology

More images and analysis coming from Yole SystemPlus Report

YMTC 3D NAND 128 layers

128-layer 3D NAND using Xtacking 2.0 architecture designed to increase die density and data processing speed.

