Flash Memory, Wearable Systems, and the Regulated Environment

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Wearable Medical Device Challenges

1. Regulated businesses greatly influence design
   a. High reliability required
   b. Extreme auditing required

2. Wearable requirement affects power decisions
   a. Battery
      i. Disposable -> primary (non-chargeable)
      ii. Reusable -> secondary (rechargeable)
      iii. Hybrid -> both
      Rechargeable may include super-cap to keep device functioning while battery change or recharge in progress
   b. Switch – ability to remove system power post manufacturing, before use (i.e., a shelf mode)
   c. Regulation and conversion
      a. LDO
      b. Buck converter
      c. Boost converter
      d. Buck/boost converter

3. Battery decisions greatly influence component selection
   a. Favor components that are able to quiesce (or enter standby)
   b. Minimize current consumption to maximize run time

4. Wear-ability greatly influences system design
   a. Small size is typically favored, however mechanical design can sometimes accommodate larger circuits by being ergonomically superior to smaller shapes
   b. PCBA height requirements can influence component selection and overall design
   c. Lightweight is typically favored
   d. Flexibility is sometimes interesting, but typically not worth the cost adder over more conventional designs that are cleverly packaged

Wearable Medical Device Challenges (cont.)

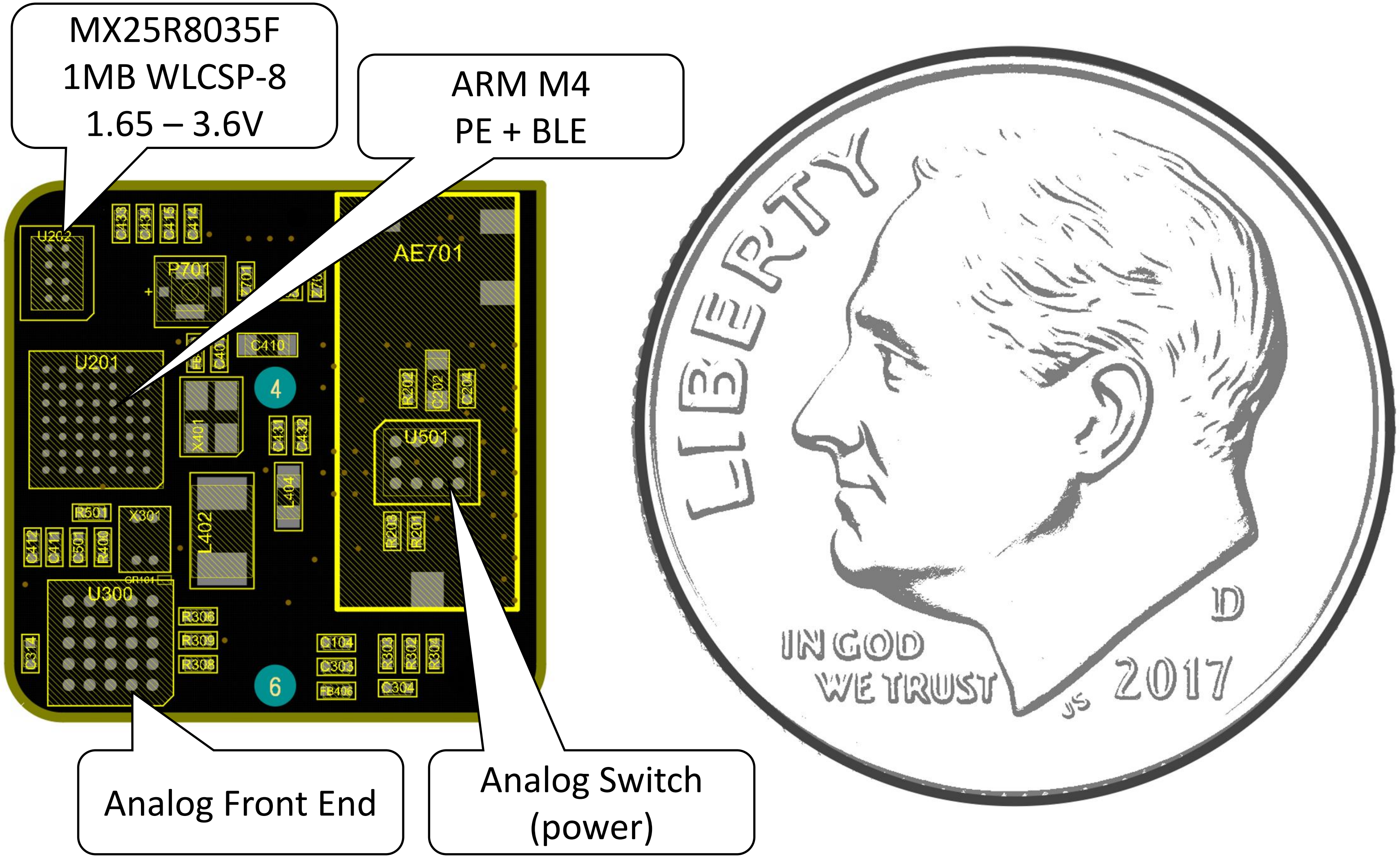
Flash Memory Summit

5. Specification irritations
   a. On critical devices, design engineers must always think worst-case
   b. Specifications containing “Typ” values are of limited, to no use. These values often fool the design engineer into thinking they will get an order-of-magnitude better performance than what may be delivered
   c. There exists a school of engineers who thinks it is valid to sample devices to determine if characteristics are better than the specified “Min” and “Max”
   d. Don’t be fooled, “Min” and “Max” specifications exist for a reason, taking into account manufacturing process deviations that may occur over the span of years, not just today’s lot

6. Other issues that affect component selection
   a. Conventional wisdom: Run processor and peripherals as slow as possible to spread out the pulsatile current consumption to better fit battery profile
   b. My preference: Current consumption is a function of speed (linear relationship) and overhead (nearly constant regardless of speed). Thus, run like hell (within the limits of the battery’s ability to handle the current), then put processor and peripherals into low power sleep mode(s) until time to perform the next function. The mode change will reduce the constant part of the current consumption equation.
   c. The ability to enter low power modes may affect the choice of processor and peripheral devices
   d. Time required to effect mode change from quiescent -> active may affect component selection

YEARS OF NAND FLASH MEMORY INNOVATION

Wearable Medical Device Compared to US Dime

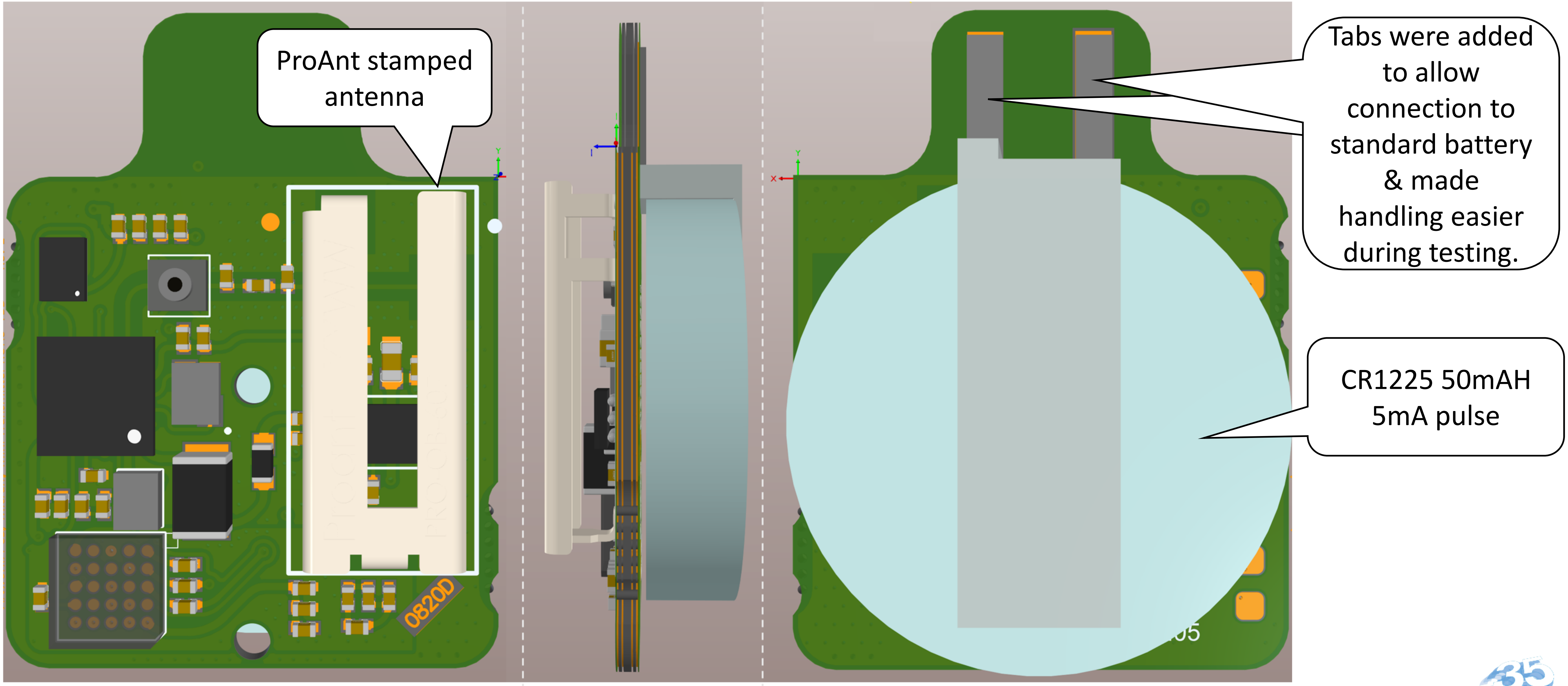


This project was designed to determine if *existing* components and PCB fabrication techniques could be used to create a small, low-power device that could:

- Stimulate and process sensor signals using EIS techniques
- Communicate and coordinate with mobile application using BLE
- Run for up to 30 days on a standard 3V Lithium coin cell

The result was a resounding yes, yes, and yes

3D Views of Design Variation



Design Notes

- This design exceeded the theoretical battery pulse current capacity, but long recovery periods between high current intervals yielded sufficient performance. It was a successful prototype, but not a design that should be put into high volume commercial use until the battery issue is further investigated and understood.

- The next iteration added a system-wide buck converter which was enabled because of the mechanical team's need to change the shape of the PCBA. That created an opportunity to reposition existing components as well as to add new components.

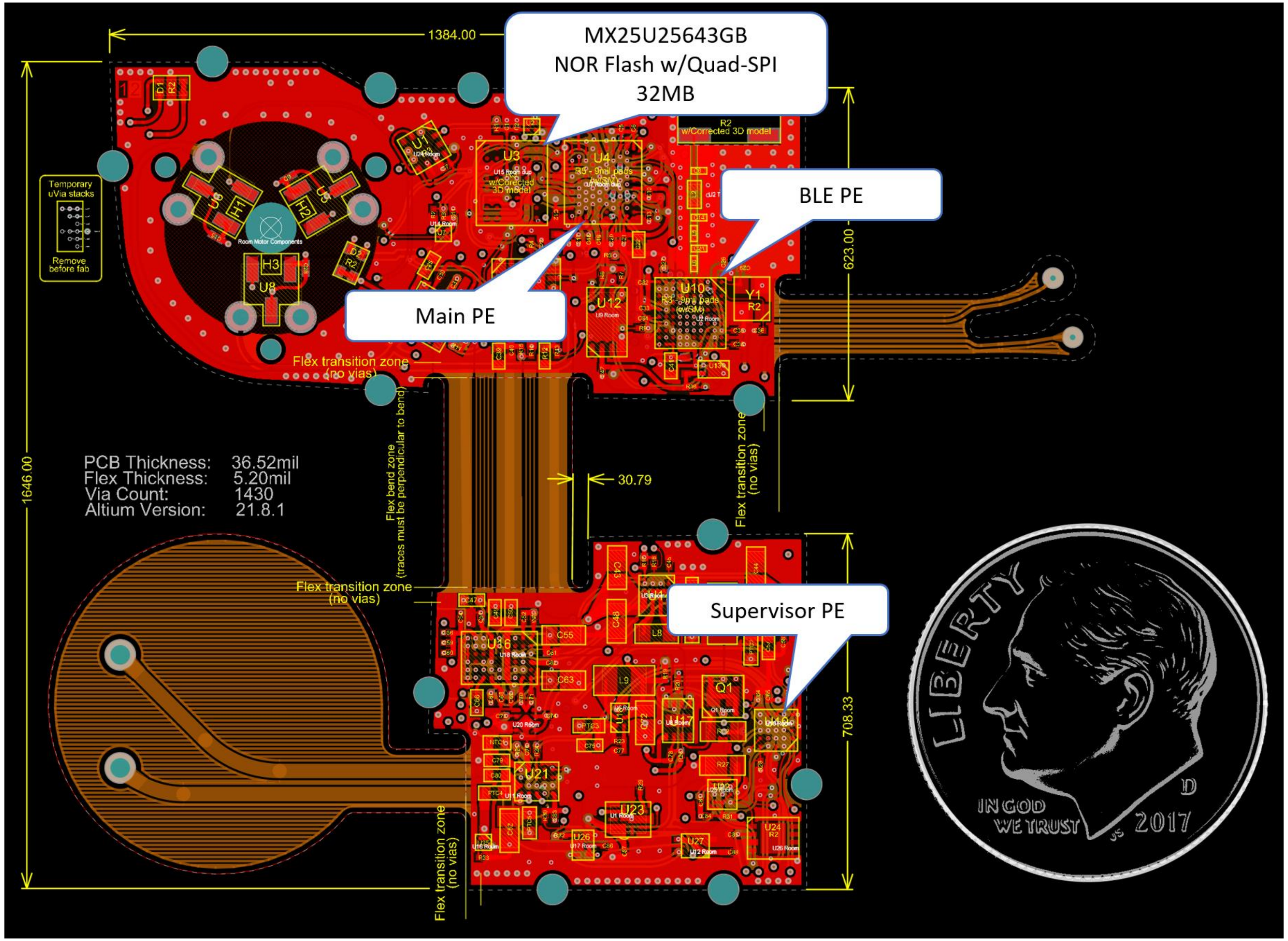
- That iteration also targeted 1.7V for the flash, AFE, and other peripherals.

- Preparation began for a 1.2V system as suitable peripheral components became available. The targeted processor is capable of running at 1.2V when externally regulated (i.e., when using a system buck converter).

- Most ARM processor chips already reduce the core voltage to about 0.9V using a built-in LDO or buck converter. If you are lucky they have a SIMO arrangement where the rest of the system can tap into the IO domain voltage supply. Unfortunately, that domain usually is not capable of providing sufficient current to run flash devices, hence the move to a system buck converter.

- Split supplies are vexing, but we'll have to deal with them until we can get processors and peripherals that all operate in the same voltage ranges.

Another Wearable Device Example

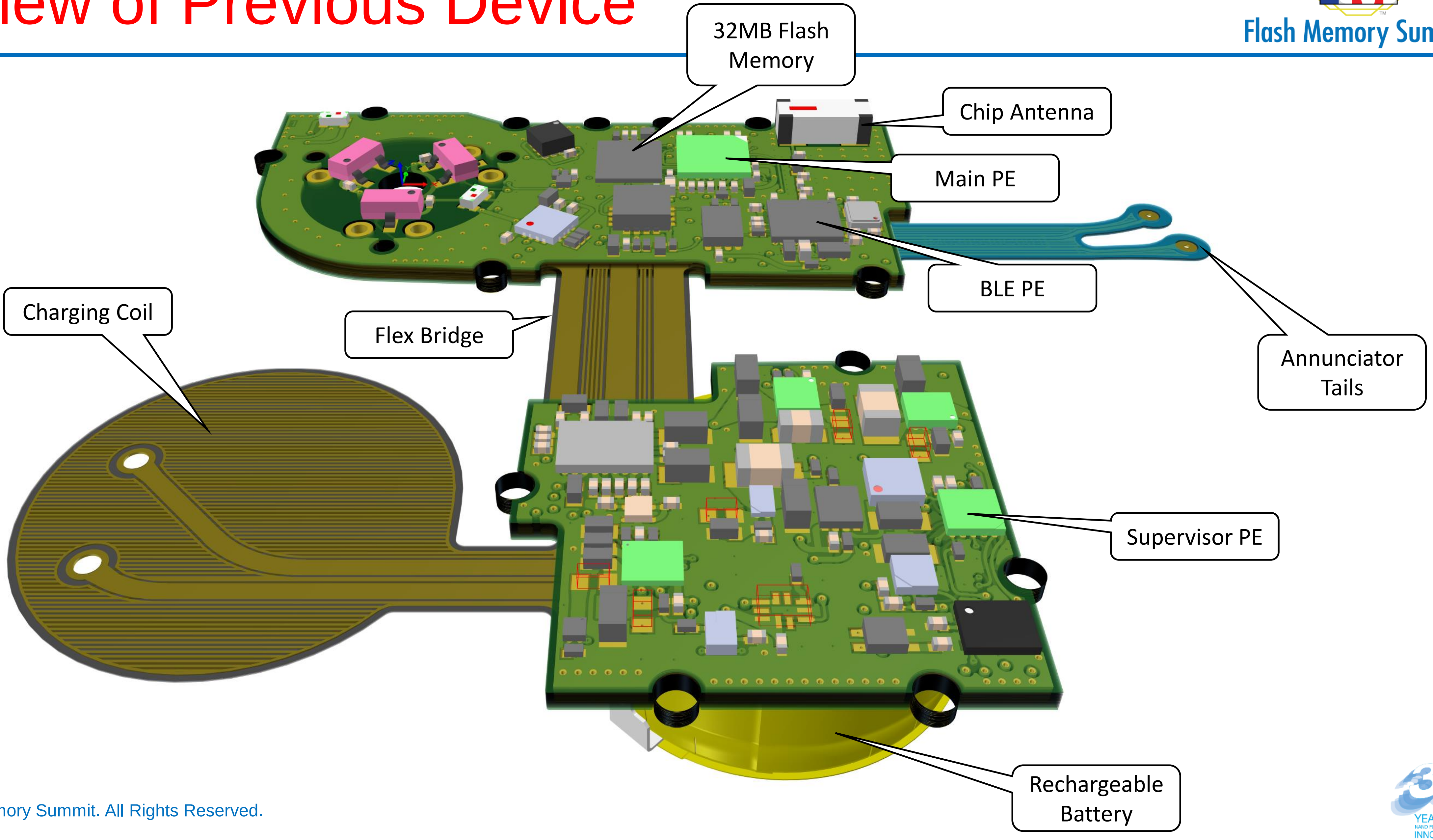


This project was designed to determine if rigid-flex techniques could make the device more compact.

- Interconnect density required 10 layers
- Flex portion required 2 layers + coverlays
- Selected fab house was unable to stack µVias deeper than 3 layers each side, making it challenging to get from middle 4 to the outer layers
- This is a rechargeable device, so while still important, power consumption was not the most significant issue

The result was a success and allowed the mechanical team considerably more flexibility in packaging options.

3D View of Previous Device



Flash Memory Wishlist

1. All regulated devices are well served by comprehensive logs.
   a. Traditionally these logs are circular and contain only the last *'n'* events
   b. All devices can benefit from a permanent, complete log. Certainly medical devices benefit from some form of this
   c. Write-once technologies (formerly referred to as OTP, one time programmable) are well suited for this purpose.
   d. Much, much larger OTP memories are desirable for this function

2. All devices benefit from capability of over-the-air (OTA) updates. This requires a datastore that can be quite large.
   a. If the OTP is sufficiently large, the OTA image can be stored there before overwriting program store
   b. Preferably, If read access to this image in OTP is reasonably fast, modern processors can execute-in-place (EIP) directly from this image, avoiding the secondary transfer to program store for live operation (i.e., OTP becomes the program store)
   c. Quad and Octa-SPI are preferred interface for EIP operation

3. The expected volumes for current projects are massive (from 1KK to 10KK per month).
   a. Ultra low cost is extremely important to make the concept viable
   b. Failure rate must be nearly non-existent
   c. Built in ECC is interesting, particularly if used as program store
   d. Page of rewritable flash (or battery backed SRAM) to serve as a directory or index into OTP pages is interesting

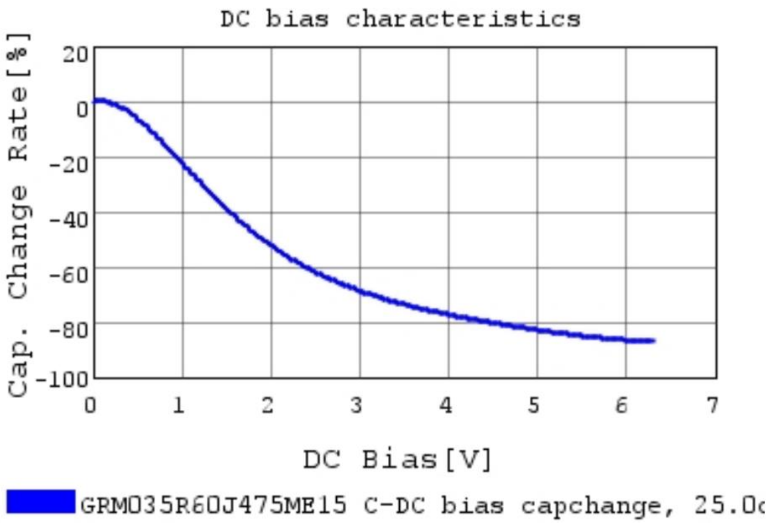
4. Current consumption must be considerably lower than existing flash technologies, perhaps 1/10th

Desirable Flash Memory Traits

Prioritized by Importance

1. Small package (WLCSP)
    a. Minimize pinouts
    b. Octa-SPI preferred (with Q-SPI option)
    c. Q-SPI
2. Low current (at least 1/10th existing levels)
3. Low voltage (target < 1V)
    a. 3V Lithium (3.3V+ unloaded), buck is required
    b. 1.14 -1.6V Silver Oxide, buck probably required
    c. 0.9 – 1.5V Zinc-air, buck may be required
4. Thin package
5. Encrypted, secured, and write protected at the device level is becoming more important
    a. Need for encryption at device level depends on attack vectors and use case assessment (nature of the data)
    b. IF OTP device, write protection is moot
6. Secondary Vin that supplies interface level converter voltages

One non-obvious reason for emphasizing low supply voltages is that the effective values of small sized capacitors (e.g., 0201) go down as the DC bias goes up.



As the sizes get smaller and the values go higher, the bias curve drops precipitously requiring greater derating by the designer.

It goes without saying that supply-conditioning capacitors are always under bias.

