Flash Memory Summit

YOLE SystemPlus

Advances in EUV Memory Manufacturing

Belinda Dube

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35 YEARS OF NAND FLASH MEMORY INNOVATION

Biography

Belinda Dube, Technology & Cost Analyst

Belinda Dube serves as a Technology & Cost Analyst at Yole SystemPlus, part of Yole Group.

Belinda's core expertise is memory technology, especially DRAM and 3D NAND flash memory. At the same time, she also investigates IC technologies as well as advanced packaging.

Belinda's mission is to develop reverse engineering & costing reports. She also works on custom projects, where she works closely with the laboratory team to set up significant physical & chemical analyses of innovative memory chips. Based on the results, Belinda identifies and analyzes the overall manufacturing process and all technical choices made by the memory makers.

In addition, a significant portion of her mission is dedicated to a strategic technology watch, where her aim is to identify innovative memory chips and manufacturing processes. Based on her expertise, Belinda updates internal simulation tools and runs custom training sessions and demos with industrials.

She regularly has an opportunity to reveal pertinent results during key onsite presentations and webcasts.

Prior to System Plus Consulting, Belinda had the opportunity to work on several R&D projects dedicated to MEMS technologies and new substrates at INSA (Lyon, France).

Belinda holds a master's degree in Instrumentation & Nanotechnology Engineering from INSA (France).

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MARKET ANALYSIS
DRAM MARKET
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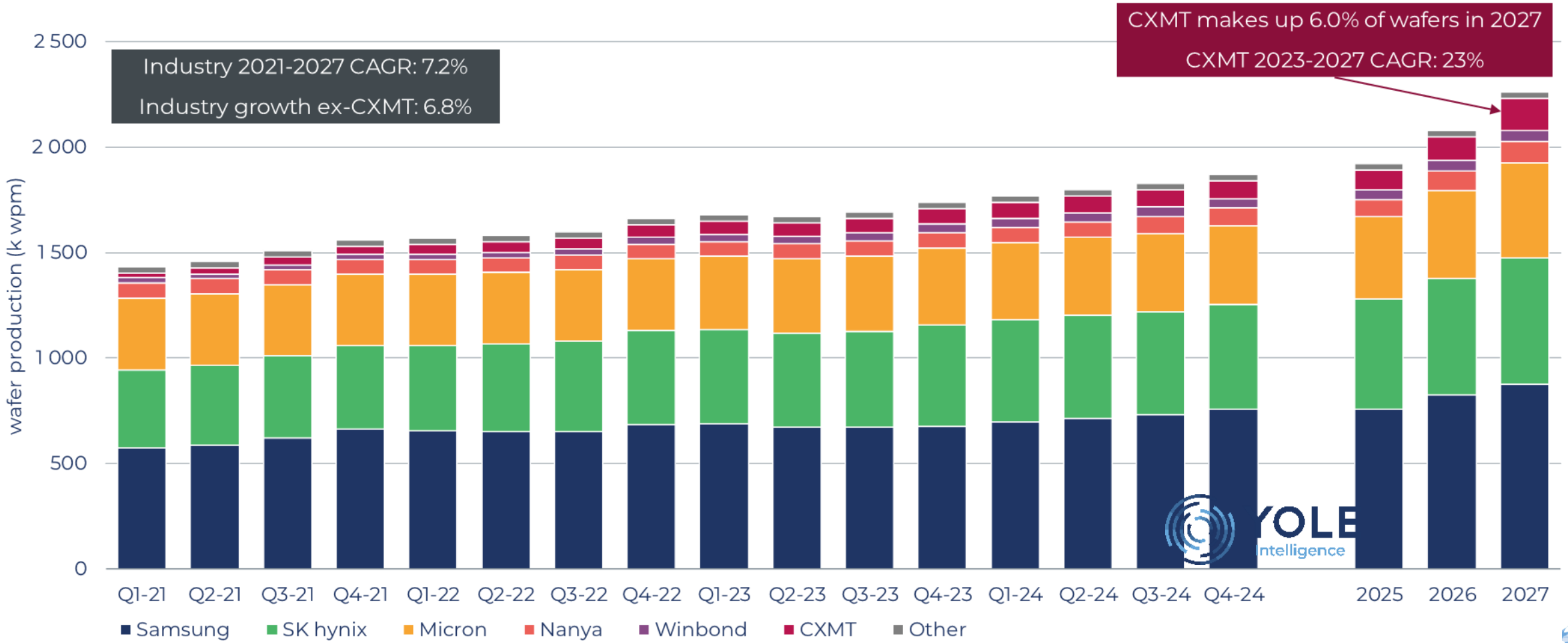
DRAM MEMORY MARKET

- Over the long-run wafer production will increase to keep pace with bit demand.



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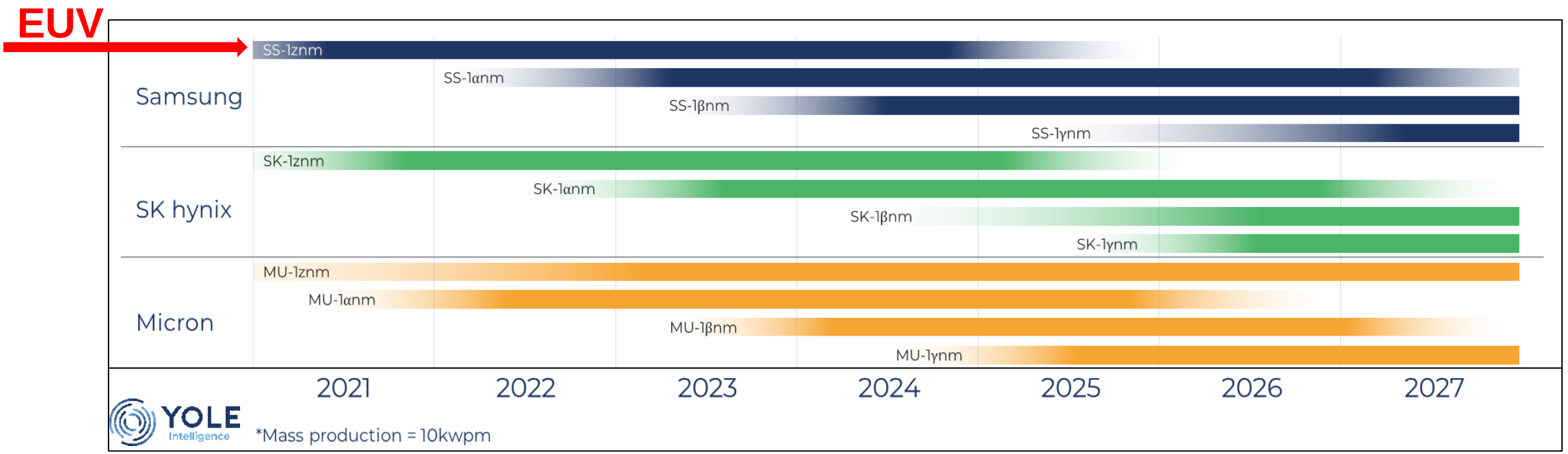
DRAM EVOLUTION

- EUV Lithography has been adopted to overcome the limitations of DRAM scaling in memory manufacturing.
- Samsung is the first in the industry to successfully apply EUV processing and has been mass-producing specific EUV-applied products.



DRAM Market Monitor Q2 2022

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DRAM TECHNOLOGY ANALYSIS

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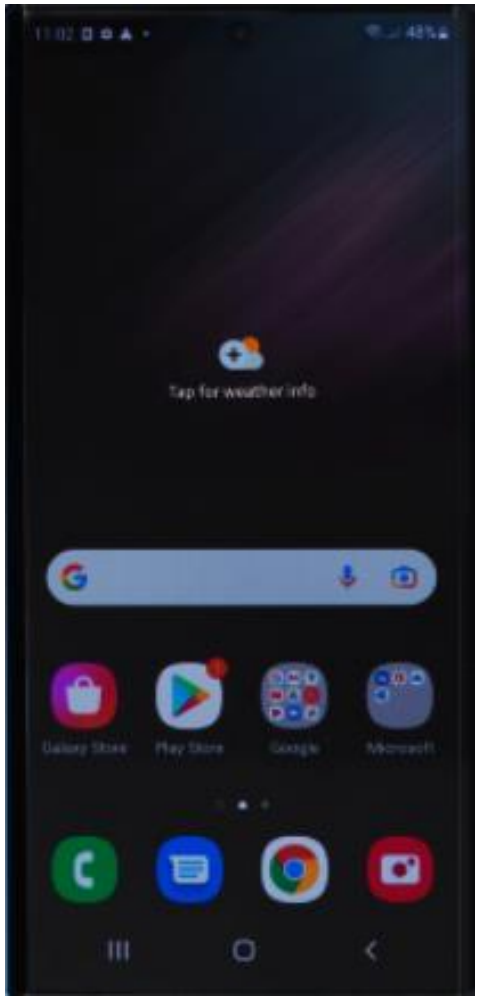
SAMSUNG DRAM



Samsung Galaxy S22 Ultra 5G (International Version)
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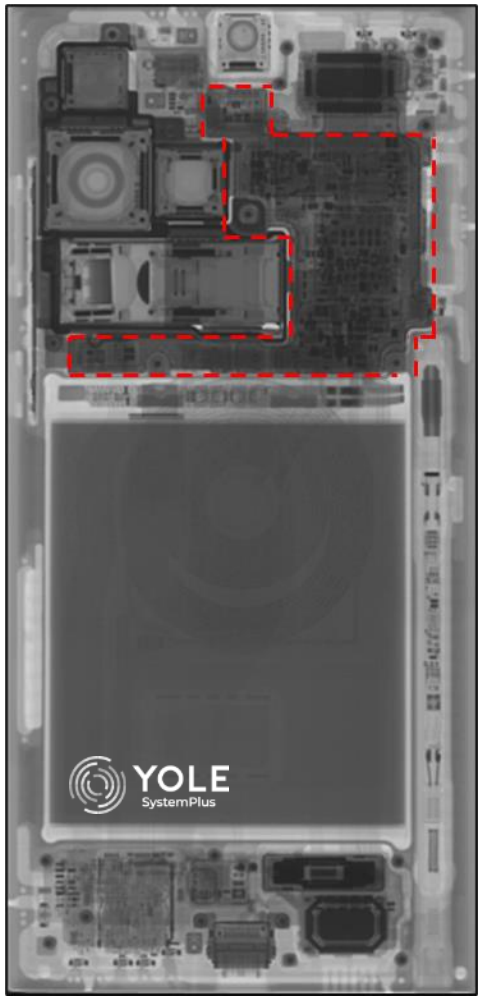

Samsung Galaxy S22 Ultra 5G –X-Ray Image (International Version)
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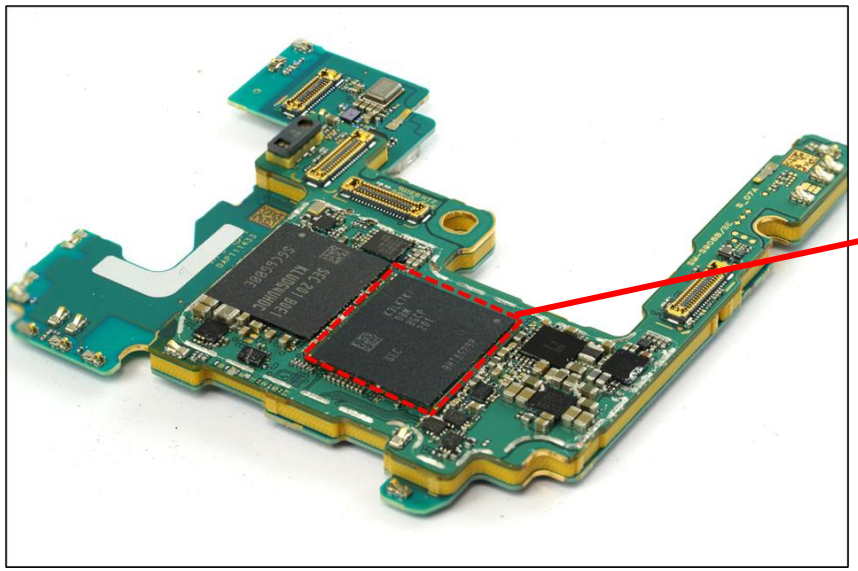

Main PCB on Samsung Galaxy S22 Ultra 5G
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Samsung LPDDR5 Frontside View
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- Huawei Honor Magic3 Pro 5G
- SAMSUNG Galaxy S22+ 5G
- SAMSUNG Galaxy S22 Ultra 5G
- XIAOMI 12 Pro
- OnePlus 9 Pro 5G
- Huawei P50 Pro
- ASUS Zenfone 8 Flip
- XIAOMI Black Shark 4
- SAMSUNG Galaxy S21 5G
- GOOGLE Pixel 6
- SAMSUNG Galaxy Z Flip3
- XIAOMI POCO F4 GT

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SAMSUNG DRAM

Samsung Memory 8GB Package
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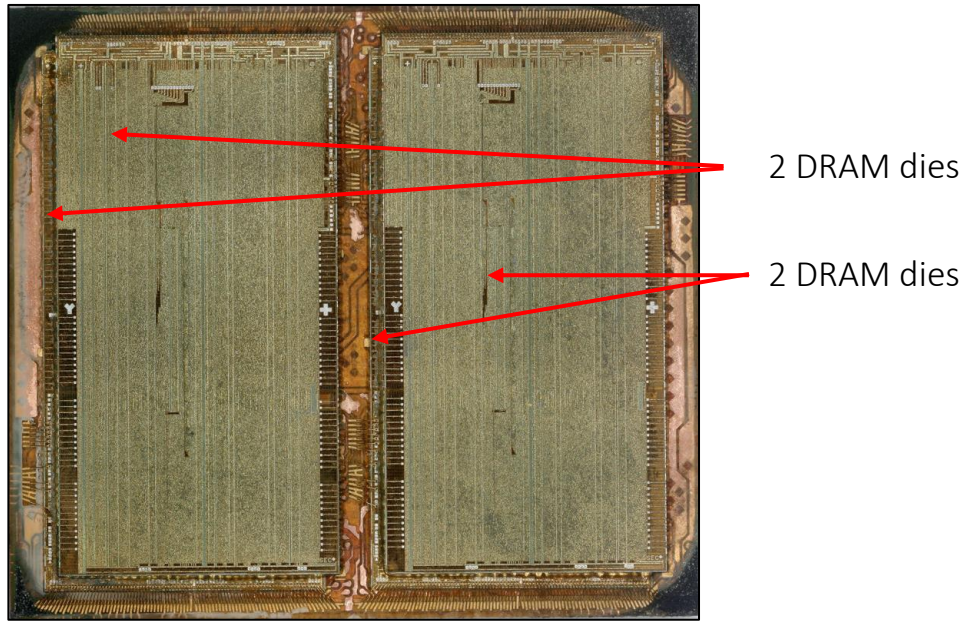

Samsung Memory 8GB –Package Opening
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Samsung Memory Package Cross Section – Optical View
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- Dies in package : 4
- Die capacity: 16Gb

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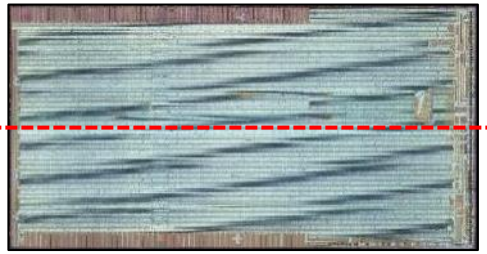
SAMSUNG DRAM EUV LITHOGRAPHY



Die Cross Sectioning
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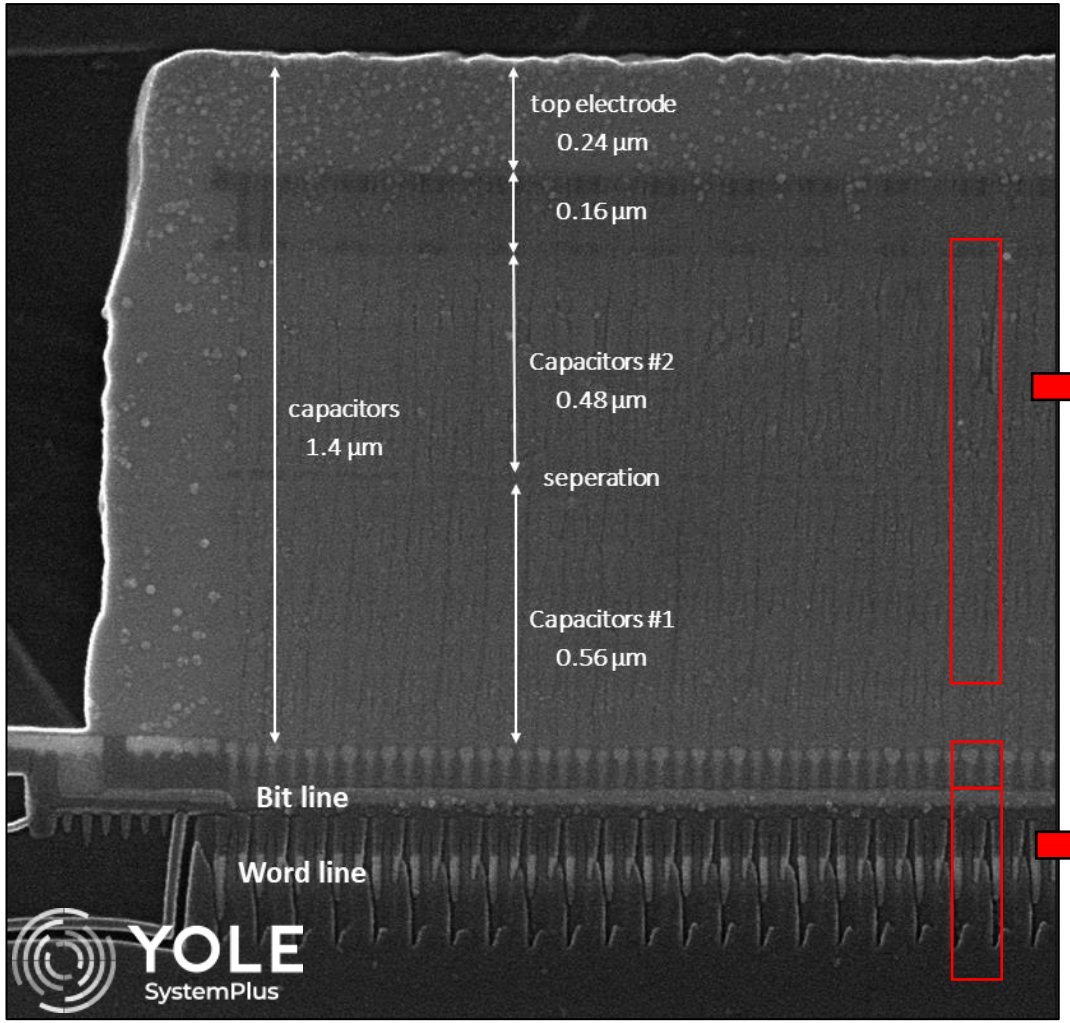

Die Cross Section – SEM View
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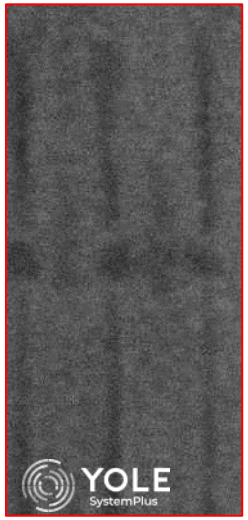
Capacitor opening



Capacitors – SEM View
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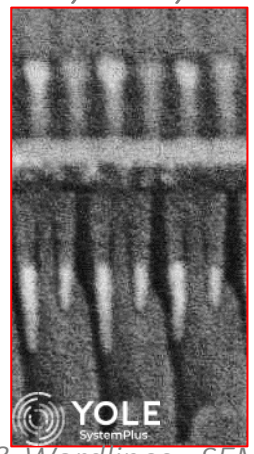
Wordline & contacts



Contacts & Wordlines– SEM View
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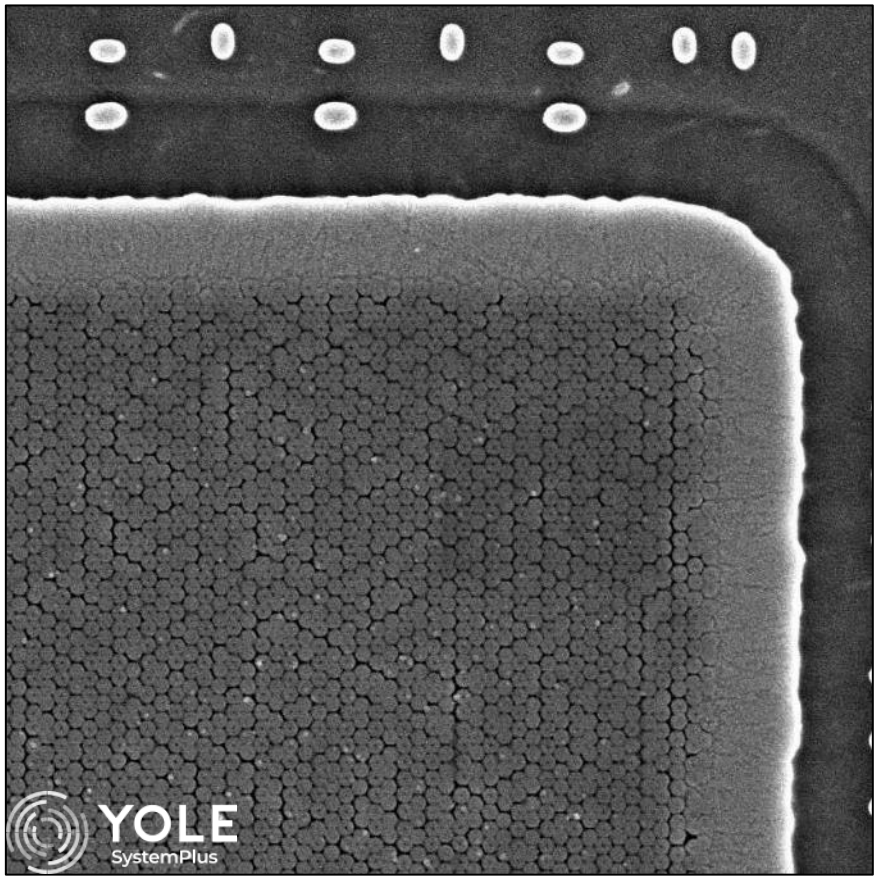
SAMSUNG DRAM EUV LITHOGRAPHY

- Cell size ~ 0.018 µm²
- Reduced Cell size results in higher density.



Die Delayering SEM View
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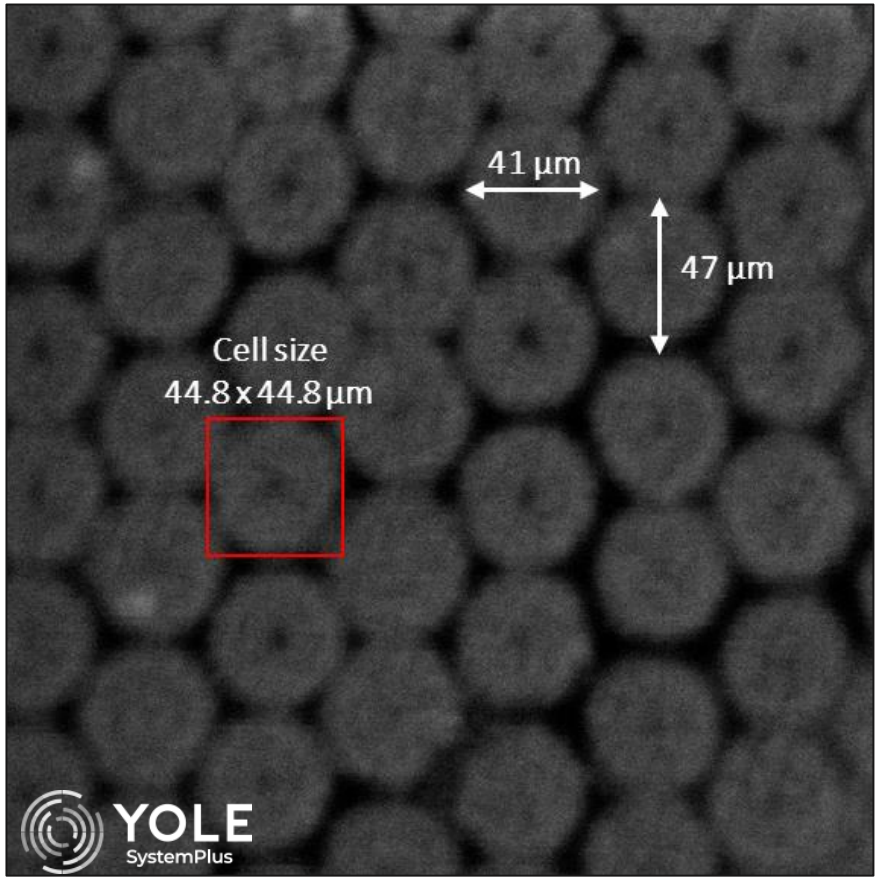

Die Delayering SEM View
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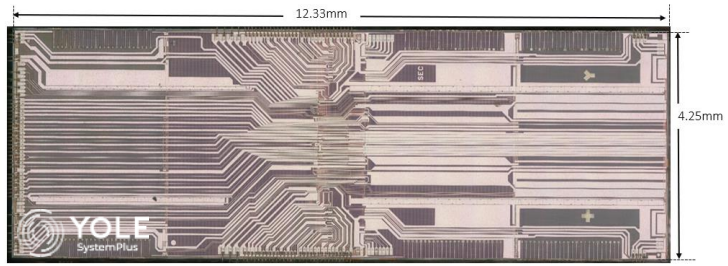
35 YEARS OF NAND FLASH MEMORY INNOVATION

SAMSUNG EUV DRAM vs NON EUV DRAM



Samsung LPDDR5 (1y gen)

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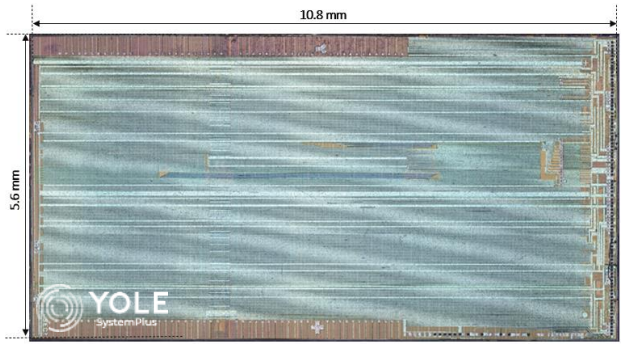

Samsung LPDDR5 (1z gen)

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	Samsung LPDDR5 (non EUV)	Samsung LPDDR5 (EUV)	
Die capacity	12Gb	16Gb	30%
Die dimensions	12.3 x 4.2 mm	10.8 x 5.6 mm	
Die area	52 mm²	60 mm²	
Die density	0.23 Gb/mm²	0.264 Gb/mm²	15%
Potential dies/wafer	1,204	1,048	
Potential capacity /wafer	14,448 Gb/300mm wafer	16,768 Gb/300mm wafer	15%

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DRAM COST ANALYSIS

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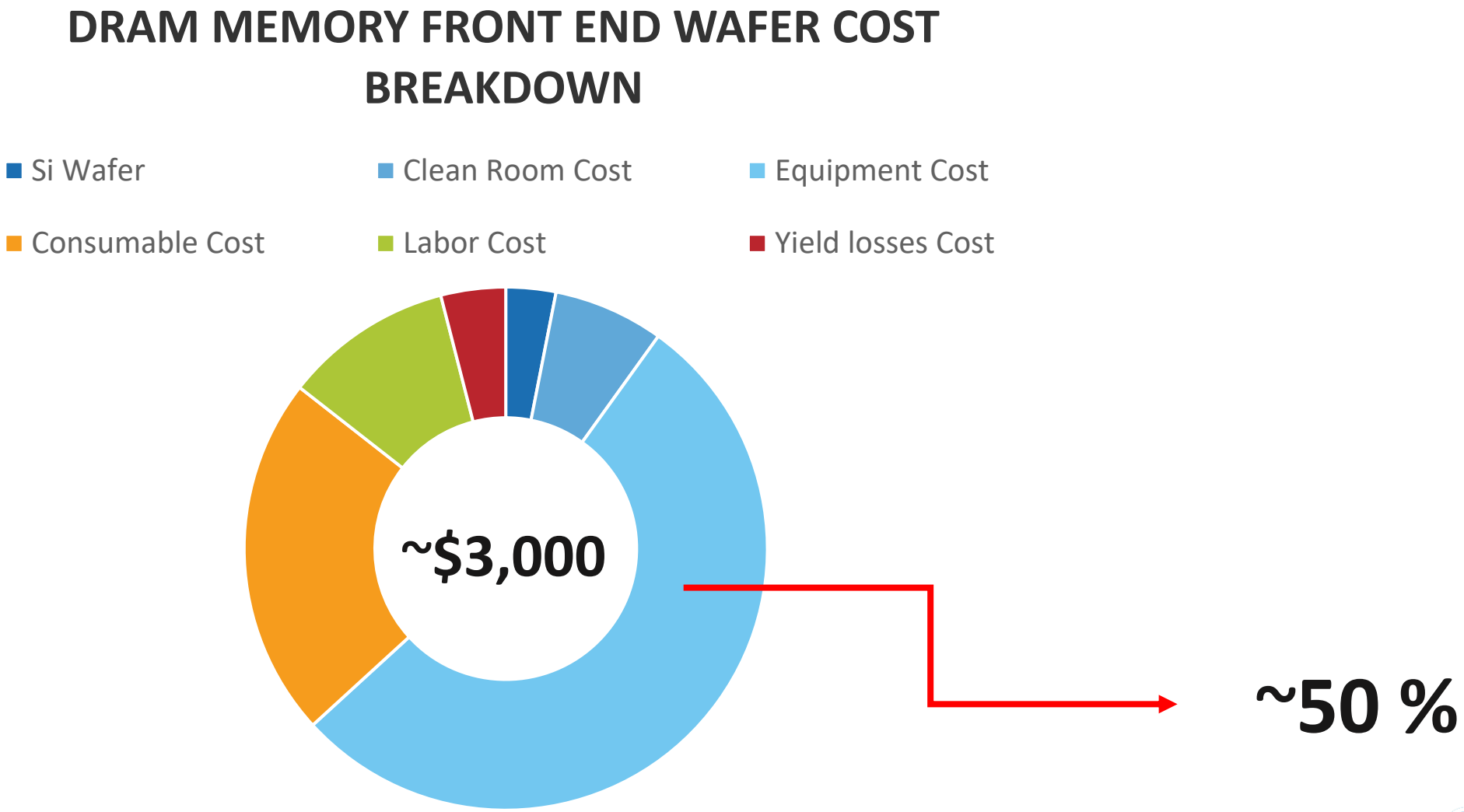
SAMSUNG COST ANALYSIS



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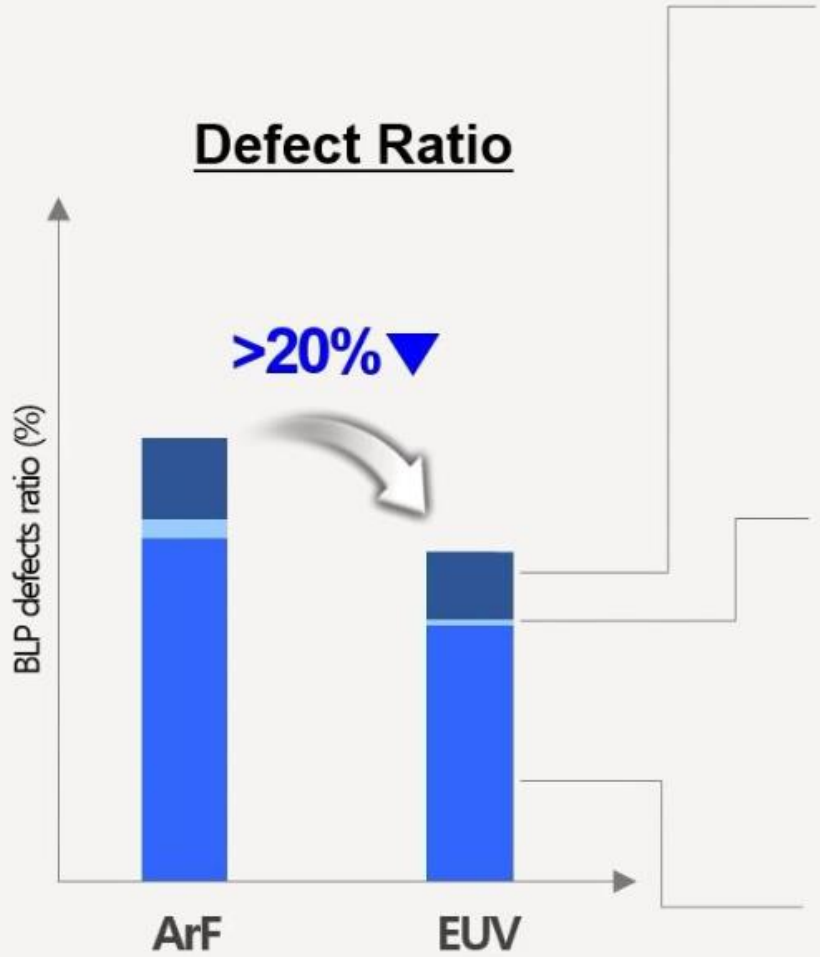
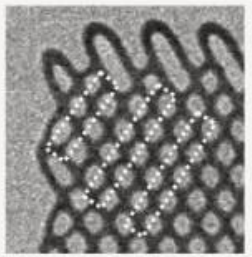
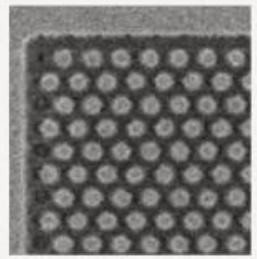
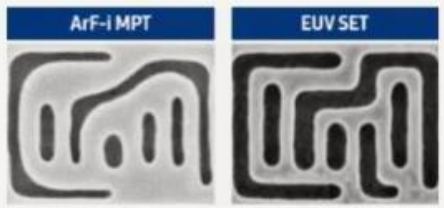
SAMSUNG EUV BENEFITS



✓ **Eliminating multi-patterning related defects**

Patterning	ArFi MPT	EUV SET
DRAM D1x BLP SEM Image		

✓ **Enhancing patterning precision and cost**



✓ **Reducing number of steps and accumulated defects**

Source : Samsung Investor Meeting 2020

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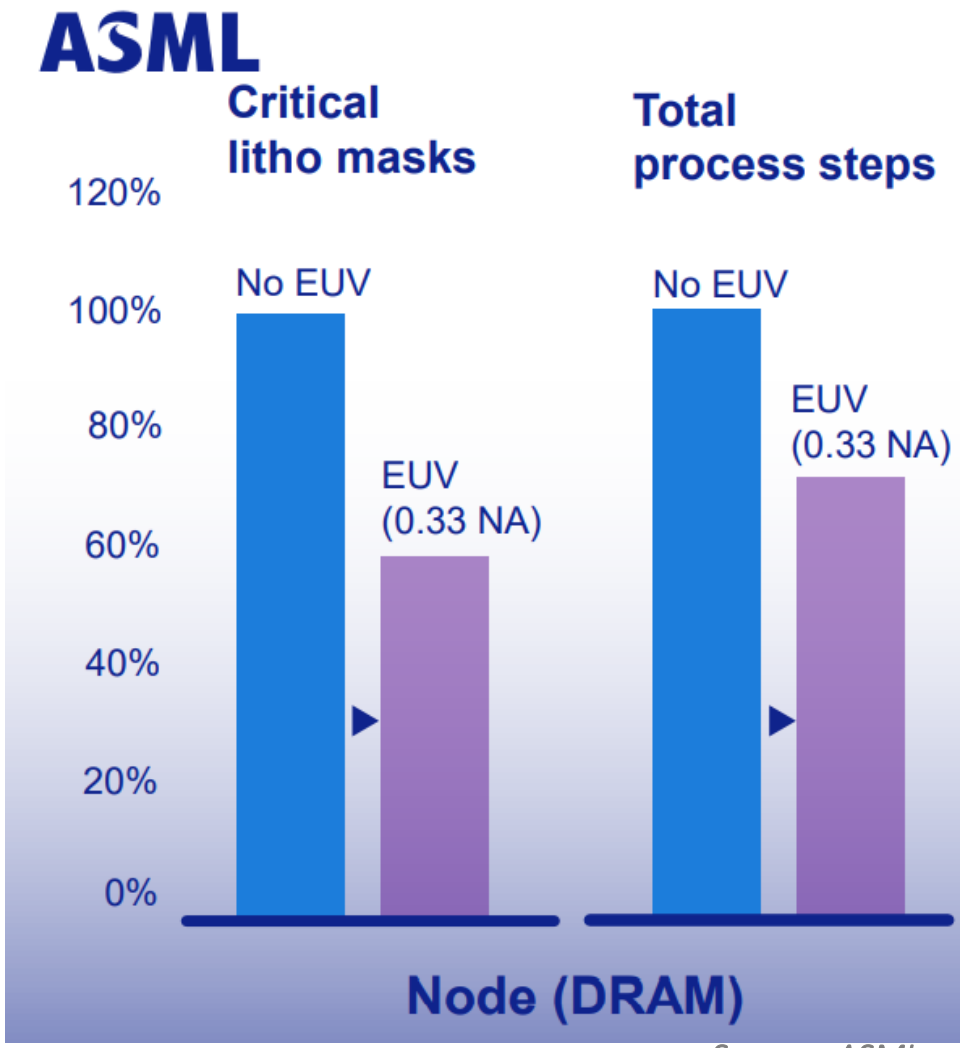
SAMSUNG EUV BENEFITS



Source : ASML

EUV lowers the lithography and total number of process steps, resulting in :

- Reduced Defect
- Shorter Cycle time
- Cost reduction
- Higher productivity per wafer
- Density increase

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EUV LITHOGRAPHY

BENEFITS

- IMPROVED YIELDS
- HIGHER DENSITY DIES
- REDUCED PRODUCTION TIME
- COST REDUCTION

DISADVANTAGES

- HUGE INVESTMENTS IN EQUIPEMENT
- EUV WAVELENGTH CAN BE EASILY ABSORBED
- EUV EQUIPEMENT FOOTPRINT

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CONCLUSION

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CONCLUSION

- EUV lithography process allows the memory to store more capacity within the same area to meet increasing demands for high capacity.
- EUV can greatly enhance the feature density of chips without heavy reliance on multi-patterning, Multi patterning to single patterning reduces the processing steps and time.
- Samsung has been the first to introduce EUV lithography patterning in DRAM memory, in the future other players will join and adopt EUV process.
- Heavy investments is necessary for this process adoption.

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