Flash Memory Summit

CXL Controllers for Memory Disaggregation in the Data Center

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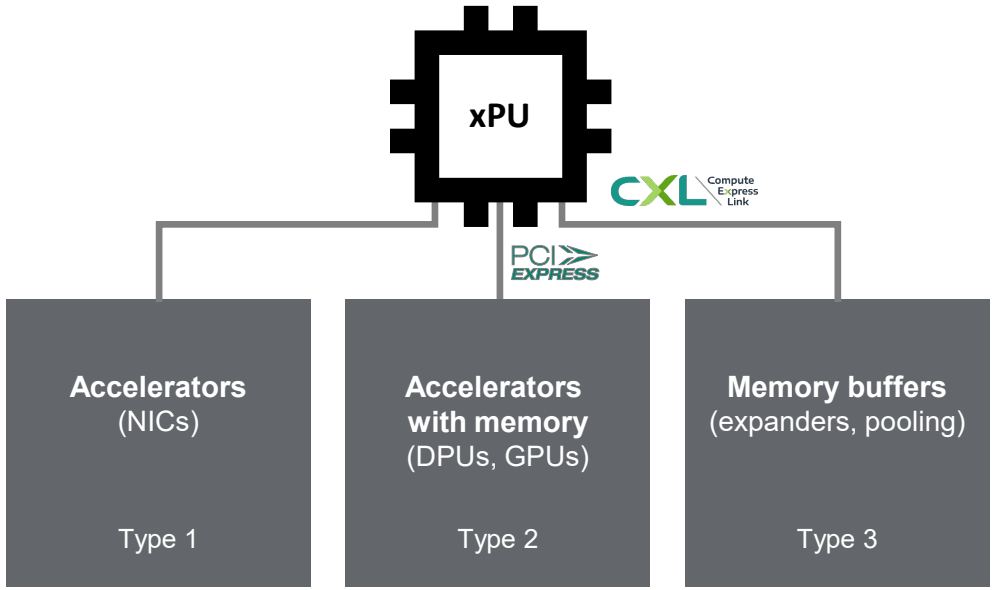
Outline

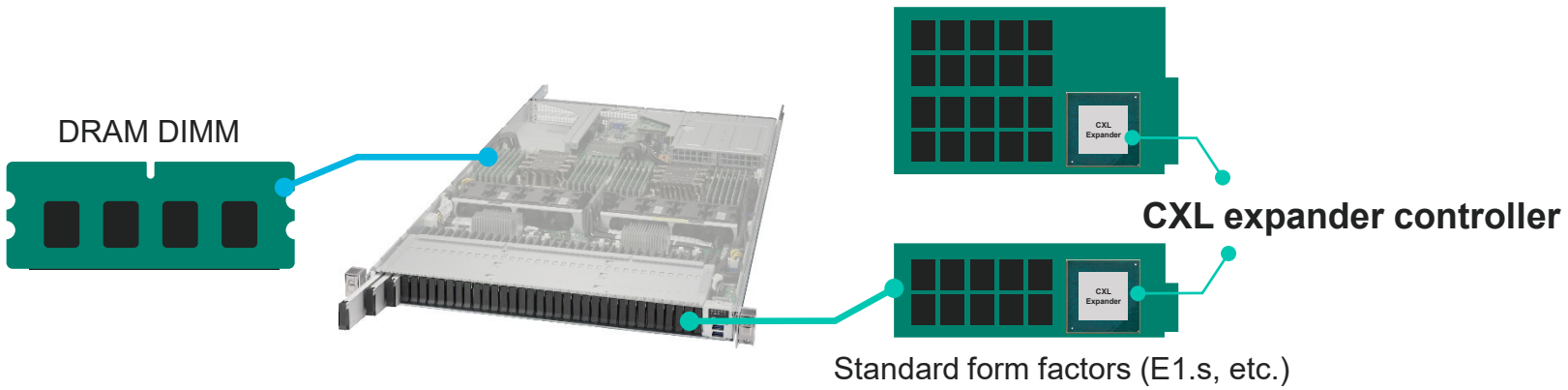
1. Compute Express Link™ (CXL™) standard
2. CXL controller architecture
3. Latency and bandwidth
4. Key features

Compute express link



- Industry standard protocol
- Runs over PCI Express
- Low-latency interconnect
- Memory-optimized
- Cache-coherent

Memory expansion with CXL



DIMM challenges

- Limited scalability
- Not serviceable
- No telemetry

CXL solution

- Scalable
- Pluggable
- Telemetry
- Improved thermals
- Mix-and-match DRAM
- Config flexibility

CXL memory expansion and acceleration

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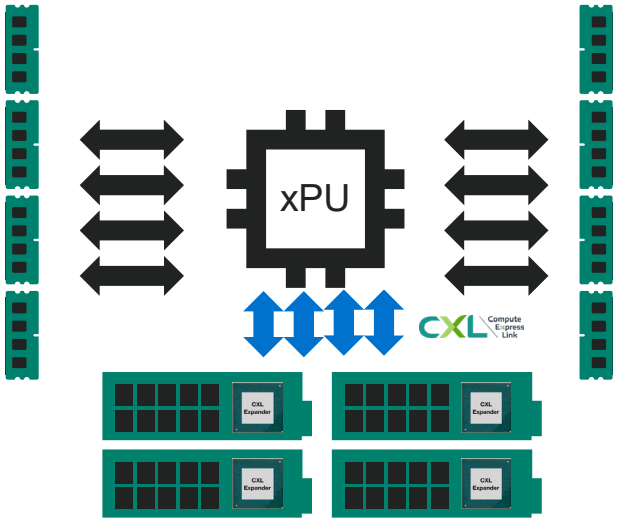
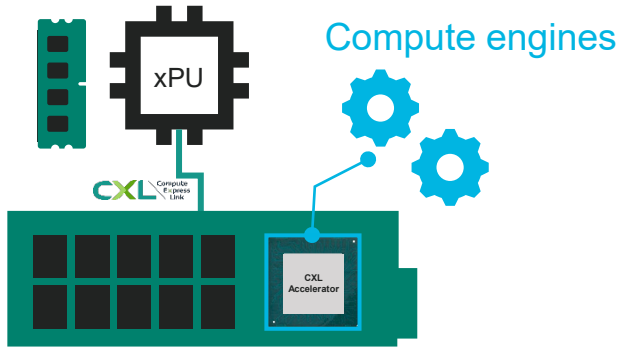
CXL memory expansion



- Add memory through PCIe / CXL links
- Increases capacity and performance

CXL accelerator



- Coherent and efficient
- Accelerates analytics, ML, search, etc.

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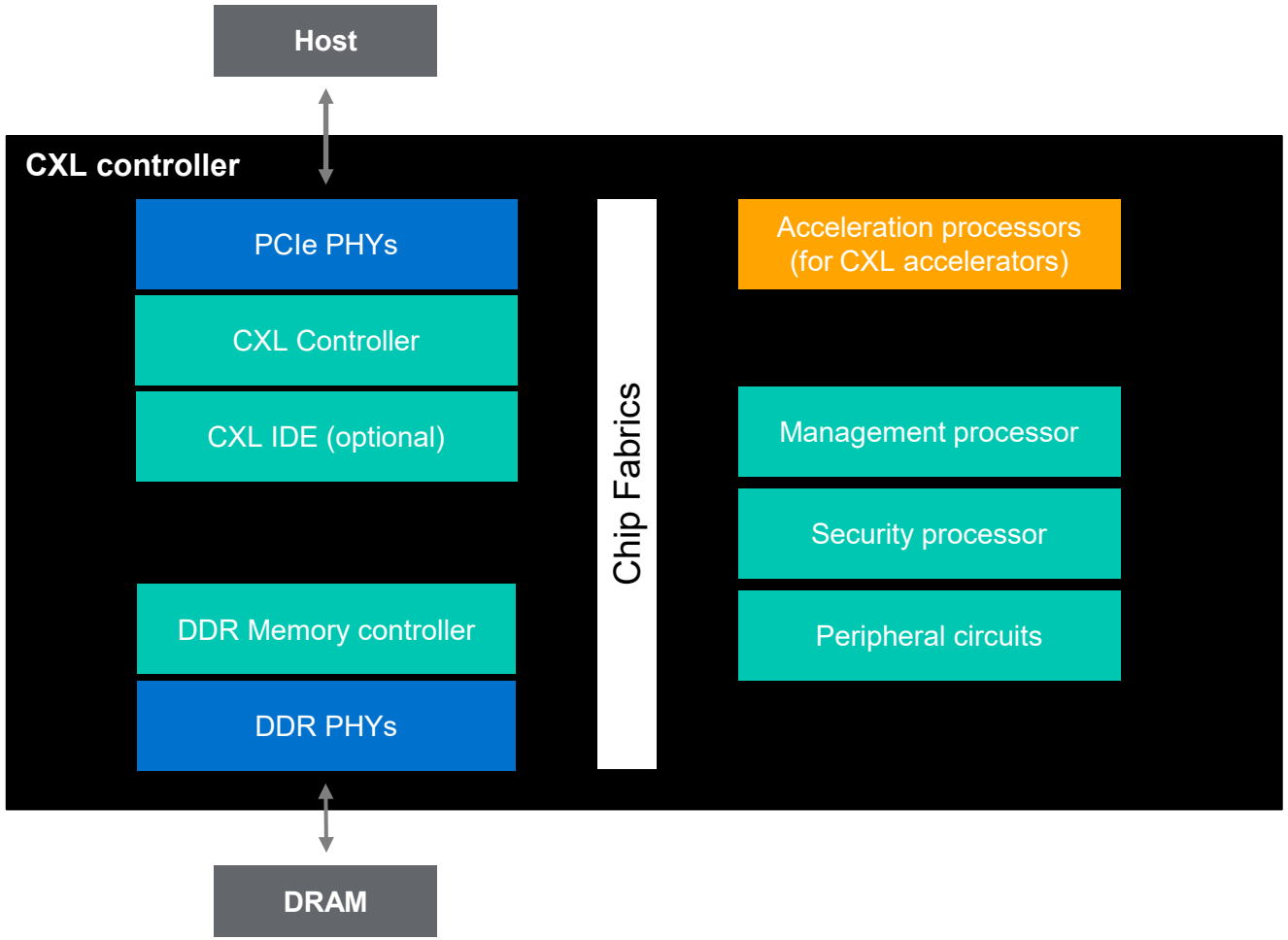
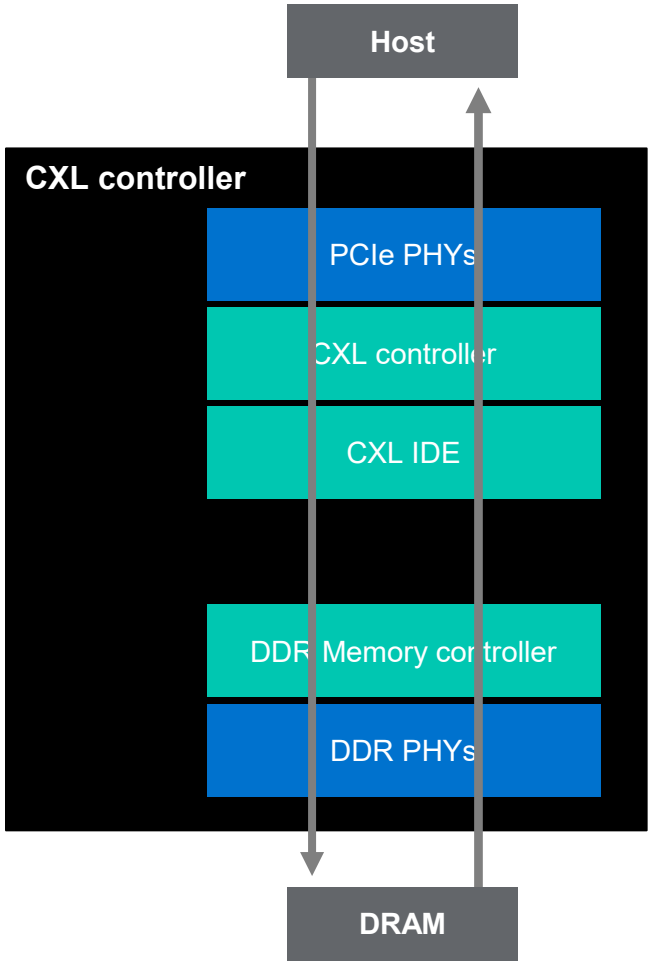
CXL controller architecture



- Acceleration processors not needed for memory expansion only
- CXL integrity and data encryption (IDE) is optional feature

CXL controller latency

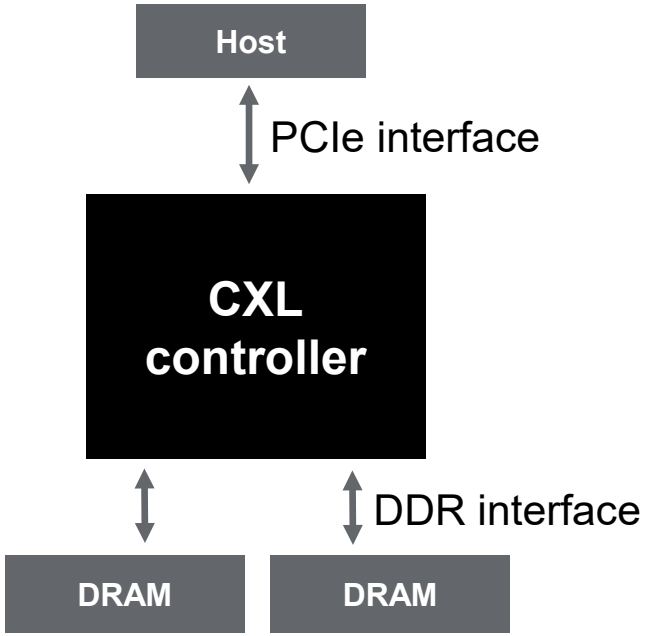


Component latency targets

- Memory Read: 80ns
- Memory Write: 40ns

- Analog and digital data path needs to be optimized to reduce controller latency
- Optional security features such as IDE security and data encryption add additional latency

CXL controller bandwidth



- **CXL controller BW should be matched to DDR and host BW**
- **Host BW depends on**
  - PCIe link speed (Gen4, Gen5, Gen6)
  - Number of PCI lanes (x4, x8, x16)
- **DDR BW depends on**
  - Number of DDR channels
  - DDR channel width
  - DDR channel speed

Important features

Security	Data protection	RAS	Telemetry
▪ CXL link integrity and data encryption (IDE) ▪ FIPS ▪ Secure boot ▪ Authentication ▪ Key management	▪ End-to-end data path ▪ Memories	▪ Error detection, correction, reporting and injection ▪ Data poisoning ▪ Viral handling ▪ Reset	▪ QoS Telemetry ▪ Load indication ▪ Throttling ▪ QoS classes

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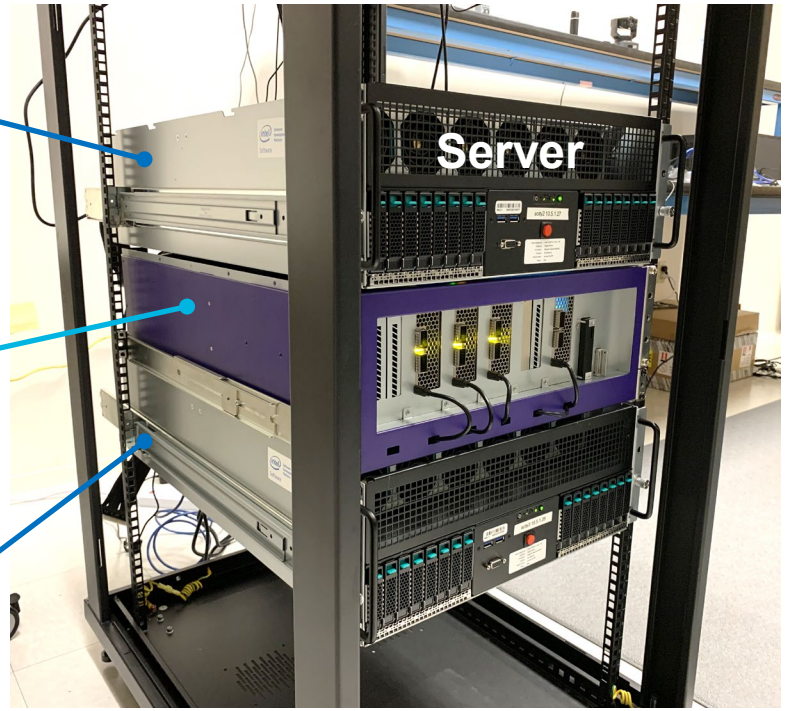
Memory Appliance

- Up to 6 memory devices (3 installed)
- Up to 2 E3s memory cards

Intel Archer City Sapphire Rapid Hosts



Memory pooling demo chassis

Summary

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1. CXL memory expanders improve performance and capacity of memory in the data center
2. Acceleration can be added to CXL memory expanders
3. It is critical to optimize analog and digital data paths in CXL controllers for low data path latency

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