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Alternative for NAND Flash Innovation

Flash Memory Summit 2022

Presenter

Andy Hsu | Founder and CEO

Andy has more than 25 years of experience in the semiconductor industry including positions as VP of Engineering and leader of R&D and engineering teams. He is an accomplished technology visionary and inventor of more than 120 granted U.S. patents.

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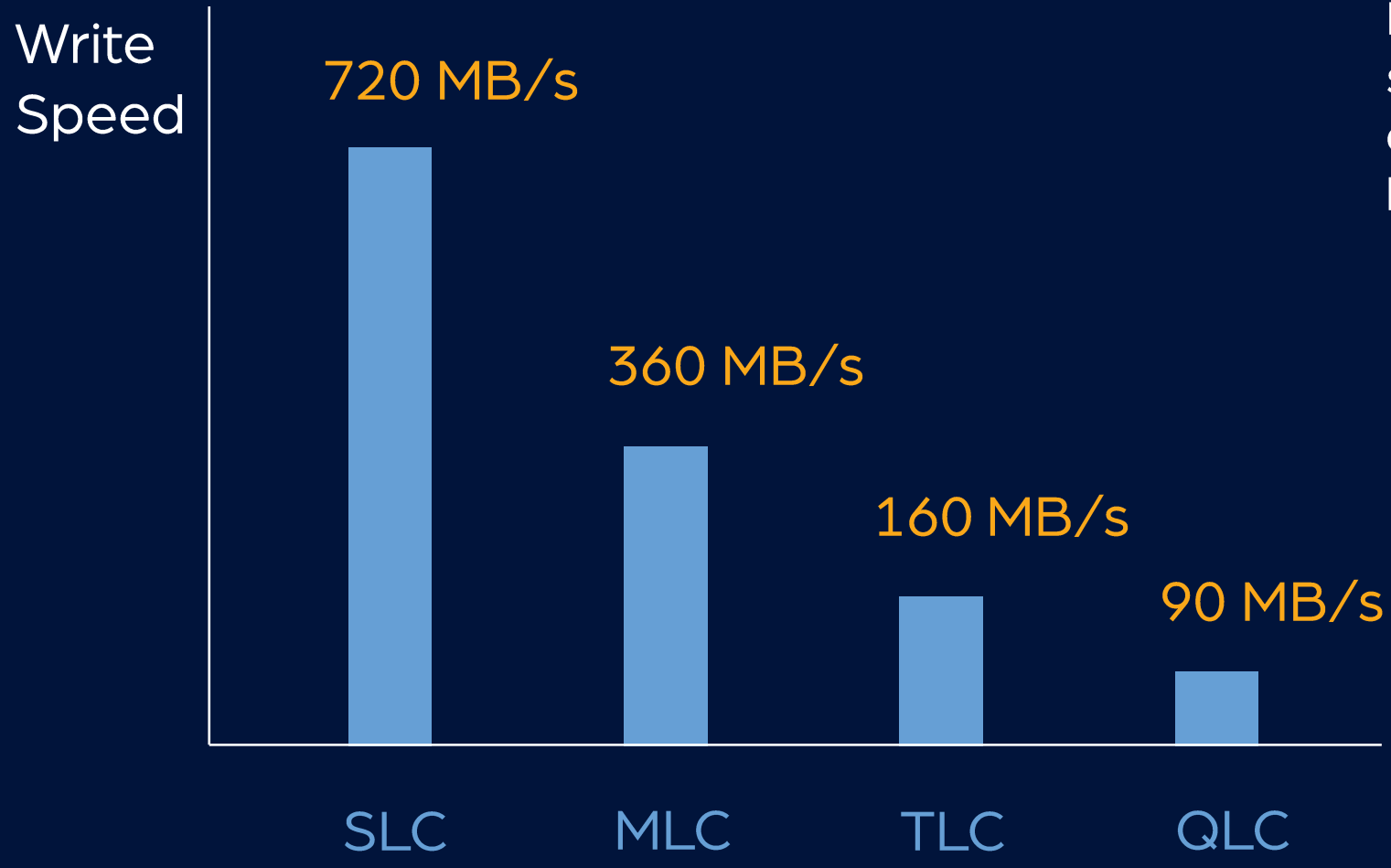
Each Generation's Speed Became Slower



Each generation's write speed becomes 2X slower due to a doubling of Vt levels needing verification.

* Vt – Threshold Voltage

Next Gen Memory Architecture

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X-NAND™

0%
Die Size Increase

3X
Random R/W Speed

Gen1
10X
Sequential Write Speed

Gen2
20X
Sequential Write Speed

* Based on simulation

Page Buffer Architecture

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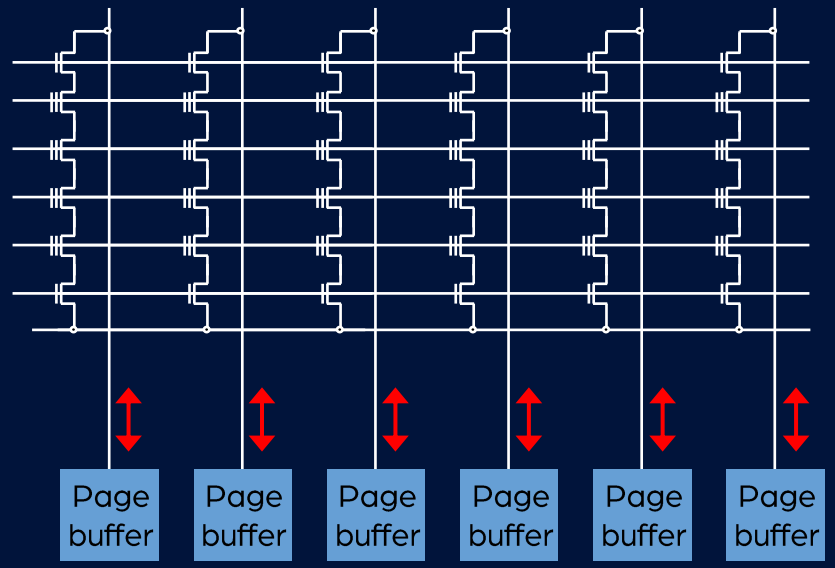
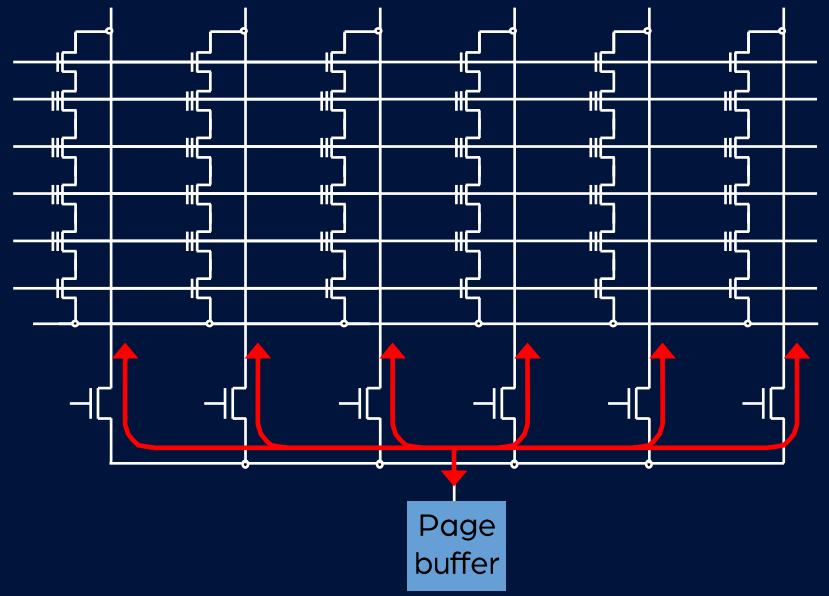
Conventional NAND



One page buffer to read and write data to one bit line (BL).

X-NAND



Shared page buffer to multiple bit lines and reduced layout size.

Bit Line Architecture

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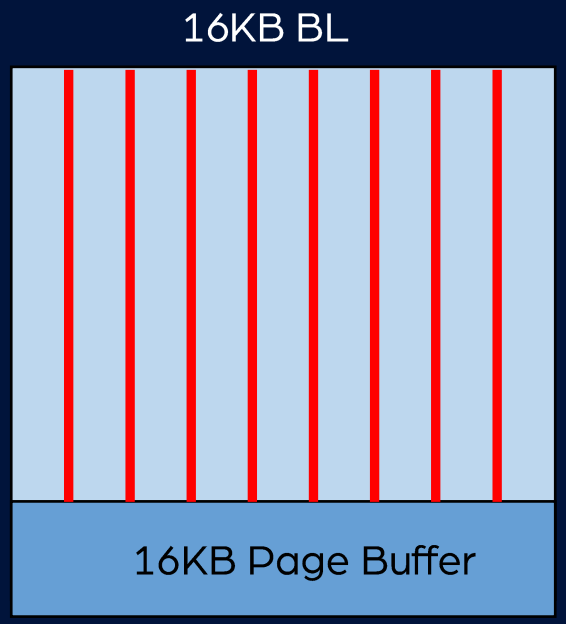
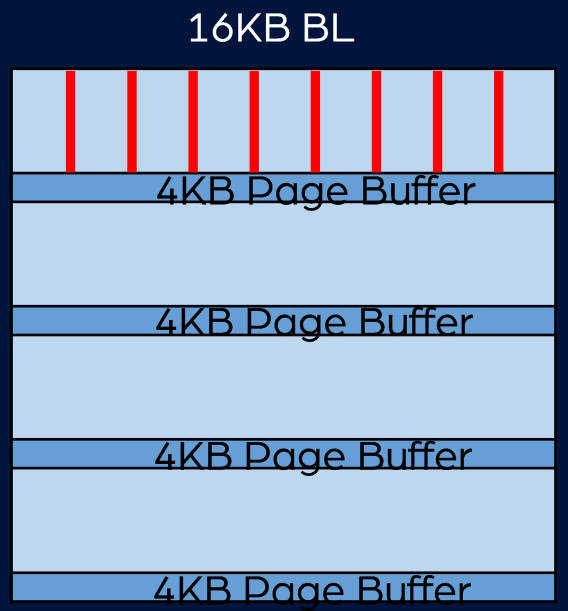
Conventional NAND



Full BL length

1 plane

X-NAND



1/4 BL length

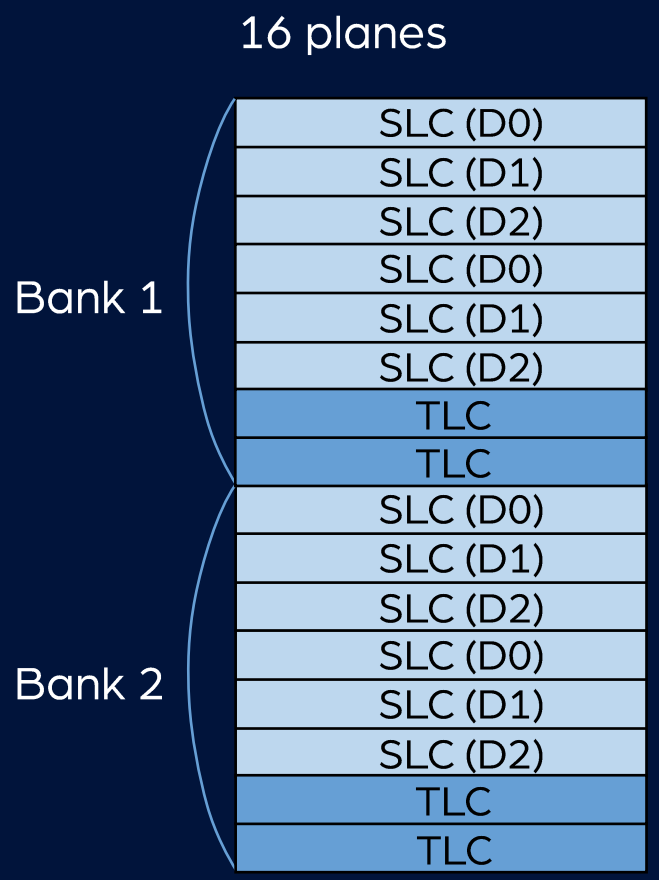
4 planes

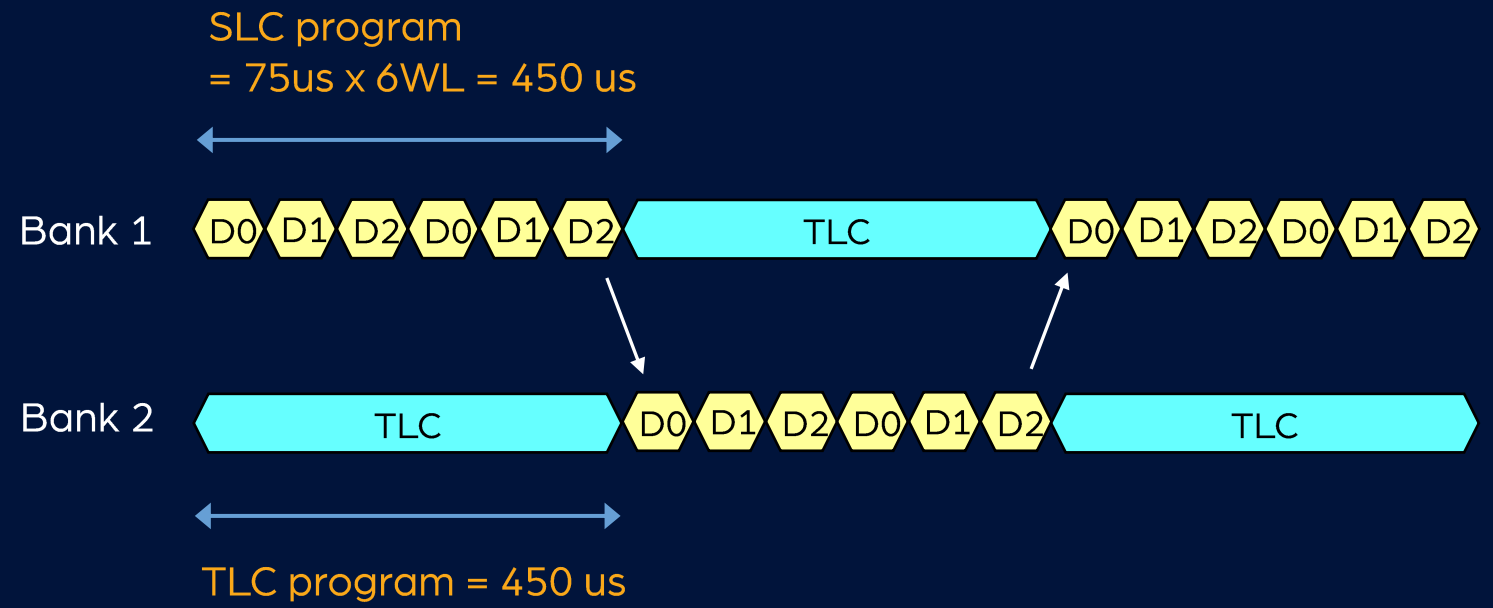
1/4
BL Delay

4X
Parallelism

Shorter bit lines and more planes without increasing die size.

SLC/TLC Parallel-Programming



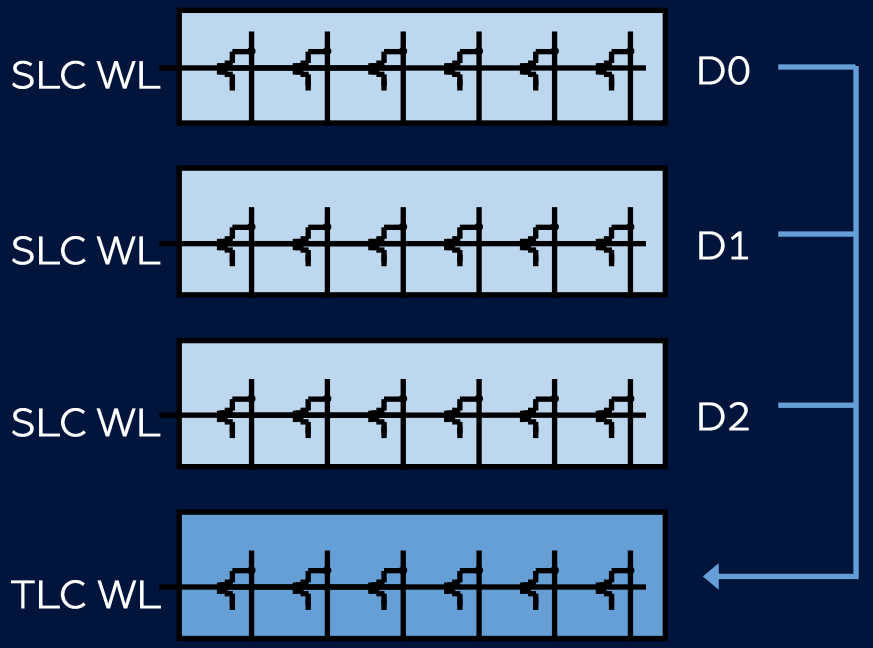


Data can be continuously programmed into TLC cells using SLC speed !

X-NAND Gen 1 vs. Gen 2

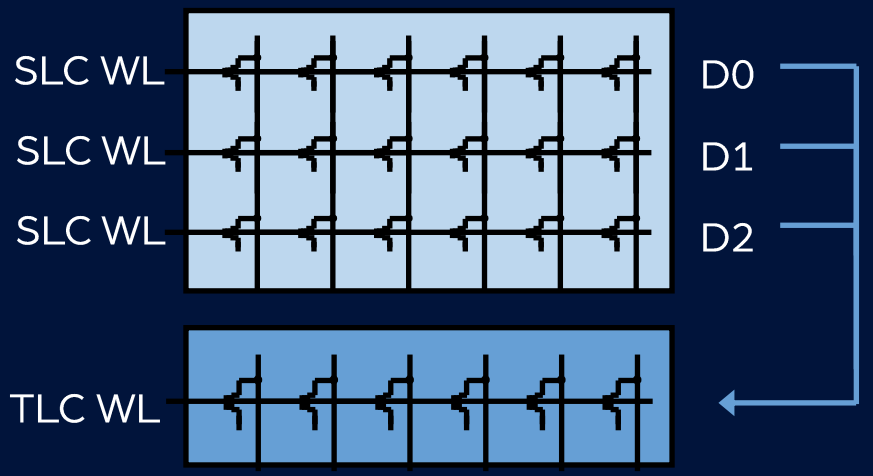
X-NAND Gen1

4 planes



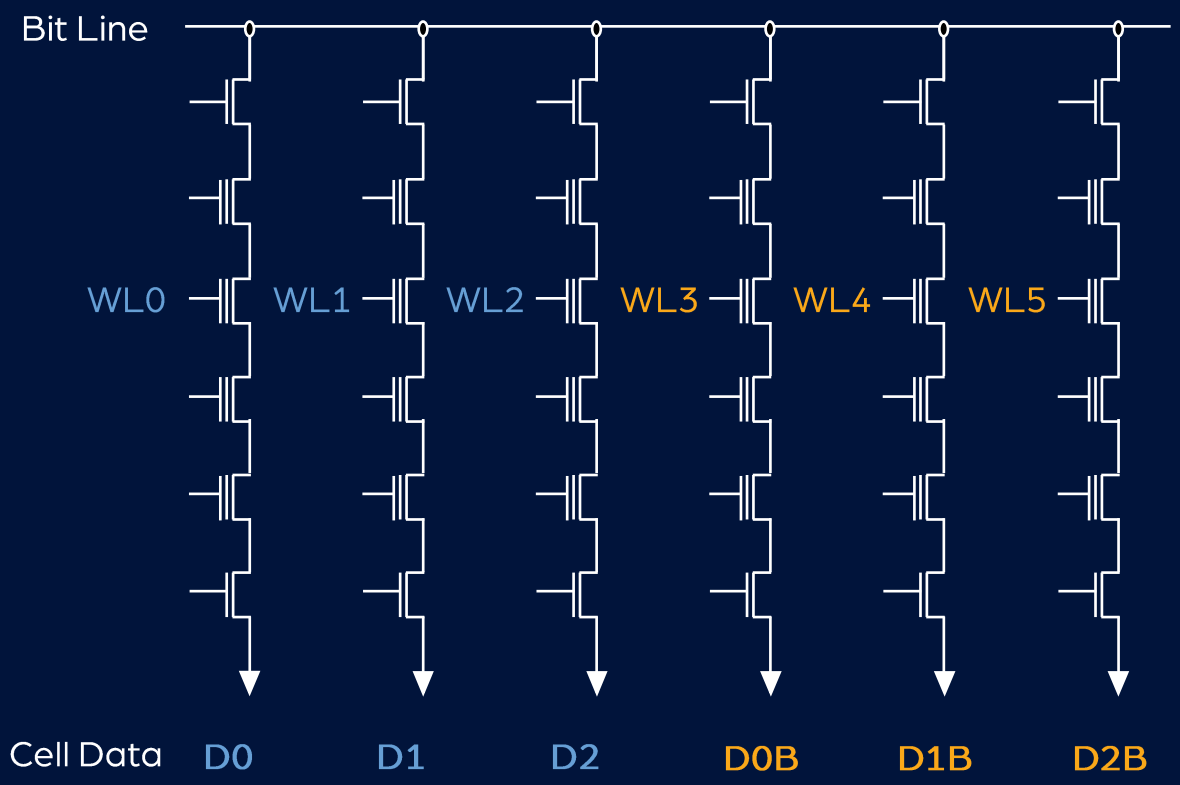
X-NAND Gen2

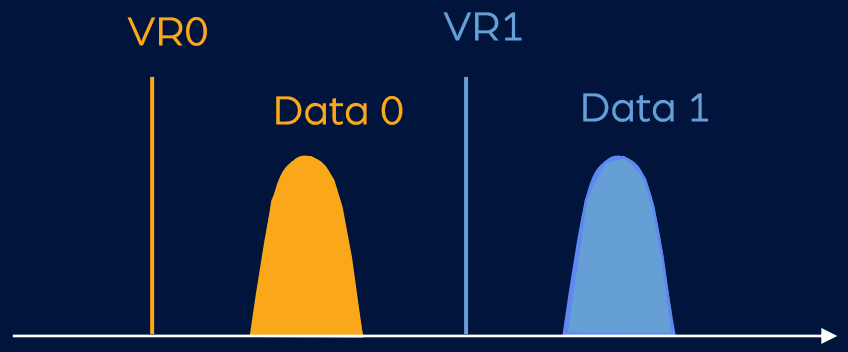
2 planes



2X Program Throughput

Data-Match Verification (DMV)

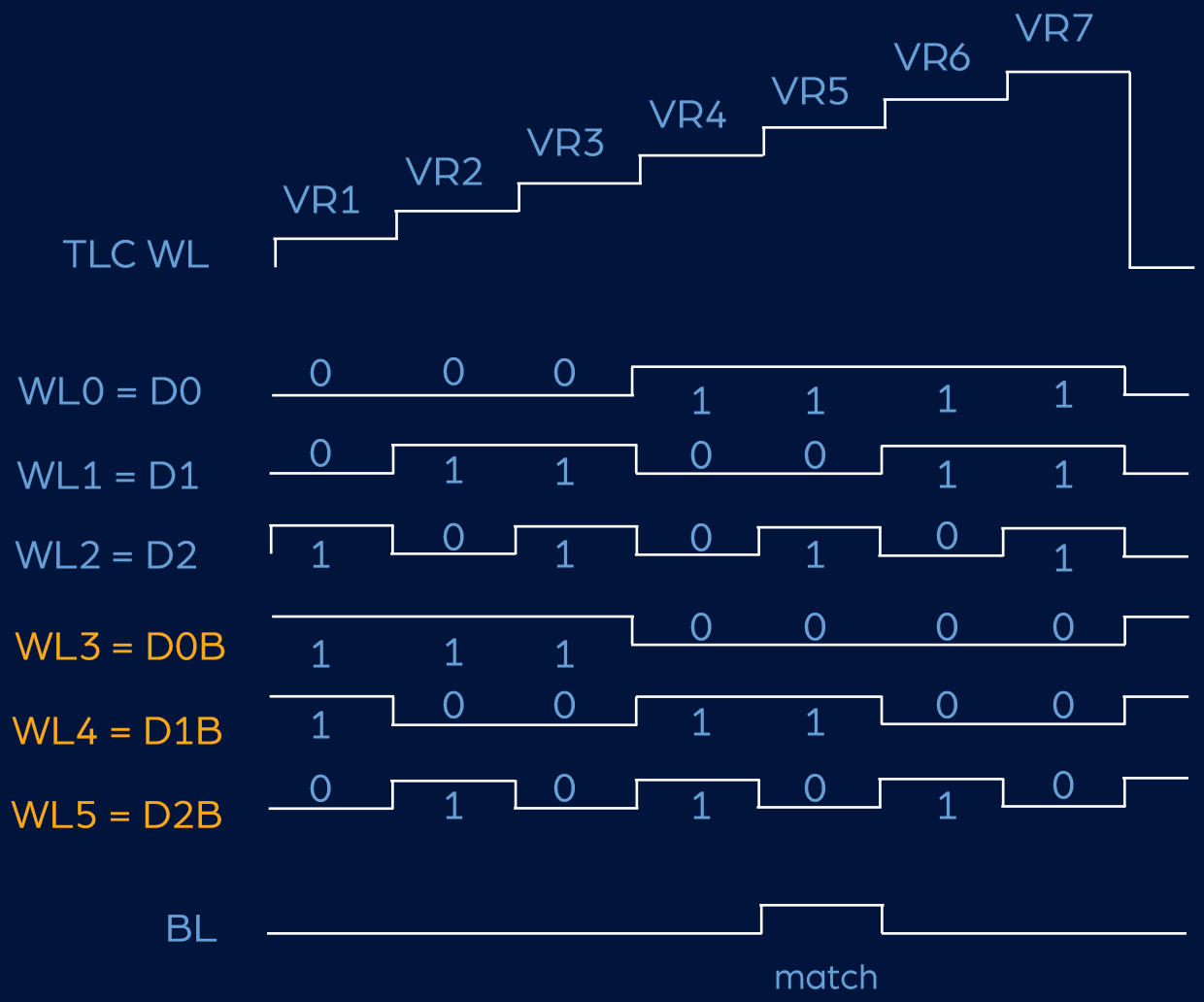




Cell = off when data is matched

X-NAND Gen2 uses a special DMV operation to match the data stored in three SLC word lines in one plane.

Data-Match Verification (DMV)



The SLC word lines are applied with sequential data from 000 to 111 to match the data stored in the cells.

TLC Program Throughput

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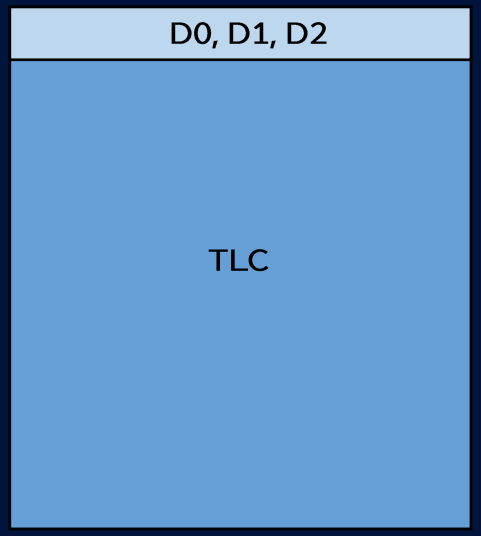
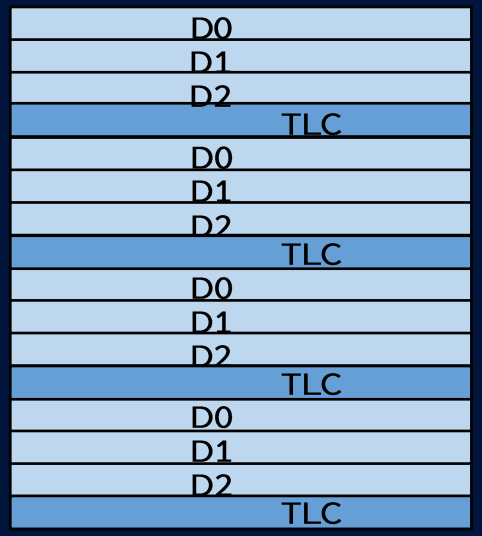
NAND
160MB/s

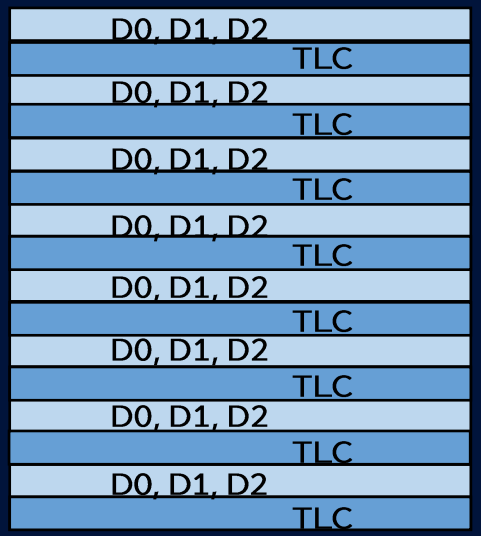


X-NAND Gen1
1.6GB/s



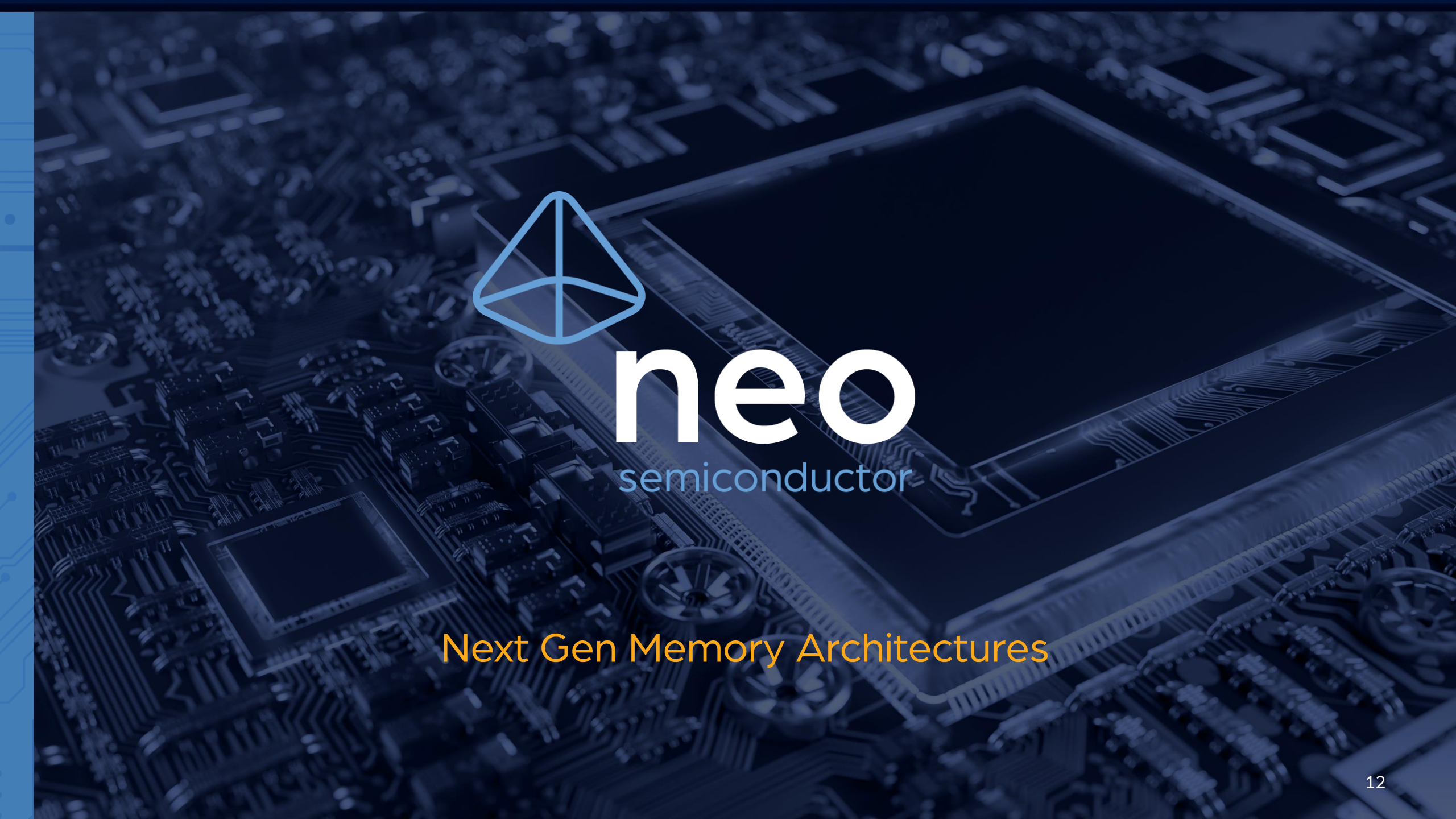
10X

X-NAND Gen2
3.2GB/s



20X

* Based on simulation



Next Gen Memory Architectures