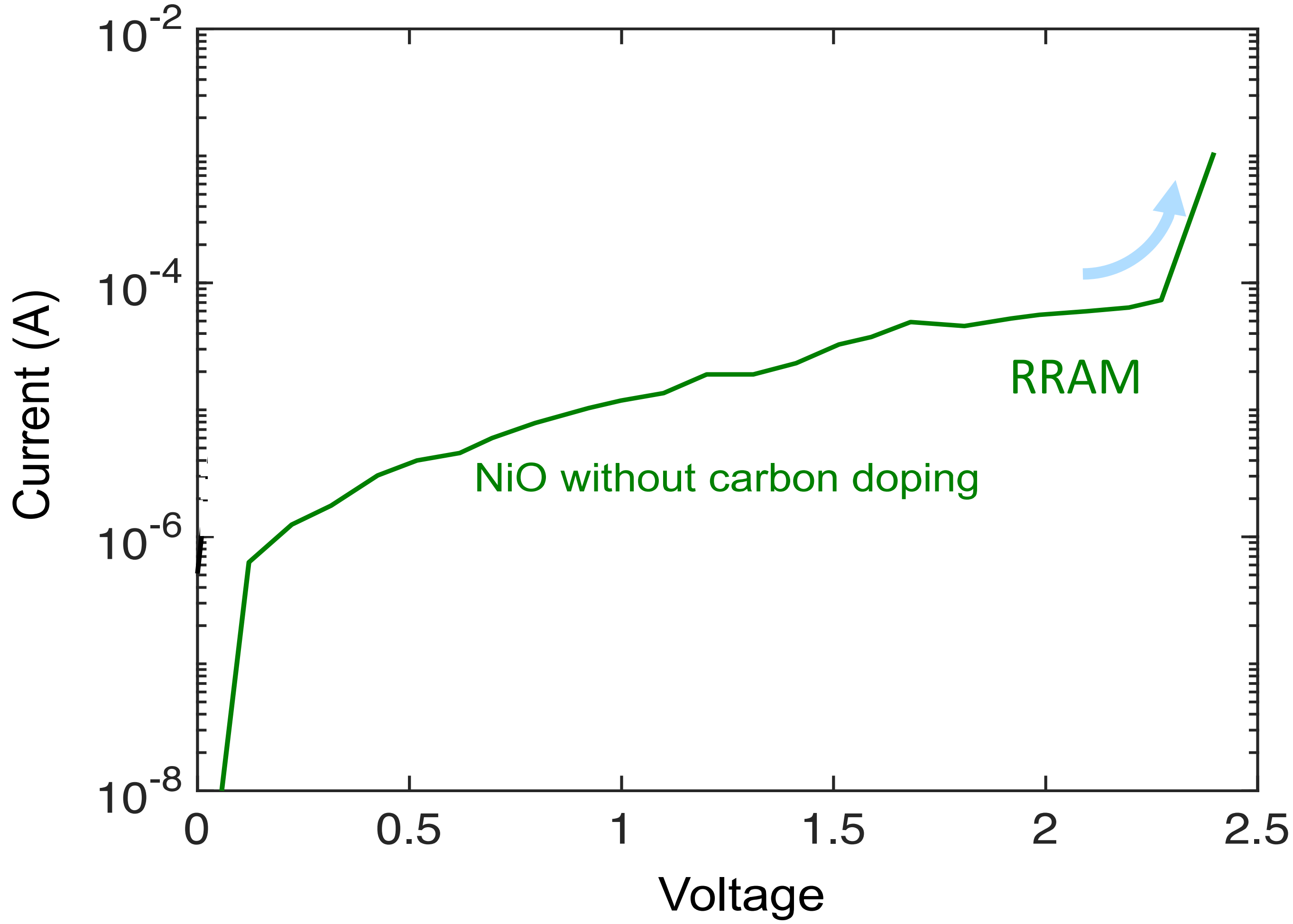
CeRAM:
A Scalable, Fast, Low-power, Extreme Temperature NVM

Greg Yeric, CTO
Cerfe Labs

Greg.Yeric@cerfelabs.com
www.cerfelabs.com

 ©2022 Flash Memory Summit. All Rights Reserved.

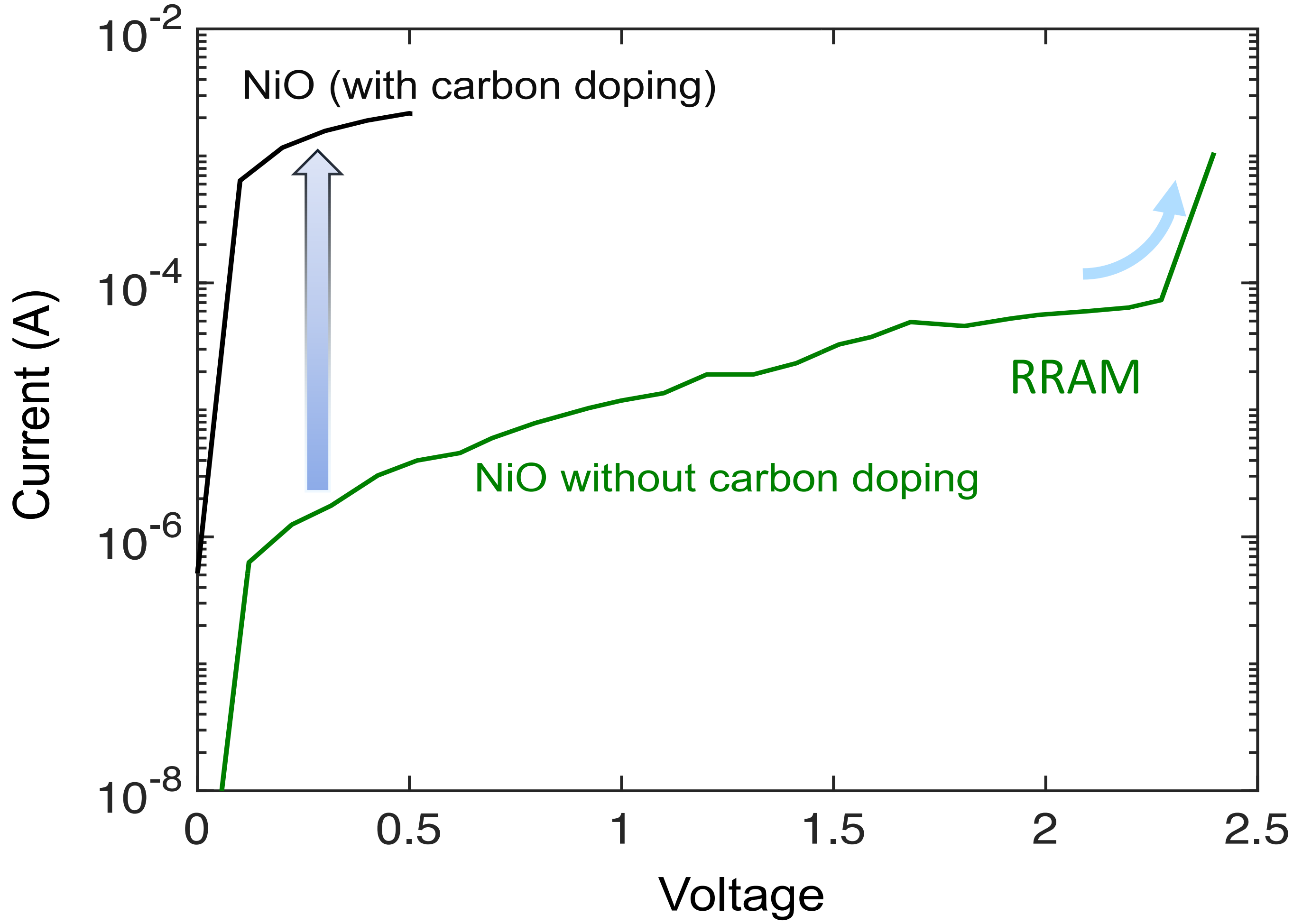
Start with: Nickel Oxide



NiO is insulating, but with a forming voltage it can be transitioned to a conductor and this transition can be reversed with negative bias: ReRAM

 ©2022 Flash Memory Summit. All Rights Reserved.

Now add carbon doping

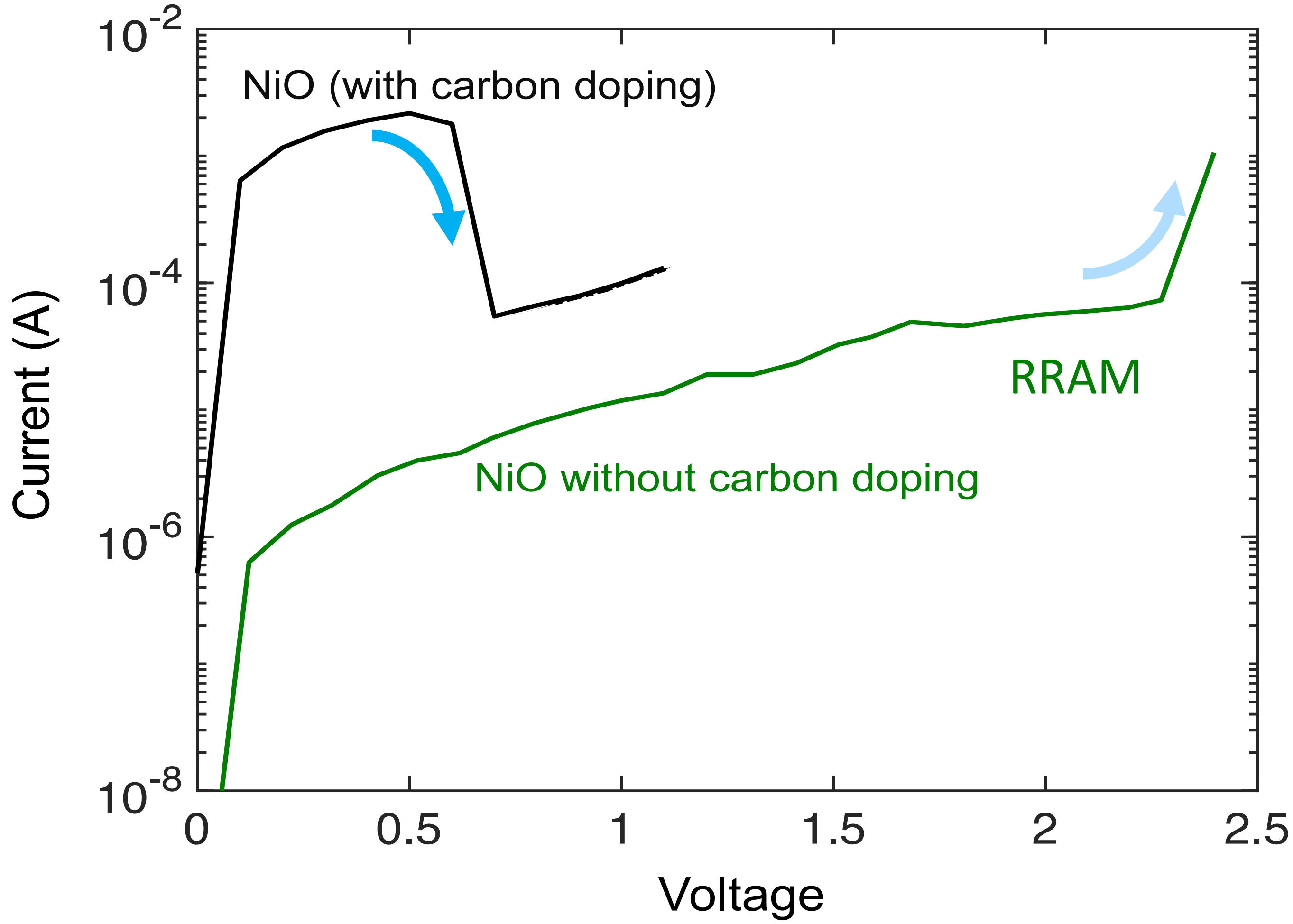


With carbon doping, the NiO is initially conductive: “born on”

NiO is insulating, but with a forming voltage it can be transitioned to a conductor and this transition can be reversed with negative bias: RRAM

 ©2022 Flash Memory Summit. All Rights Reserved.

Now add carbon doping



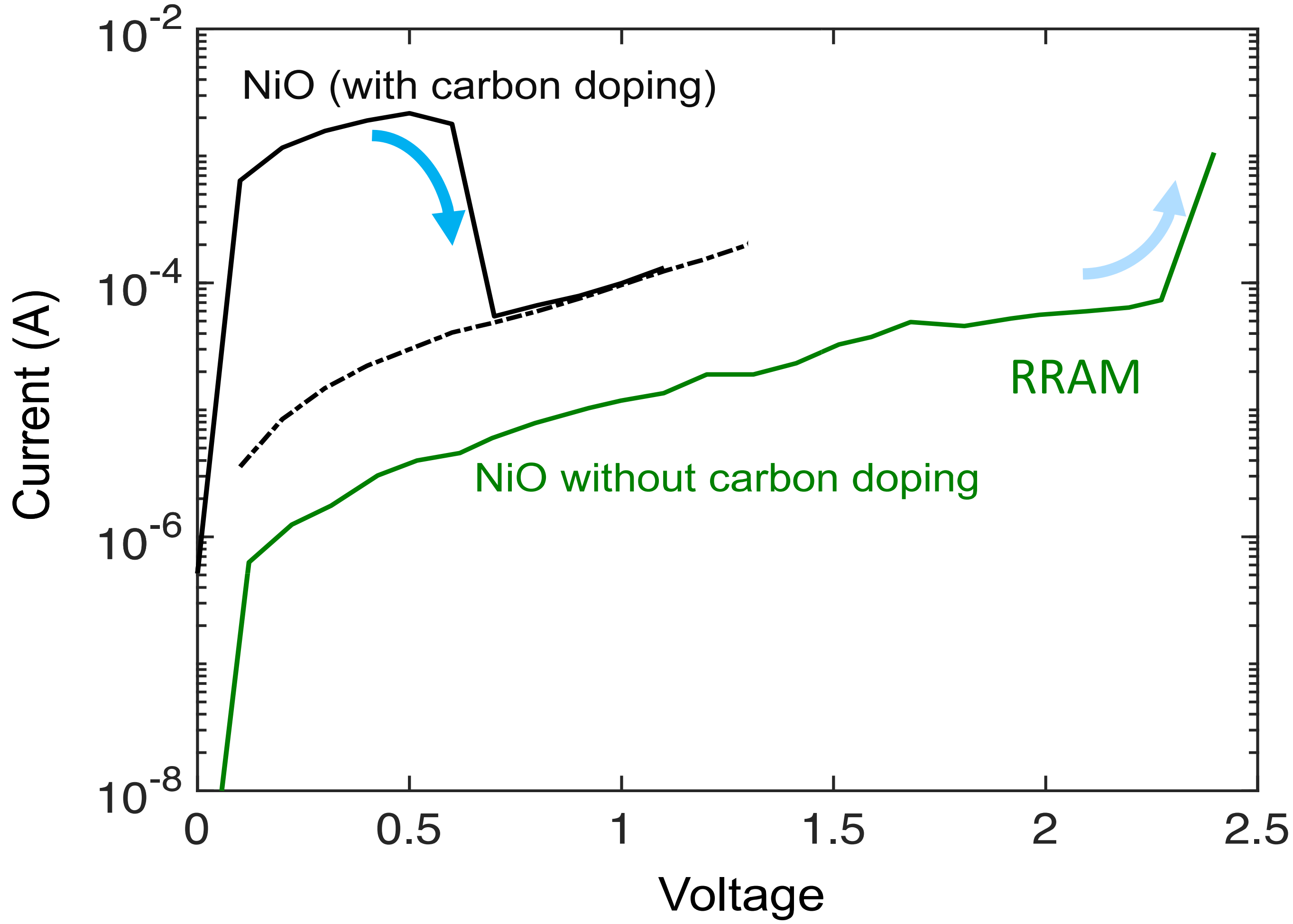
With carbon doping, the NiO is initially conductive: “born on”

Sub-1V transition to non-volatile HRS

NiO is insulating, but with a forming voltage it can be transitioned to a conductor and this transition can be reversed with negative bias: RRAM

 ©2022 Flash Memory Summit. All Rights Reserved.

Now add carbon doping



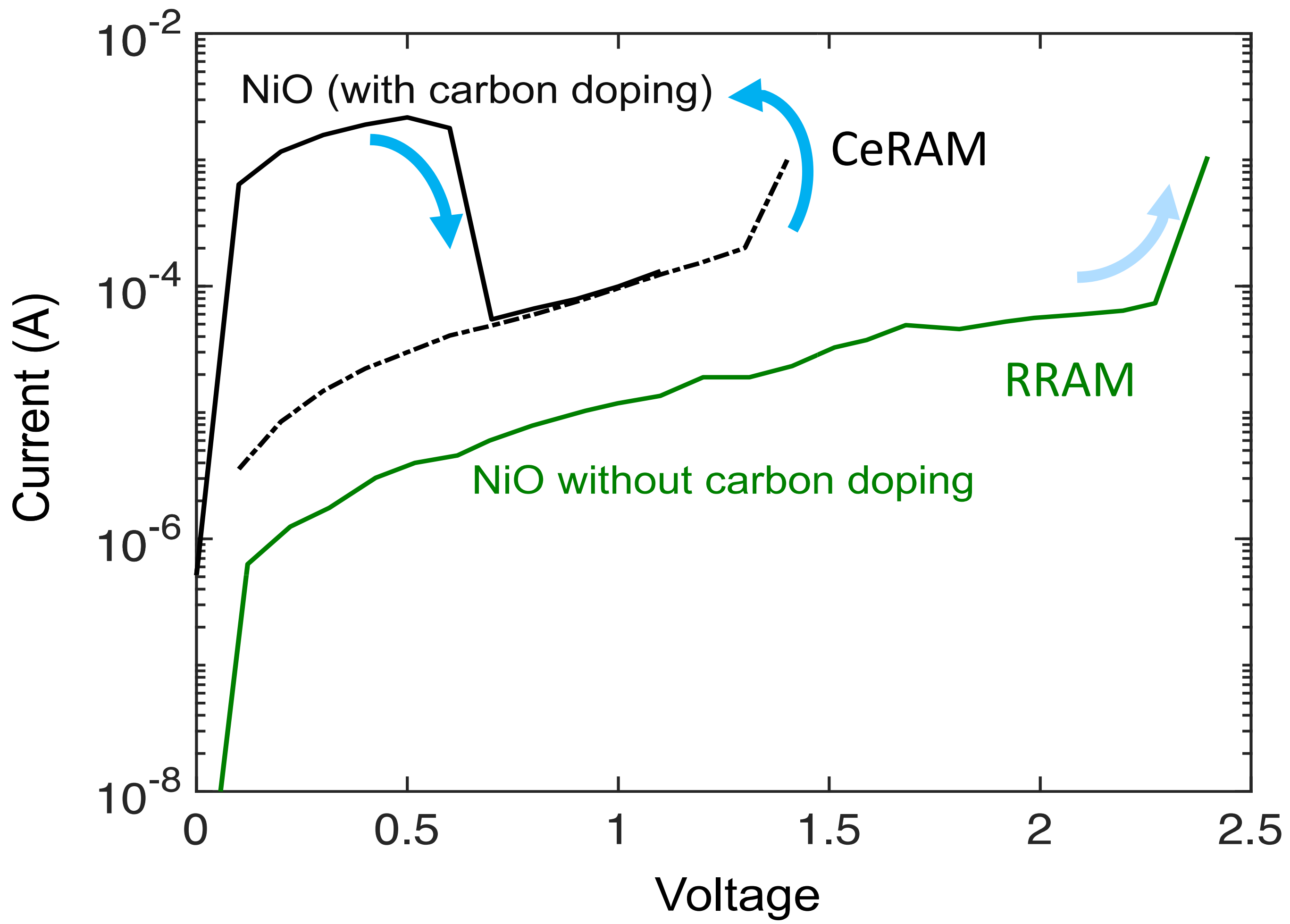
With carbon doping, the NiO is initially conductive

Sub-1V transition to non-volatile HRS

NiO is insulating, but with a forming voltage it can be transitioned to a conductor and this transition can be reversed with negative bias: RRAM

 ©2022 Flash Memory Summit. All Rights Reserved.

Now add carbon doping



With carbon doping, the NiO is initially conductive

Sub-1V transition to non-volatile HRS

The subsequent "Set" transitions at a much lower voltage than filamentary ReRAM forming voltage

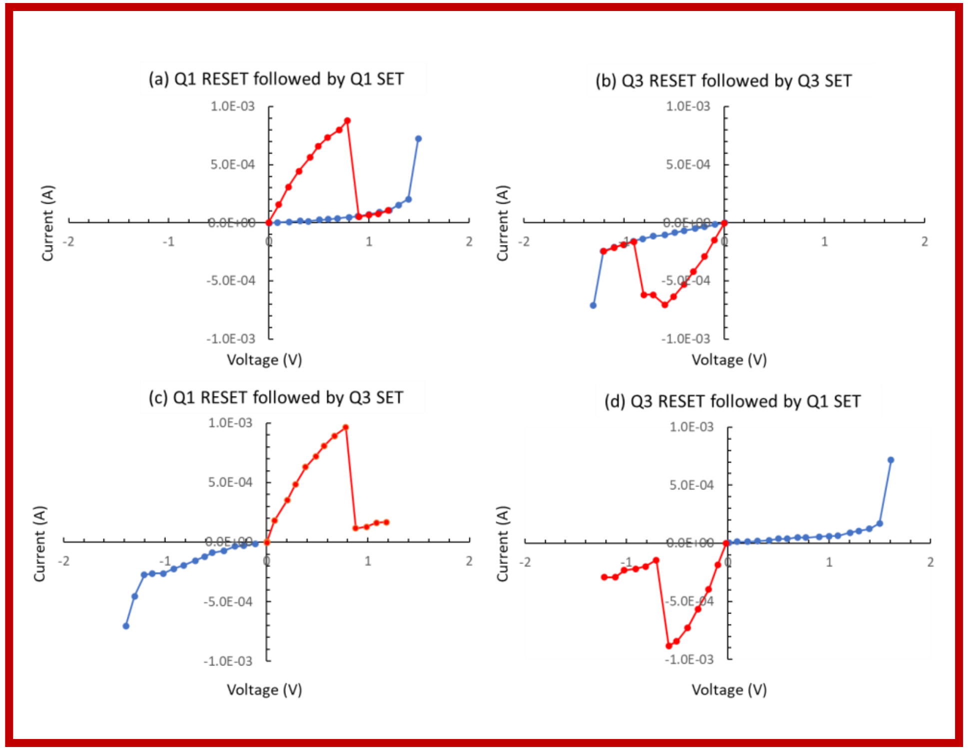
NiO is insulating, but with a forming voltage it can be transitioned to a conductor and this transition can be reversed with negative bias: RRAM

 ©2022 Flash Memory Summit. All Rights Reserved.

Non-polar, low voltage, forming-free, 100x On/Off

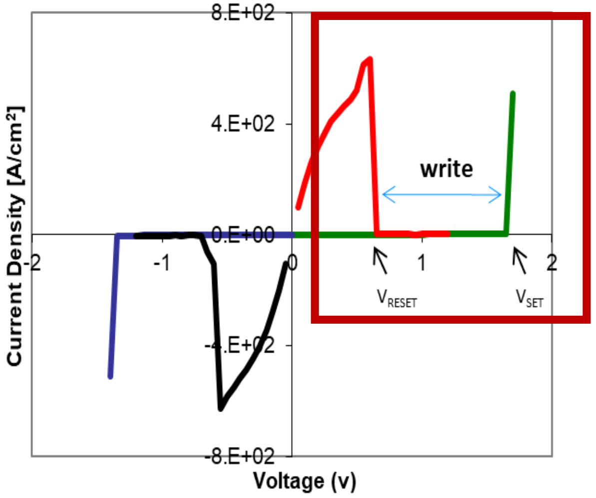
Both SET and RESET states are non-volatile

SET or RESET in any quadrant



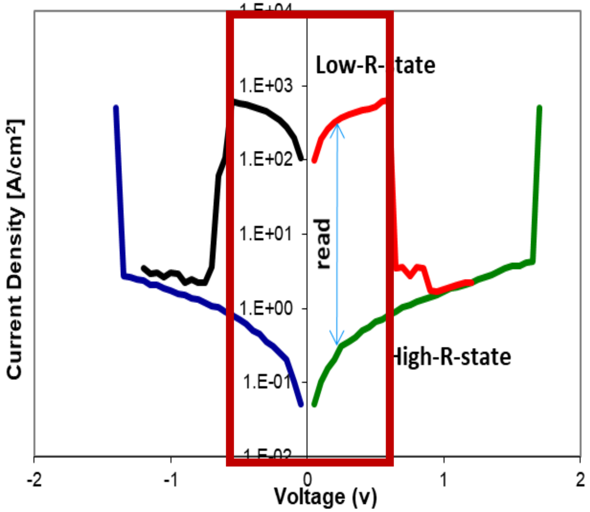
Sharp, deterministic write window

Linear plot



100x read window

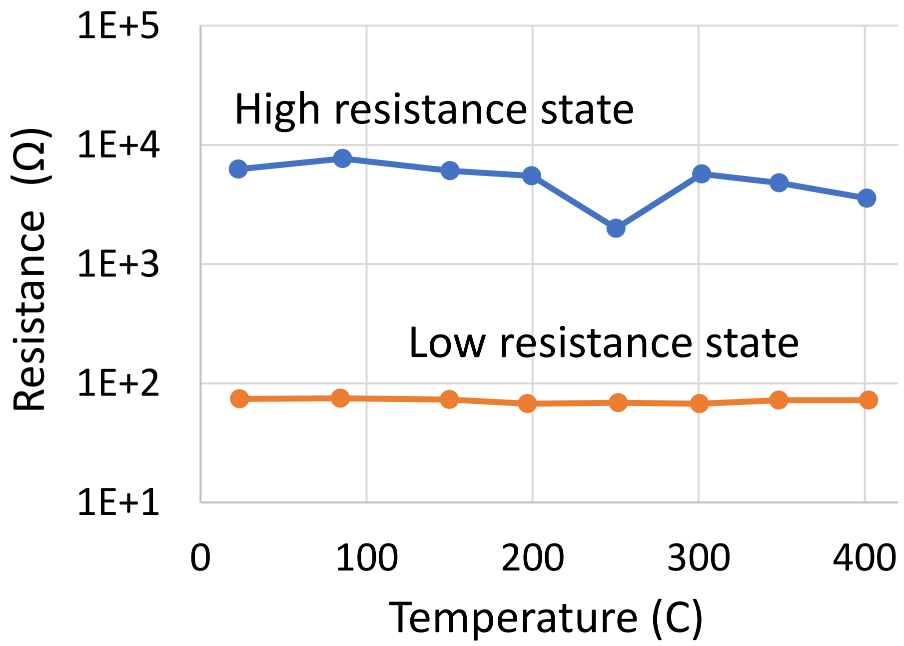
Log-linear

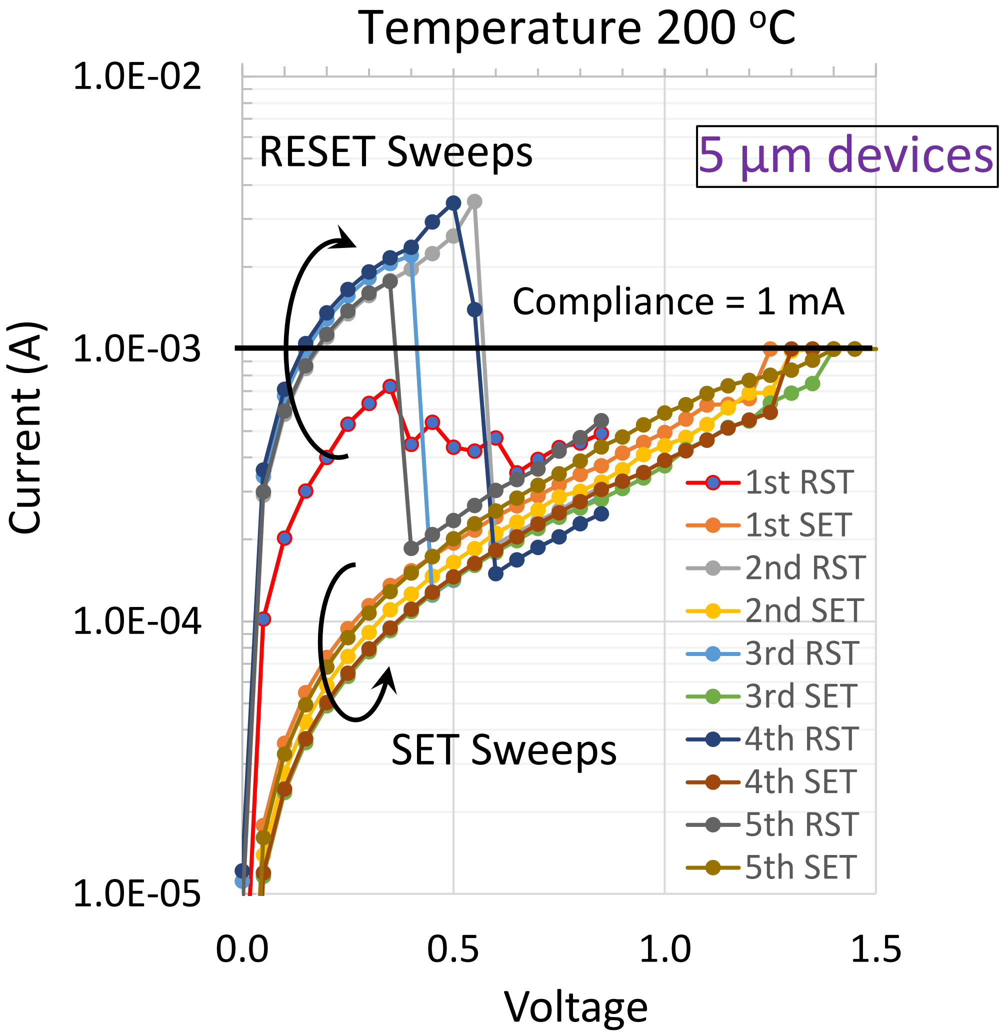


 ©2022 Flash Memory Summit. All Rights Reserved.

Extreme high temperature operation

- Operation demonstrated up to 200 C, work in progress to increase the operation up to 300 C
- Retention bake for one hour up to 400 C



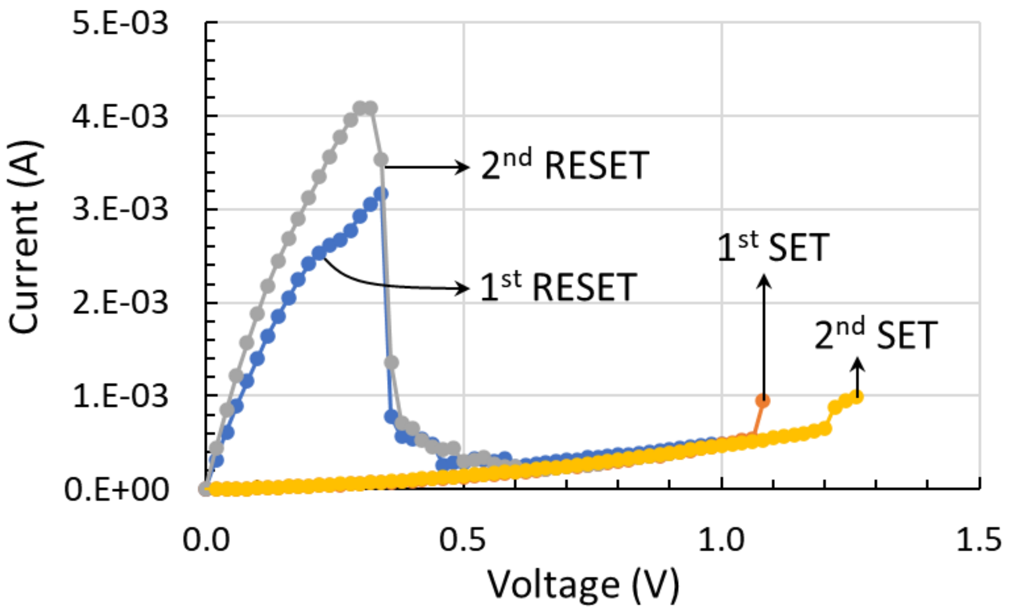


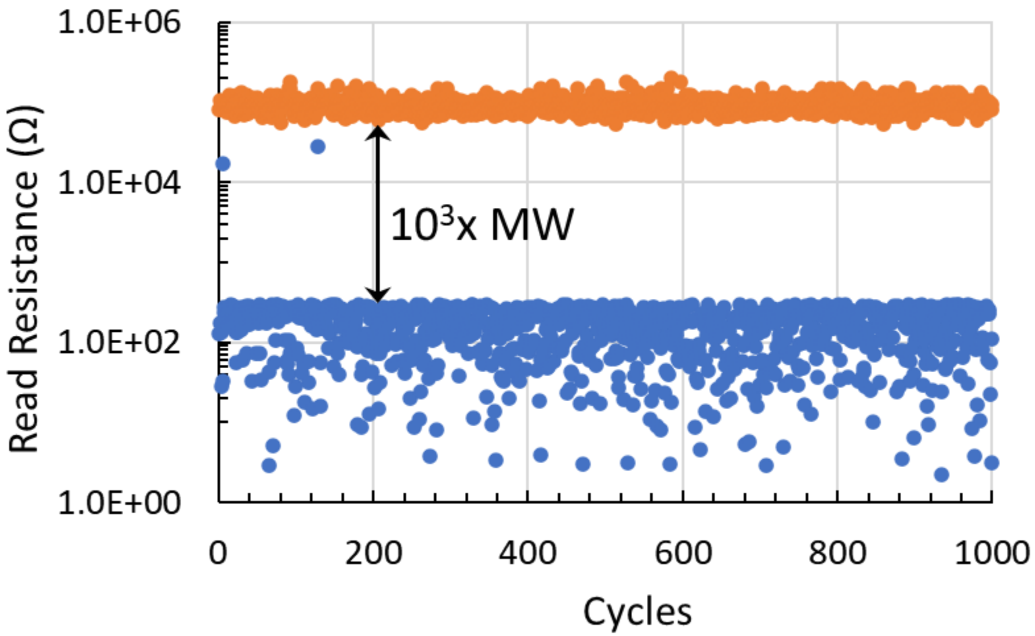
Collaboration: Prof. Chad Young, UT Dallas

©2022 Flash Memory Summit. All Rights Reserved.

Ultra-Cryogenic operation: 870 mK

- These devices are from the same lot as high temperature measurements, no special modifications required
- It is highly unlikely that switching is driven by filaments, traps or defects



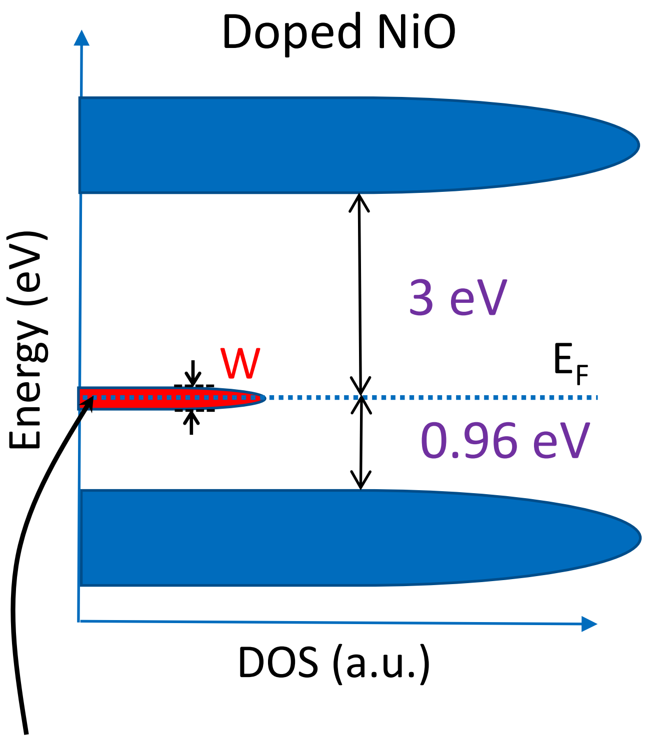


Collaboration: Prof. Daniel Dessau, CU Boulder

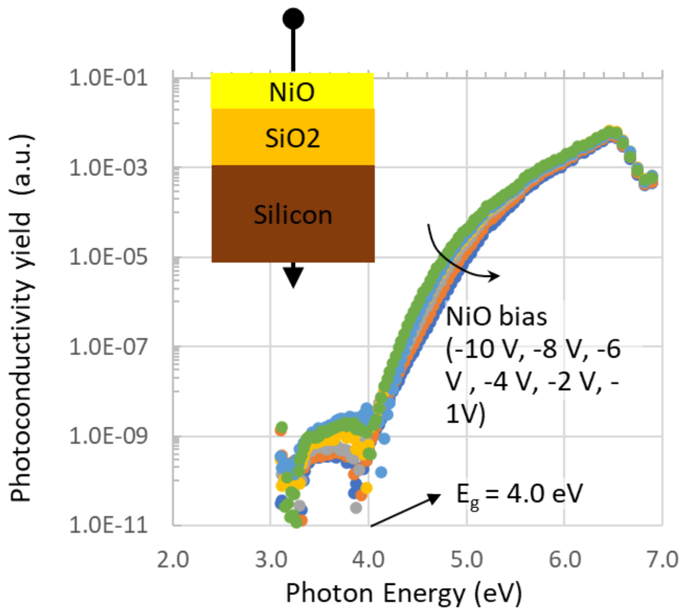
 ©2022 Flash Memory Summit. All Rights Reserved.

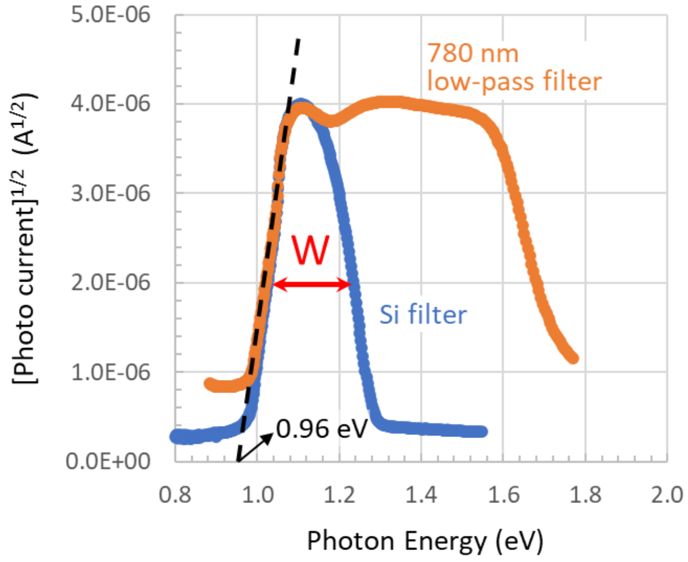
Hypothesis: carbon unlocks correlated electrons

- Undoped NiO is well known Mott material with large band gap (4.0 eV)
- Internal photo emission (IPE) of carbon-doped NiO



Narrow band causing correlation effect



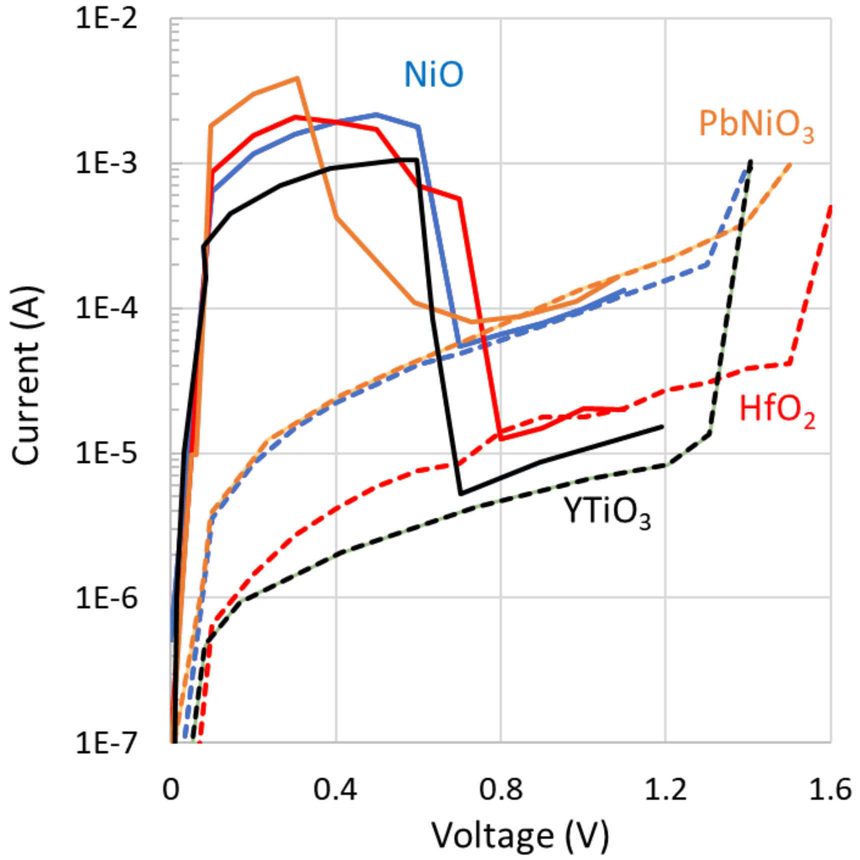


Collaboration: Prof. Valeri Afanasiev, KU Leuven

 ©2022 Flash Memory Summit. All Rights Reserved.

Confirmation of universal effect in TMOs/PTMOs

Flash Memory Summit



CeRAM demonstrated in multiple Transition Metal Oxides and Post-Transition Metal Oxides

Thanks in part to:
DARPA MTO
Electronic Resurgence Initiative
2017-18

©2022 Flash Memory Summit. All Rights Reserved.

Converting promise to product: "lab to fab"

Flash Memory Summit

5 um

bits

70% yield

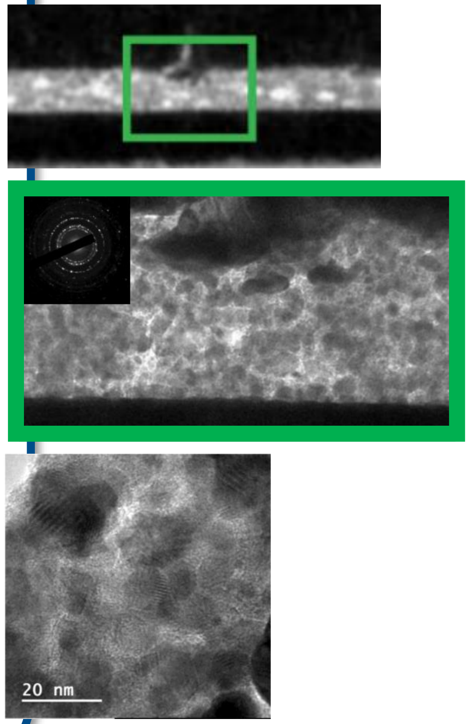
UT DALLAS

KU LEUVEN

Boulder

UBC

UCCS University of Colorado Colorado Springs



Discovery → Product

RRAM: 1967 → 2013

MRAM: 1984 → 2003

- Integration
- Scalability
- Variability
- Reliability

5 nm

Gbits

99.999% yield

KIOXIA

SAMSUNG ELECTRONICS

SK hynix

Western Digital

YANGTZE MEMORY

 ©2022 Flash Memory Summit. All Rights Reserved.

35 YEARS OF INNOVATION

Going from lab to fab:

Flash Memory Summit

5 um
bits
70% yield

UT DALLAS
KU LEUVEN
CU Boulder
UBC
UCCS University of Colorado Colorado Springs

50 nm
kbits
90% yield

imec

Discovery → Product

RRAM: 1967 → 2013
MRAM: 1984 → 2003

Integration
Scalability
Variability
Reliability

5 nm
Gbits
99.999% yield

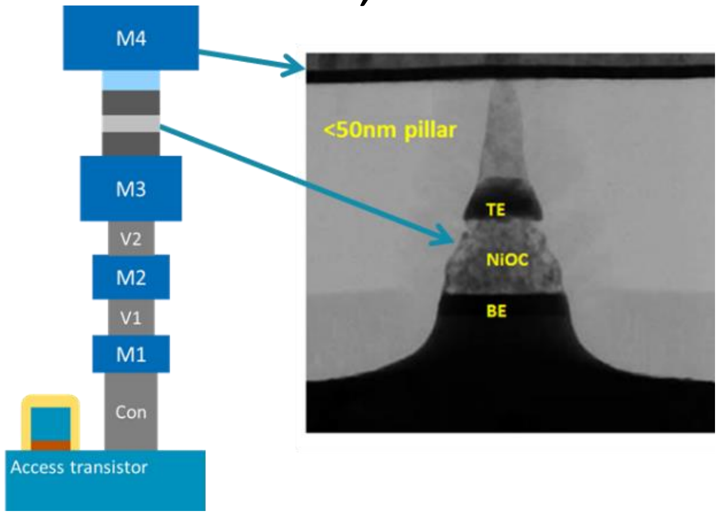
KIOXIA
SAMSUNG ELECTRONICS
SK hynix
Western Digital
YANGTZE MEMORY

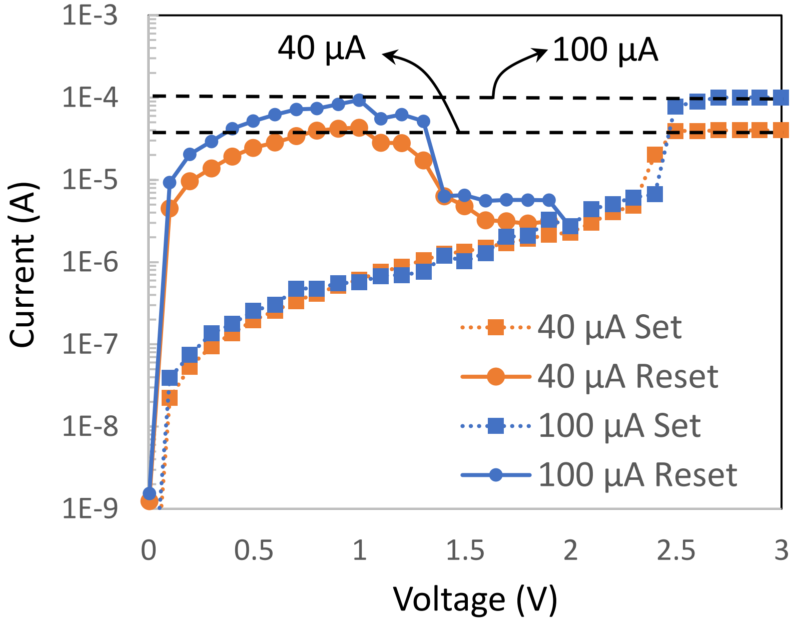
 ©2022 Flash Memory Summit. All Rights Reserved.

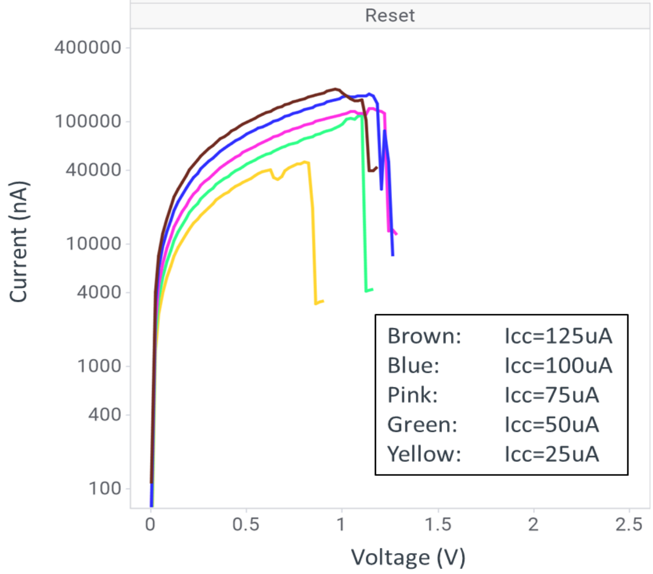
35 YEARS OF INNOVATION

µm to nm / mA to uA

PVD, 47 nm diameter





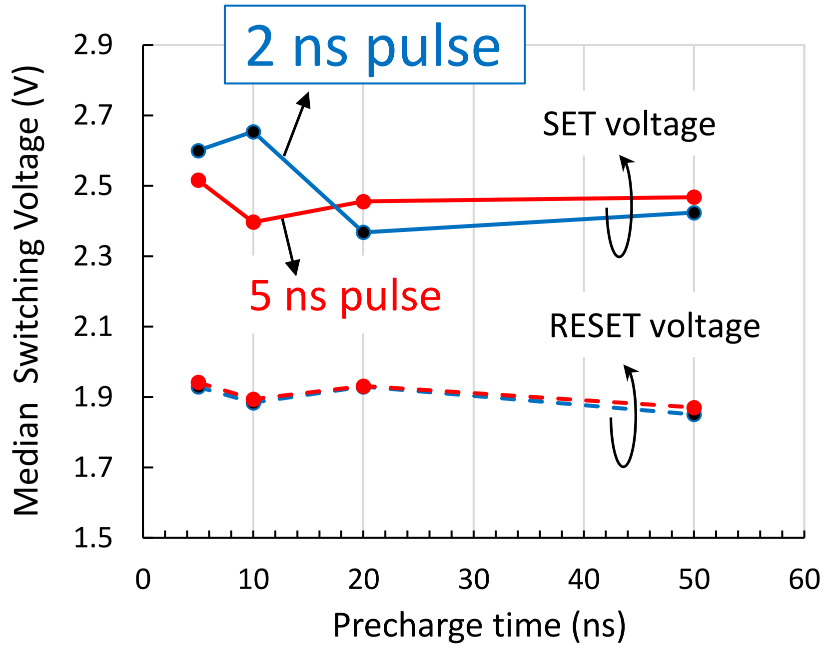


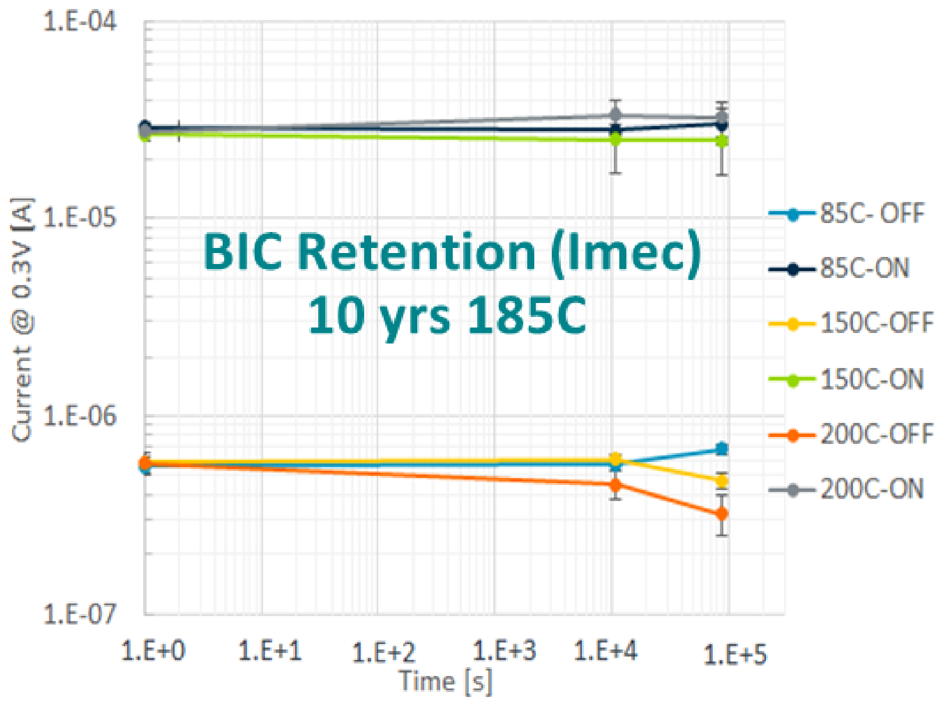
The 47nm devices could be driven by a 2-fin 7nm FinFET, resulting in a 1T1R bitcell area of 0.014µm^2

Same area as projected 2nm SRAM bitcell

 ©2022 Flash Memory Summit. All Rights Reserved.

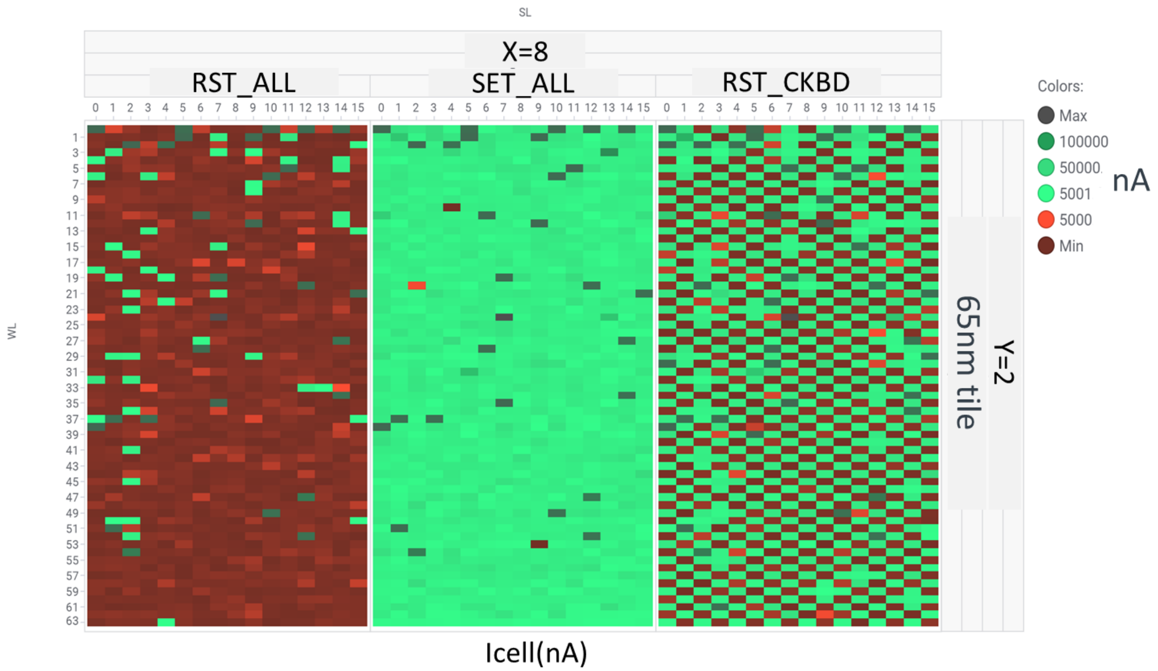
GHz speed, excellent retention

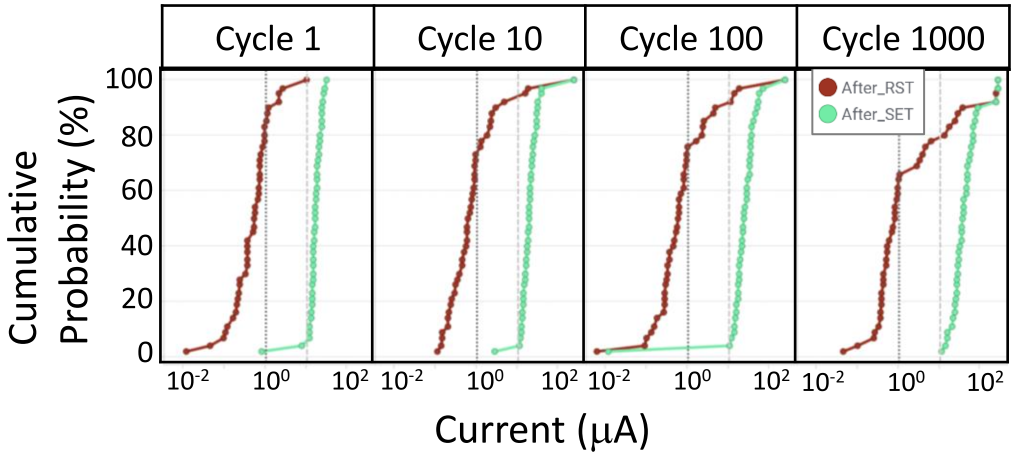




 ©2022 Flash Memory Summit. All Rights Reserved.

90% functional yield on 1kb arrays





■ Insulating current (RESET)

■ Conducting current (SET)

 ©2022 Flash Memory Summit. All Rights Reserved.

Goal: The most universal NVM

	CeRAM
Scalability	<5 nm logic node*
Multi-Level Cell	Yes
Mask Cost	2
Required voltage	< 1.5V
Write speed	< 2nS*
Write energy	< 1 pJ/bit
Access	Byte
Low temp operation	< 0.9 K*
High temp operation	> 200 ºC*
High Temp Retention	185 ºC*
Harsh environment	Immune to radiation
Tamper resistant	MLC, EMP, Rowhammer proof
Endurance (# cycles)	10^4

- Scales to GB
  (with added MLC benefit)
- Scales to low energy
- GHz speed
- Widest temperature range available
- Variety of oxides, deposition techniques, and electrodes can be used

* Improved test chip / test equipment is required to understand the true device limit.

 ©2022 Flash Memory Summit. All Rights Reserved.

Going from lab to fab, via extreme enviroments

Flash Memory Summit

5 um	50 nm	5 nm
bits	kbits	Gbits
70% yield	90% yield	99.999% yield

UT DALLAS

KU LEUVEN

CU Boulder

UBC

UCCS University of Colorado Colorado Springs

imec

Discovery → Product

RRAM: 1967 → 2013
MRAM: 1984 → 2003

- Integration ✓
- Scalability ✓
- Variability
- Reliability

key RRAM limiters

KIOXIA

SAMSUNG ELECTRONICS

SK hynix

Western Digital

YANGTZE MEMORY

 ©2022 Flash Memory Summit. All Rights Reserved.

35 YEARS OF NAND FLASH MEMORY INNOVATION

Going from lab to fab, via extreme enviroments

Flash Memory Summit

5 um	50 nm	5 nm
bits	kbits	Gbits
70% yield	90% yield	99.999% yield

UT DALLAS

KU LEUVEN

CU Boulder

UBC

UCCS University of Colorado Colorado Springs

imec

Discovery → Product

Volume learning

KIOXIA

SAMSUNG ELECTRONICS

SK hynix

Western Digital

YANGTZE MEMORY

 ©2022 Flash Memory Summit. All Rights Reserved.

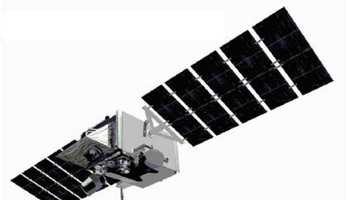
35 YEARS OF INNOVATION

Cerfe Labs have been awarded 6 SBIR grants

DARPA MTO
Electronic Resurgence Initiative
2017-18

AFWERX: (AF/SF)
large devices for adaptable RF

Jet fuel-cooled electronics



Space cryogenic SIGINT / ISR

Ballistic missile electronics

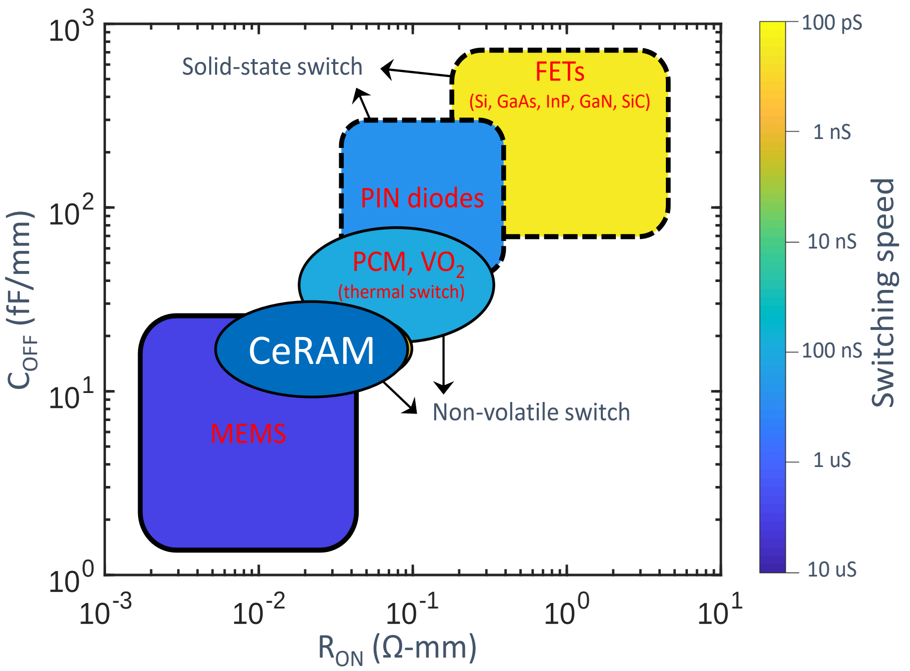
 ©2022 Flash Memory Summit. All Rights Reserved.

Cerfe Labs have been awarded 6 SBIR grants

DARPA MTO
Electronic Resurgence Initiative
2017-18

AFWERX: (AF/SF)
large devices for adaptable RF

Larger, discrete device market



 ©2022 Flash Memory Summit. All Rights Reserved.

Cerfe Labs have been awarded 6 SBIR grants

DARPA MTO
Electronic Resurgence Initiative
2017-18

AFWERX: (AF/SF)
large devices for adaptable RF

1 Mb (50k CLBs), > 100 cycles endurance

CIR CS-22-1301 for Strategic Radiation Hardened Field Programmable Gate Array

Cornerstone Initiative Request (CIR)

For

Strategic Radiation Hardened Field Programmable Gate Array (FPGA)

For

Government Fiscal Year 2022
Cornerstone Initiative Request (CIR) Number: CS-22-1301

Issued by:
Army Contracting Command - Rock Island

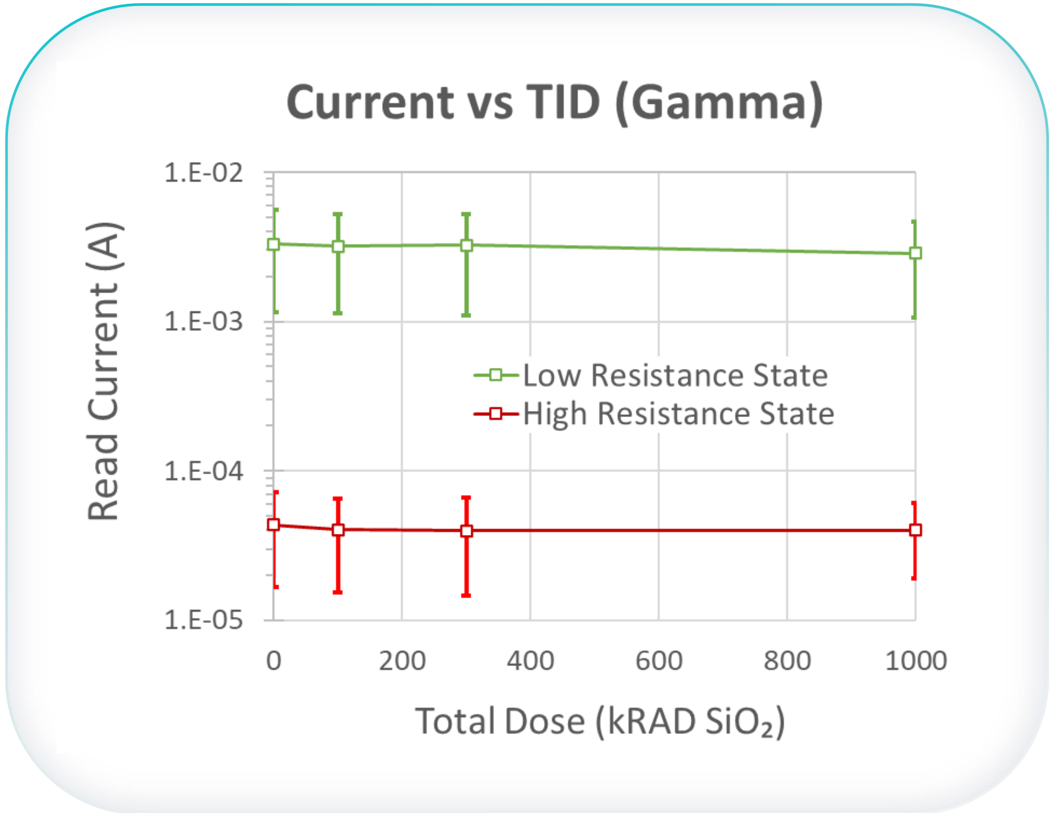
 ©2022 Flash Memory Summit. All Rights Reserved.

Cerfe Labs have been awarded 6 SBIR grants

Flash Memory Summit

DARPA MTO
Electronic Resurgence Initiative
2017-18

AFWERX: (AF/SF)
large devices for adaptable RF



Courtesy Prof. Bharat Bhuva, U. Vanderbilt

 ©2022 Flash Memory Summit. All Rights Reserved.

Cerfe Labs have been awarded 6 SBIR grants

DARPA MTO
Electronic Resurgence Initiative
2017-18

AFWERX: (AF/SF)
large devices for adaptable RF

DoE QIS
(Quantum Information Systems)

VLSI 2022

A 0.31V Vmin Cryogenic SRAM in 14 nm FinFET for Quantum Computing

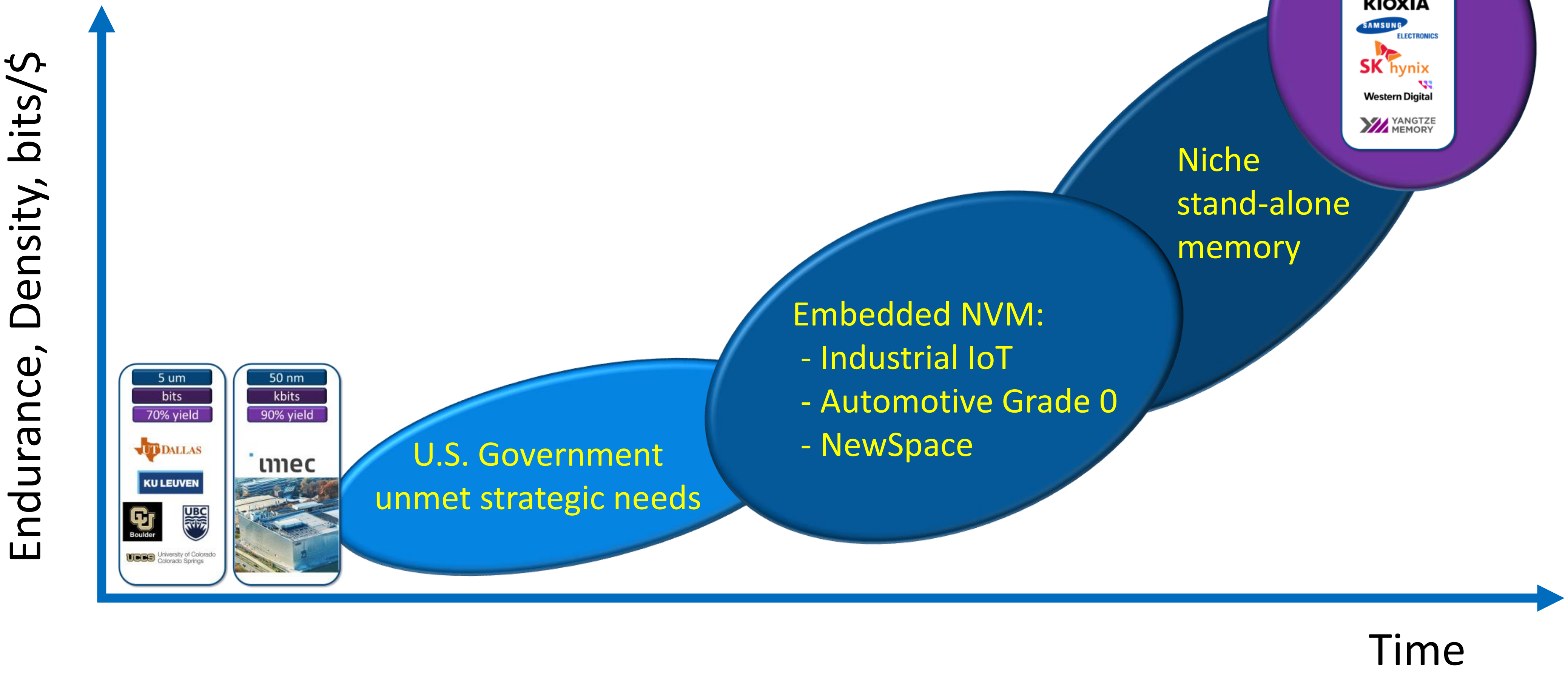
R. Joshi, J. Timmerwilke, K. Tien, M. Yeck, S. Chakraborty
IBM T. J. Watson Research Center, Yorktown Heights, NY 10598
rvjoshi@us.ibm.com

Abstract- A fully functional compile-able 4.1Kb 6T SRAM macro in 14nm FinFET technology targeting low-voltage cryogenic operation with a configurable multi-supply boosting capability with VCSmin of 0.23V (room temperature) and 0.31V (6K) is demonstrated.

technique, which combines boosting with power gating. A unique standard cell inverter-based approach is taken: the basic circuit consists of two opposite polarity FETs in parallel, connected between the fixed external voltage and the virtual supply node, with the PFET acting as header and NFET as the

 ©2022 Flash Memory Summit. All Rights Reserved.

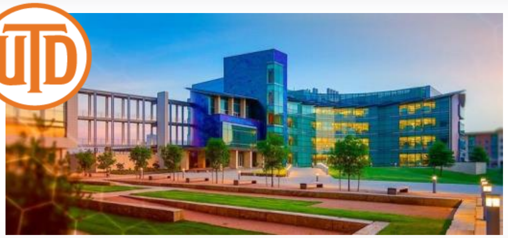
Phases of technology maturity



 ©2022 Flash Memory Summit. All Rights Reserved.

Forward plans

- Trusted commercially relevant prototypes with CeRAM integrated on commercial CMOS



- Materials science researchers and lab
- CeRAM transfer underway

Boulder

- Cryogenics, physics, spectroscopy

- IPE and SCALPEL
- Morphology effects
- Add HfO (PVD)

- Add HfO (ALD)
- Extreme Harsh characterization
- Theory and failure mechanisms
- Sub-20nm scaling
- RF

Open to collaborations

©2022 Flash Memory Summit. All Rights Reserved.

To learn more:

Email: greg.yeric@cerfelabs.com

Website: www.cerfelabs.com

APL Materials

Universal non-polar switching in carbon-doped transition metal oxides (TMOs) and post TMOs

Cite as: APL Mater. 10, 040904 (2022); https://doi.org/10.1063/5.0073513
Submitted: 30 September 2021 • Accepted: 07 April 2022 • Published Online: 27 April 2022

C. A. Paz de Araujo, Jolanta Celinska, Chris R. McWilliams, et al.

COLLECTIONS

Paper published as part of the special topic on Materials Challenges for Nonvolatile Memory

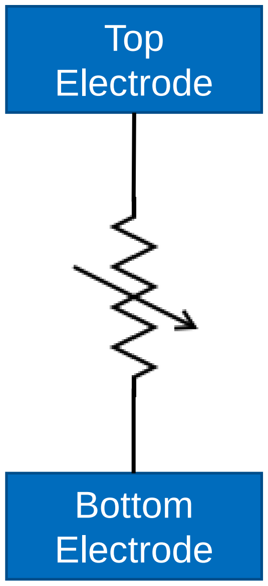
Link to publication
(open access)

 ©2022 Flash Memory Summit. All Rights Reserved.

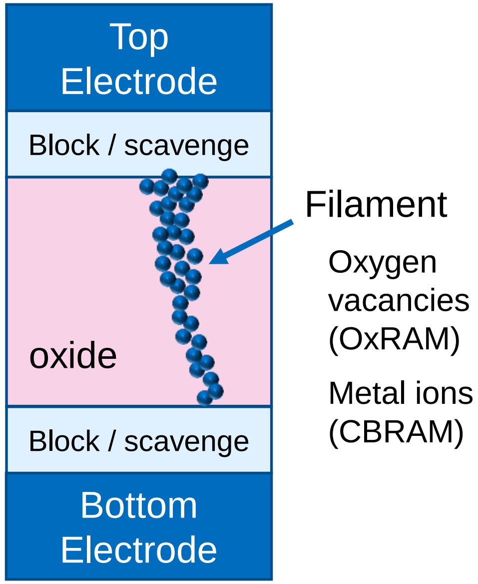
Thank You

©2022 Flash Memory Summit. All Rights Reserved.

So far, the “emerging NVM’s” are niche

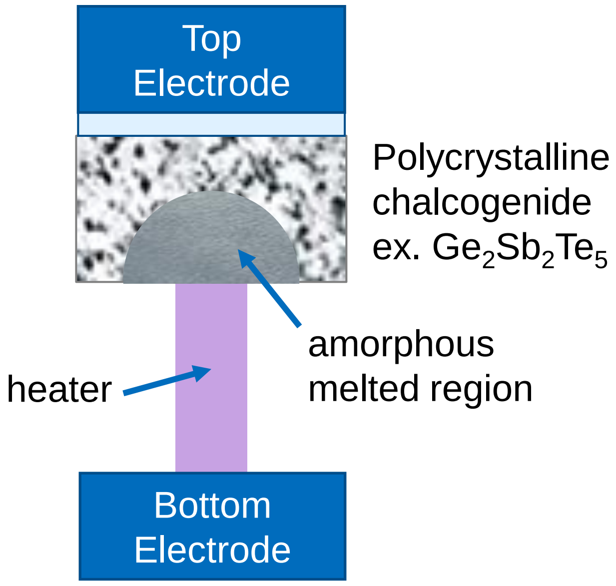


ReRAM
1967-



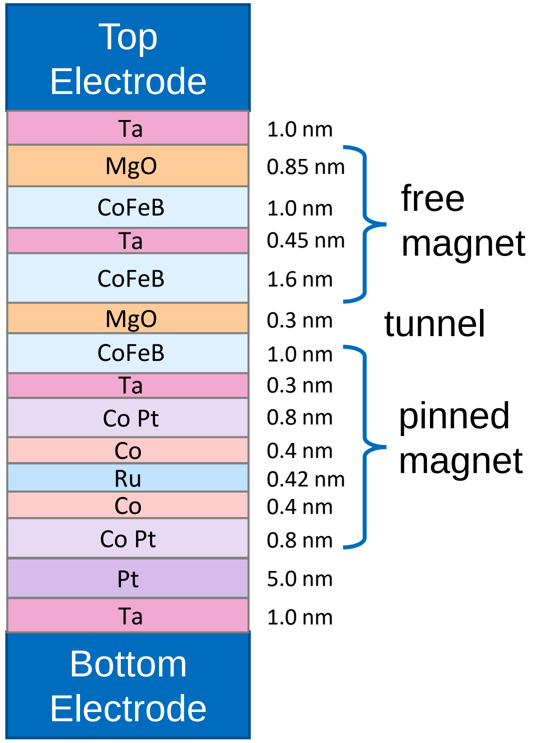
- Randomness
- Low endurance
- Lack of scalability

PCM
1968-



- Temperature limits
- Drift
- Thermal disturb
- Power

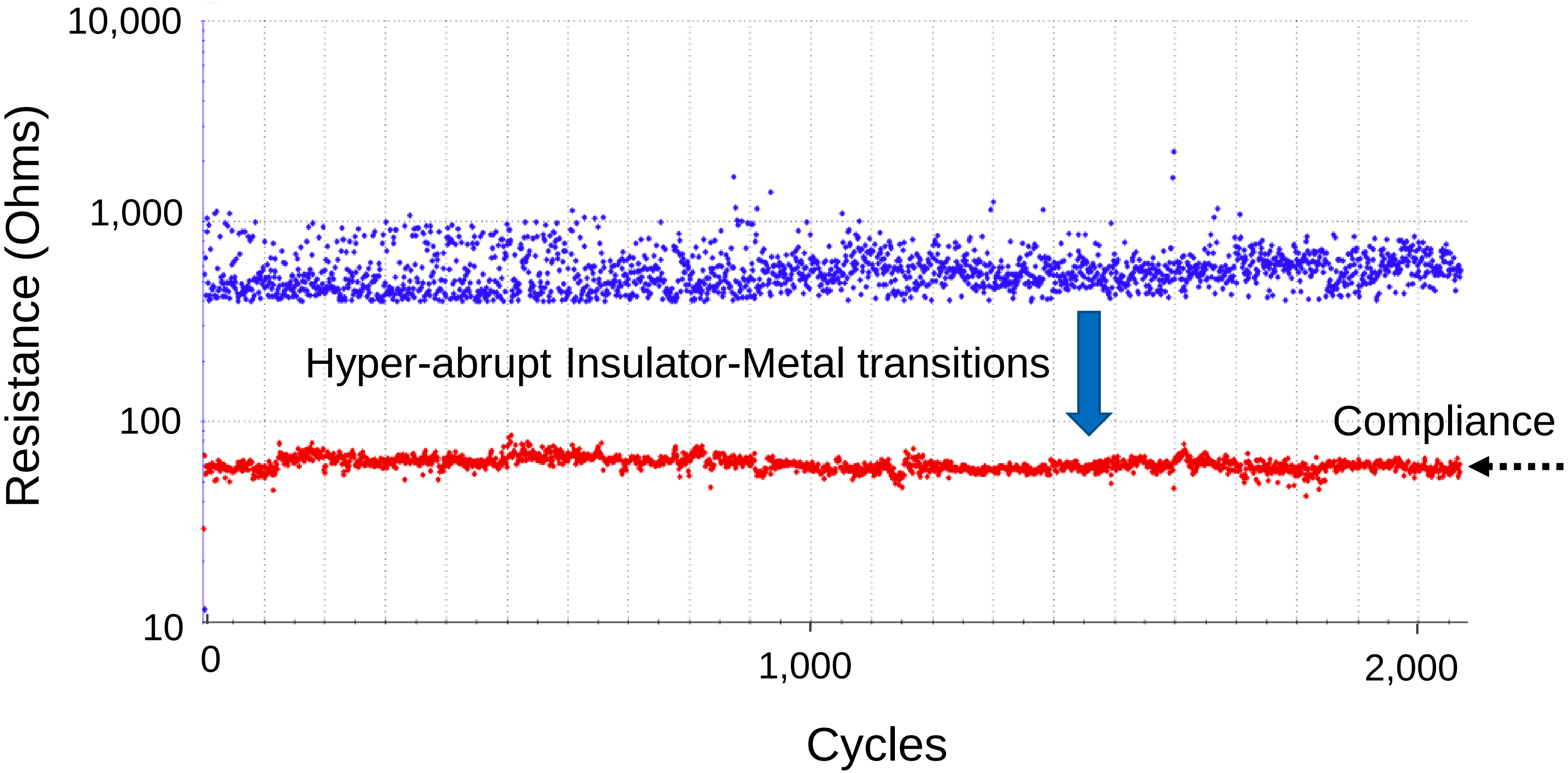
MRAM
1984-

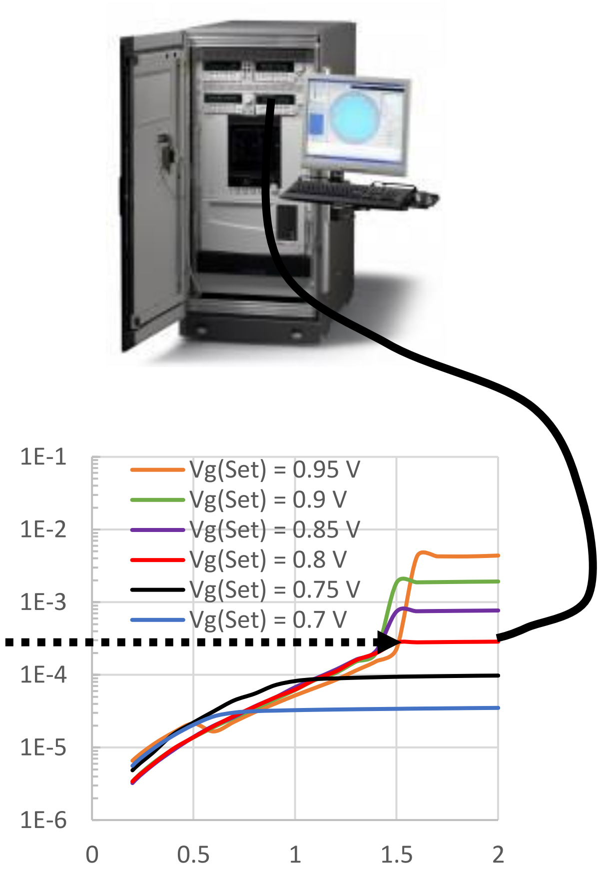


- Complexity / yield
- Low on/off signal
- Retention / speed tradeoff
- Magnetic disturb
- Scaling difficulties

 ©2022 Flash Memory Summit. All Rights Reserved.

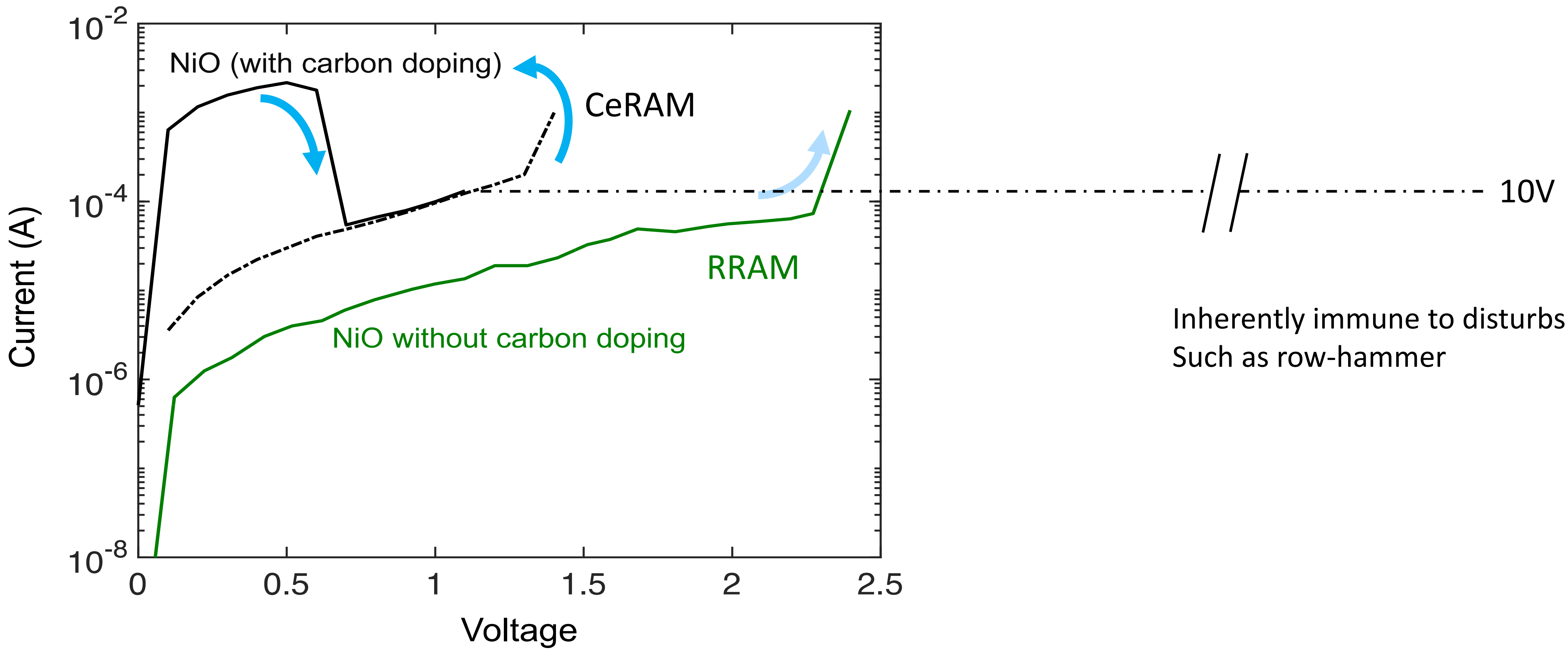
Typical results from 5um diameter devices
(best case is 15,000)





©2022 Flash Memory Summit. All Rights Reserved.

Now add carbon doping



Inherently immune to disturbs
Such as row-hammer

©2022 Flash Memory Summit. All Rights Reserved.

Goal: The most universal NVM

	CeRAM	Next Year's Update
Scalability	<5 nm logic node*	15nm diameter proof
Multi-Level Cell	Yes	
Mask Cost	2	
Required voltage	< 1.5V	
Write speed	< 2nS*	< 1 nS testing
Write energy	< pJ/bit	< 100 fJ/bit
Access	Byte	
Low temp operation	< 0.9K*	
High temp operation	> 200ºC*	300 ºC
High Temp Retention	185ºC*	300 ºC
Harsh environment	Immune to radiation	heavy ions and mag field
Tamper resistant	MLC, EMP, Rowhammer proof	
Endurance (# cycles)	10^4	10^6

©2022 Flash Memory Summit. All Rights Reserved.