Flash Memory Summit

ReRAM's Development Path Towards Commercialization

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VP Technology Development at Weebit Nano

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Weebitnano THE FUTURE MEMORY

35 YEARS OF NAND FLASH MEMORY INNOVATION

Outline

- Weebit overview
- ReRAM module
- Initial qual results
- Summary

Who is Weebit Nano?

Flash Memory Summit

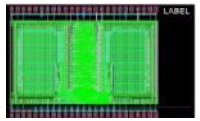
Leading developer of innovative next-gen memory technology – Weebit ReRAM – for the global semiconductor industry

Founded: 2015
Israel & France 50 personnel*
(90% engineers/scientists)

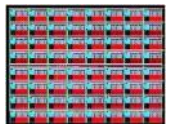
R&D Partner: Leti
Leveraging years of research experience in NVM

Current Business Model:
IP licensing to semiconductor companies & fabs

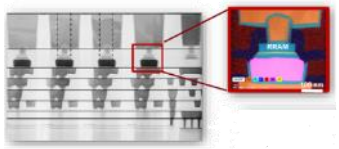
Silicon-Proven Technology
Mbit arrays avail @ 28-130nm
Volume production 2023



4Kb



1Mb



Successfully Scaled to 28nm

LETI INNOVATION DAYS

IP Module Live Demonstration

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Initial IP Module Qual Results

2017 | Q1 2018 | Q2 2018 | Q4 2018 | Q3 2019 | ••• | Q4 2021 | Q1 2022 | June 2022 | July 2022 | Aug 2022

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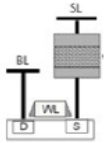

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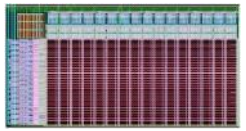
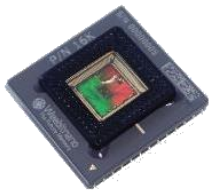
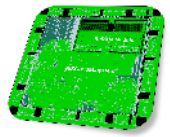


FMS AI Demo



Scaling to 22nm FD-SOI

IP Module Tape-out to SkyWater



*Includes employees and permanent contractors.

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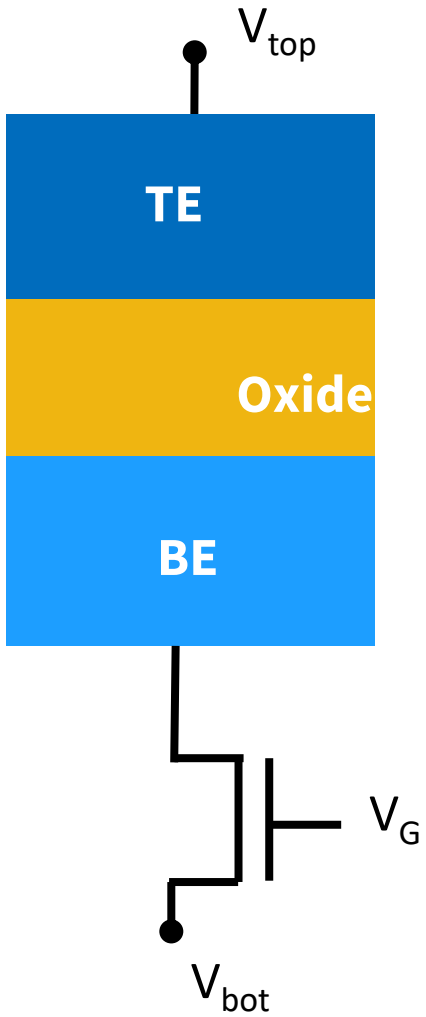
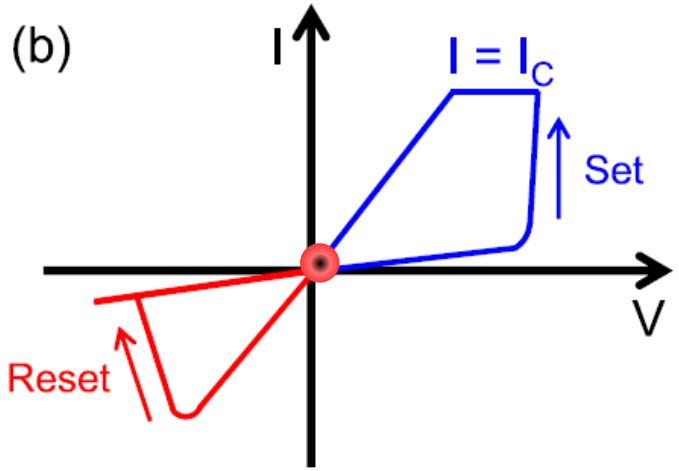
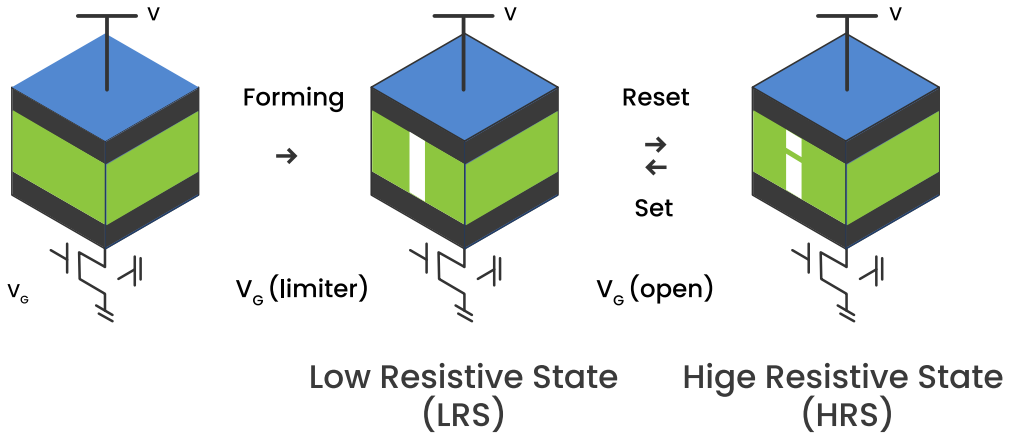
ReRAM Basic Operation



- SET (Program) – HRS-> LRS
- RESET (Erase) – LRS –> HRS





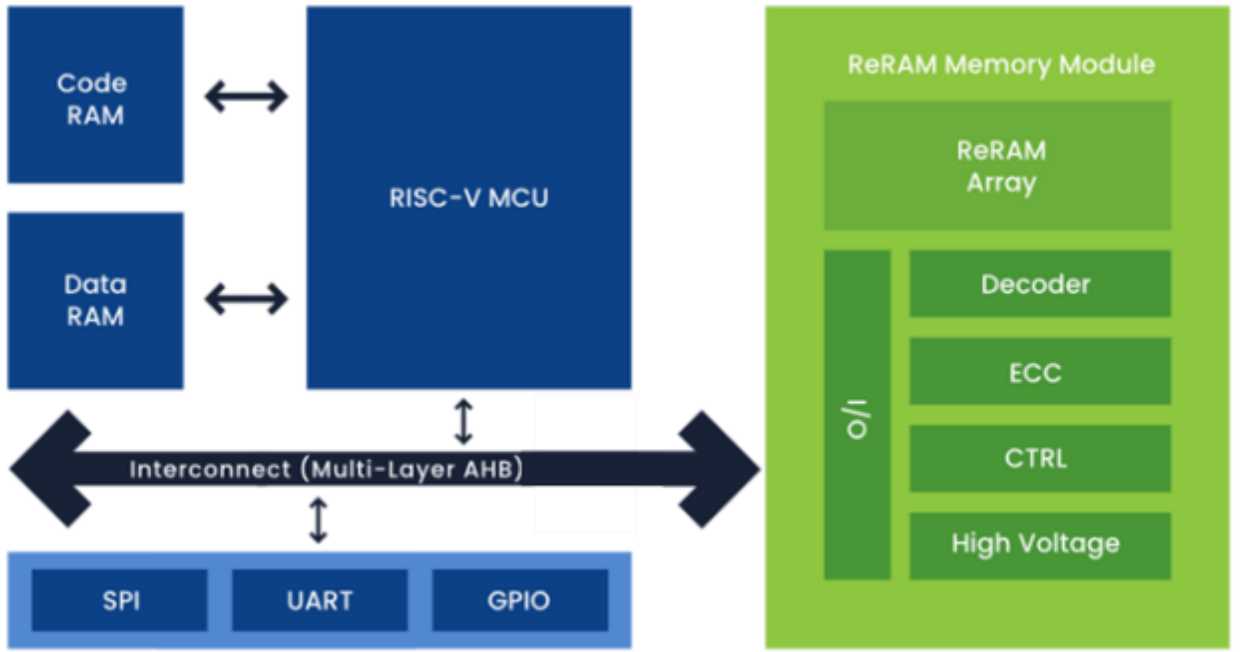
MCU/IoT: A Natural Fit for ReRAM Integration

- Billions of Battery-operated Edge Devices
  - By 2026*: 55B connected devices worldwide;
    73 ZB of data generated from connected IoT devices
- Name of the game: System Integration
  - Flash stuck at 28nm
- Embedded ReRAM has significant advantages over external NOR flash
  - Power: eliminate external memory interfaces
  - Speed: Avoid data fetching from external memory
  - Cost: Cut expensive SRAM or external flash
  - Reliable: Handles higher temps; built for longevity
  - Endurance: Enables new use-cases
  - Secure: Instantiated on-chip, difficult to hack

** Source: IDC Research 2021*

Weebit ReRAM Module Design in Qualification

- Integrating a ReRAM array in a complete module in 130nm technology
- Module includes
  - All analog circuitry
  - Smart algorithms (read, set/reset, forming)
  - Control logic and data manipulation
  - Redundancy, ECC
- The ReRAM module is further integrated into a complete subsystem
  - Based on a RISC-V processor
- Silicon is fully functional, now undergoing Characterization & Qualification



Embedded ReRAM Demo-Chip

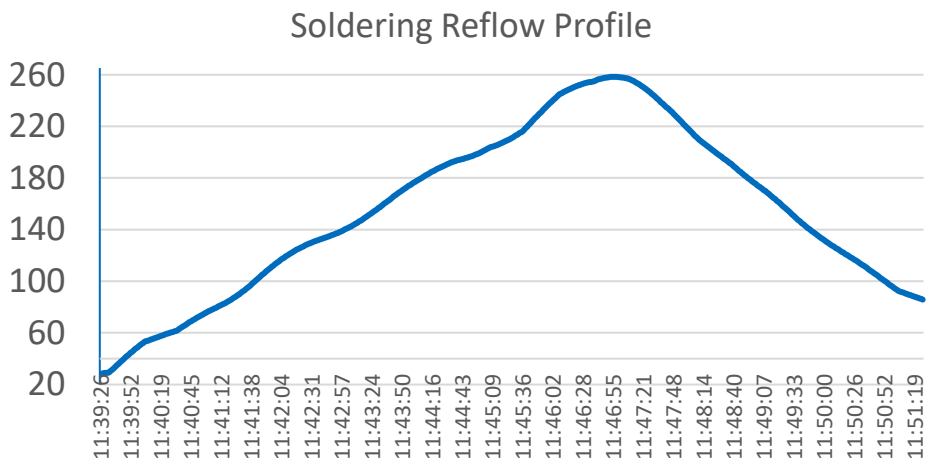
ReRAM Qualification Process

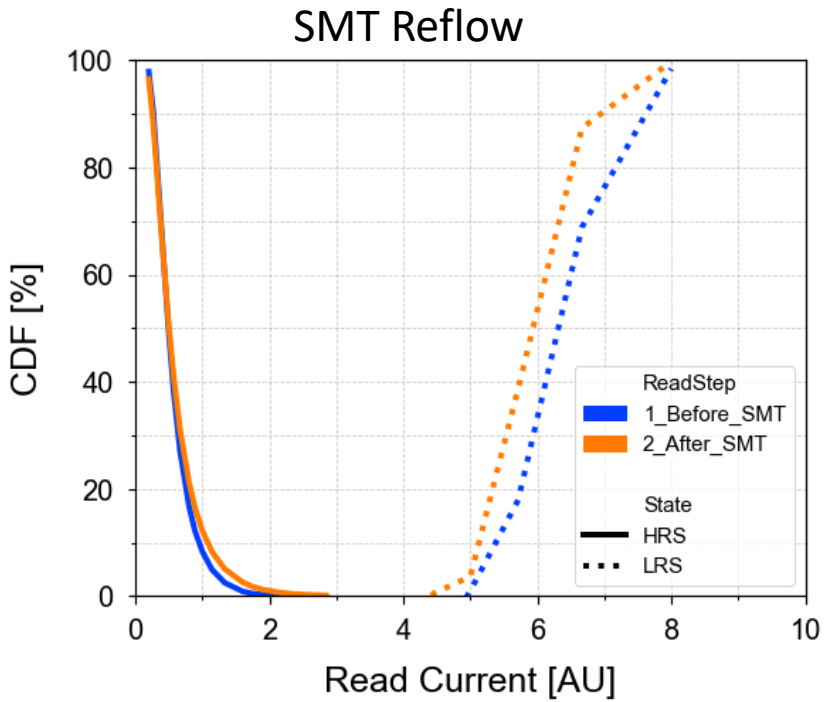
- Weebit is now qualifying its 1st ReRAM module
- Qualification process (unlike technology demonstration) requires meeting industry standards (JEDEC, AEC, MIL) to show technology maturity

Stress	Test Item	Reference	Stress Conditions	Test Conditions / Acceptance Criteria	Sample Size	Comments
NVCE	**Endurance**	**JESD22-A117 JEDEC 47**	25°C and 85°C V=Vcc max	**Datasheet Spec**/ 0 Fails	3 Lots/ 77 units	Test all the array bits to 100% Max spec
UCHTDR	**Data Retention**	**JESD22- A117 JESD47**	**Tstress – 125°C**	**1000** hrs/ 0 Fail	3 Lots/ 77 units	Readout at 25°C and 85°C
PCHTDR	**Post Cycle Data Retention**	**JESD22- A117**	**Tstress = 125°C 100% spec**	**10** hrs/ 0 Fail	3 Lots/ 39 units	Readout at 25°C and 85°C
SMT	**SMT Reflow**	ESD22 - A113	Tc 260 °C	3 cycles/ 0 fails	3 Lots/ 25 units	Pb-Free Assembly Profile

SMT Reflow Results (Memory Module)

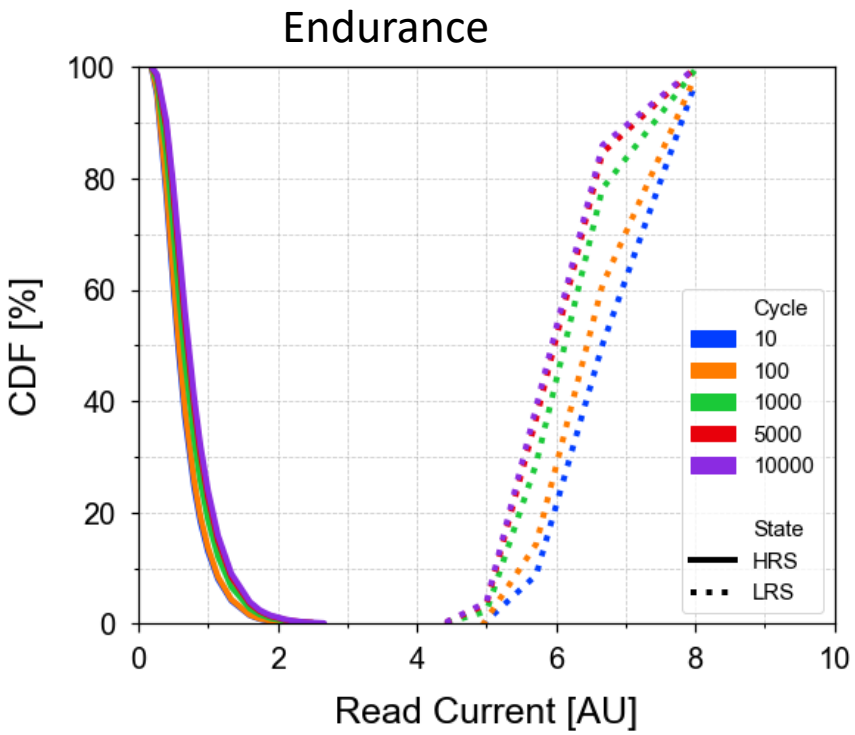
- The main challenge of any new technology is demonstrating thermal stability
- SMT reflow cycles (up to 260°C) are a good indication for data retention
- Results: Showing high thermal stability performance
  - 3 consecutive SMT reflow cycles
  - 1st lot, 25 units, passed with zero failures





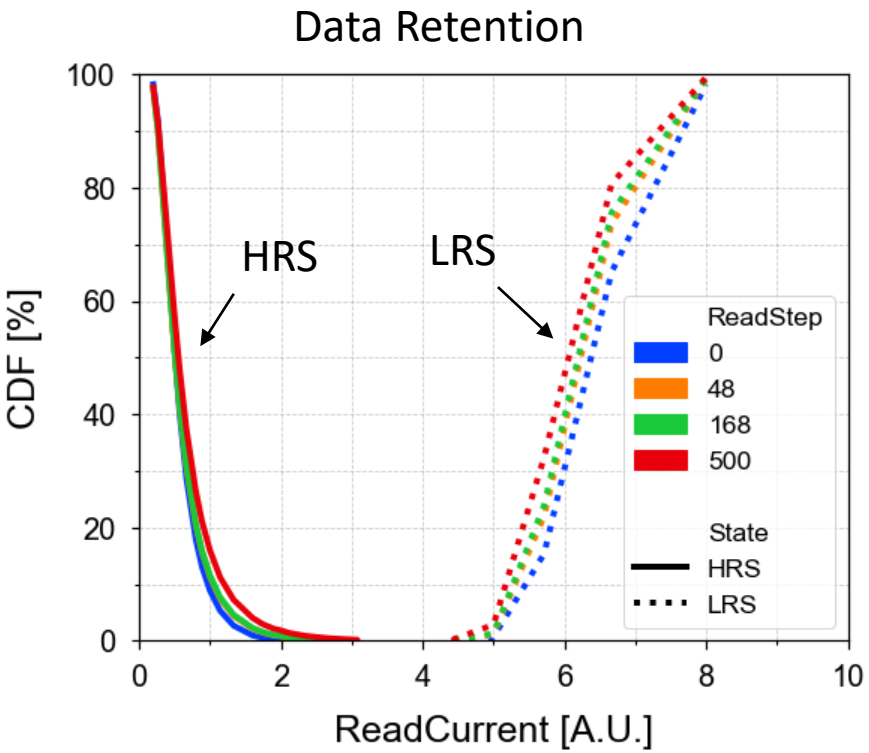
Non-Volatile Cycling Endurance - NVCE

- Sample size – 77 units
- Test sequence – alternating CHBD pattern and monitoring each cycle for errors
- Results – passed 10K cycles with no failures
- Endurance testing continues



Memory Module Data Retention

- High temp bake for data retention
  - Bake at 130°C (accelerated conditions) to predict 10 years operation at hot temperature
- 1st lot, 77 units, passed with zero failures*
  - Also showing stability after first few hours bake
- Retention after endurance cycles:
  - Passed zero failures after 10K cycles, 168h@130ºC

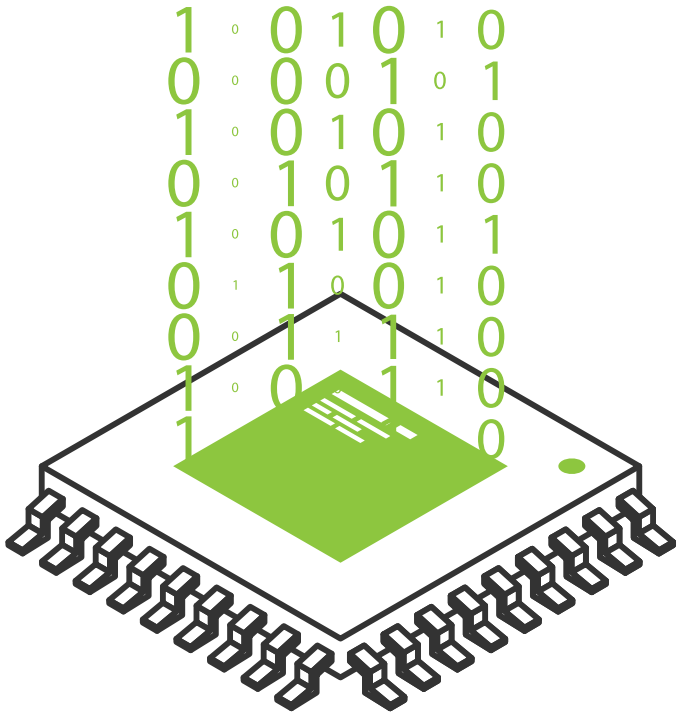


* Currently 500h, final RO 1000h.

Conclusions

- Weebit has functional ReRAM modules under qualification now
- Successful initial qualification results:
  - Showing good data retention before and after cycling
  - Endurance test showing good results up to spec, extended cycling characterization on-going
  - High temp stability is demonstrated by passing 3x SMT

Come & see
our live ReRAM Demos
at Booth #639



Thank You!

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Read more on www.weebit-nano.com

