Flash Memory Summit

High Performance Computing with Hybrid Bonding 3D Interconnect

Laura Mirkarimi, Abul Nuruzzaman, Guilian Gao, Gill Fountain, Tom Workman, Dominik Suwito, Bongsub Lee, Cyprian Uzoh, Jeremy Theil, Gabe Guevara, K.M. Bang

Adeia
San Jose, CA 95134

adeia™

35 YEARS OF NAND FLASH MEMORY INNOVATION

XPERI

adeia

XPERI IP BUSINESS IS NOW ADEIA

[AHH-dee - uh]

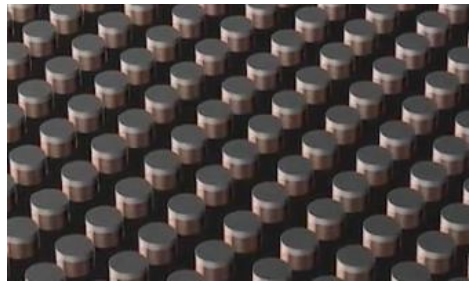
Adeia turns ideas into innovations

Our name may be new, but our roots run deep with decades of continued innovation. We invent, develop and license innovations that advance how we live, work and play.

Motivation/Background

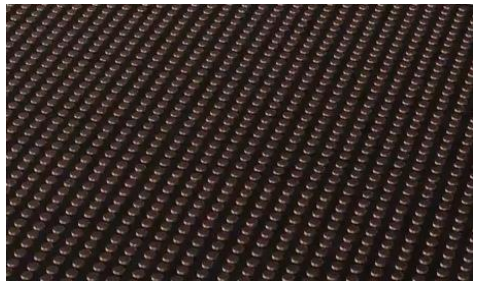
- High Performance Compute Challenges
  - Bandwidth Limitation with Interconnect Technology (Cu Post vs Hybrid Bond)

Micro-bump



~ 625 interconnect / mm²

DBI-Hybrid



100,000 to 1,000,000 interconnect/mm²

  - Thermal Performance Challenge
    - Speed binning and temperature sensitivity[2] with performance
      - Degradation begins at 85-90; 90-95C, very problematic.
    - Minimize differential temperature from die 1 to die 16
  - Cost Management is Key
    - Assembly Costs
    - Yield (stacking, compound)

Karen Heyman, DRAM Thermal Issues Reach Crisis Point; June, 2022.

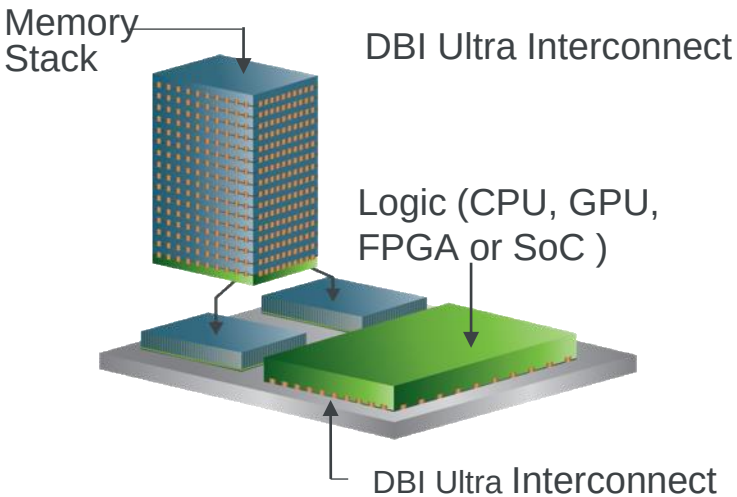
The Interconnect Matters

Flash Memory Summit

Hybrid Bonded Module

DBI®

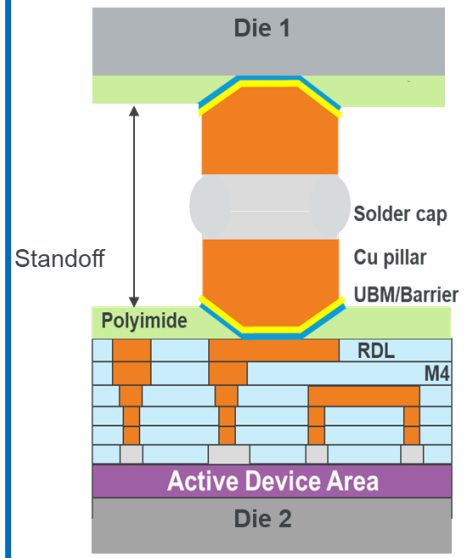
DBI® Ultra



2.5 D / 3D DBI® Ultra
Hybrid Bonding Solutions

Interconnect Comparison

Micro-Bump

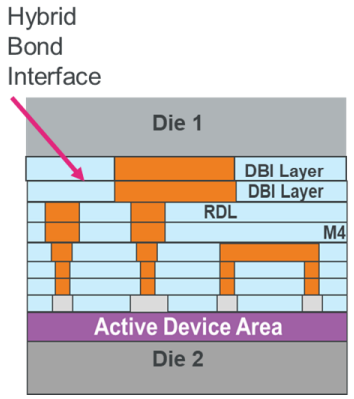


Key Challenge

Standoff of ~20 um
UBM Fab… (Masks)
Underfill
High Temp Bonding
>35 um pitch

Direct Bond Interconnect

When Less is More …



Advantage

No Standoff
No UBM
No Underfill
No Heat at Bond
No Pitch constraints

More

Scalability to <1um
High Throughput Bonding
Improved Thermal Performance
Higher Speed Binning Stacks
Improved Electrical Performance
Improved Reliability and Yield
Heterogenous Integration
Cost Savings
Flexibility in Architecture
Path to Chiplet Proliferation
Uniformity of Packaging Platforms

adeia™

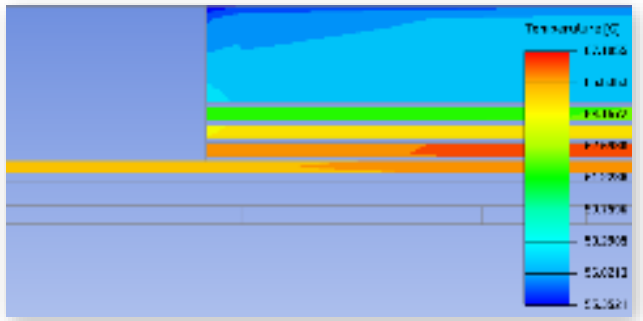
35 YEARS OF NAND FLASH MEMORY INNOVATION

Enhanced Thermal Performance with Hybrid Bonding

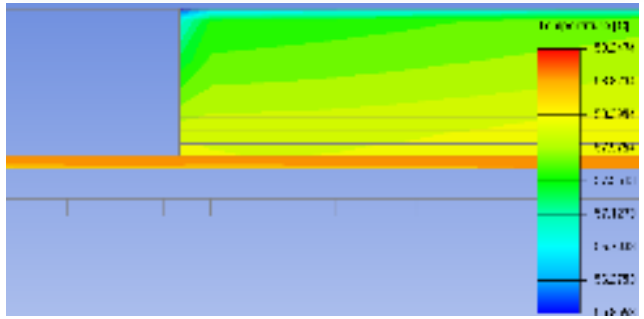
Flash Memory Summit

4-Die Stack Results

TCB-Pad



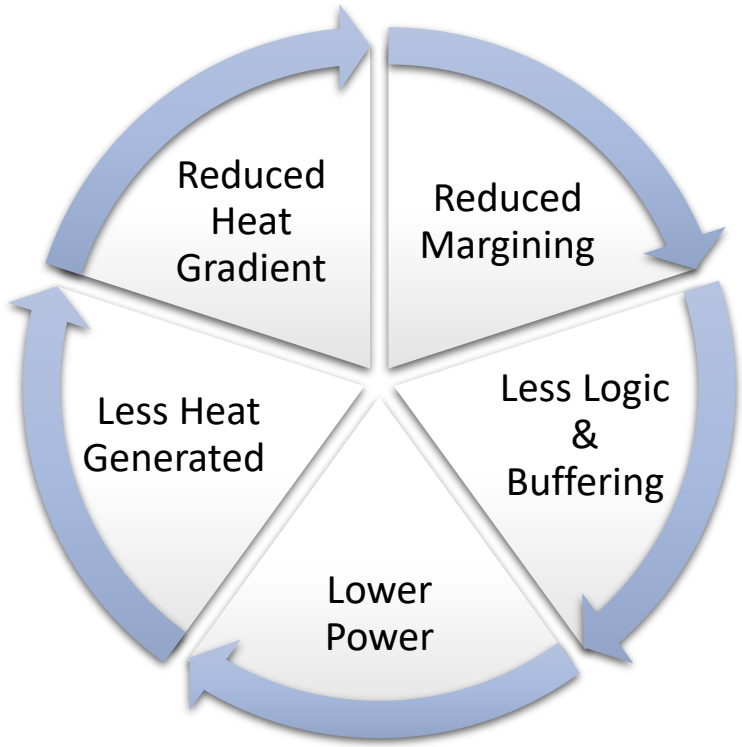
DBI-Pad



4-Die and 8-Die Stack Results

	4-Die Stack		8-Die Stack	
	TCB	DBI-HB	TCB	DBI-HB
Total Power (Watts)	10	10	18	18
TJunction (C)	67	59	97	70
ΔT (between bottom/top Die in Stack) (C)	9	1	28	4

A. Agrawal et al, ECTC 2017



- *T_J is reduced by 19- 25C*
- *Differential temperature between bottom/top die in stack*
  - *1 degree for 4 die stack (9x better)*
  - *4 degrees for 8 die stack (7x better)*

adeia™

35 YEARS OF NAND FLASH MEMORY INNOVATION

Enhanced Performance with Hybrid Bonding Design

Design Analysis 2D/3D; Hybrid/TCB

PARAMETER	2D	3D	IMPROVEMENT
Clock period(ns)	4.98	4.98	+0.0%
Total Power(mW)	26.1	20.4	+21.8%
CLK power(mW)	*9.68*	*9.52*	*+1.6%*
Logic power(mW)	*16.4*	*10.8*	*+33.9%*
Area (μm^2)	193,600	174,050	+11%
Routed wire length(mm)	3030	1315	+57%

		IMPROVEMENT OVER 2D		
PARAMETER	*2D*	*HyB*	TCB_{noSD}	TCB_{SD}
Clockperiod(nS)	5.5	+0.68%	-13%	+0.66%
Power(mW)	23.5	+20%	+18%	-103%
Area(μm^2)	193,600	+10%	-429%	-86%

T. Niguisse et al, " Design Benefits of Hybrid Bonding for 3D Integration"; et al, ECTC 2021

Hybrid Bond Pads 3D Architectural Advantage

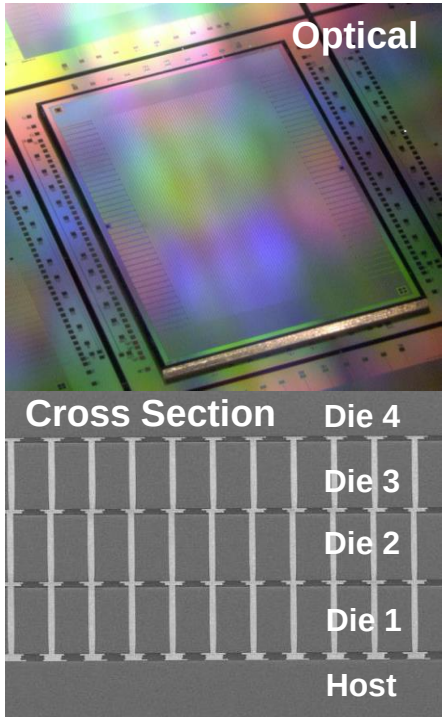
- Up to 33% Improvement in Power Reduction
- Up to 10% of an Area Improvement over

adeia™

Hybrid Bond Integration: Reduced Process Steps

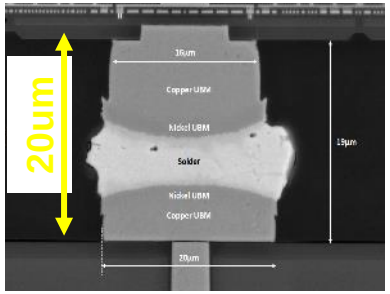
Flash Memory Summit

4-Die Stack Test Vehicles

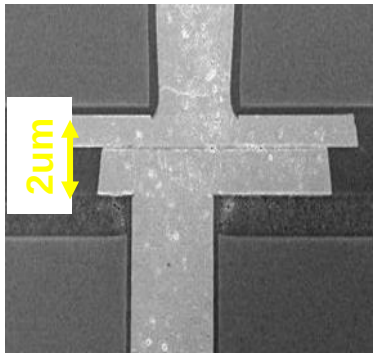


Interconnects:
Face to Face at Die to Host
Face to Back at Die to Die

Solder µBump



DBI



G. Gao et al, ECTC 2020

Die-Wafer Level Process Savings

Module Steps	Frontside Process		TSV Side Processing	
	UBM Solder	DBI	UBM Solder	DBI
1	Passivation opening	Yes	TSV reveal and Planarization	Yes
2	Lithography	Yes	UBM (Adhesion layer, seed layer)	NO
3	Adhesion layer, Cu seed layer	Yes	Lithography	NO
4	Cu electroplating	Yes	Cu electroplating	NO
5	Ni electroplating	NO	Ni electroplating	NO
6	Solder electroplating	NO	Resist strip	NO
7	Resist strip	NO	Wet etch (Cu + adhesion layer)	NO
8	Wet etch (Cu + adhesion layer)	NO		
9	Solder reflow	NO		
10	Cu CMP: NO	Yes		

DBI Module Steps = 5 - 1 CMP = 4
TCB Module Steps = 9

DBI Module Steps = 1
TCB Module Steps = 7

11 Fewer Wafer Process Module Steps for DBI over Solder µBump

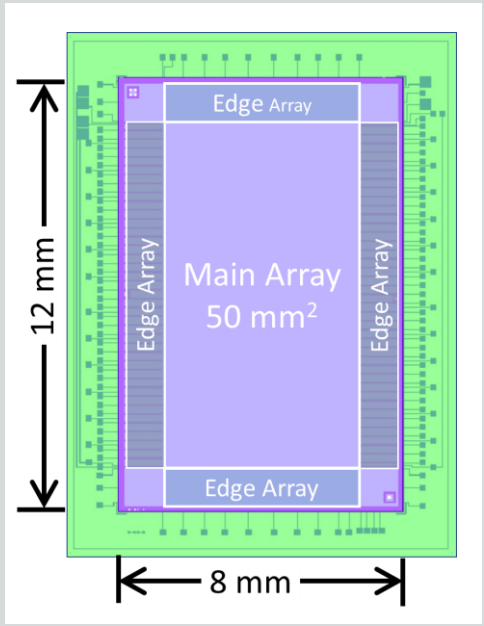
adeia™

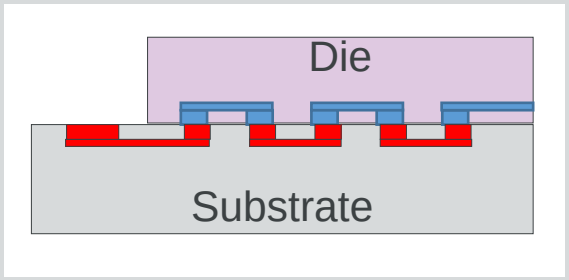
35 YEARS OF NAND FLASH MEMORY INNOVATION

Hybrid Bonding Test Vehicle Demonstrations

Flash Memory Summit

Single Die Stack

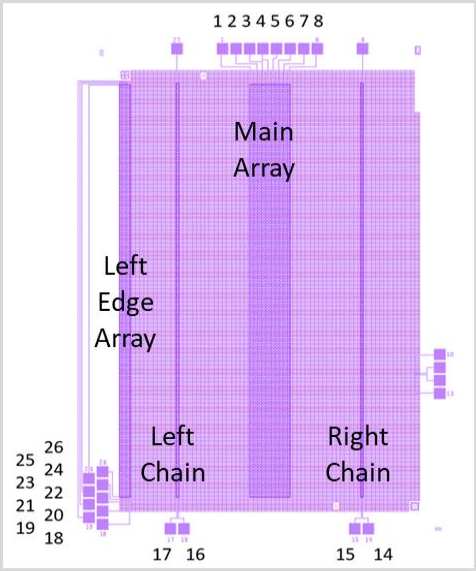


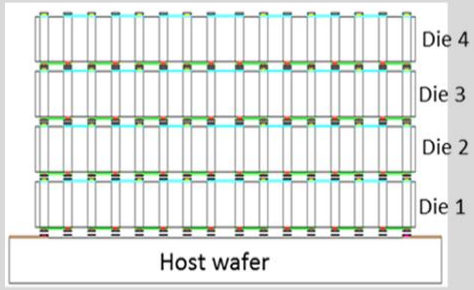


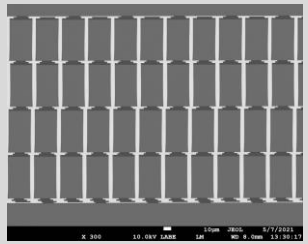
T. Workman et al., IMAPS (March 2020)

- 8 x 12 mm Test Chip
- 2 Layer Metal Pattern: RDL + DBI Bond Pads
- 10 μm pad on 40 μm pitch
- Main Center Array: 50 mm² with **31,356** daisy chain links
- Edge Arrays: 3400 – 5000 links, with links within 200 μm of die edge
- Both 200 mm and 300 mm substrates and component die

5- Die Stack with TSV







G. Gao et al, "ECTC 2021

- Size: 8 mm x 12 mm x 50 μm thickness
- TSV: 5 μm diameter on 35 μm pitch / DBI 15um on 35um pitch
- Main Array: 316 x 30 = **9,480** links
- Right & Left Chains: 316 x 2 = 632 links
- Left Edge Array: 316 x 8 = 2,528 links

adeia™

35 YEARS OF NAND FLASH MEMORY INNOVATION

Hybrid Bond Interconnect Reliability Performance

	Single Layer DBI		5-die TSV Stacked DBI	
Test	Test Condition	Results	Test Condition	Results
Temperature Cycling	-40C to 150C 2000 cycles	Pass	-40C to 125C 2000 cycles	Pass
High Temperature Storage	225C, 2000hrs 275C, 2000hrs	Pass	150C, 2000hr	Pass
Autoclave	121C, 100%RH, 15PSI, 168hrs	Pass	121C, 100%RH, 15PSI, 168hrs	Pass
Moisture Sensitivity MLS3	24hr prebake+30C/60% RH 192hrs + 3X Reflow	Pass	24hr prebake+30C/60% RH 192hrs + 3X Reflow	Pass

- Hybrid Bond Interconnect (DBI) is More Reliable than μbump Interconnect:
  - Enhanced Reliability (all Cu interconnect, no underfill)
  - Enhanced Resistance to Electromigration (all Cu interconnect)
  - Dielectric Hermeticity protection (<10^{-11} atm-cc/s)

adeia™

Scalable Hybrid Bond Interconnect Demonstrations

Flash Memory Summit

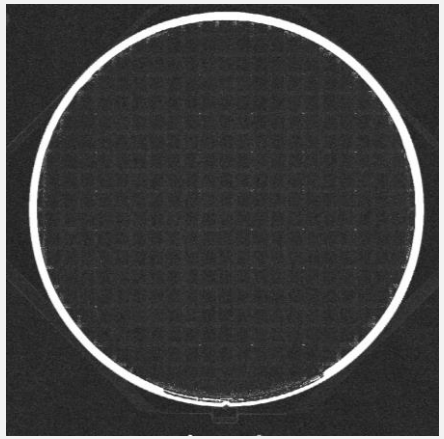
Wafer to Wafer

- 0.8 um pad (1.6 um pitch)
- >**8M** DBI interconnects within a cell
- Manufacturability Evaluations:
  - Technology Transfer of CMP 96-100% within First Lot
  - Hybrid Bond Interconnect Easily Integrates BEOL

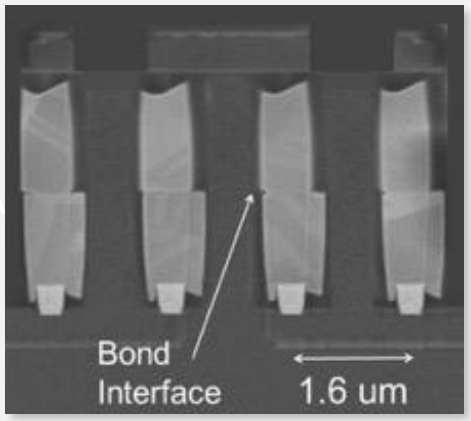
Die to Wafer

- 2 um pad (4 um pitch)
- **1.8 M** DBI interconnects within a die
- Manufacturability Evaluations in Prototype Lab:
  - High Yield Bonding ~1-3% bond voids
  - Electrical test tolerates (80%) pad mis-alignment

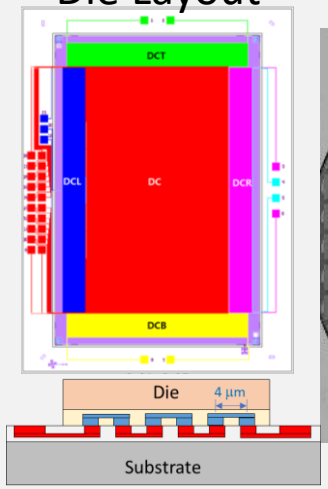
CSAM



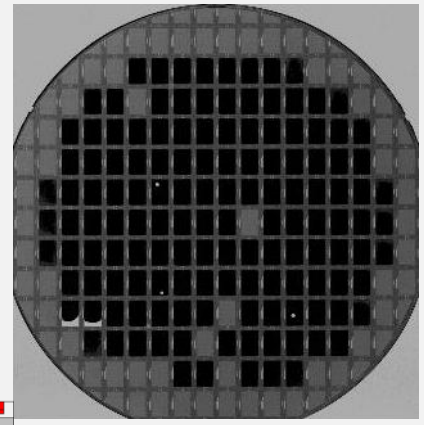
SEM Cross Section



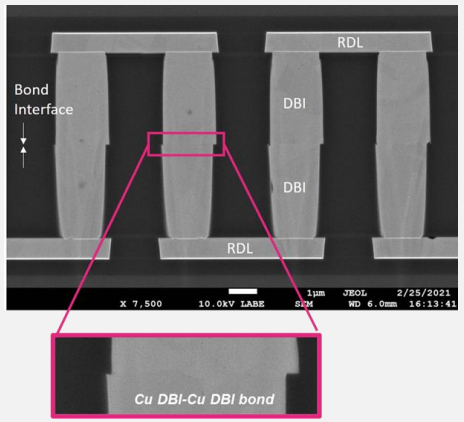
Die Layout



CSAM



SEM Cross Section



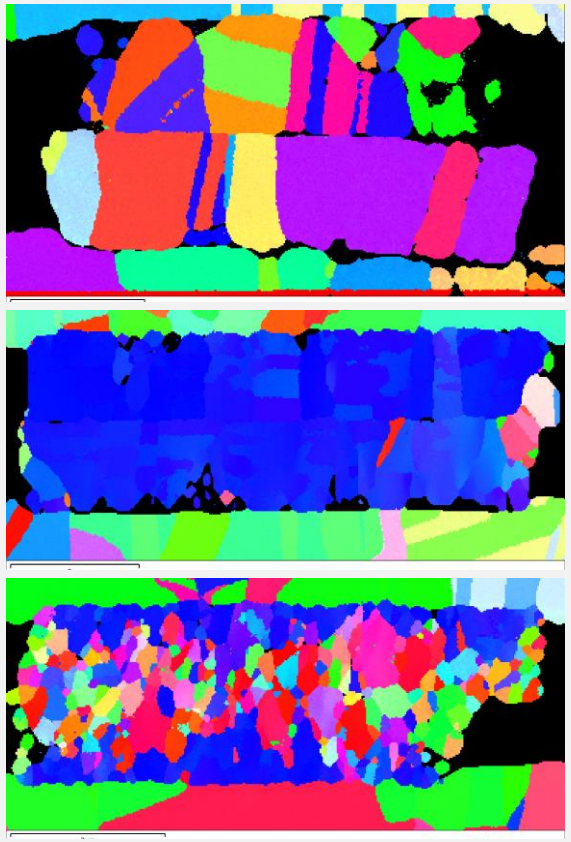
adeia™

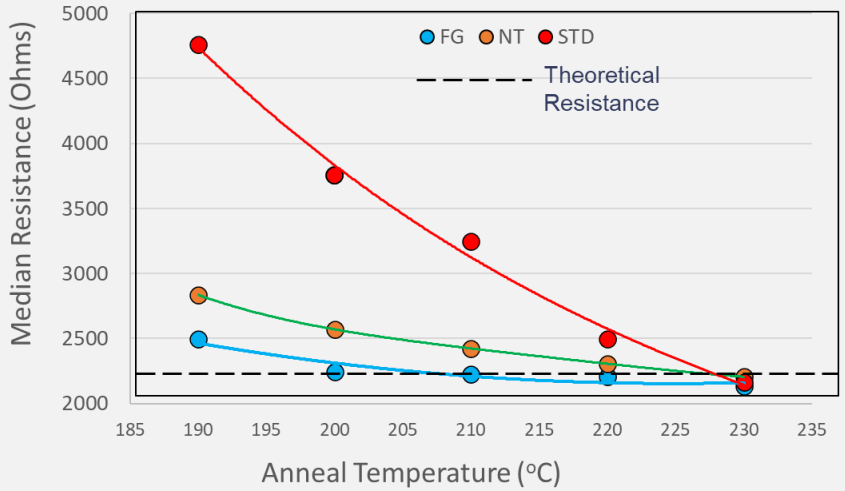
35 YEARS OF NAND FLASH MEMORY INNOVATION

Advances toward Ubiquitous Heterogenous Integration

Flash Memory Summit

Lower Cu-Cu Joining Temperature with Grain Engineering (<200C)





Interconnect Formation Completes

- 230C for Standard Cu
- 220C for Nanotwin Cu
- 210C for Fine Grain Cu

- The fastest diffusivity path for Cu depends on the temperature, microstructure, grain size, impurity content of the film, film stress, interfacial adhesion.
- At our experimental temperatures, the activation energy for copper creep is near the value expected for grain-boundary self-diffusion.

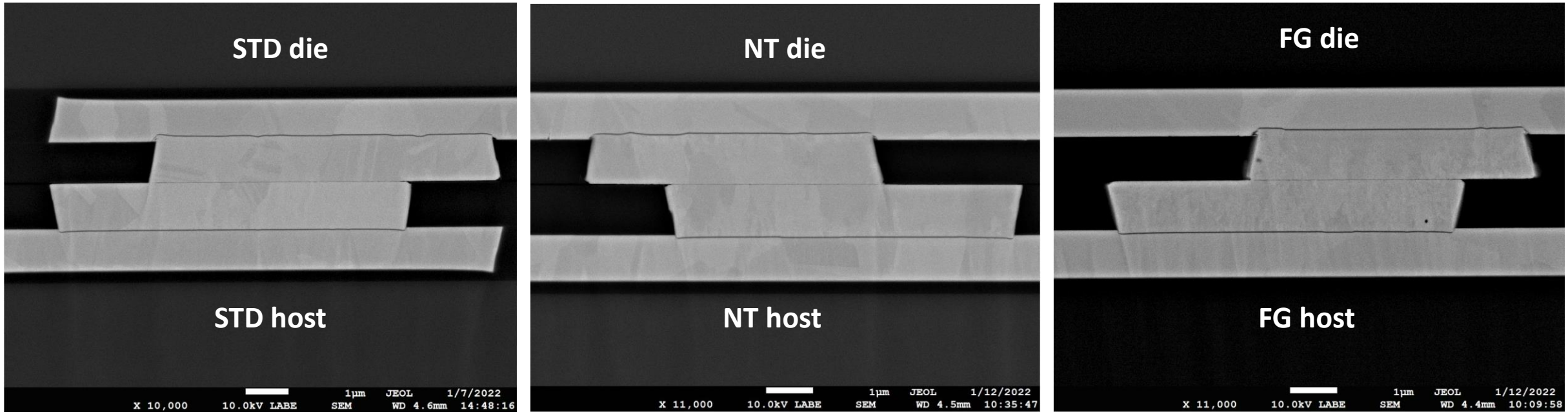
Mirkarimi et al, ECTC 2022.

Nanotwin Cu and Fine Grain Cu provide a pathway to lower thermal budgets

adeia™

35 YEARS OF NAND FLASH MEMORY INNOVATION

Pathway to <200C Cu-Cu Bonding

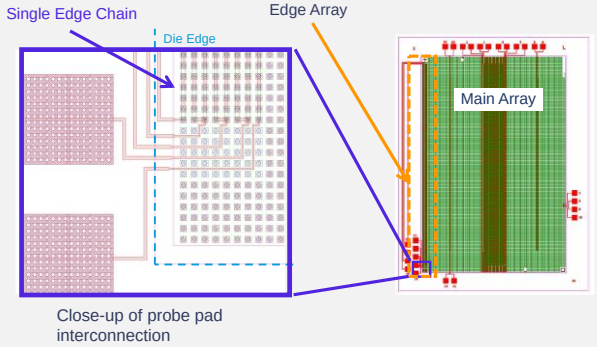


Thermal Treatment 180C anneal for 8 hours

Advances toward Ubiquitous Heterogenous Integration

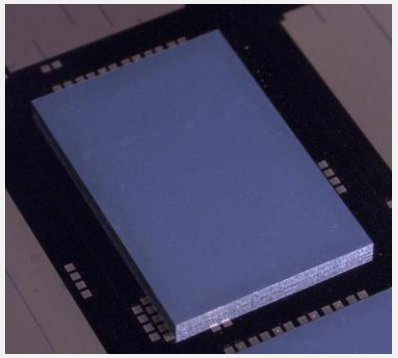
Flash Memory Summit

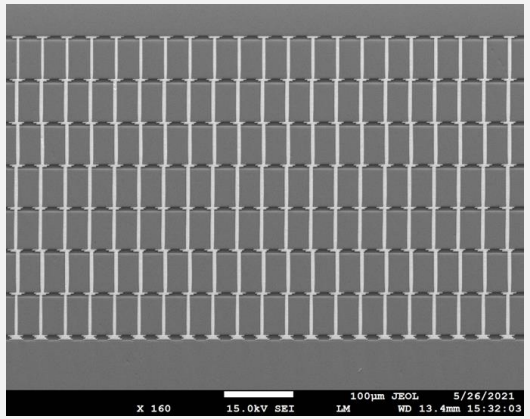
Aggressive Design Testing for Packaging to Ensure Ease of Integration with Hybrid Bond Layer

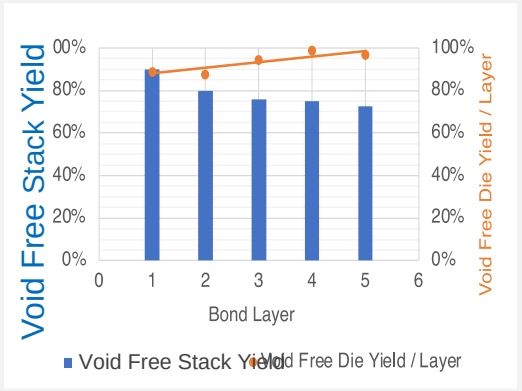


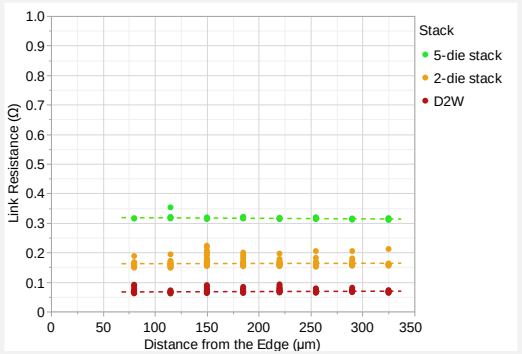
Column	Distance to the Die Edge (µm)
1	85
2	120
3	155
4	190
5	225
6	260
7	295
8	330

Edge Array: 2,528 links
Access Column Level Data









Theil et al, ECTC 2022

Consistent Interconnect Performance Tested to within 80 um of Dicing Street

adeia™

35 YEARS OF NAND FLASH MEMORY INNOVATION

Summary Slide

- Test vehicles were fabricated and tested to JEDEC standards demonstrating reliable hybrid bond interconnect in configurations for memory to memory (HBM – type layout) and logic to memory interconnect.
- Interconnect scalability was demonstrated for 10um to 0.8 um pad diameters.
- R&D studies suggest that the Cu grain engineering will deliver a technology with thermal budgets <200C.
- Design and layout studies confirmed high yielding interconnects designed to within 80 um of the dicing street for both one and two-die stacks.

