Flash Memory Summit

Using Floating Gate and Replacement Gate Technologies to Address Diverse Storage Market Needs

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Solidigm

35 YEARS OF NAND FLASH MEMORY INNOVATION

The New Paradigm of Solid-State Storage

$8B+ Revenue*

*Solidigm + SK Revenue

3 NAND Factories

Global Organization,
HQ in California

- Solid-State Innovation Since 1987

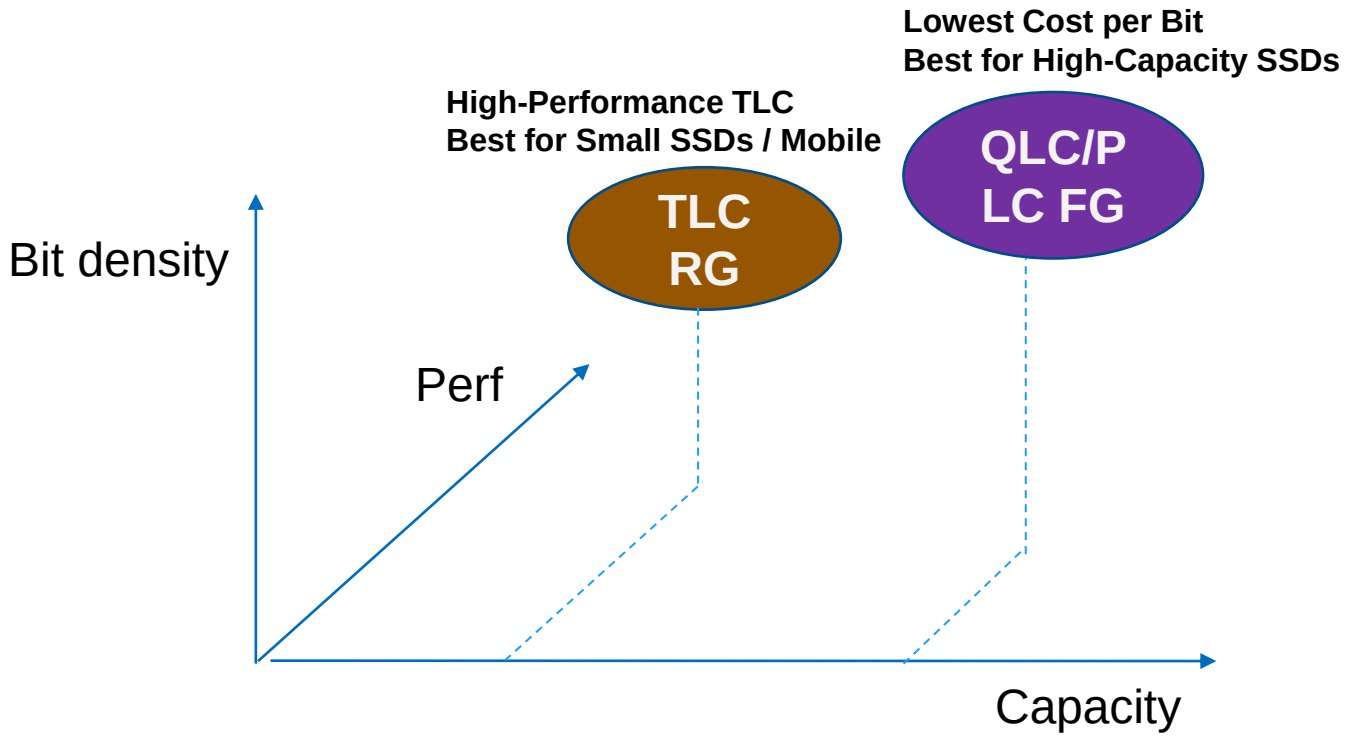
intel + SK hynix

- Leadership in Enterprise,
Cloud & Client

- Pace-setting innovation across
Floating Gate & Charge Trap, TLC & QLC

Executive Summary

Having access to both technologies can enable independent delivery of optimized QLC/PLC bit density at higher capacities and, at the same time, deliver competitive bit density and higher performance at lower TLC capacity in parallel



Floating Gate vs. Replacement Gate Structure

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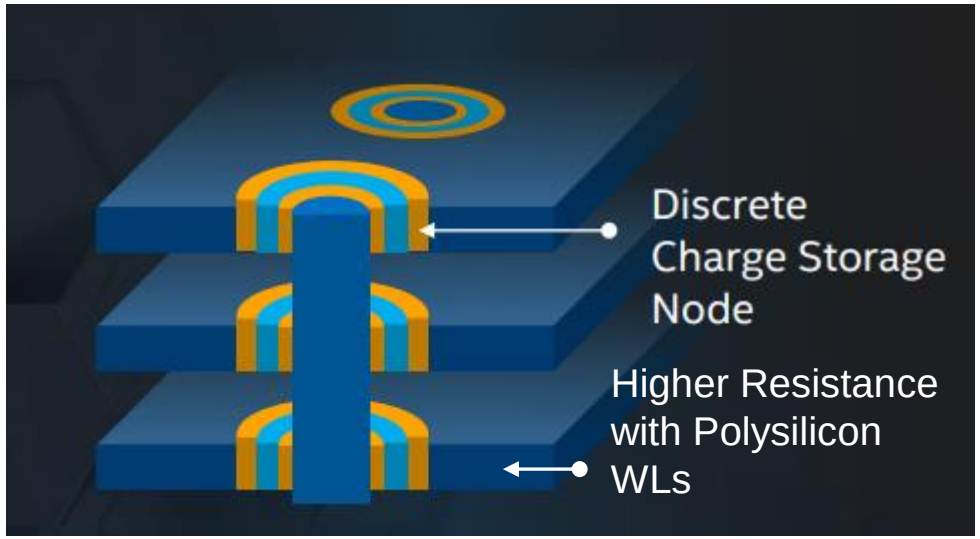
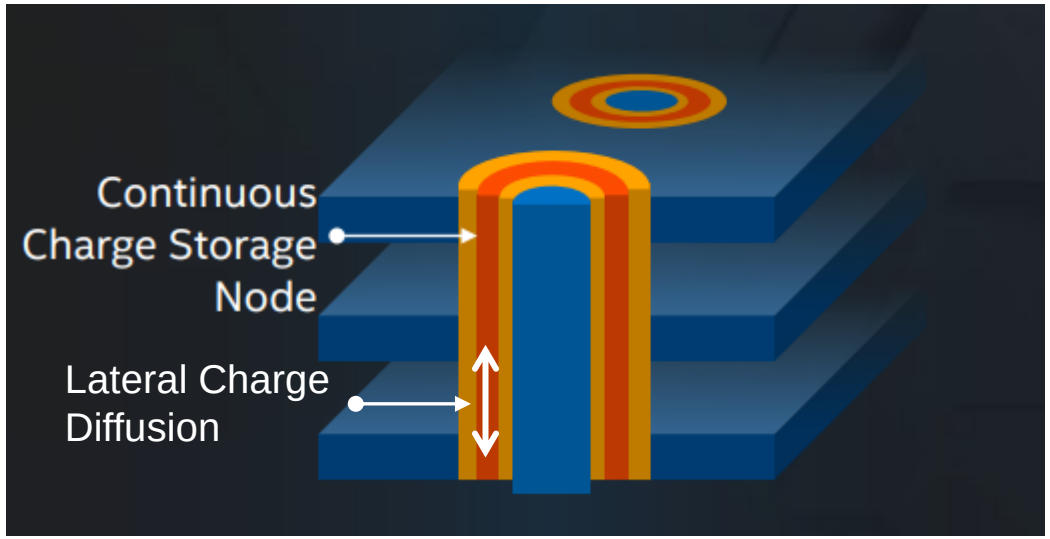
Floating Gate 3D NAND



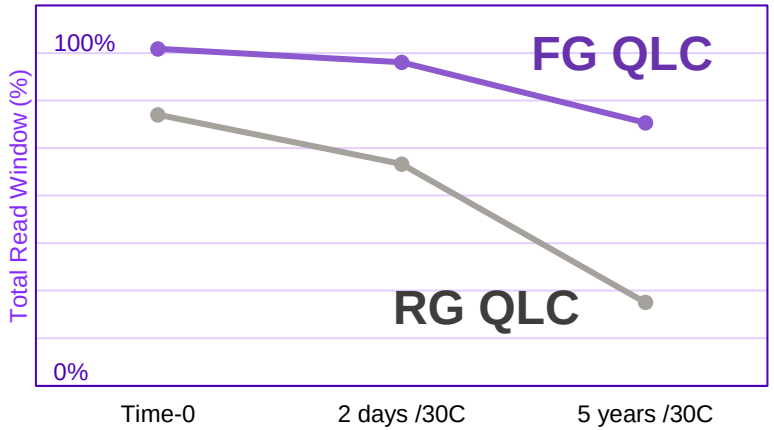
- ✓ Discrete cell isolation minimizes risk of cross-cell interference: Clear advantage for QLC and PLC.
- ✓ Good charge retention.
- • Higher resistance of polysilicon WLs requires tile architecture to reduce WL RC.

Replacement Gate 3D NAND



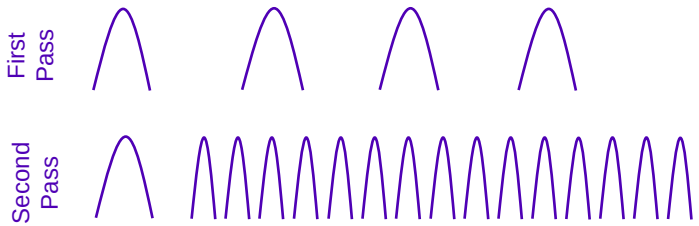
- ✓ Lower resistance of metal WLs enables faster operation.
- • Lateral charge diffusion in nitride (storage element) leads to data retention challenge.

QLC Implementation: FG vs. RG

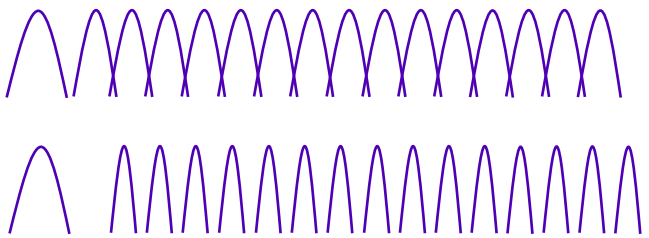


P. Kalavade, "Completing the memory and storage hierarchy," Intel Memory and Storage Day, 2019.

Floating Gate



Replacement Gate

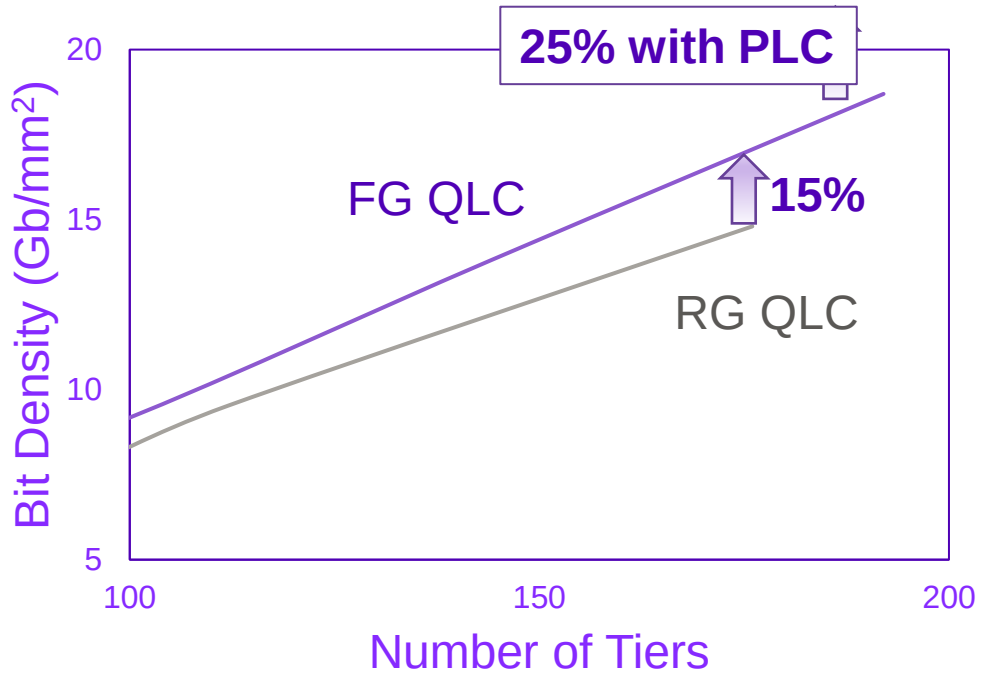


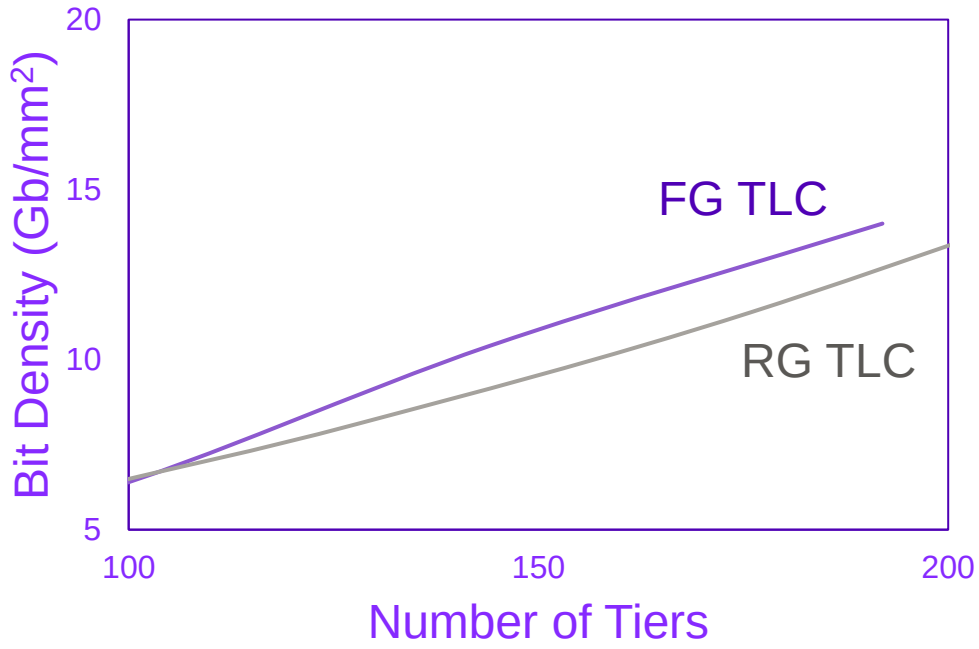
- ✓ A **4-16 algorithm** is implemented, leveraging the intrinsic immunity of FG cell to quick charge loss
- ✓ Data from First Pass is readable, minimizing the data storage in DRAM/SLC cache
- ✓ Each page of data is dispatched to the NAND only once, minimizing the channel I/O traffic
- ✓ Floating gate NAND cell has higher retention due to immunity to lateral charge diffusion. FG has higher RWB margin

- To compensate for quick charge loss, cells are placed close to their final V_T during the first pass
- **A 16-16 algorithm coarse fine** is typically used which requires all four pages of data dispatched to NAND during **both** first pass and second pass
  - **Requires first pass data to be cached in DRAM/SLC cache**
- RG has higher rate of charge loss and lower retention

A. Khakifirooz, et al., "1Tb 4b/Cell 144-Tier Floating-Gate 3D-NAND Flash Memory with 40MB/s Program Throughput and 13.8Gb/mm^2 Bit Density," ISSCC 2021.

Higher Bit Density With FG Technology



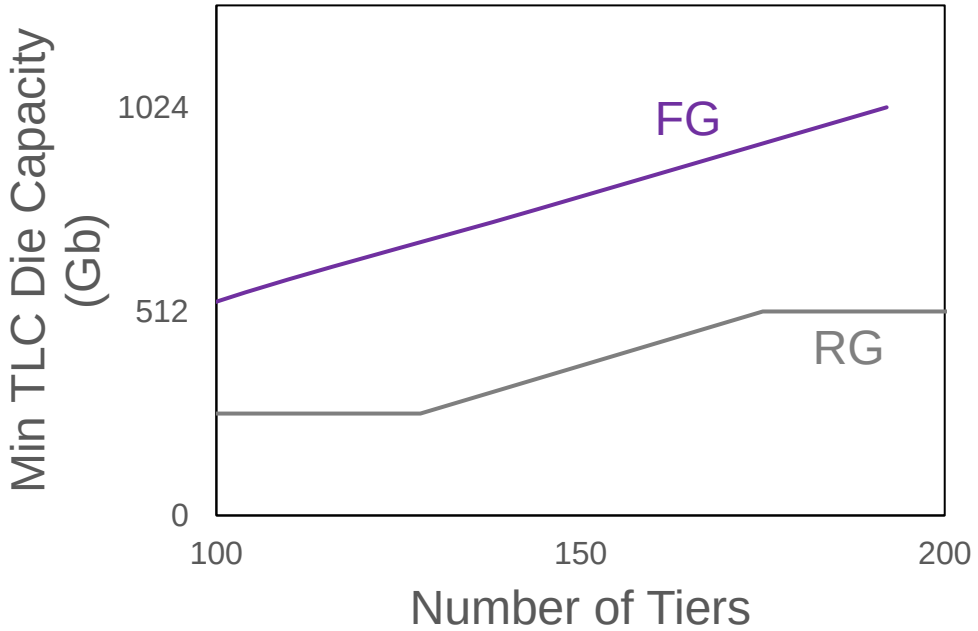


- FG technology delivers 15% higher bit density normalized by number of tiers
- This is significant, considering the quoted cost reduction from one generation in 3D NAND is about 18%
- FG technology can enable PLC, leading to an additional 25% bit density

Source: Solidigm internal research

Challenge of Maintaining Small Die Capacity

- To tackle higher WL resistance issue, FG technology uses tile architecture to reduce WL RC to levels comparable to typical RG technology
- This makes it more challenging to maintain small die capacity with best bit density, even though FG has been using Circuit-under-Array (CuA) and Zero-Periphery since its first generation of 3D NAND
  - WL segmentation via string drivers result in higher CuA area
  - Tile architecture requires splitting periphery circuits into multiple smaller sections, resulting in higher CuA area.
- RG technology is a better option to design small capacity dies needed for mobile and small SSDs
  - Minimum FG die size is ~70mm^2 (144layer) whereas minimum RG die size in ~40mm^2 (176 layer) (state of art)



Intel 64-Tier TLC

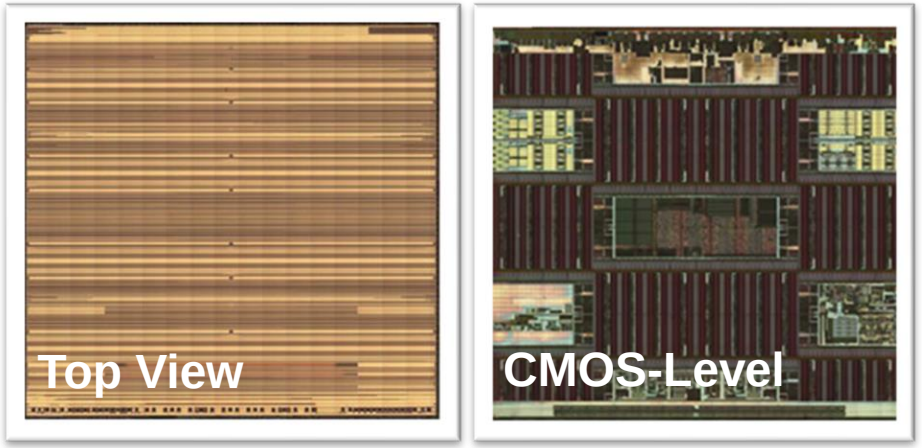
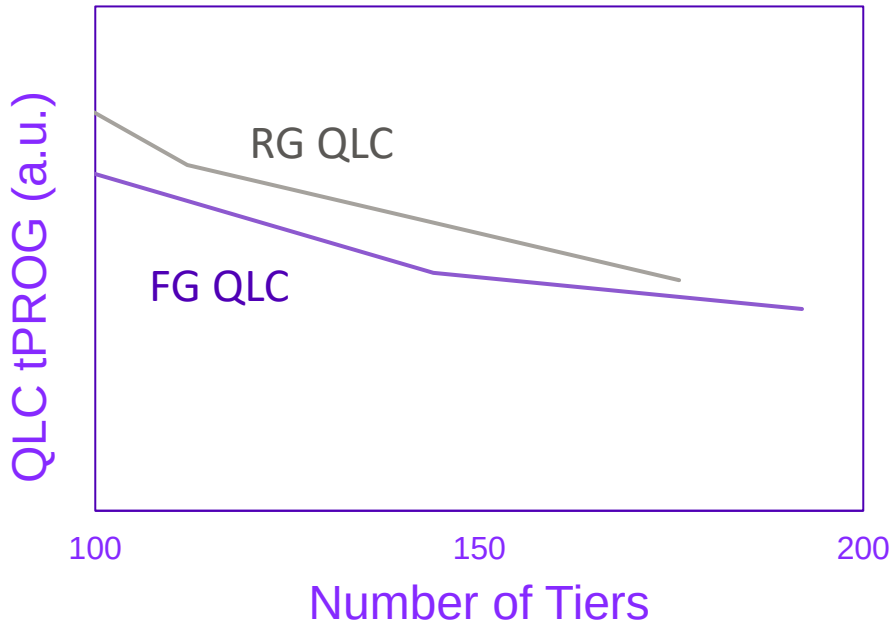
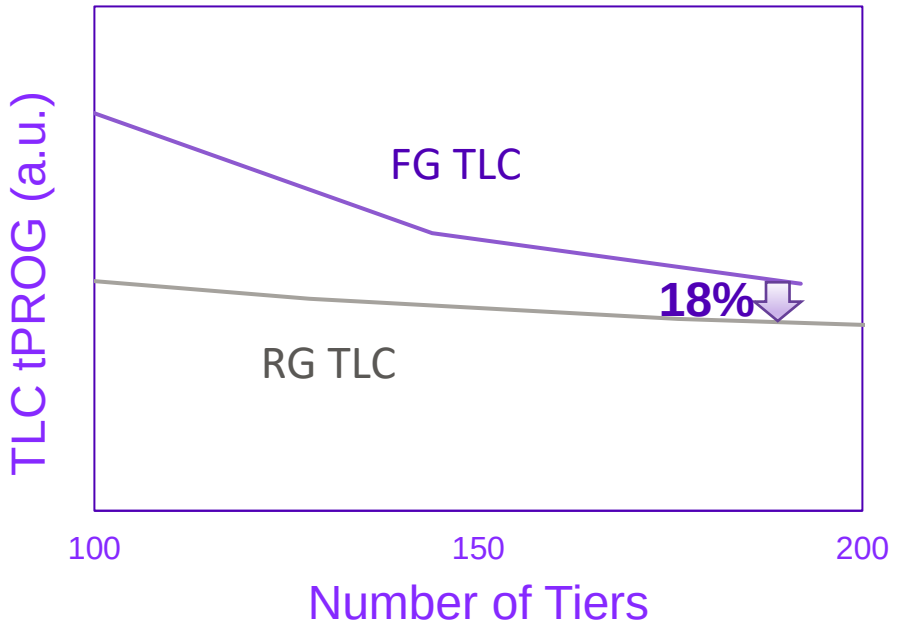


Image courtesy of TechInsights

Performance Comparison

- RG technology offers higher TLC performance, enabled by choice of smaller die (shorter BLs) and lower WL RC delay
  - State-of-the-art RG is ~18% faster than FG technology
- For QLC, the choice of program algorithm (4-16 vs 16-16) compensates for the higher WL RC delay of FG technology
  - FG is actually faster than RG





Source: Solidigm internal research

Conclusion: Optimizing for Diverse Market Segments

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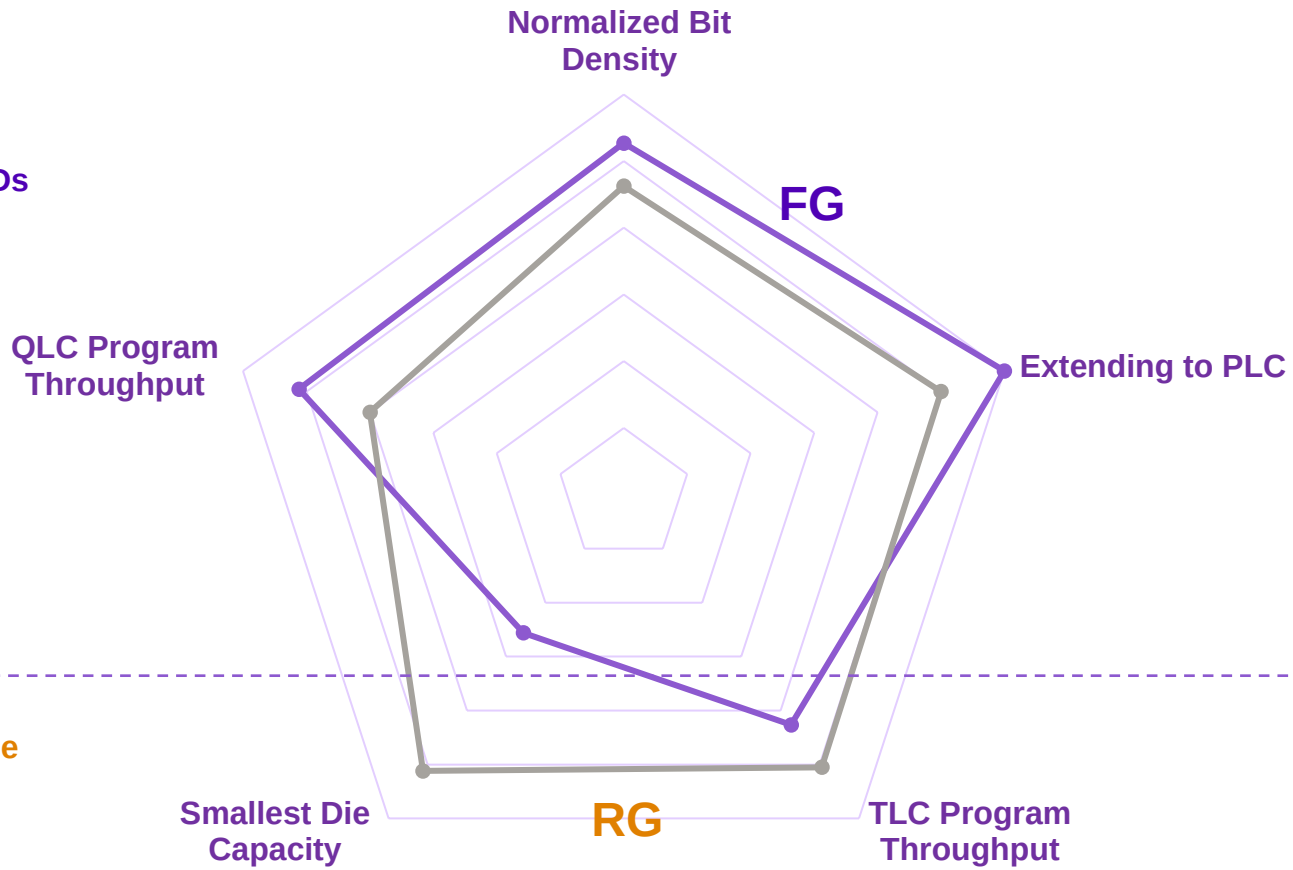
Having access to both technologies can enable independent delivery of optimized QLC/PLC bit density at higher capacities and, at the same time, deliver competitive bit density and higher performance at lower TLC capacity in parallel

FG: Lowest Cost per Bit
Best for High-Capacity QLC/PLC SSDs



RG: High-Performance TLC
Best for Small capacity SSDs / Mobile

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Solidigm at Flash Memory Summit 2022

Flash Memory Summit

Find us at booth 509!

Tuesday	Wednesday	Thursday
QLC Value With No Compromise 8:30 a.m. • Ballroom B (Session DCTR-101-1) **Keynote** 2:10 p.m. • Mission City Ballroom **Unlocking a Next-Level User Experience in Client/Edge Storage With Software** 3:20 p.m. • Ballroom C (Session EDGE-102-1)	**SSD Firmware Resilience: Approaches and Challenges to Protect Against Emerging Threats** 3:30 p.m. • Ballroom D (Session SECR-202-1) **Using Floating Gate and Replacement Gate Technologies to Address Diverse Storage Market Needs** 3:30 p.m. • Ballroom A (Session SSDS-202-1) **5 Reasons You Should Be Adopting QLC NAND SSDs in Your Data Center Now** 3:30 p.m. • Great America Ballroom K (Session SSDS-202-1)	**Above the Average: A Thoughtful Approach to Client Performance Reporting** 8:30 a.m. • Great America Ballroom K (Session TEST-301-1) **Client Usage: The Need for Speed Beyond High-QD Read** 9:45 a.m. • Great America Ballroom K (Session TEST-301-2) **Expanding Your SSD Assessment Beyond 4 Corners to Make the Best Storage Choice** 3:10 p.m. • Great America Ballroom K (Session TEST-302-2)

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