


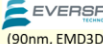




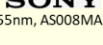



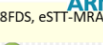















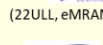




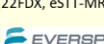


















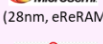




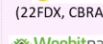








































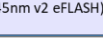




OMEM-102-2: New/Emerging Memories Part 1

Technology Insights: Emerging Memory 2022 and Beyond

***Jeongdong Choe Ph. D.
Senior Technical Fellow
TechInsights***



Emerging Memory Products & Technology

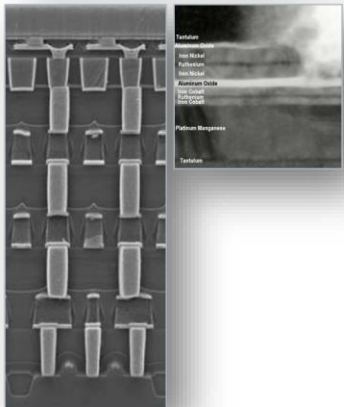
MRAM STT-MRAM	 (180nm, MR2A)	 (90nm, EMD3D64)	 (150nm, HXNV)	  (90nm, CT32)	  (55nm, AS008MA)	  (40nm STT-MRAM)	  (28FDS, eSTT-MRAM)	  (28nm eSTT-MRAM)	  (28 nm, eMRAM)	 (N14/12, eMRAM) * eFLASH RP (4Q21) * Cache RP (4Q22)	  (1X, eSTT-MRAM)
	 (180nm, Toggle)						 (40nm, M10xx, M30xx)		  (22ULL, eMRAM)	 (18FDS, eMRAM)	 (14nm eSTT-MRAM)
	 (Aeroflex, UT8MR)		Ver. ME-2205-01 Jeongdong Choe TechInsights				 (22FFL, eSTT-MRAM)		 (28FDS, 1 Gb)	  (22FDX, eSTT-MRAM)	  (1Gb, 22nm, Aerospace)
										 (xSPI, eSTT-MRAM)	
PCRAM XPoint	 (90nm, NP8P)	 (1Gb PCM+LPDDR2)			 (128Gb, Optane SSD)	 (Optane DC P4800X)	 (Optane DCPM)	 (Optane Barlow Pass PMEM200)	 (Gen.2 Optane P5800X, P1600X SSD)		
	 (65nm, K571229)							 (XPoint: X100 SSD)	 (28nm FD-SOI, ePCM)		
ReRAM Memristor OxRAM CBRAM		 (180nm, MN101 MCU)	 (130nm, RM24)	  (4Mb, MB85AS4MT)	  (40nm, 8Mb)	 (130nm, RM331x)	  (28nm, eReRAM)	 (22nm, eReRAM)	 (40 nm, OxRAM)	 (2X, ReRAM)	  (22FDX, CBRAM)
							 (8Mb, MB85AS8MT)	 (22FFL, eReRAM)	 (1X nm, eReRAM)	 (28nm, ReRAM)	  (28 nm, ReRAM)
FeRAM NRAM	 (130nm, XMS430)	 (180nm, MB89R)		 (130nm, CY15B)	 (LP, MR45V100A)	 (4/8 Mb, MB85R)	 (130nm, Excelon)	  (55nm SPI, NRAM)		  (55nm DDR3, NRAM)	 (40nm DDR4, NRAM)
		 (2Mb, MR45V200B)									
eDRAM (Cache) eFLASH	  (32nm eDRAM)	 (22nm eDRAM)	  (22nm SOI eDRAM)	 (14nm eDRAM)	  (40nm eFLASH)	  (14HP SOI eDRAM)	  (28LP eFLASH)	 (N28 HPC eFLASH)	 (22nm eFLASH)	  (10nm eDRAM)	  (7nm eDRAM)
	 (45nm v1 eFLASH)			  (40nm eFLASH)	  (40nm eFLASH)	 (40ULP eFLASH)	 (28nm eFLASH)		 (28nm Auto G1 eFLASH)		
					 (45nm v2 eFLASH)						

MRAM Products: Examples



Flash Memory Summit

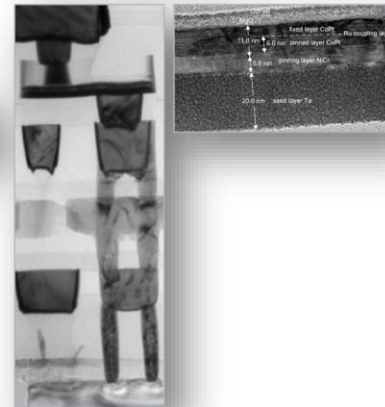
Everspin 1st Gen. MRAM
2006 ~
200mm, Chandler/(Kulim) fabbed
Toggle-mode MRAM
128 Kb ~ 16 Mb
180 nm/90 nm, AlO Based



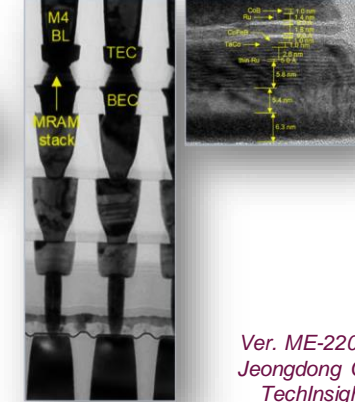
Everspin 2nd Gen. MRAM
2013 ~
300mm, GlobalFoundries
In-Plane STT-MRAM
64 Mb/256 Mb
90 nm, MgO Based



Everspin 3rd Gen. MRAM
2016 ~
300mm, GlobalFoundries
pMTJ STT-MRAM
256 Mb
40 nm, MgO Based

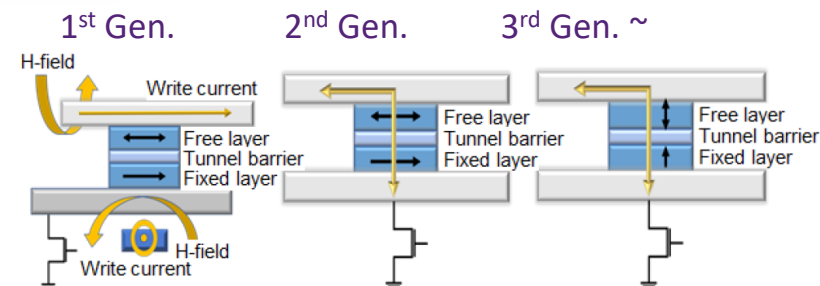
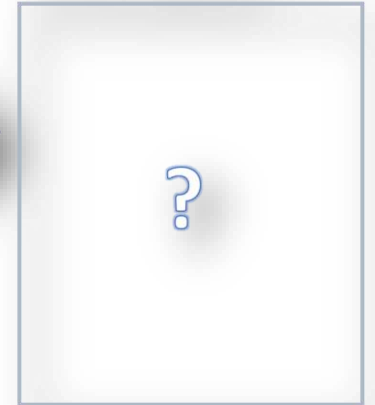


Everspin 4th Gen. MRAM
2019 ~
300mm, GlobalFoundries
pMTJ STT-MRAM
1 Gb
28 nm, MgO Based



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Everspin 5th Gen. MRAM
2021 (2022) ~
300mm, GlobalFoundries
pMTJ STT-MRAM
Embedded (16~48 Mb), Auto
22 nm FDX, MgO Based

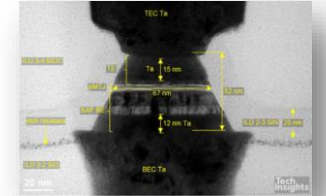


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MTJ/MRAM Structure: Everspin



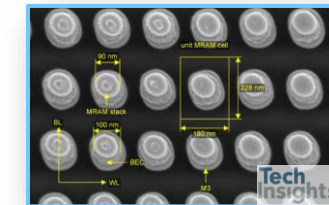
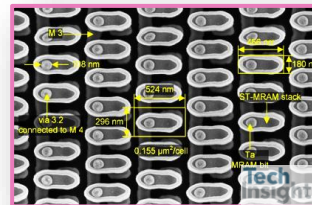
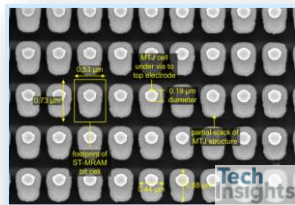
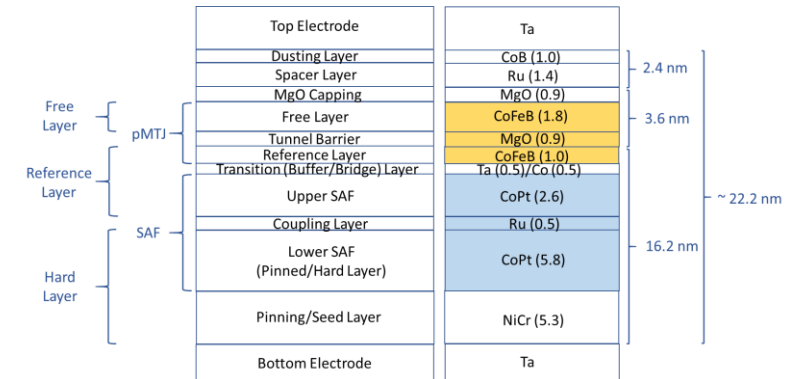
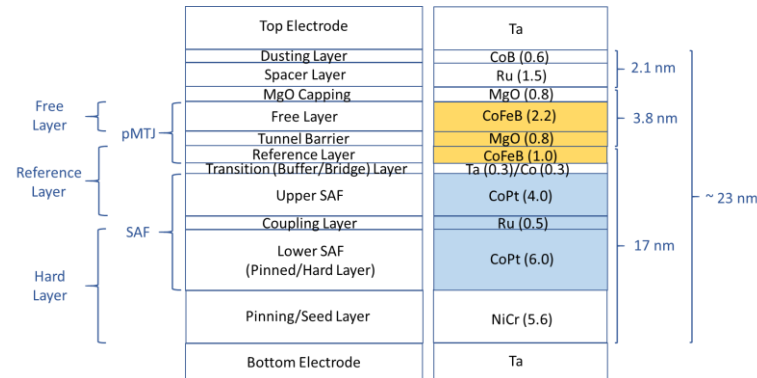
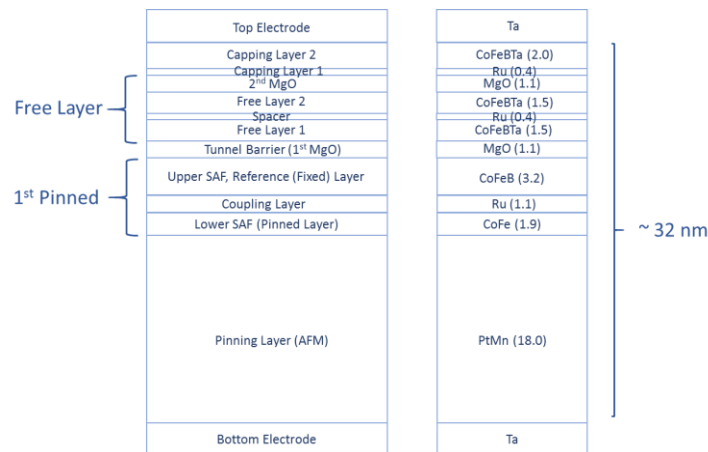
Flash Memory Summit



❑ 2nd Gen. STT-MRAM: In-plane MTJ

❑ 3rd Gen. STT-MRAM: p-MTJ

❑ 4th Gen. STT-MRAM: p-MTJ



- SAF: Synthetic antiferromagnetic structure
- SyF: Synthetic ferromagnetic structure
- DSF: Dual spin filter structure
- DTB: Dual tunnel barrier structure

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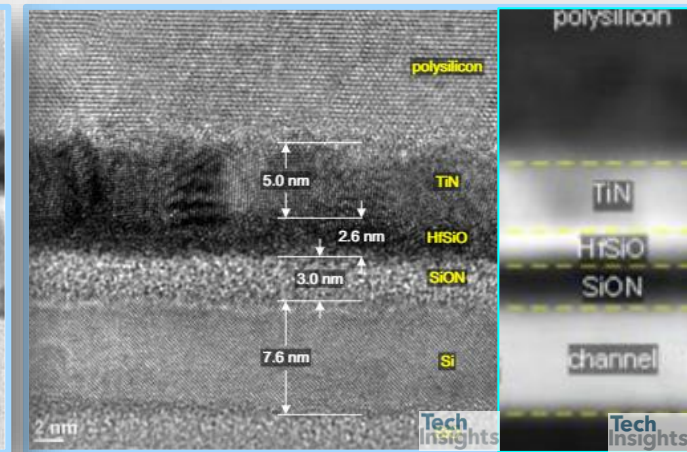
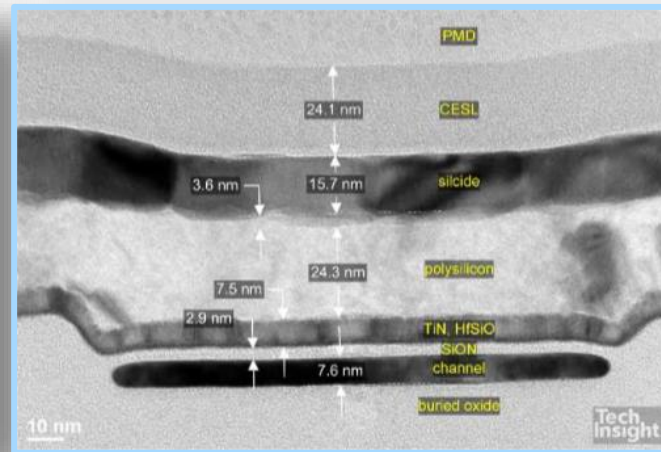
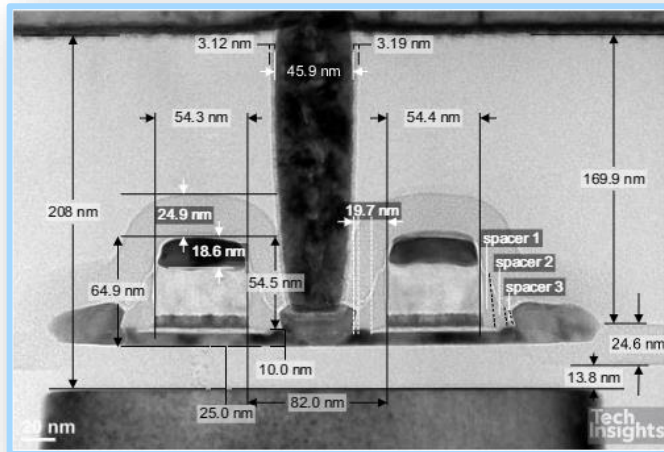
Tech
Insights

Access Gate Structure: Samsung MRAM

- ✓ Samsung FDS SOI & HKMG process
- ✓ BOX=25 nm, SOI channel thickness=7.6 nm
- ✓ GOx: HfSiO/SiON
- ✓ Gate: NiPtSi/Poly-Si/TiN, Lg=50 nm
- ✓ Al detected at HfSiO layer just under TiN ¹⁾



Ref.
Everspin 28 nm
MRAM Cell Gate
(NiPtSi/Si/TiAl/TiN/(La)HfON/SiO)



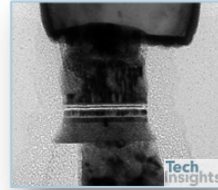
¹⁾ Al additives affect reliability (TDD). Al addition in PMOS devices increases the T_{BD} , which is caused by a decrease in the leakage current with Al dose. This current reduction is responsible for lower defect creation in the gate oxide, and thus for the higher breakdown time T_{BD} .

MRAM/pMTJ Structure: Avalanche vs. Everspin vs. Samsung



Flash Memory Summit

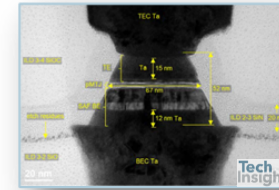
Avalanche



Top Electrode	Ta
Capping Layer	Ru (7)
Capping Layer	Ta (1.1)
Upper Free Layer	CoFeB (0.9)
Spacer Layer	MgO (1.1)
Lower Free Layer	CoFeB (1.1)
Tunnel Barrier	MgO (1.1)
Reference Layer	CoFeB (1.3)
Transition (Buffer/Bridge) Layer	CoIr (0.7)
Upper SAF	Co/Pt (3.0)
(Interleaved layer: Pt)	Cr/Fe (1.6)
Lower SAF	
Seed Layer	Ir (3.4)
Bottom Electrode	Ta

VS.

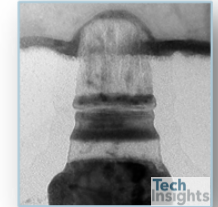
Everspin



Top Electrode	Ta
Dusting Layer	CoB (1.0)
Spacer Layer	Ru (1.4)
MgO Capping	MgO (0.9)
Free Layer	CoFeB (1.8)
Tunnel Barrier	MgO (0.9)
Reference Layer	CoFeB (1.0)
Transition (Buffer/Bridge) Layer	Ta (0.5)/Co (0.5)
Upper SAF	CoPt (2.6)
Coupling Layer	Ru (0.5)
Lower SAF	CoPt (5.8)
(Pinned/Hard Layer)	
Pinning/Seed Layer	NiCr (5.3)
Bottom Electrode	Ta

VS.

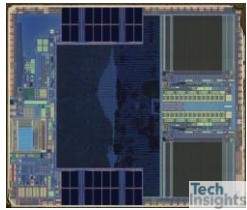
Samsung



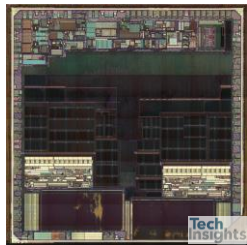
TE	TiN
Capping-1	Ru (2.3 nm)
Capping-2	Ta (1.3 nm)
Capping-3	Ru (1.6 nm)
Spin-Engineered	TaO (1.2 nm)
Free Layer	CoFeB (1.1 nm)
TB Layer	MgO (1.0 nm)
Pinned-1 Layer	CoFeB (0.5 nm)
Separation Layer	W (0.7 nm)
Pinned-3 Layer	CoIr (3.1 nm)
Pinned-2 Layer	CoPt (1.5 nm)
Pinning Layer	Ru (4.6 nm)
Seed Layer	Ta (5.6 nm)
BE	TiN

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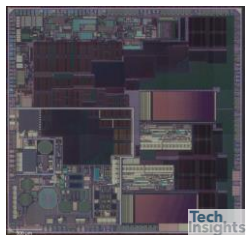
eFLASH vs. eMRAM: Ambiq Apollo MCU Series



Apollo

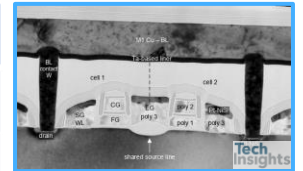


Apollo2

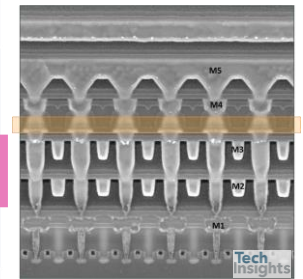


Apollo3

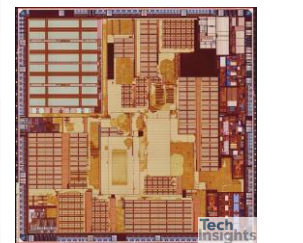
Device	Ambiq Apollo Blue MCU	Ambiq Apollo2 Blue MCU	Ambiq Apollo3 Blue MCU	Ambiq Apollo4 Blue MCU
Product Example	Misfit Shine 2 Fitness	Huawei ERS-B29 Band 2 Pro	Huawei TER-B19 Band 3 Pro	Fitbit Luxe (Fitness Band)
Package Markings	APOLLO	AMAPH	AMA3B	AMA4B
Supply Current	35 μ A/MHz (eFLASH)	10 μ A/MHz (eFLASH)	6 μ A/MHz (eFLASH)	3 μ A/MHz (eMRAM)
Die Markings	ambiq apollo 1 2014	apollo 2 ambiq micro 2016	apollo 3 ambiq micro 2017	apollo 4 ambiq 2020
Die size (seal)	6.98 mm ² (2.86 mm x 2.44 mm)	6.43 mm ² (2.55 mm x 2.52 mm)	10.72 mm ² (3.21 mm x 3.34 mm)	15.56 mm ² (3.95 mm x 3.94 mm)
CMOS Process	90 nm	40 ULP	40 ULP	22 ULL
Foundry	TSMC	TSMC	TSMC	TSMC
Number of Metals	7 (6 Cu, 1 Al)	8 (7 Cu, 1 Al)	9 (8 Cu, 1 Al)	10 (9 Cu, 1 Al)
Logic Gate Pitch (min.)	740 nm	170 nm	170 nm	120 nm (HKMG)
Embedded Memory	eFLASH (2D NOR ESF3)	eFLASH (2D NOR ESF3)	eFLASH (2D NOR ESF3)	eMRAM
eMemory Gate Pitch	300 nm	250 nm	230 nm	110 nm
Bit Cell Size	0.087 μ m ²	0.068 μ m ²	0.068 μ m ²	0.046 μ m ²
eMemory Area Portion & Capacity	19.7 %, 4 Mb	14 %, 8 Mb	9 %, 8 Mb	10.4 %, 16 Mb



40 nm eFLASH 2D NOR ESF3 Cell (Apollo3)



22 nm eSTT-MRAM Cell (Apollo4)



Apollo4

MRAM: Samsung, Avalanche, Everspin, TSMC

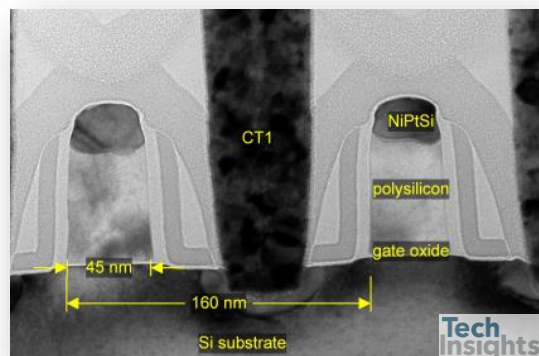
Device	Samsung MRAM	Avalanche MRAM	Everspin MRAM	TSMC MRAM
Parent Products	Sony CXD5605 GPS Receiver @ Huawei GT 2 Smartwatch	Renesas M3008204 (Avalanche AS3008204)	EMD3D256M08G1	Ambiq Apollo4 2M AMA4B Fitbit Luxe (Fitness Band)
Memory Block Capacity	8 Mb (embedded)	8 Mb (embedded)	256 Mb (Stand-alone Die)	16 Mb (embedded)
Device Type	STT-MRAM	STT-MRAM	STT-MRAM	STT-MRAM
Technology Node (CMOS Process)	28 nm	40 nm	40 nm	22 nm
Cell Size	0.036 μm^2	0.032 μm^2	0.155 μm^2	0.046 μm^2
MTJ Type	P-MTJ (perpendicular)	P-MTJ (perpendicular)	P-MTJ (perpendicular)	P-MTJ (perpendicular)
MRAM Layer	Between M6 and M7	Under M1 SL	Between M3 and M4	Between M3 and M4
Die Markings	S4LP173	AV16B	EMD3D256M WHITNEY	apollo 4 ambiq 2020
# Metal Layers	11	7	5	10



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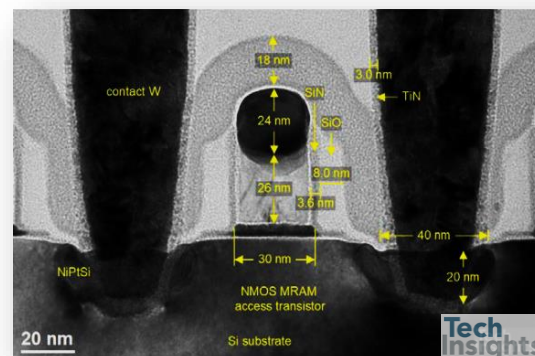
MRAM Cell Gate Structure

Avalanche 40nm



- NiPtSi/Poly-Si Gate
- SiO(2.0nm) GOx
- Lg=45nm
- L-shape SiN Spacer

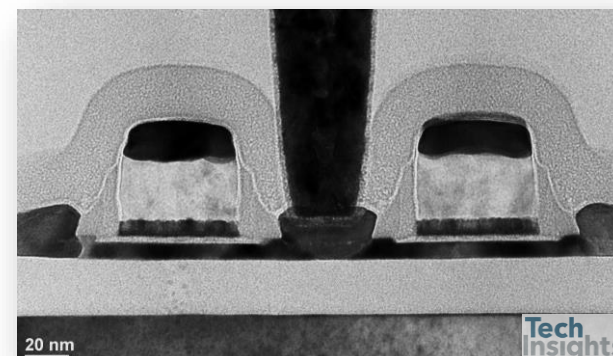
Everspin 28nm



- Gate-First, HKMG
- NiPtSi/Poly-Si/TiAl/TiN Gate
- La-doped HfON/SiO GOx
- Lg=30nm

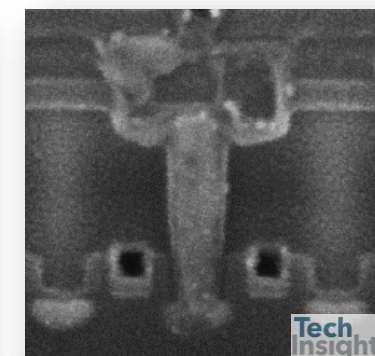
Ref. PMOS: HfON/SiO/SiGe

Samsung 28nm



- Gate-First, HKMG
- NiPtSi/Poly-Si/TiN Gate
- HfO/SiON GOx
- SOI(7.6nm)/BOX
- Lg=50nm

TSMC 22nm



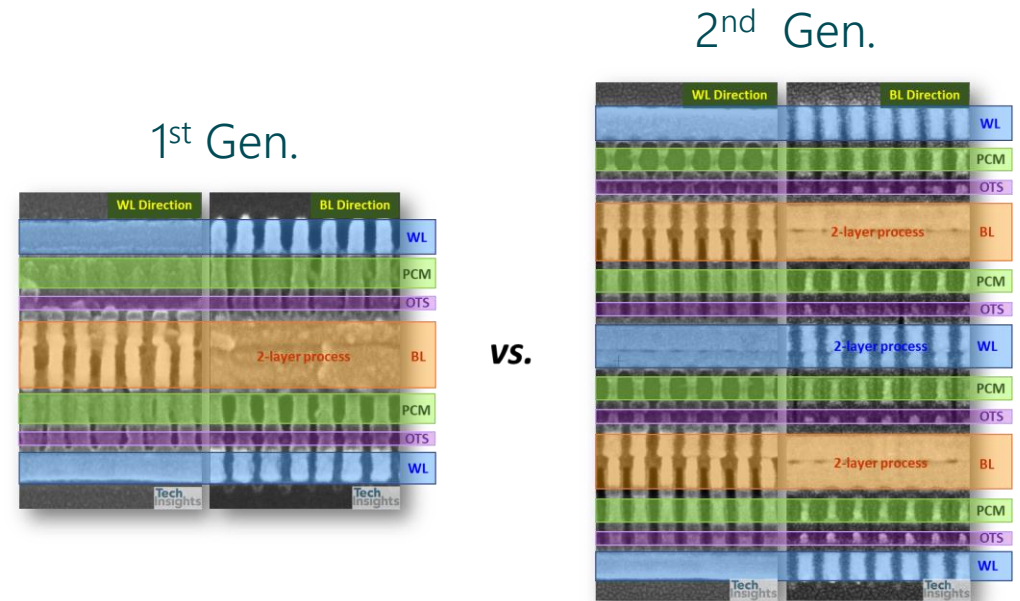
- Gate-Last, HKMG
- NiPtSi/Poly-Si/TiN Gate
- HfO/SiON GOx
- Lg=28nm

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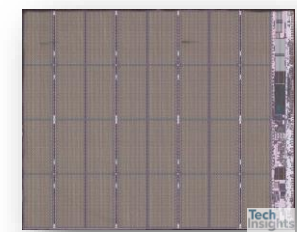
Intel XPoint Memory: Gen1 vs. Gen2

XPoint Memory	1 st Gen.	2 nd Gen.
Parent Product (Ex.)	Intel Optane DC P4800X SSD	Intel Optane DC P5800X SSD
Storage Device	29P16B1BLDNF2 (single-die package)	29P64B14MDSG1 (two-die package)
Process (Tech. Node)	XPoint 1 st gen. (20nm)	XPoint 2 nd gen. (20nm)
Die Markings	S15C	S26A
Memory Capacity (Die)	128 Gb	256 Gb
Die Size	206.5 mm ²	195.6 mm ²
Bit Density	0.62 Gb/mm ²	1.31 Gb/mm ²
Unit Cell Size	1,600 nm ²	1,600 nm ²
# Metals (excluding WLs/BLs)	5 (4 Cu, 1 Al)	5 (4 Cu, 1 Al)
Cell Design (Effective)	2F ²	1F ²
Memory Structure	2-stack array between M4 and M5 (WL/BL/WL)	4-stack array between M4 and M5 (WL/BL/WL/BL/WL)
Pitch (WL, BL)	40 nm, 40 nm	40 nm, 40 nm
# Bond Pads (Die)	81	85
Memory Array Efficiency	57.8 %	67.4 %

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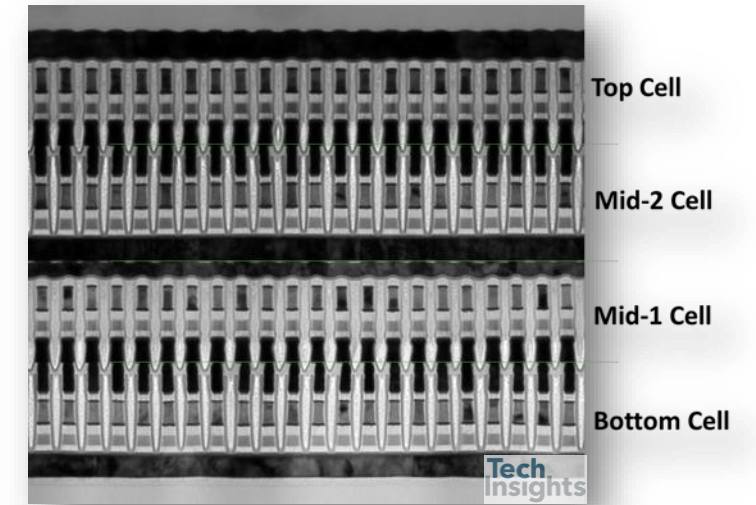
128 Gb Die



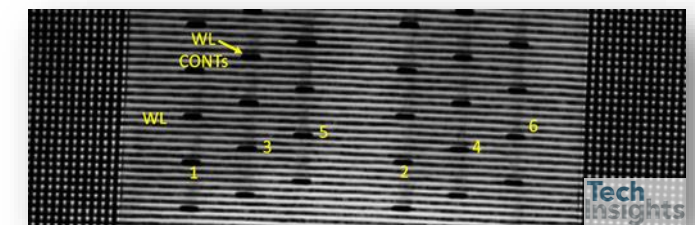
256 Gb Die

Intel XPoint Memory: Gen1 vs. Gen2

XPoint Memory	Gen1	Gen2
Stack	WL2/PCM/OTS/BL/PCM/OTS/WL1	WL3/PCM/OTS/BL2/PCM/OTS/WL2/PCM/OTS/BL1/PCM/OTS/WL1
PCM Materials, Thickness	In-doped GST, 37 nm	In-doped GST, 33 nm
PCM Capping Layer, Thickness	W, 4.3 nm	W, 4.7 nm
OTS Materials, Thickness	In-doped GeAsSe, 14 nm	In-doped GeAsSe, 18 nm
Middle electrode, Thickness	Amorphous carbon, ~ 16 nm	Amorphous carbon, 9 ~ 13 nm
WL/BL Diffusion Barrier	WN, 4.7 nm	WN, 5.1 nm
WL/BL Patterning	DPT, SADP	DPT, SADP
1 bit Cell Height	Ver. ME-2201-01 Jeongdong Choe TechInsights 180.4 nm / 205.5 nm (upper / lower)	190 nm / 190 nm / 170 nm / 190 nm (Top / middle-1 / middle-2 / bottom)
Unit Cell size	1,600 nm ²	1,600 nm ²
WL & BL CONT Size	100 nm x 20 nm (3 + 3, Alternative)	100 nm x 20 nm (3 + 3 Alternative)
WL/BL Interconnection (Sub-via)	WL CONT, BL CONT, 3 landing plugs (max.)	WL CONT, BL CONT, 3 landing plugs (max.)
LV TR Lg (min. measured), Gox	Lg=71 nm T _{Gox} =2.5 nm SiON/SiO	Lg=76 nm T _{Gox} =2.0 nm SiON/SiO
HV TR Lg (min. measured), Gox	Lg=280 nm T _{Gox} =11 nm SiON/SiO	Lg=390 nm T _{Gox} =8.9 nm SiON/SiO
Gate Structure	Co-silicide/As-doped poly-Si	Co-silicide/As-doped poly-Si
STI Depth (max. measured)	370 nm	360 nm



Gen2 Cell Structure



Gen2 WL CONT Layout

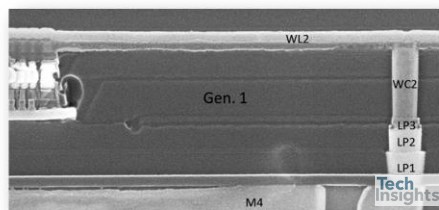
Intel XPoint Memory: Gen1 vs. Gen2



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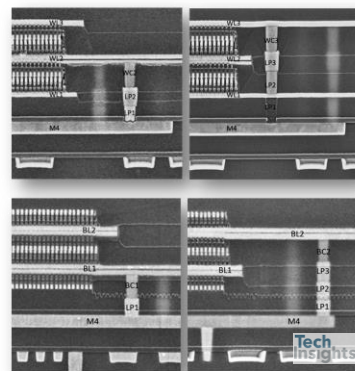
Landing Pads

- ✓ 3 Landing Pads: LP1, LP2, LP3 on M4
- ✓ WL & BL CONTs: WC1, WC2, WC3, BC1, BC2



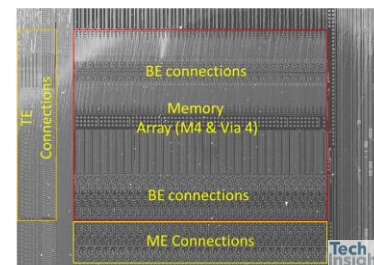
XPoint 1st Gen. 2-stack cell structure

VS.



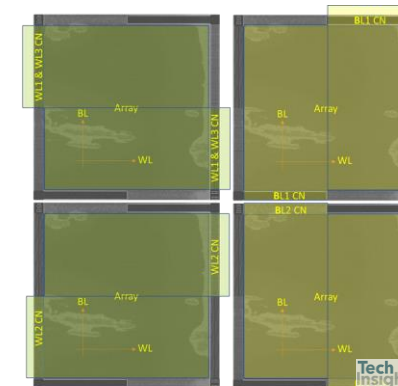
XPoint 2nd Gen. 4-stack cell structure

Interconnection



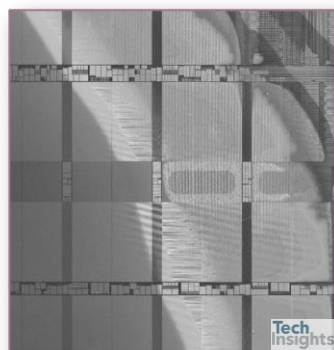
Gen1 WL/BL Interconnection Location

VS.



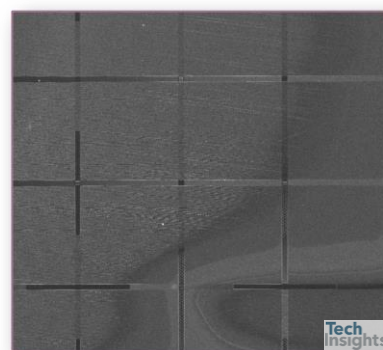
Gen2 WL/BL Interconnection Location

Dummy Blocks



Gen1 XPoint Cell Array blocks

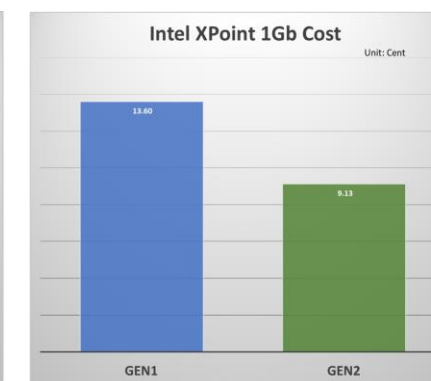
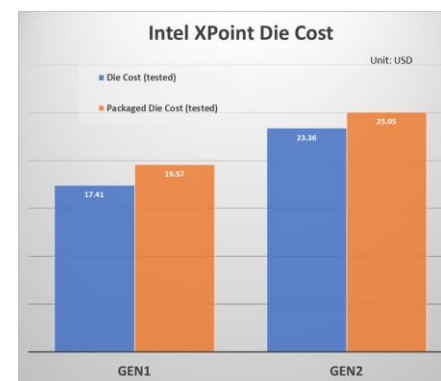
VS.



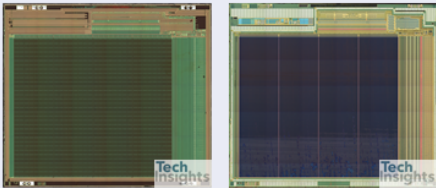
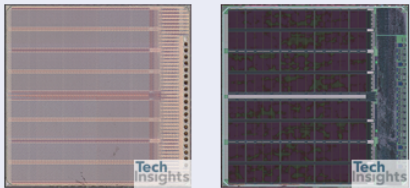
Gen2 XPoint Cell Array blocks

Cost

Cost Model Ver. 4Q-2020



FRAM Products: Fujitsu vs. Cypress

FRAM	Fujitsu Serial FRAM		Cypress Excelon FRAM
Product Example	MB85RS2MT	MB85RS2MTY	CY15V104QSN Excelon Ultra
Memory Capacity	2 Mb	2 Mb	4 Mb
Supply Voltage (VDD)	1.8 V ~ 3.6 V	1.8 V ~ 3.6 V	1.71 V ~ 1.89 V
Logic Process Node	180 nm	130 nm	130 nm
Die Size / Bit Density	11.75 mm ² (0.17 Mb/mm ²)	6.67 mm ² (0.30 Mb/mm ²)	6.63 mm ² (0.60 Mb/mm ²)
Die Markings	TP8R26 MB85RS2MT	TP8R40 MB85RS2MTY	7C15004B
FRAM Cell Size	2.496 μm ²	0.504 μm ²	0.710 μm ²
CPP (Array/Periphery)	650 nm / 650 nm	480 nm / 650 nm	480 nm / 400 nm
Gate (Lg, Cell Array)	CoSi/Poly-Si (Lg=160 nm)	CoSi/Poly-Si (Lg=90 nm)	CoSi/Poly-Si (Lg=160 nm)
Number of Metal Layers	5 (5 Al)	6 (1 W + 5 Al)	6 (5 Cu + 1 Al)
FCAP Materials	IrO/PZT/Pt	IrO/PZT/Pt	IrO/PZT/Ir
Die Image (Top & Bpoly)			

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Emerging Memory in Future?

- Ferroelectric Memory (FeFET, FTJ)
- ReRAM (Metal Oxide)
- SOT-MRAM
- Carbon Memory (Nanotube, Graphene, a-C)
- ECRAM (Electrochemical RAM)
- DNA Memory
- Mott Memory (Mott Oxide)
- Macromolecular Memory (vs. Molecular Memory)
- *etc. (OTS, Mott Switch, ...)*