



Computational Storage: Leveraging eFPGAs for Application Acceleration

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Flex Your Computing

FPGA has become a strategic technology

flexlogix
AI + eFPGA



Data Centers use FPGAs in Volume

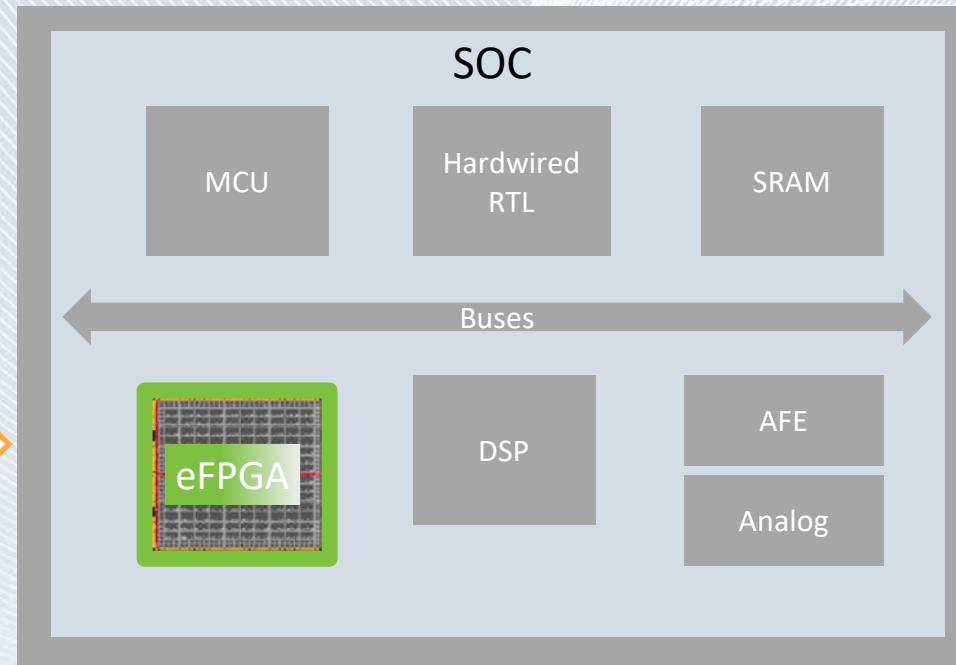
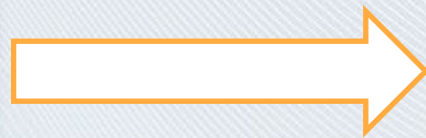
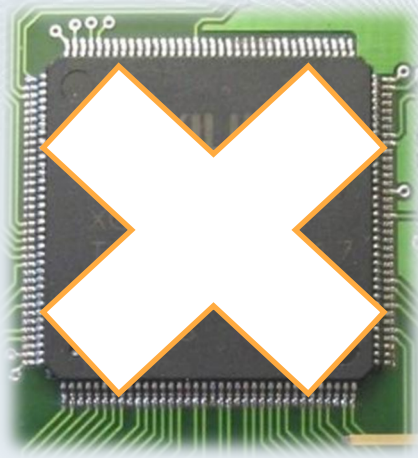
Provide Parallel Programmability to Accelerate Applications

Reduce the movement of Data

Power Problem of FPGA

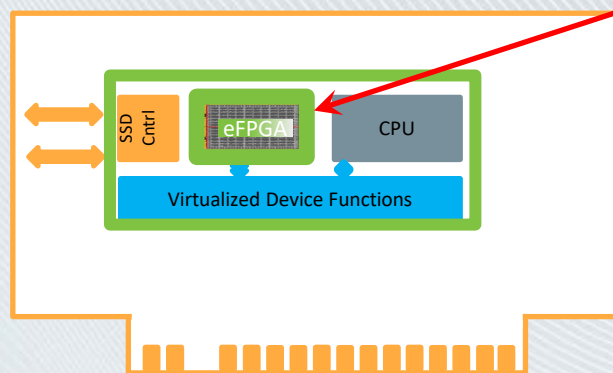
How to Reduce Power?

Integration Has Just Begun



180nm to 5nm

Reprogrammable Processor Will Benefit from Integration



Computational Storage Device

Reconfigure for
different offloads
Integrated into the SOC

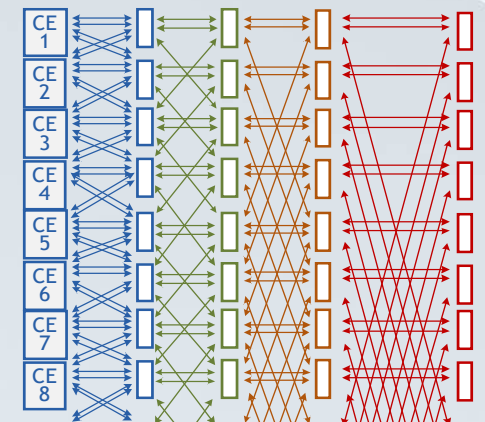
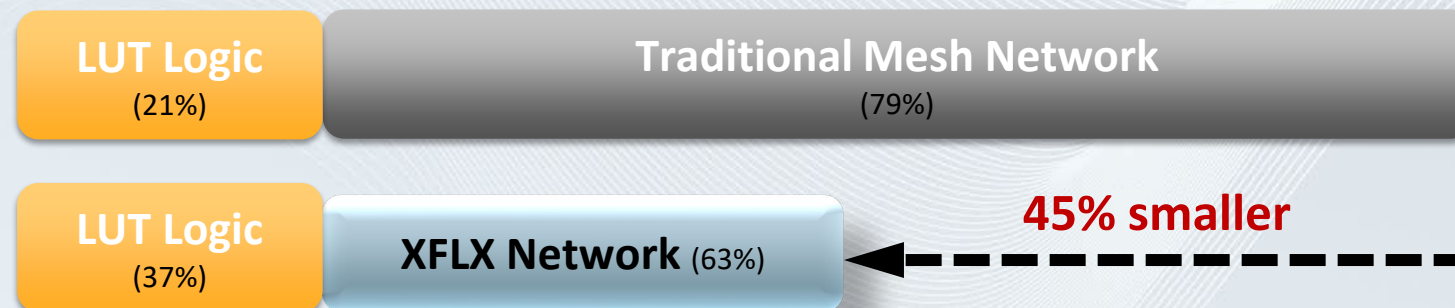


- Lower Power
- Less Heat
- Less Latency
- Smaller Size
- Less Cost

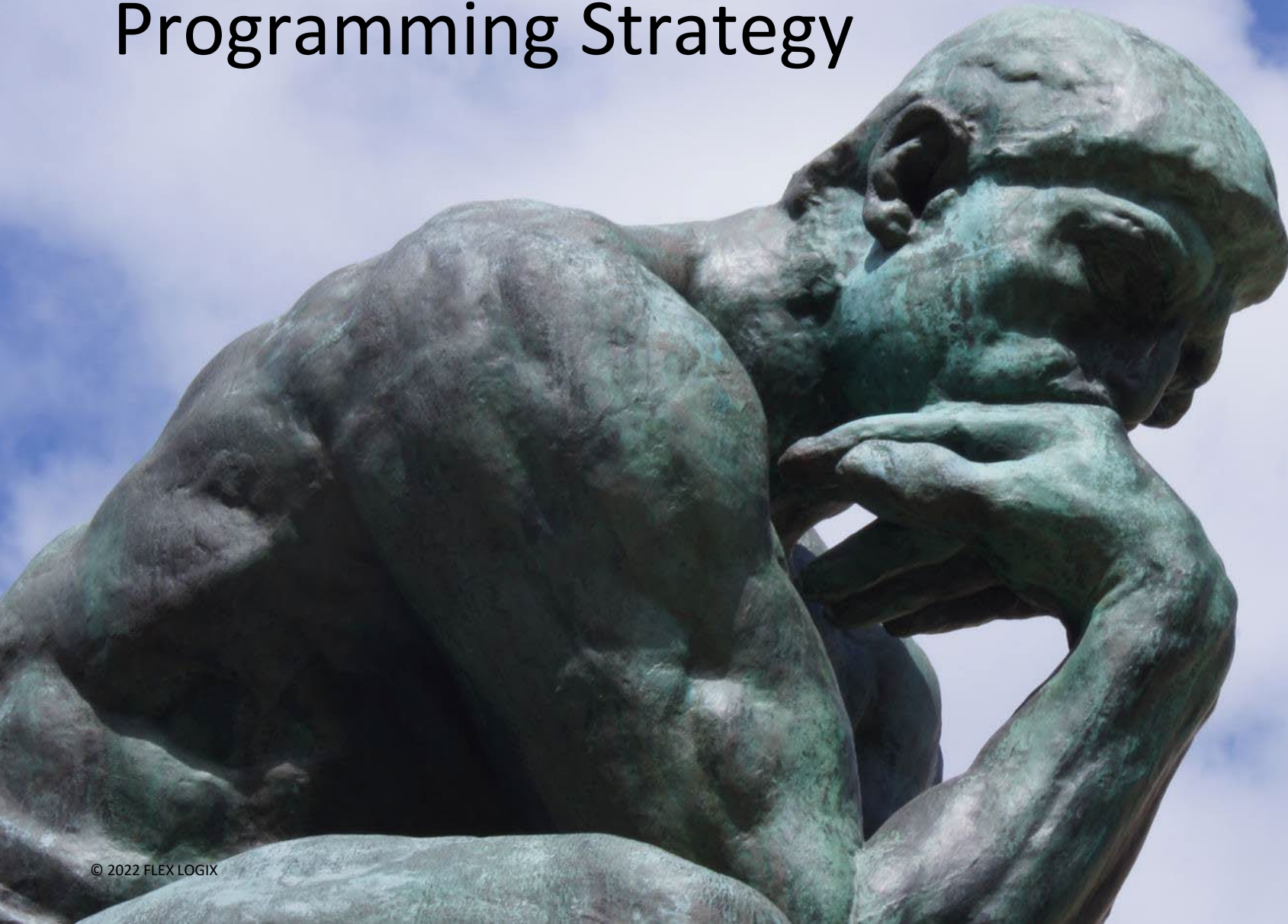
Interconnect Improvements in eFPGAs

Smaller, Faster XFLX™ Interconnect

- ISSCC Best Paper Award
- High logic density and performance: Similar to FPGA chips
 - High utilization : 90%+
- Pure logic process based on std cells

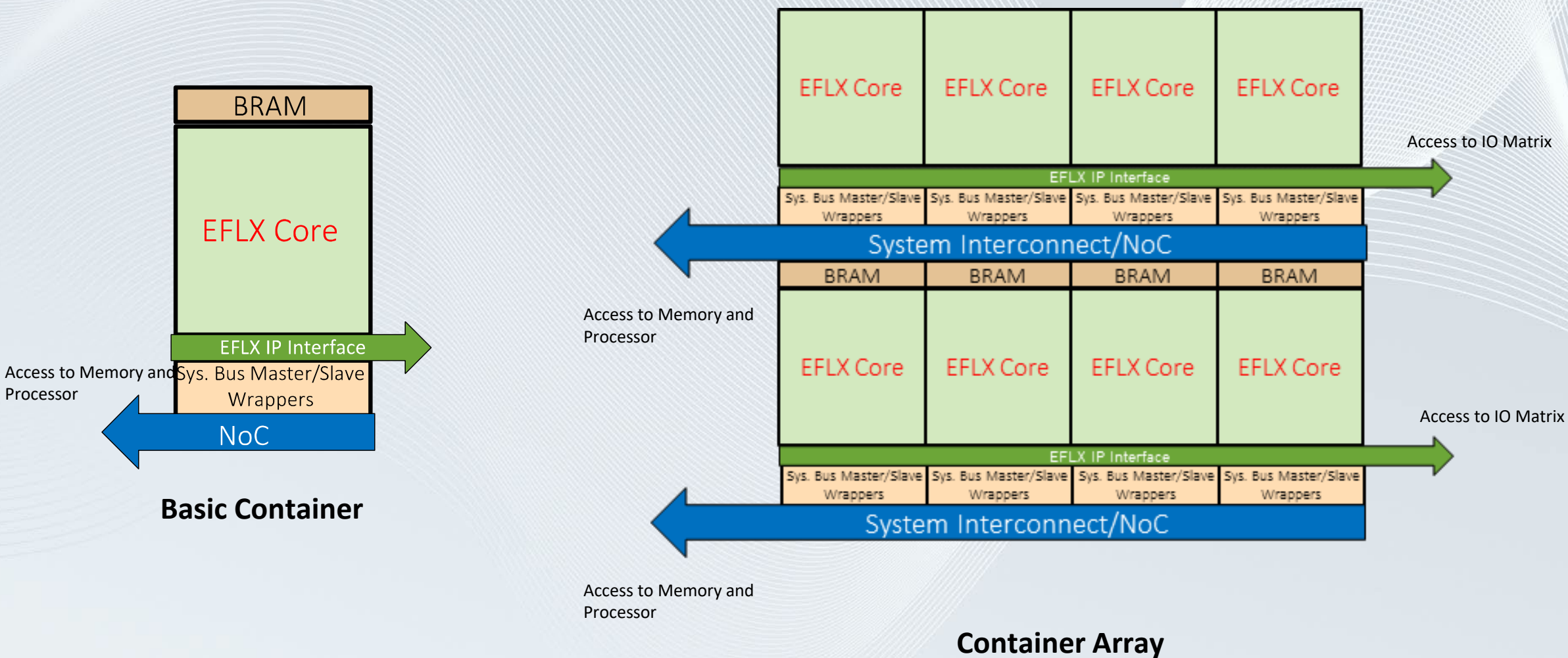


Opportunity to Re-think the eFPGA Programming Strategy

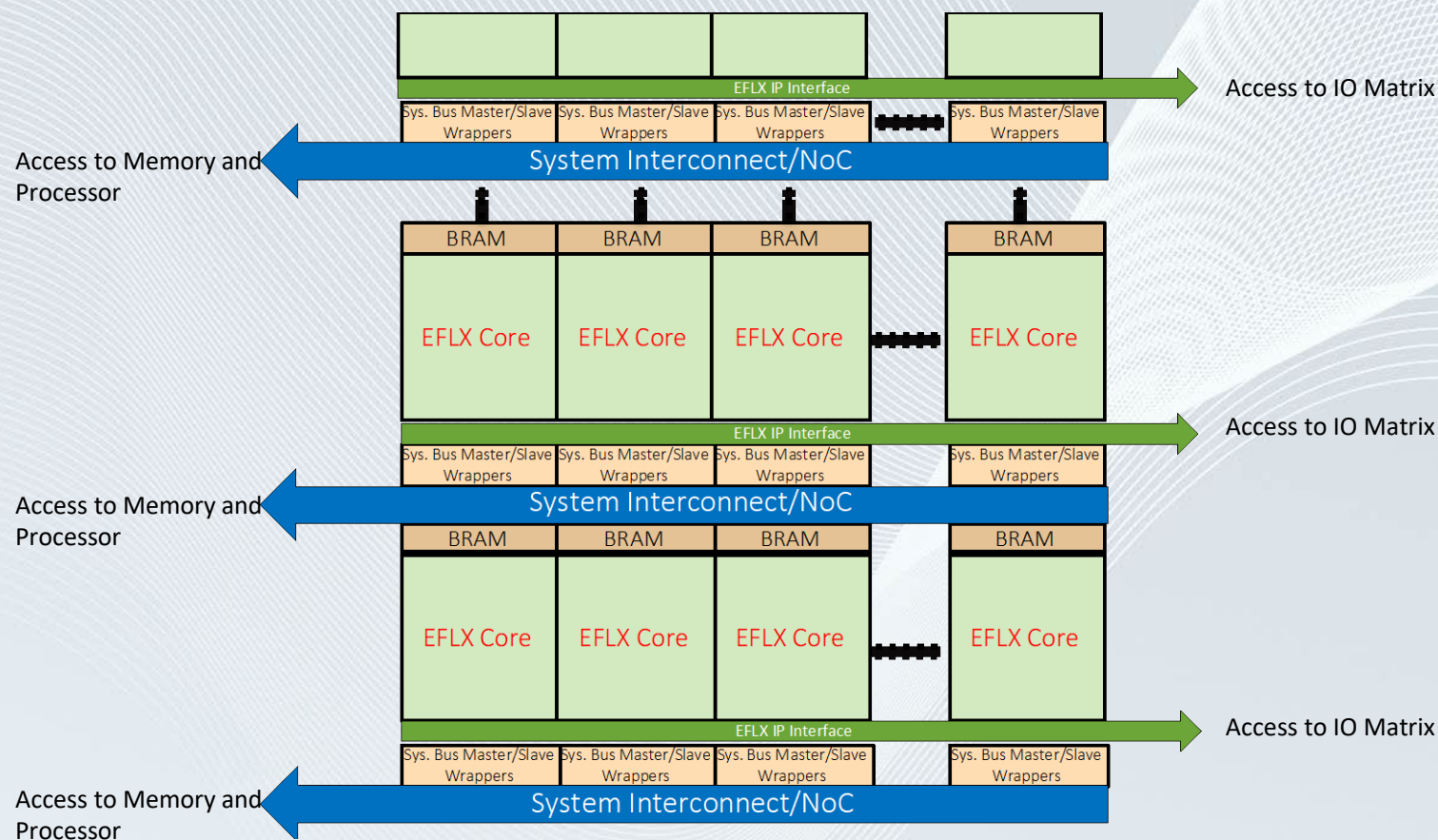


Software
control over the
eFPGA

Containerize Code Into “Subroutines”

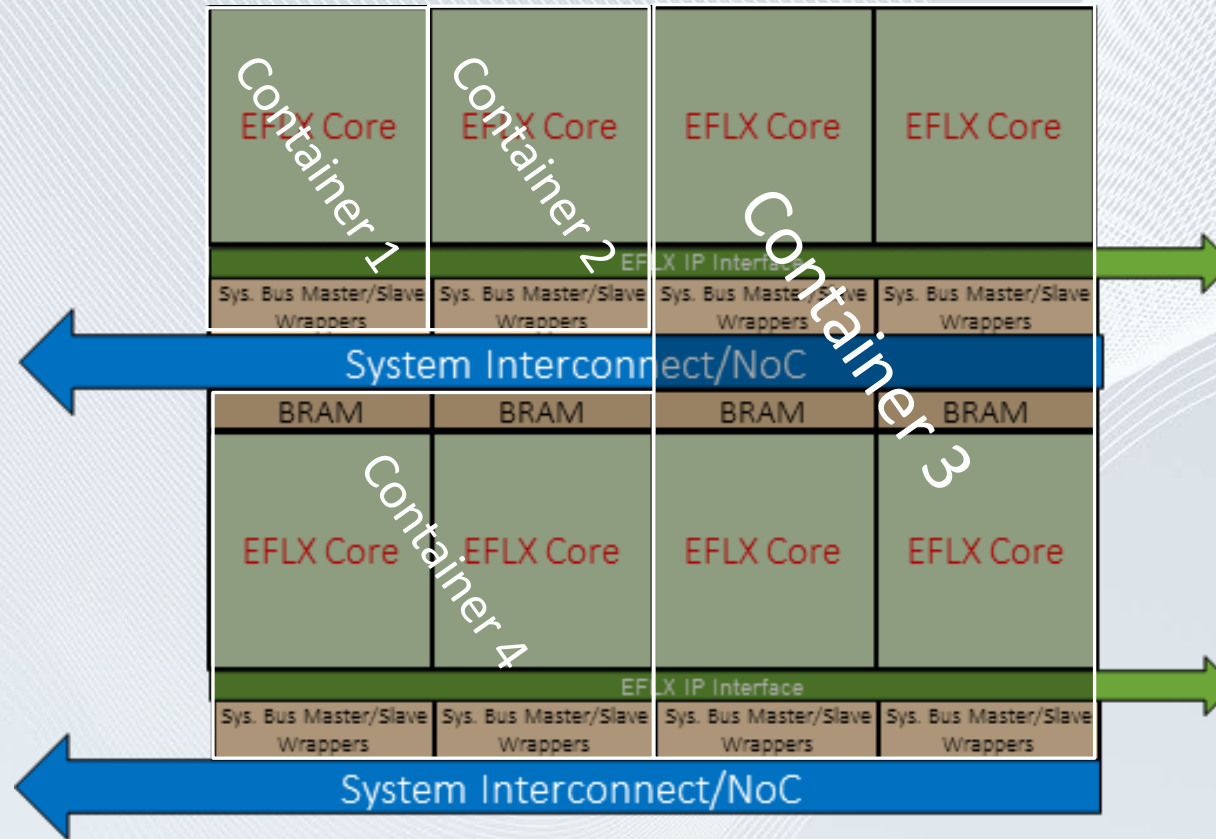


Easy to Build Arrays of Containers of Any Size

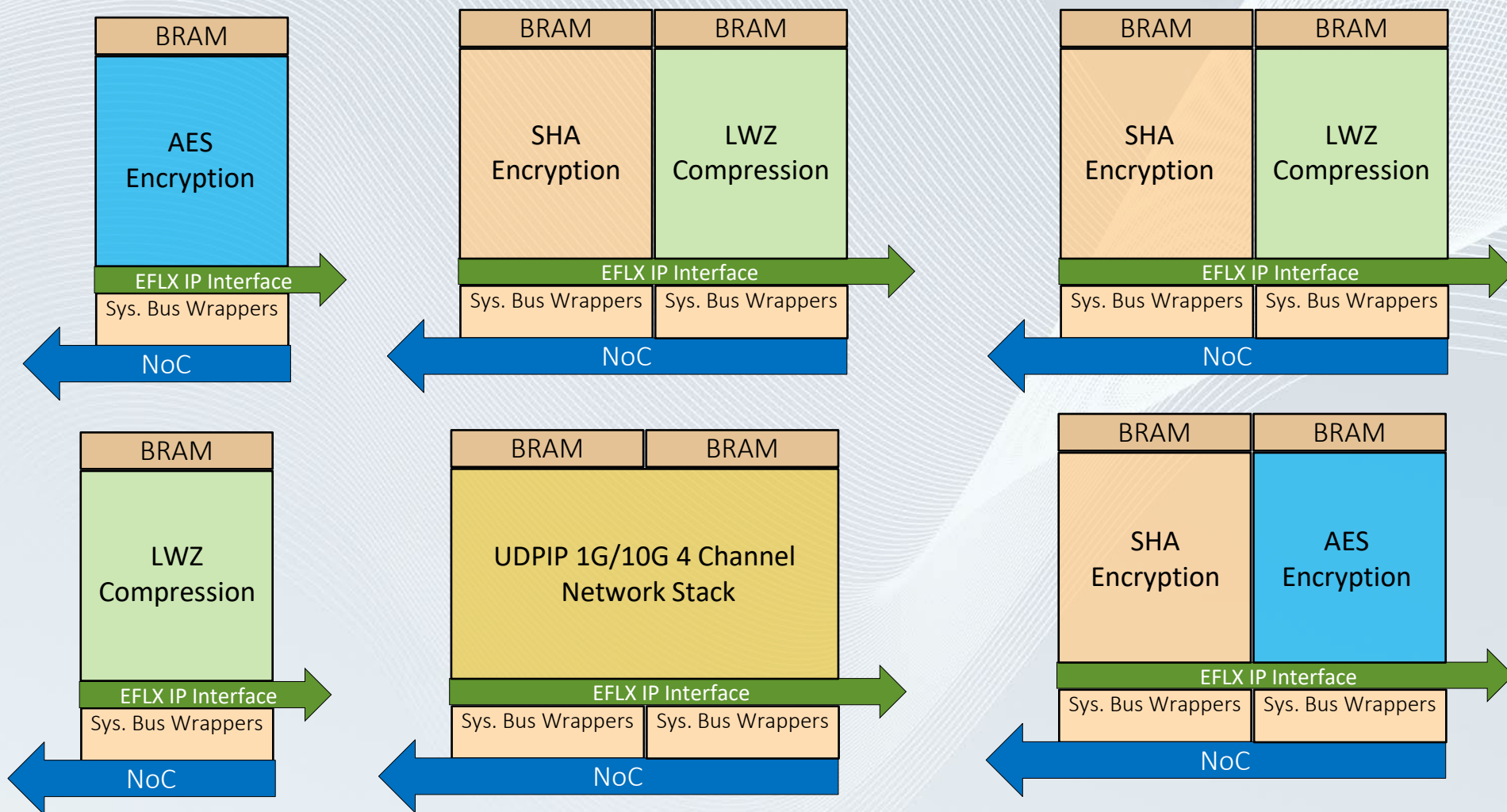


Container Array

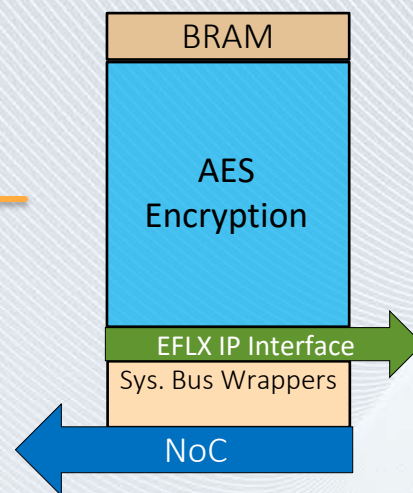
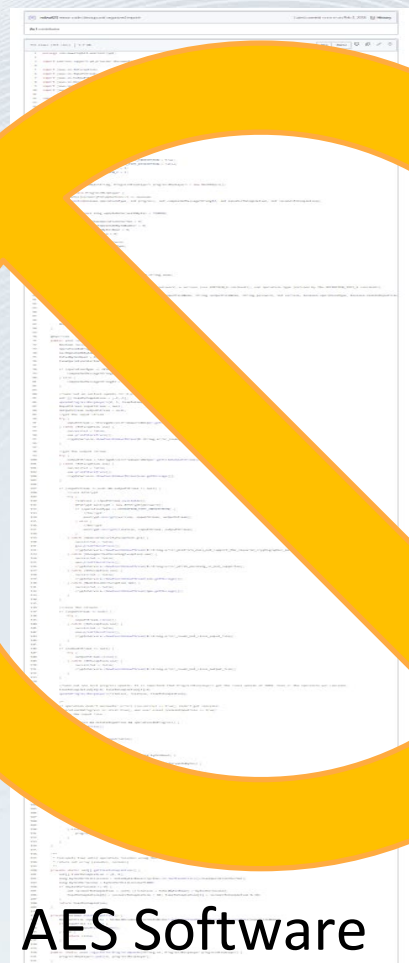
Containers are Variable in Size



Examples of Containerized Accelerators



Software Programming Model



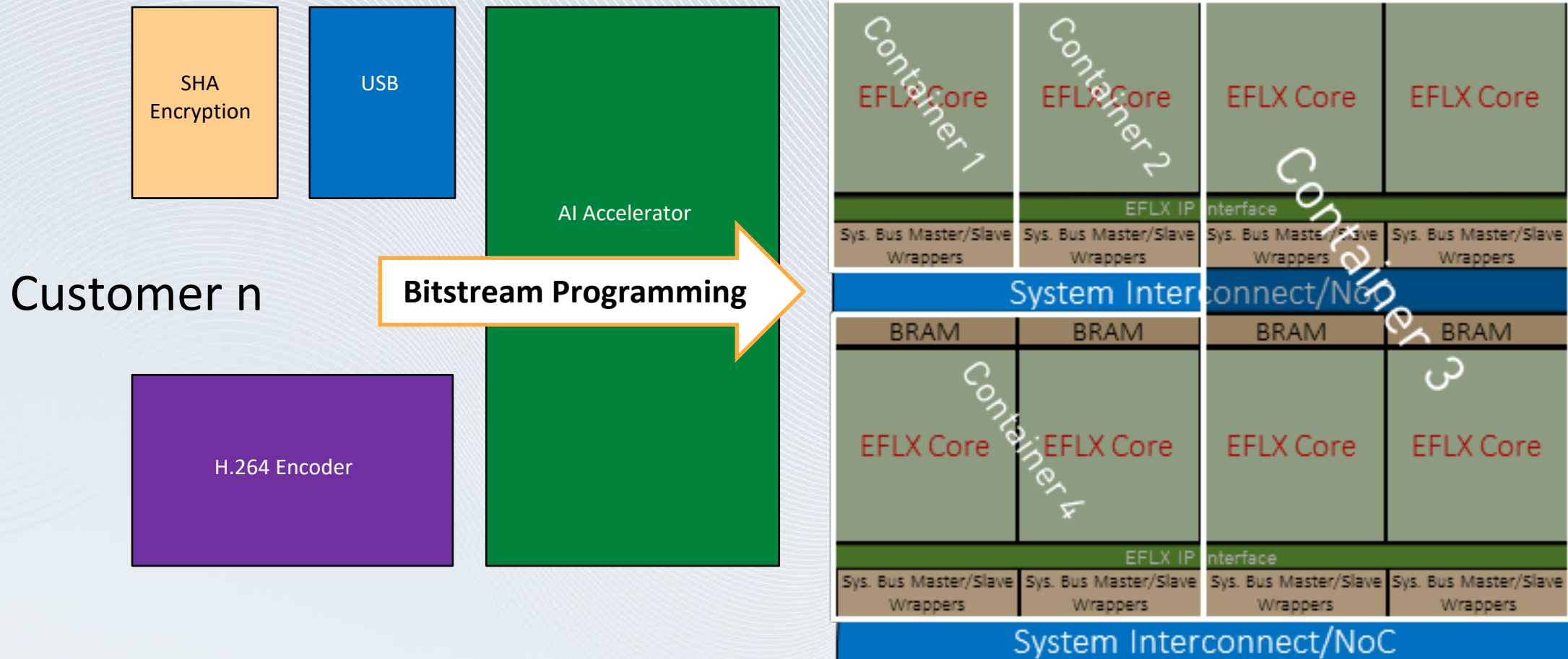
Load(AES)

AES(Filename, parameters)

Hardware

Loaded with One Line of Code

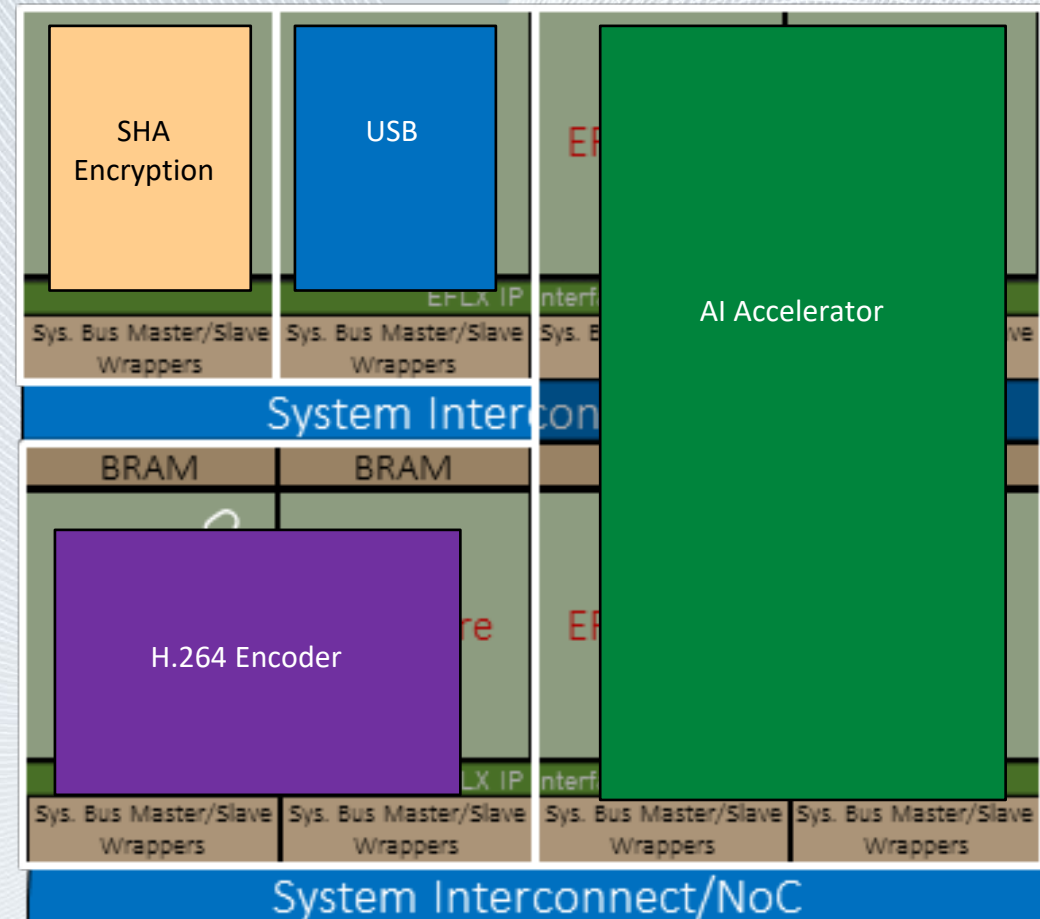
eFPGA Programmed at Boot or Run Time



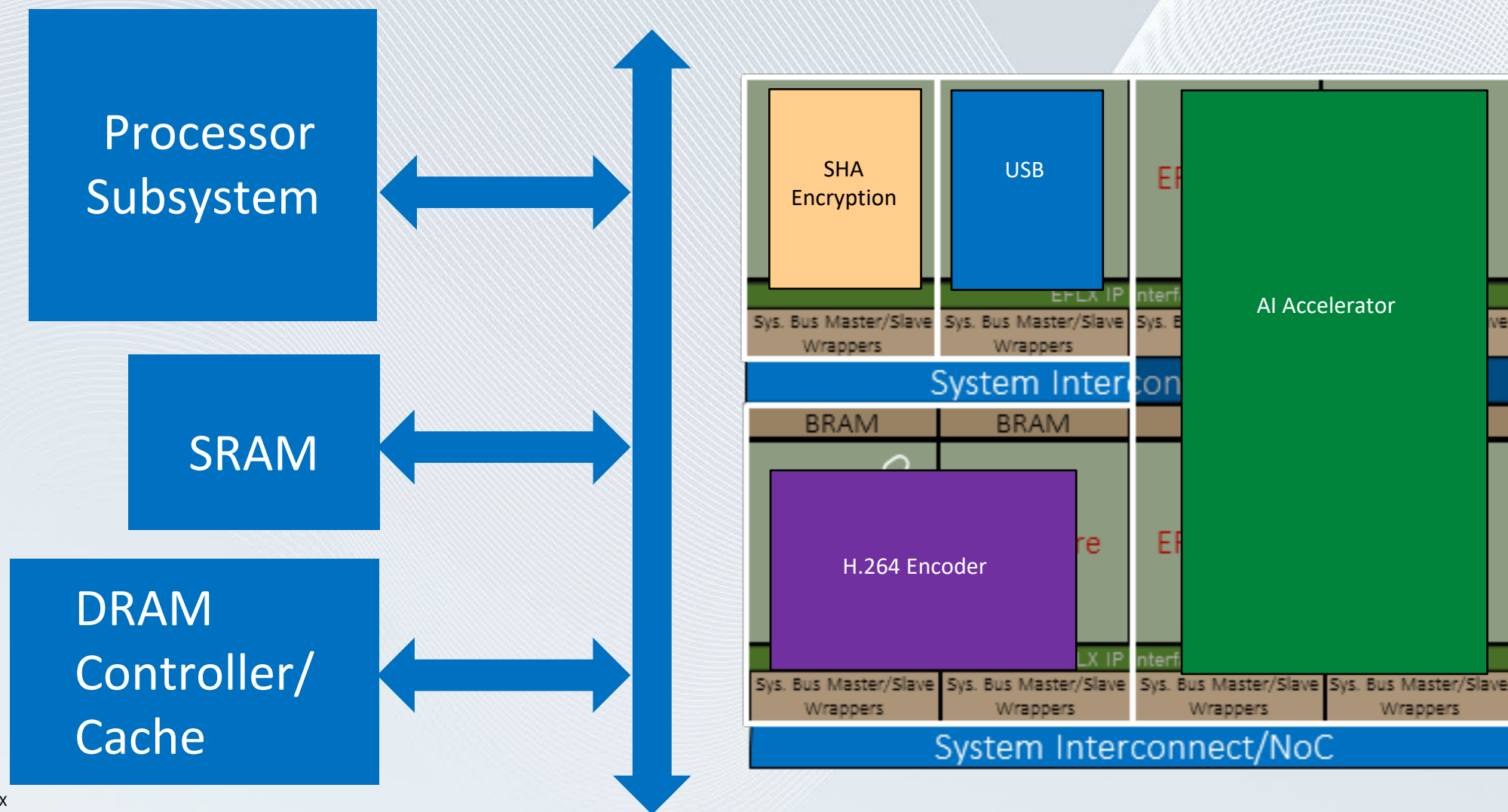
eFPGA Programmed at Boot or Run Time

Customer n

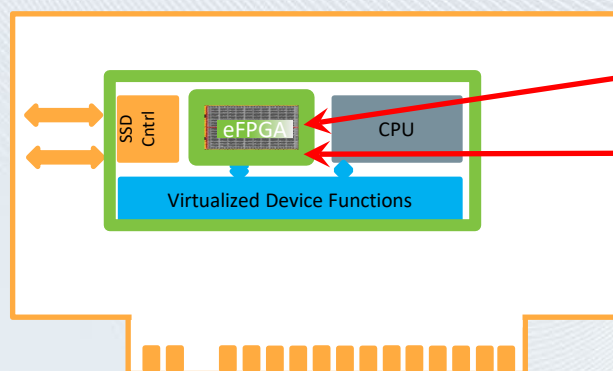
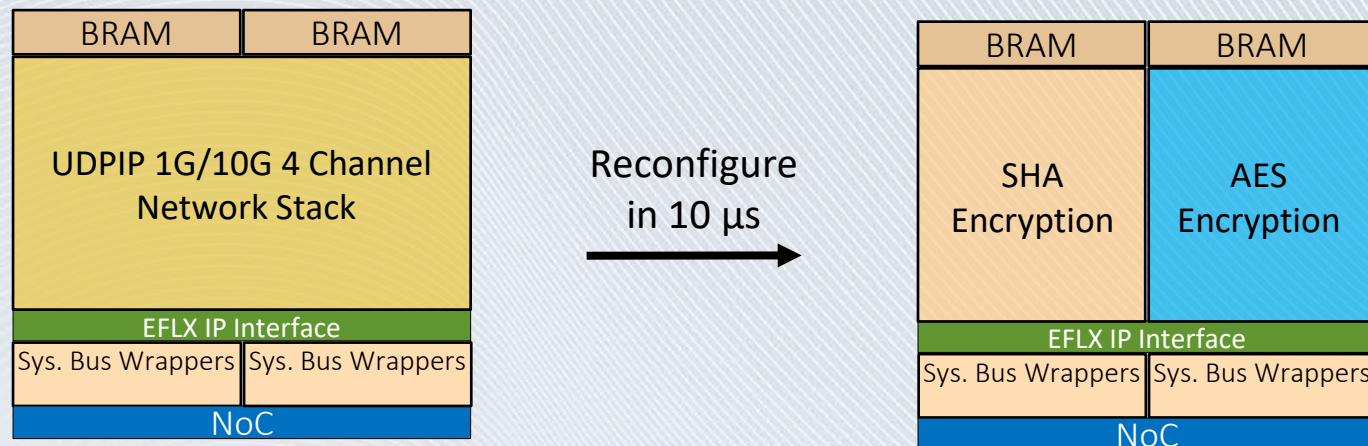
Bitstream Programming



Processor controls the Modular eFPGA



New Fast Paging eFPGA



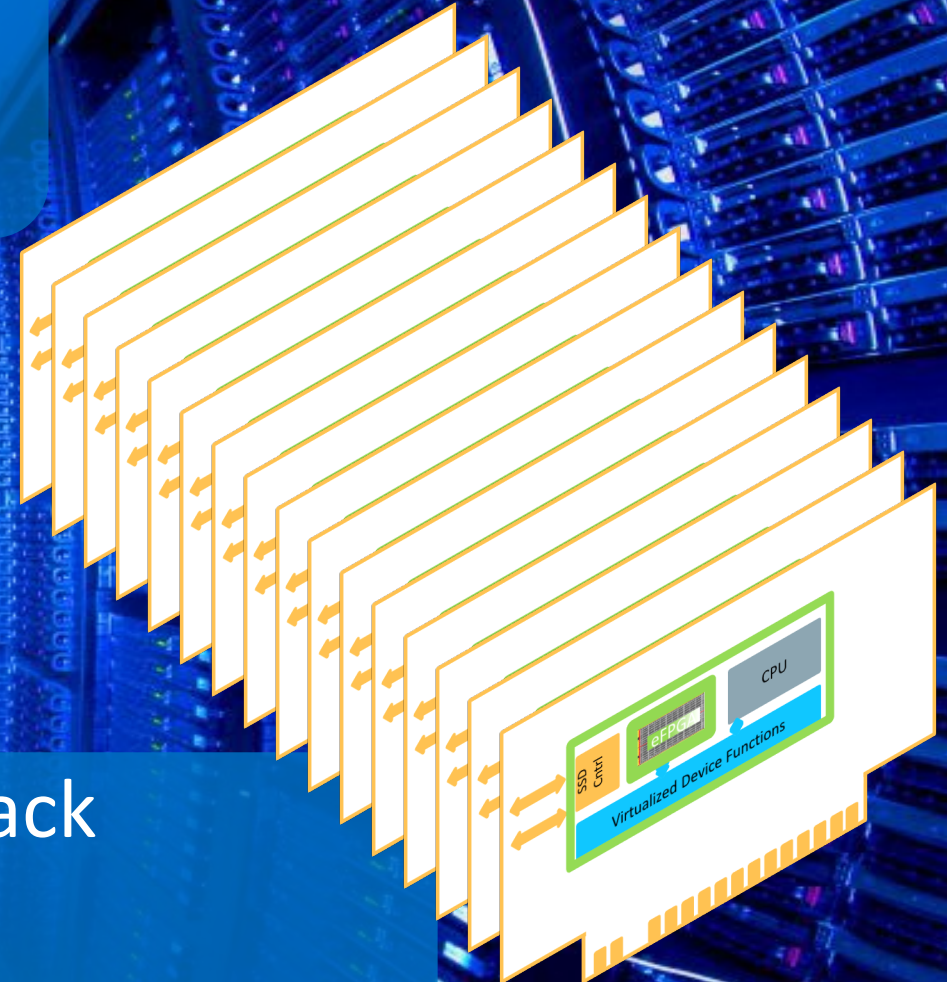
Reconfigure for
different offloads

Fast Paging for
different offloads

Allow Software to
reprogram Hardware

Integrate eFPGA

- Greater Compute Density per Rack
- Less Power & Heat
- Less Latency and Less cost



#1 eFPGA IP Provider

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Thank You

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AI + eFPGA

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