Flash Memory Summit

Life after Optane
2015, 2022, 2030 Views
SPEC 302-2

Dave Eggleston

Intuitive Cognition Consulting

35 YEARS OF NAND FLASH MEMORY INNOVATION

Flash Memory SUMMIT

3D XP: What the Hell?!!

Dave Eggleston

Flash Memory Summit 2015
Santa Clara, CA

Intuitive Cognition Consulting℠

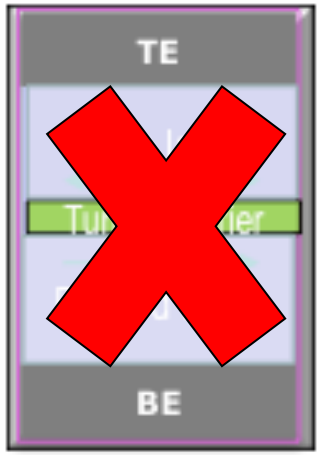
Making Sense of 3D XP

- WHY are you surprised?
- WHAT is it (really)?
- XP Array Limitations: The Litho Problem
- HOW will it be used?
- 3D XP strengths & weaknesses

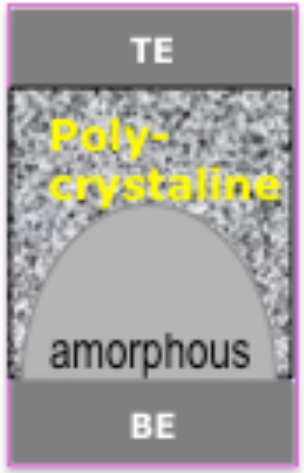
What is 3D XP?

Source: Intuitive Cognition Consulting estimates

ST-MRAM



PCMS



ReRAM

DRAM

NAND

3D XP is *NOT* ST-MRAM because:

- Can't build ST-MRAM in a XP array (1T-1R)
- Can't achieve 128Gb with ST-MRAM ($30F^2$)
- ST-MRAM more expensive than DRAM

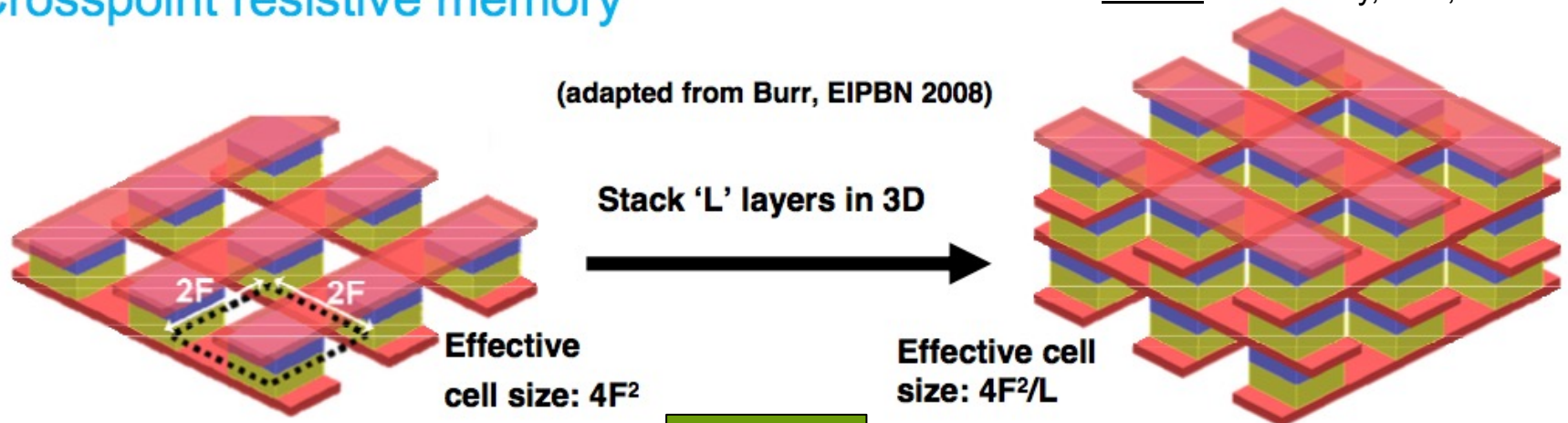
Fast	Latency	Slow
Long	Endurance	Short
Big/$$$$	Cell Size/Cost	Small/$

3D XP is *probably NOT* ReRAM because:

- ReRAM Latency is too slow for application
- ReRAM endurance may be too short for the application
- ReRAM is much more likely New Memory B (Cost focused)

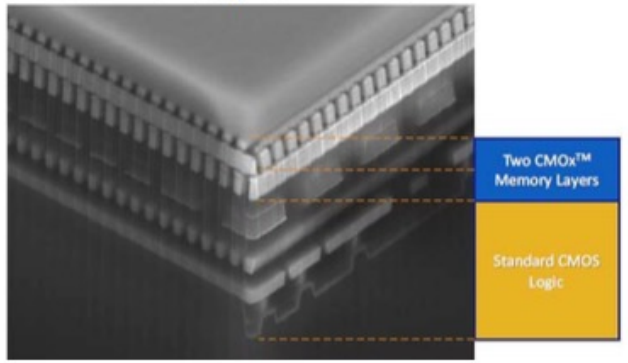
Crosspoint resistive memory

Source: R. Shenoy, IBM, IMW May 2013



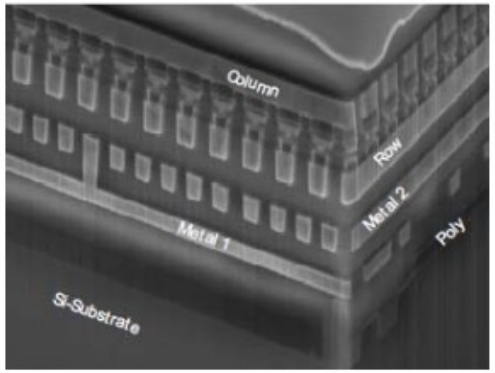
PCMS

Ref: D. Eggleston, Flash Memory Summit 2011



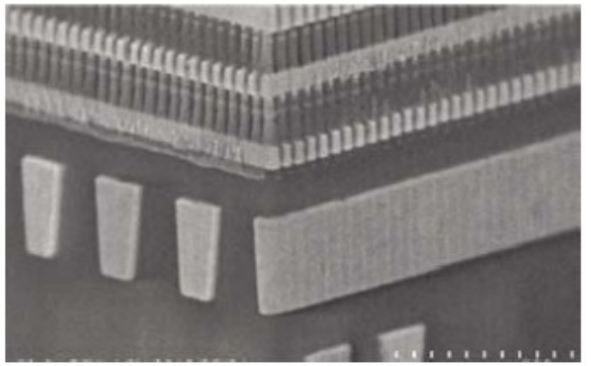
Unity Semiconductor 2 layer Conductive Metal Oxide RRAM

Ref: D. Kau, IEDM 2009



Intel/Numonyx 64Mb PCM+OTS selector

Ref: T-Y. Liu, ISSCC 2013



Sandisk/Toshiba 32Gb 2 layer MeOx ReRAM crosspoint in 24nm technology

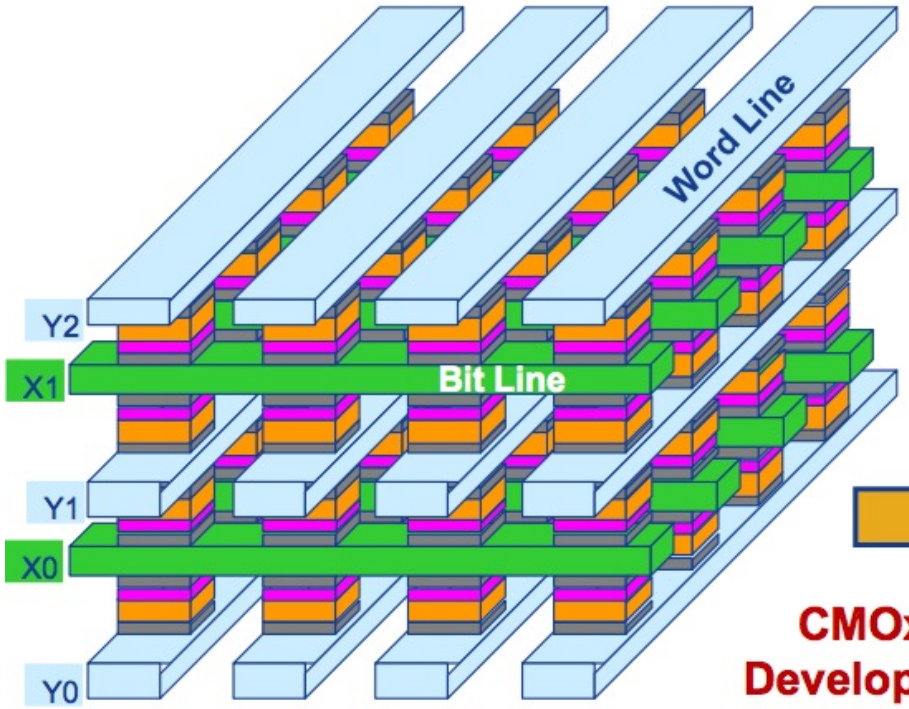
3D multilayer stacked crosspoint arrays → path to low cost memory

WRONG!

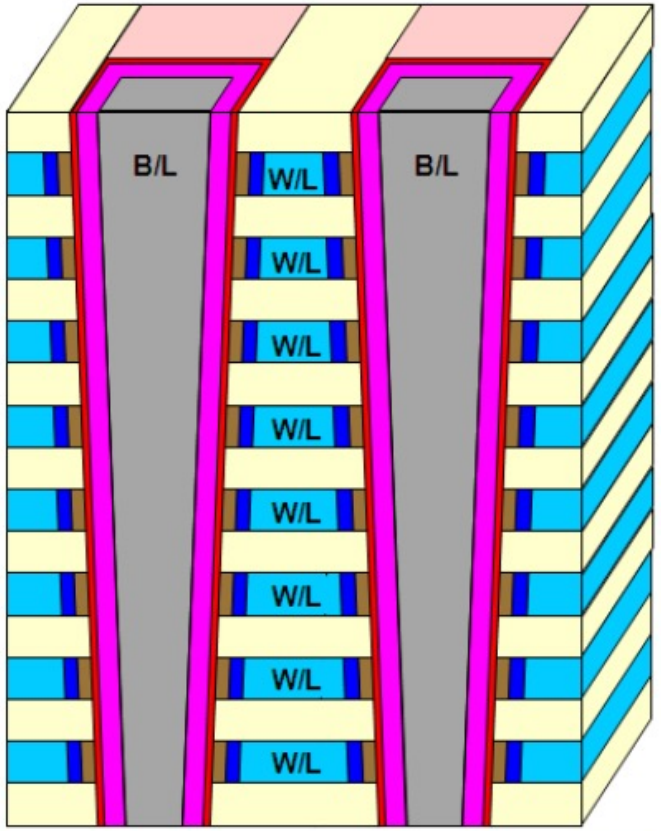
Source: C. Chevallier, Unity, CEATEC 2011

Unity

Planar CMOx™



Vertical CMOx™



CMOx™ Development Strategy (NO EUV Required)

Reuse of the 3D NAND architecture and processing is the way forward for lowest cost RRAM.

Current Major Costs of Planar CMOx™:
- Multiple immersion patterning or EUV lithography
- Fine line interconnect very challenging

Vertical CMOx™ (VXPA):
- Extension of vertical NAND
- Low cost lithography
- Fine line interconnect not required
- Earlier, Cost effective option

Intel PCM-Based DIMMs

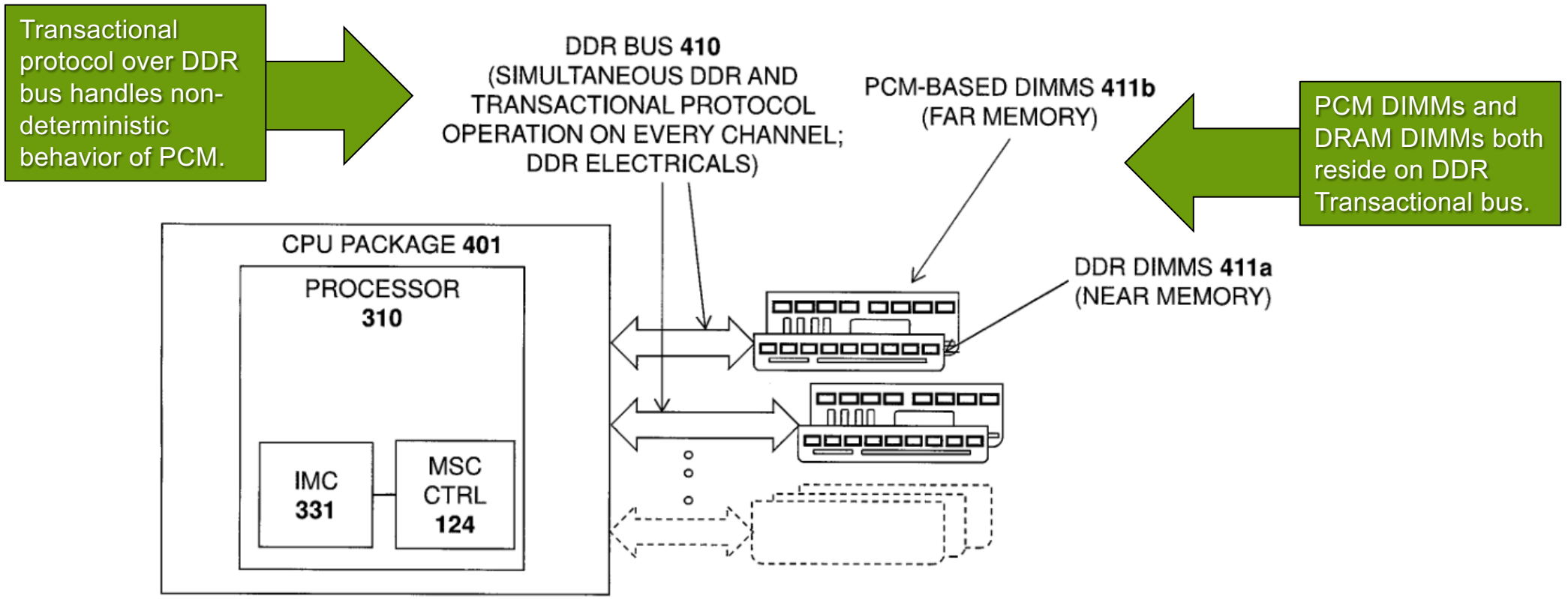


Fig. 4G

Source: Intel US patent, R. Ramanujan et al, "Dynamic partial power down of memory-side cache in a 2-level memory hierarchy" US 20140304475 A1

Strengths/Weaknesses 3D XP (2015)

Source: Intuitive Cognition Consulting estimates

❑ Strengths

- Brand new memory type brings new capabilities
- Semi-Persistent memory arrives!
- Server memory target competes with DRAM cost
- Read/write performance near full DRAM speed
- Full system approach

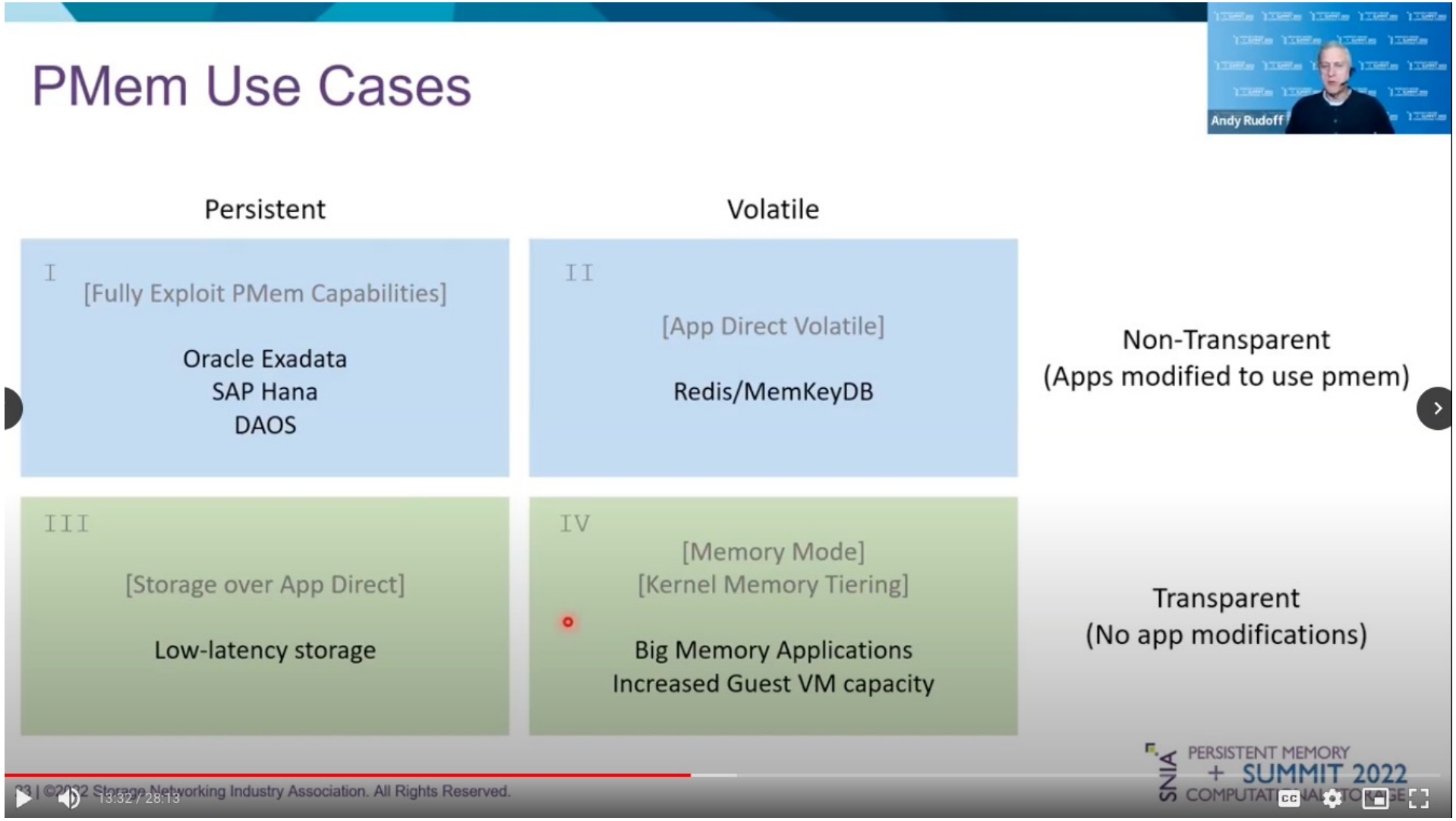
❑ Weaknesses

- 3D XP cost will be high:
  - DRAM $8/GB, 3D XP $4/GB, 3D NAND $0.2/GB
- Sole sourced from Intel/Micron
- Requires major hardware and software changes
- >12W Power requires server thermal re-design
- Non-JEDEC standardized DDR4 transactional interface

2022 View of Optane – Lessons Learned

- 3DXP Memory Array
  - Litho costs limit layer stacking
  - Way forward: Reuse 3D array processes and architecture for lowest cost
- Optane DIMMs
  - DDR DRAM DIMM slots are very precious!
  - Way forward: Attach non-DRAM performant memory using CXL
- Persistence
  - Limited value proposition for coherent persistent memory; security risk
  - Way forward: Use volatile memory (Buy more DRAM!)

Persistent Memory Usage – Andy Rudoff (Intel)



2030 View – The Future

Flash Memory Summit

- 3D DRAM or 3D ??? (volatile memory array)
  - Go 3D or go home!
- Wafer bonded 3D array + sub 1nm logic
  - BEOL and FEOL processes are optimized and distinctly different
- CXL attached disaggregated memory
  - Think rack level memory appliances
  - JBODs!
- “Fabrics”
  - Software + hardware for managing memory tiering/pooling/sharing

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Q&A

Please take the Session Survey
Thank you!

Tuesday, August 2

Wednesday, August 3

Thursday, August 4

