Perfect Read Non-Destructive Dynamic Flash Memory (DFM)

Koji Sakui, Masakazu Kakumu, and Nozomu Harada

Unisantis Electronics Singapore Pte Ltd., 60 Paya Lebar Road#10-49 Paya Lebar Square Singapore 409051

sakui@unisantis.com

 ©2022 Flash Memory Summit. All Rights Reserved.

Perfect Read Non-Destructive Dynamic Flash Memory

1. Goal for Creation of DFM and 1T-DRAM Review
2. DFM Concept and Program/Erase/Read Mechanism
3. Block and Bit by Bit “0” Refresh
4. DFM Prospects and Potential
5. Conclusion

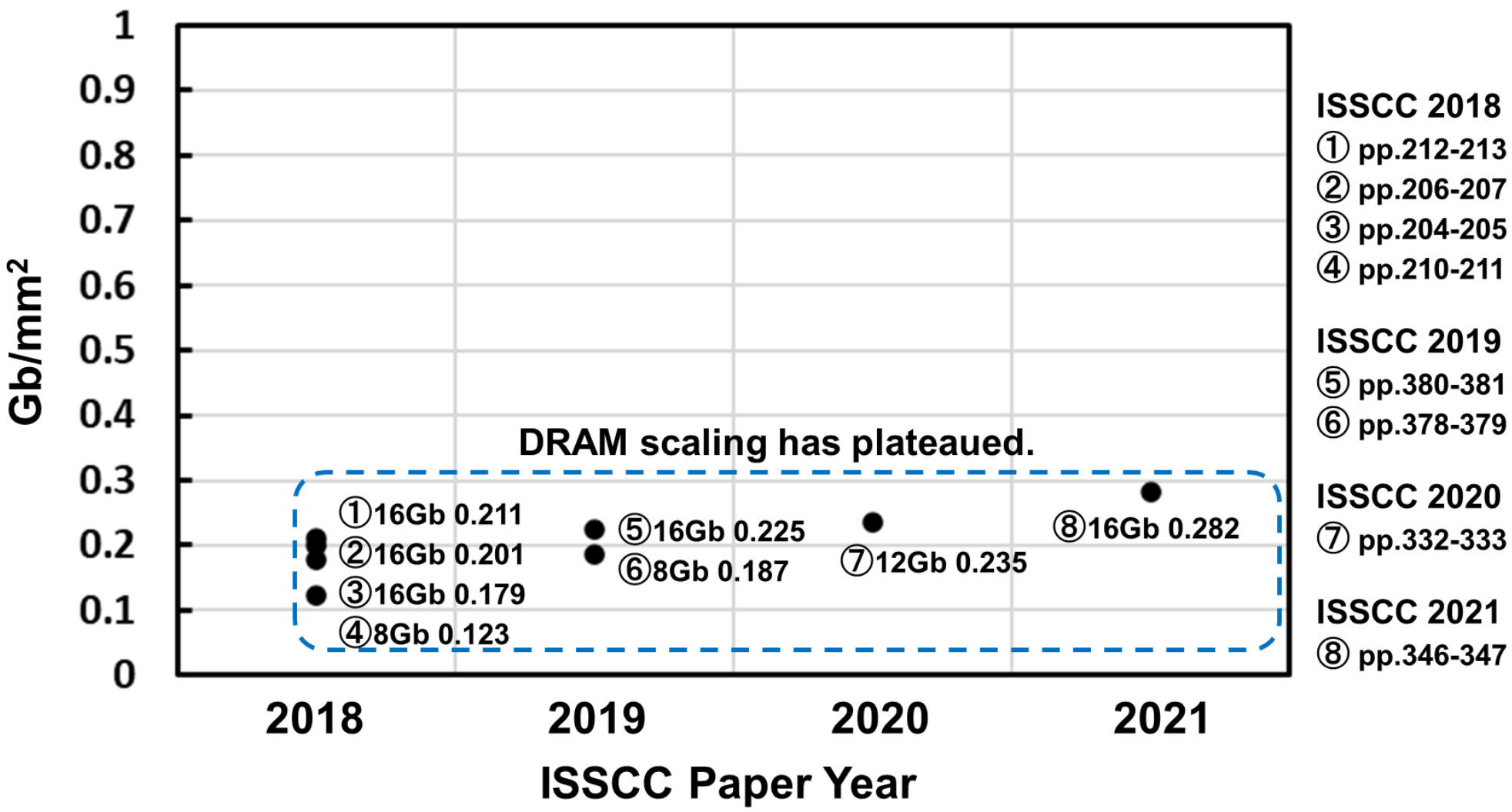
 ©2022 Flash Memory Summit. All Rights Reserved.

Perfect Read Non-Destructive DFM

1. Goal for Creation of DFM and 1T-DRAM Review
2. DFM Concept and Program/Erase/Read Mechanism
3. Block and Bit by Bit “0” Refresh
4. DFM Prospects and Potential
5. Conclusion

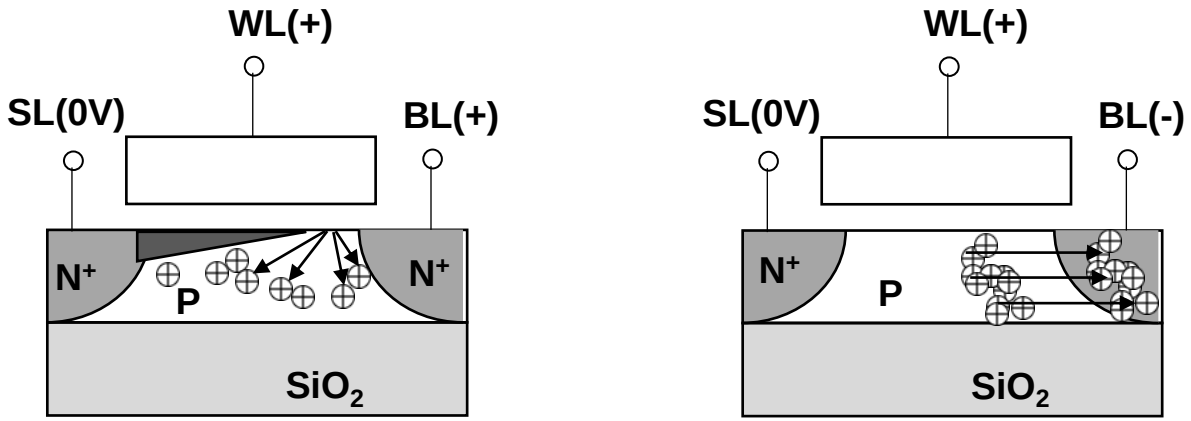
 ©2022 Flash Memory Summit. All Rights Reserved.

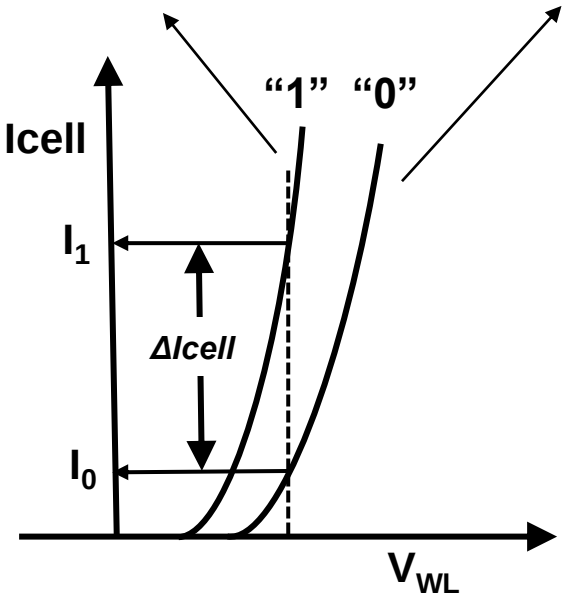
DRAM Scaling



 ©2022 Flash Memory Summit. All Rights Reserved.

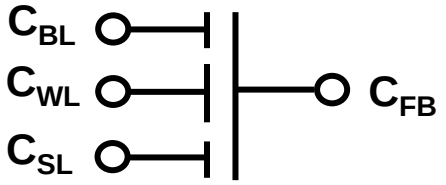
1T-DRAM (Z-RAM)



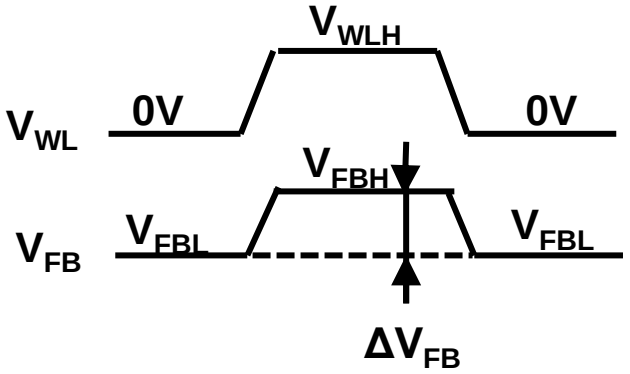


Issues

1. Large WL capacitive coupling to FB
2. Small "1" and "0" margin
   1. Cell Vth is defined by WL
   2. Negative WL is required for maintaining "1"



$$C_{FB} = C_{WL} + C_{BL} + C_{SL}$$



$$\beta_{WL} = \frac{C_{WL}}{C_{WL} + C_{BL} + C_{SL}} \Rightarrow \text{Large } \beta_{WL}$$

$$\Delta V_{FB} = V_{FBH} - V_{FBL}$$

$$= \underbrace{\beta_{WL} \times V_{WLH}}_{\text{Large}}$$

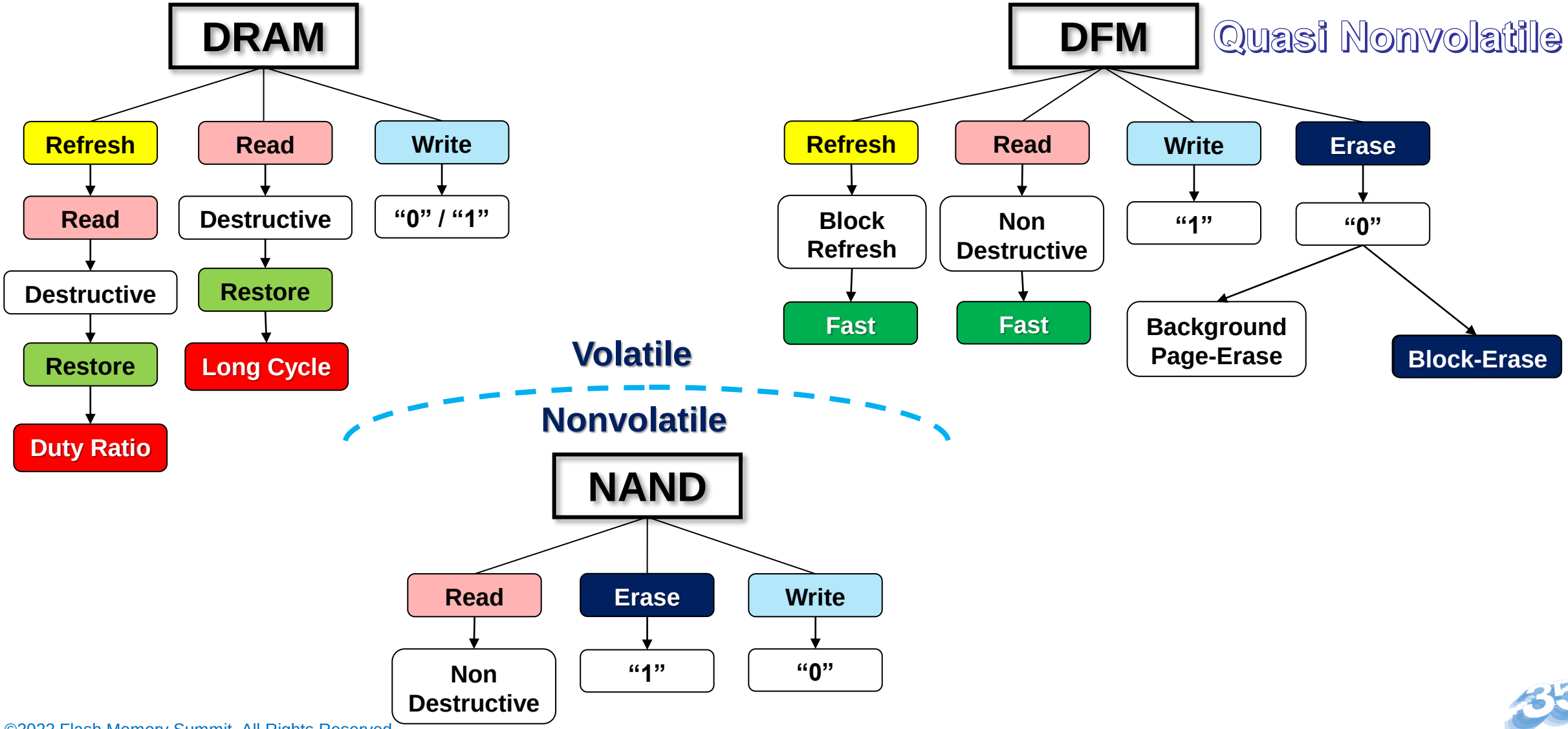
 ©2022 Flash Memory Summit. All Rights Reserved.

Perfect Read Non-Destructive DFM

1. Goal for Creating a DFM and 1T-DRAM Review
2. DFM Concept and Program/Erase/Read Mechanism
3. Block and Bit by Bit “0” Refresh
4. DFM Prospects and Potential
5. Conclusion

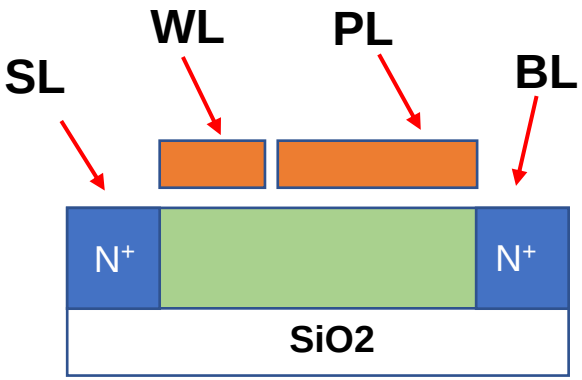
 ©2022 Flash Memory Summit. All Rights Reserved.

DFM Concept

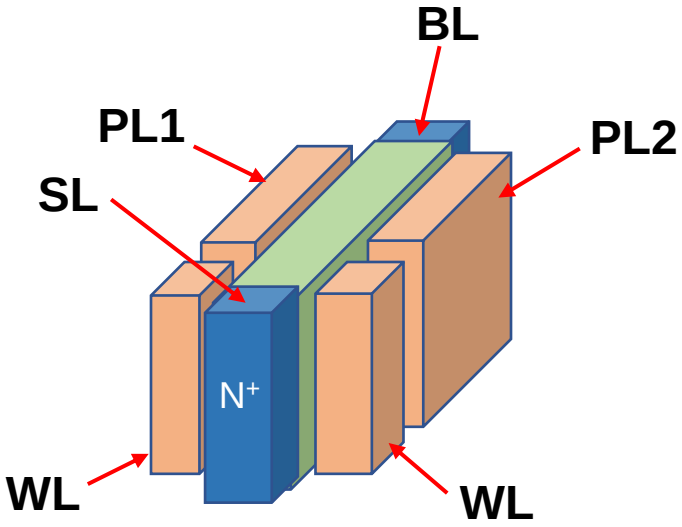


 ©2022 Flash Memory Summit. All Rights Reserved.

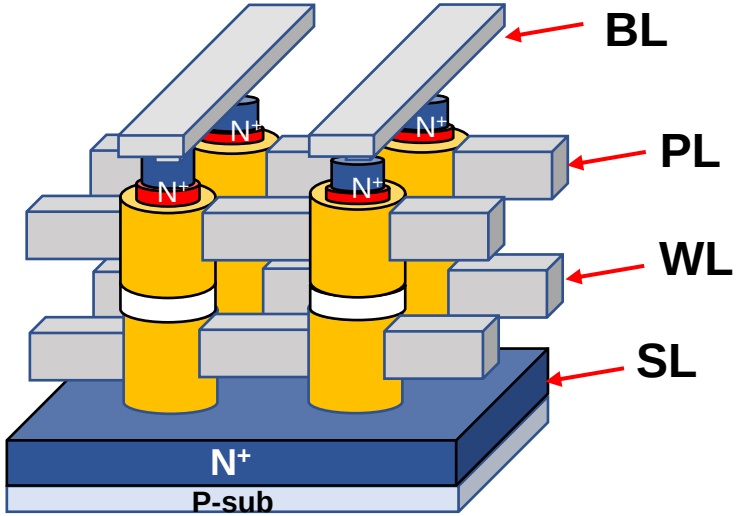
DFM Structure



(1) SOI DFM



(2) FinFET DFM



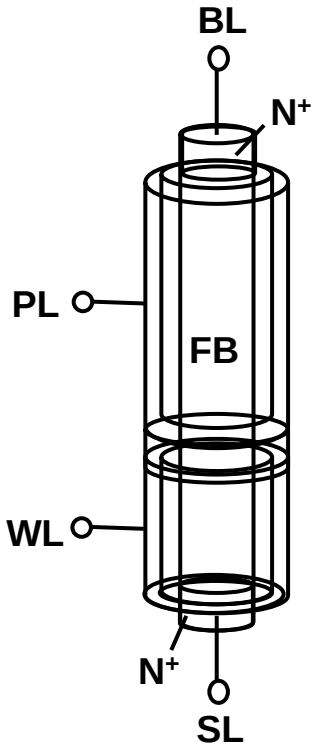
(3) SGT DFM

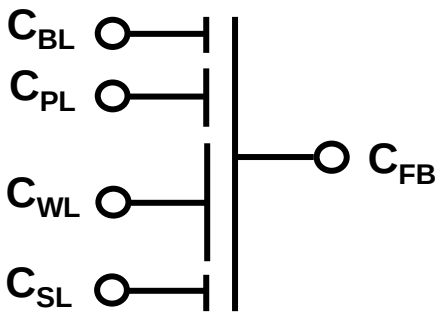
(4) Stacked GAA DFM

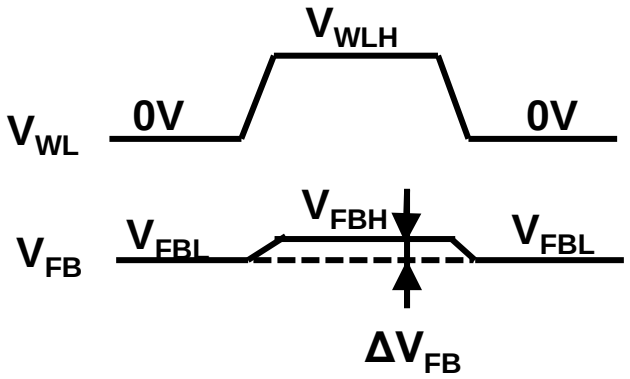
 ©2022 Flash Memory Summit. All Rights Reserved.

The FB Stabilization by the PL Gate

Small WL capacitive coupling to FB !







$$C_{FB} = C_{PL} + C_{WL} + C_{BL} + C_{SL}$$

$$\beta_{PL} = \frac{C_{PL}}{C_{PL} + C_{WL} + C_{BL} + C_{SL}} \Rightarrow \text{Large } \beta_{PL}$$

$$\beta_{WL} = \frac{C_{PL}}{C_{PL} + C_{WL} + C_{BL} + C_{SL}} \Rightarrow \text{Small } \beta_{WL}$$

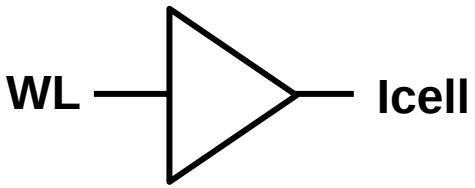
$$\Delta V_{FB} = V_{FBH} - V_{FBL}$$

$$= \underbrace{\beta_{WL}}_{\text{Small}} \times V_{WLH}$$

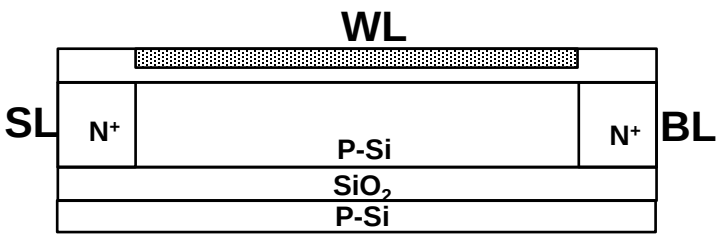
1. K. Sakui and N. Harada, "Dynamic Flash Memory with Dual Gate Surrounding Gate Transistor (SGT)," in *Proc. IEEE IMW*, pp.72-75, May 2021.
2. K. Sakui and N. Harada, "Dynamic Flash Memory with Dual Gate Surrounding Gate Transistor (SGT) for Computation In Memory," in *SSDM*, pp. 127-128, Sep. 2021.
3. K. Sakui and N. Harada, "Read Non-Destructive Dynamic Flash Memory (DFM) with Dual and Double Gates," in *SSDM*, Sep. 2022 (To be published).

 ©2022 Flash Memory Summit. All Rights Reserved.

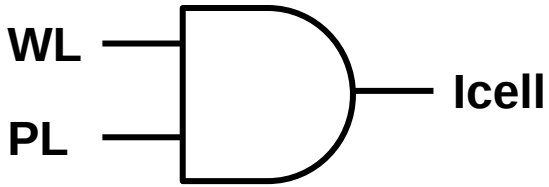
Logical Expression



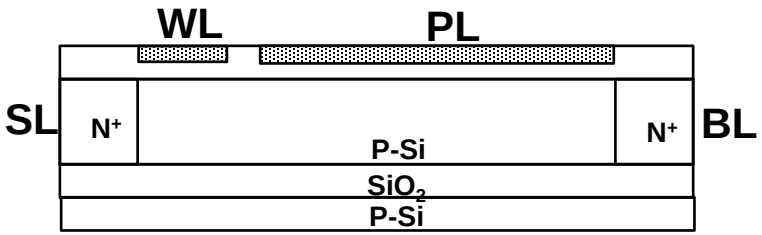
WL	Icell
1	1
0	0



(a) 1T-DRAM



WL	PL	Icell
1	1	1
1	0	0
0	1	0
0	0	0

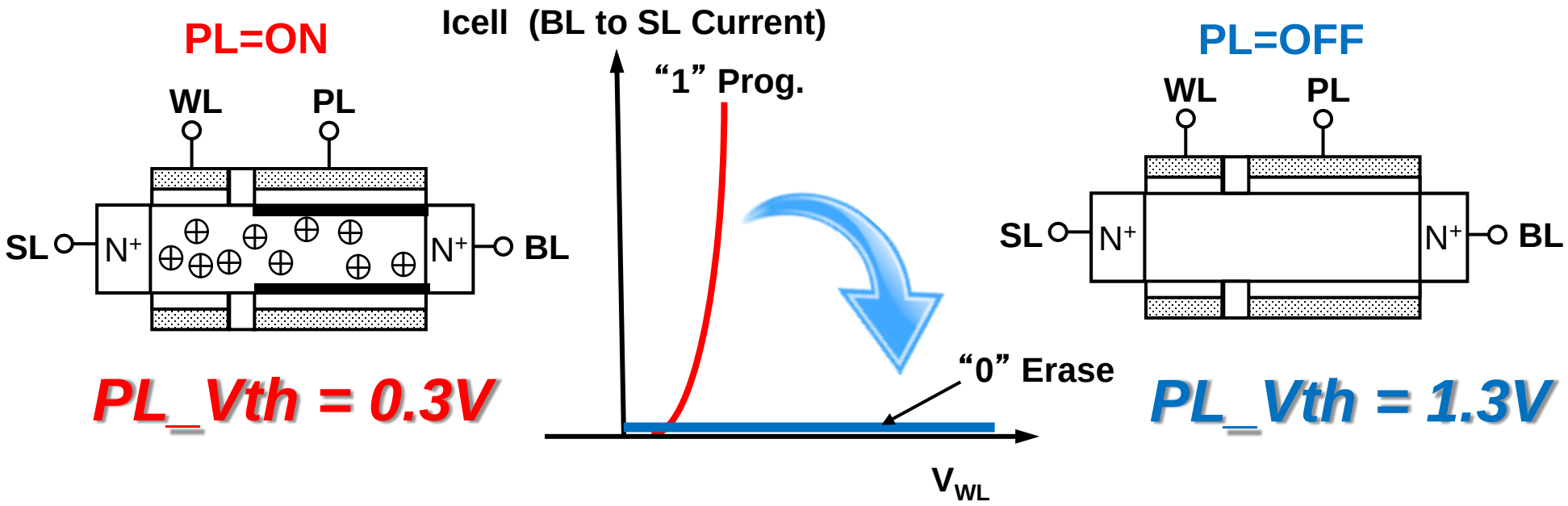


(b) DFM

 ©2022 Flash Memory Summit. All Rights Reserved.

Wide “1”-“0” Margin

PL plays a storage, while WL plays a switch !

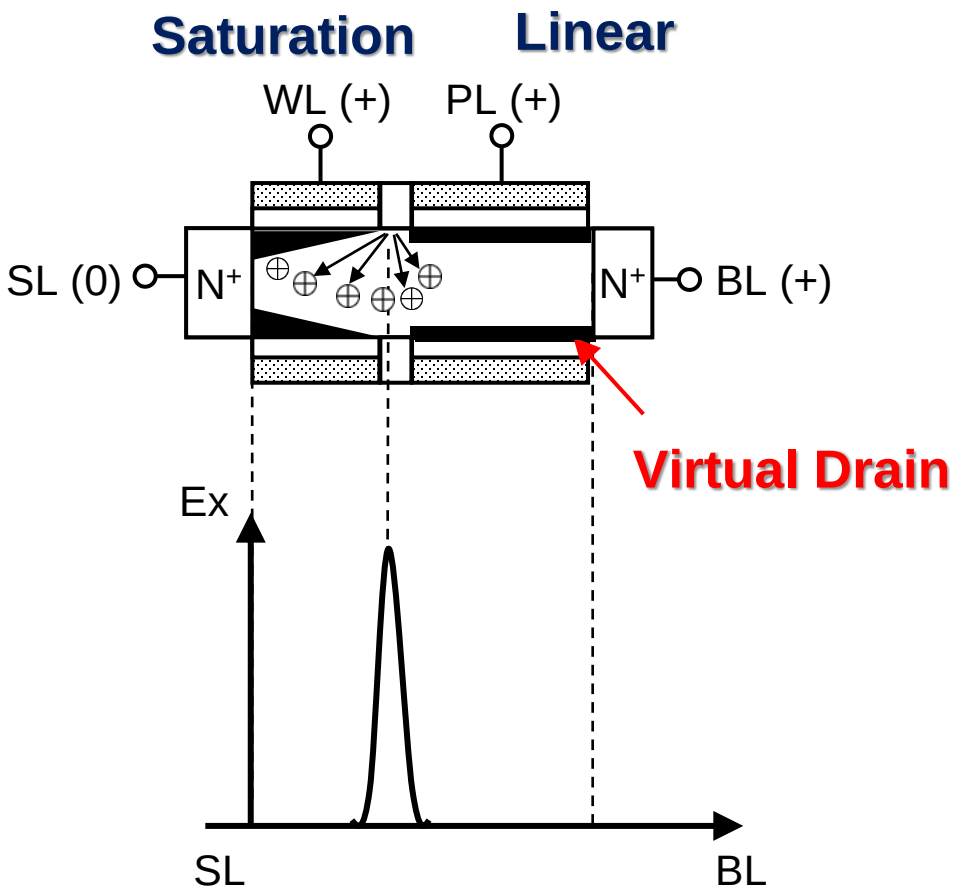


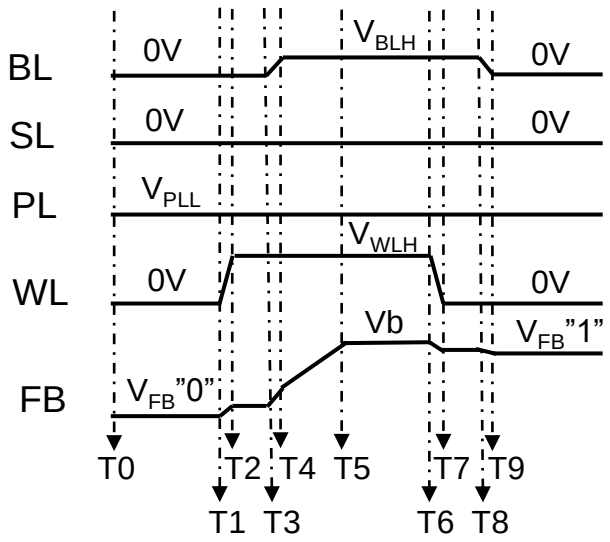
A fixed voltage of 0.8V is applied to PL on reading.

 ©2022 Flash Memory Summit. All Rights Reserved.

“1” Program Mechanism

~Source-side Impact Ionization~



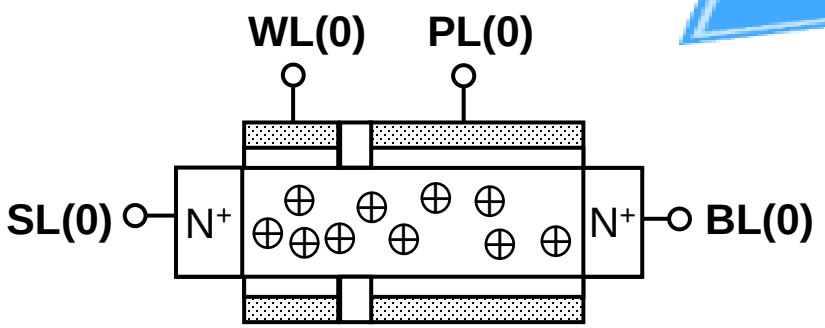


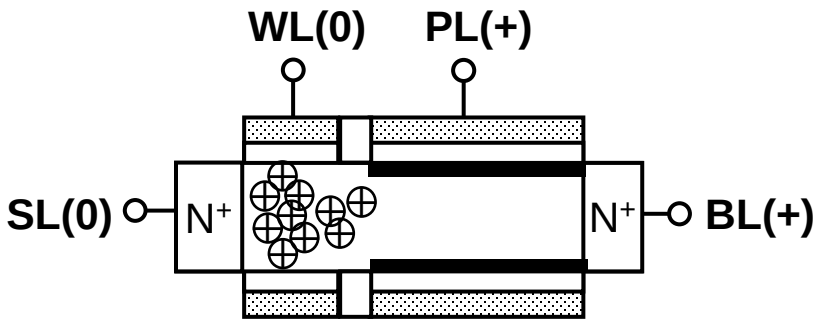
$$V_{FB}\text{”1”} = Vb - \underbrace{\beta_{WL} \times Vt_{WL} - \beta_{BL} \times V_{BLH}}_{\textbf{Small}}$$

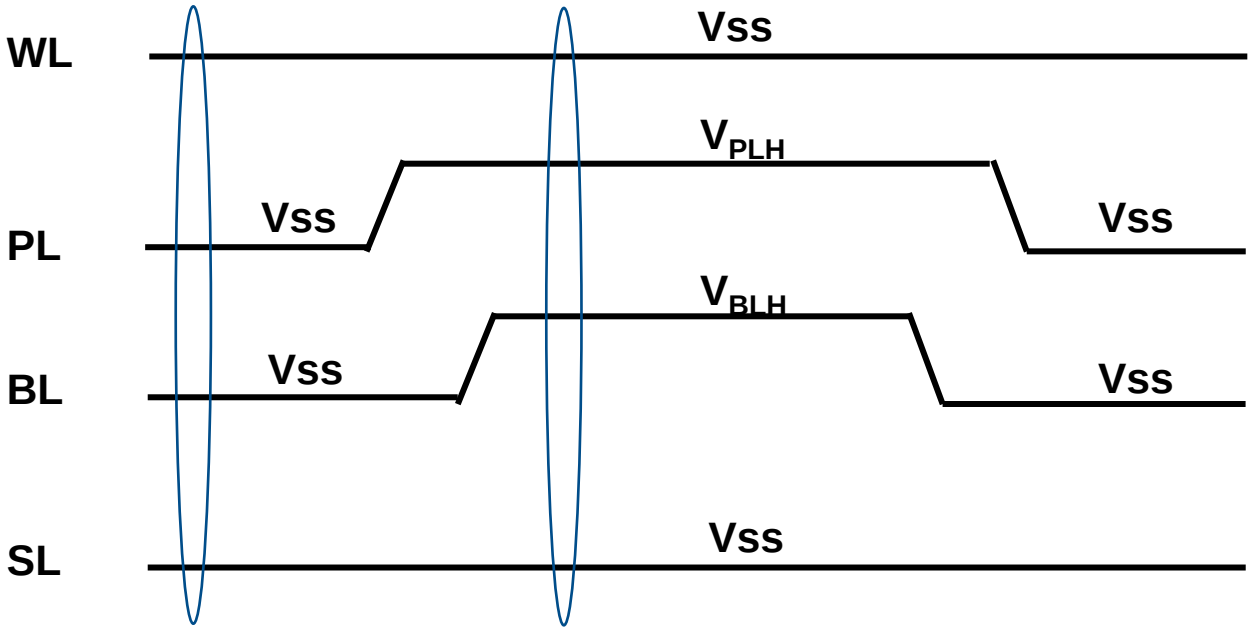
 ©2022 Flash Memory Summit. All Rights Reserved.

“0” Erase Mechanism

No negative bias is required !







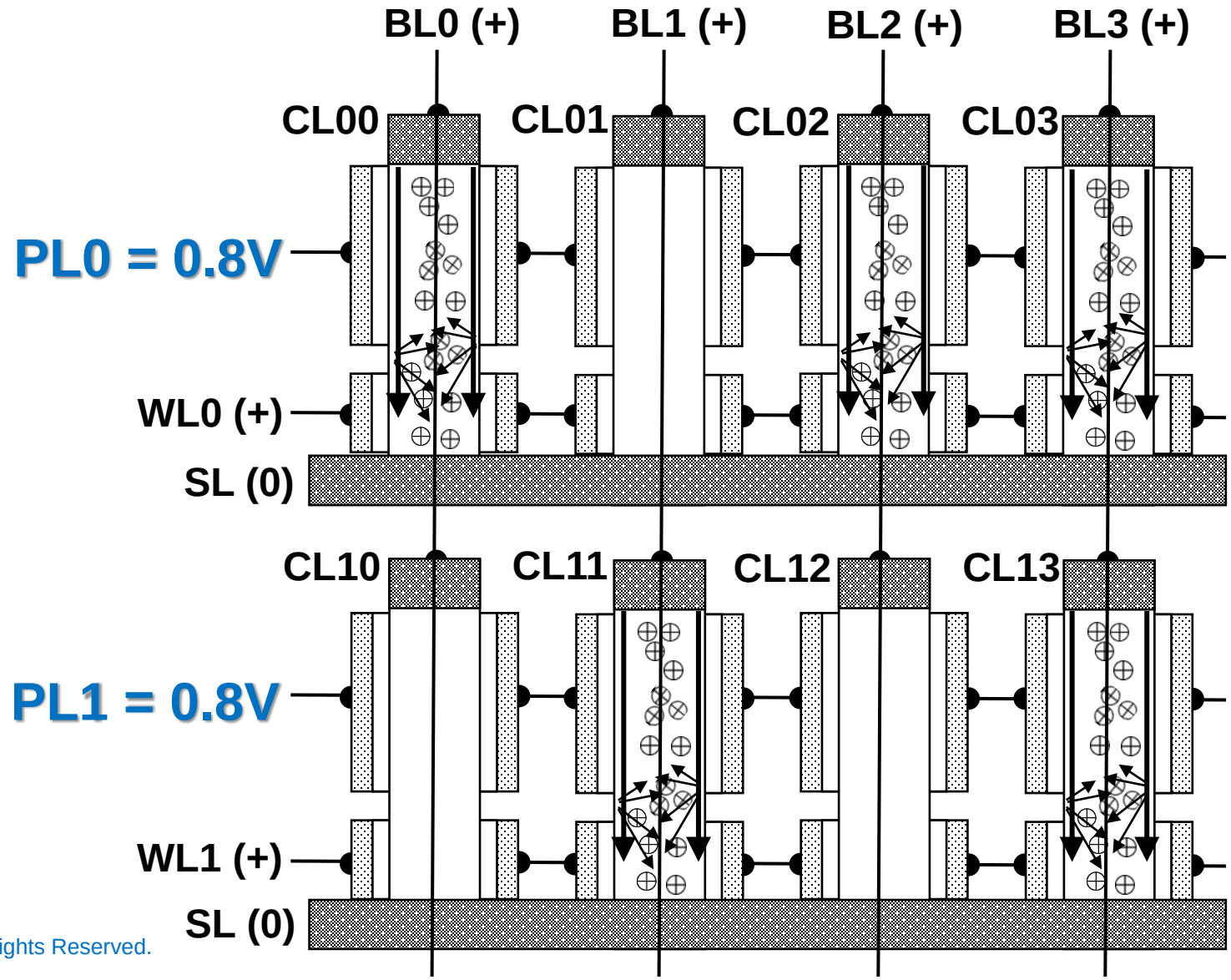
 ©2022 Flash Memory Summit. All Rights Reserved.

Perfect Read Non-Destructive DFM

1. Goal for Creating a DFM and 1T-DRAM Review
2. DFM Concept and Program/Erase/Read Mechanism
3. Block and Bit by Bit “0” Refresh
4. DFM Prospects and Potential
5. Conclusion

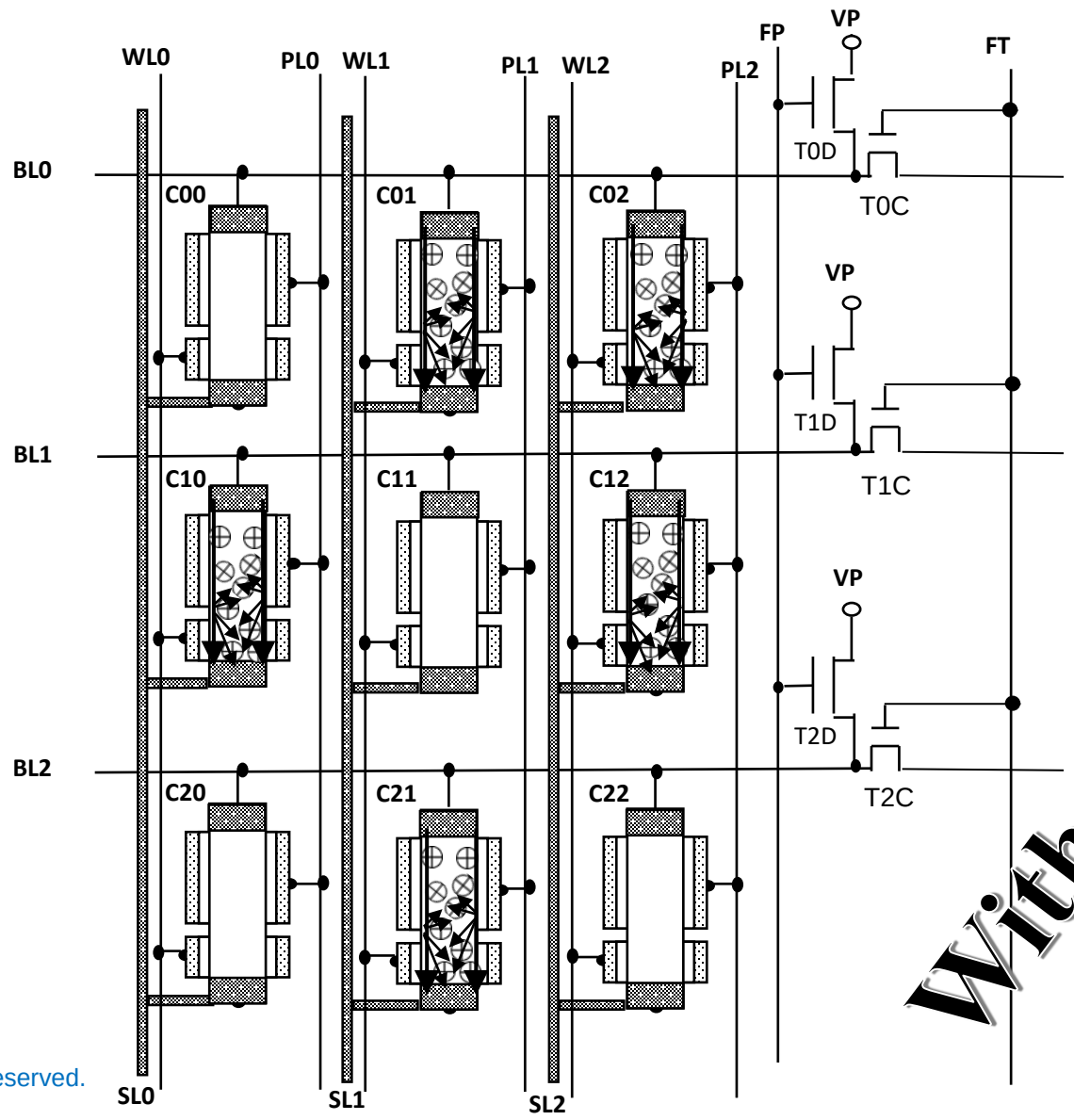
 ©2022 Flash Memory Summit. All Rights Reserved.

Block Refresh “1”



 ©2022 Flash Memory Summit. All Rights Reserved.

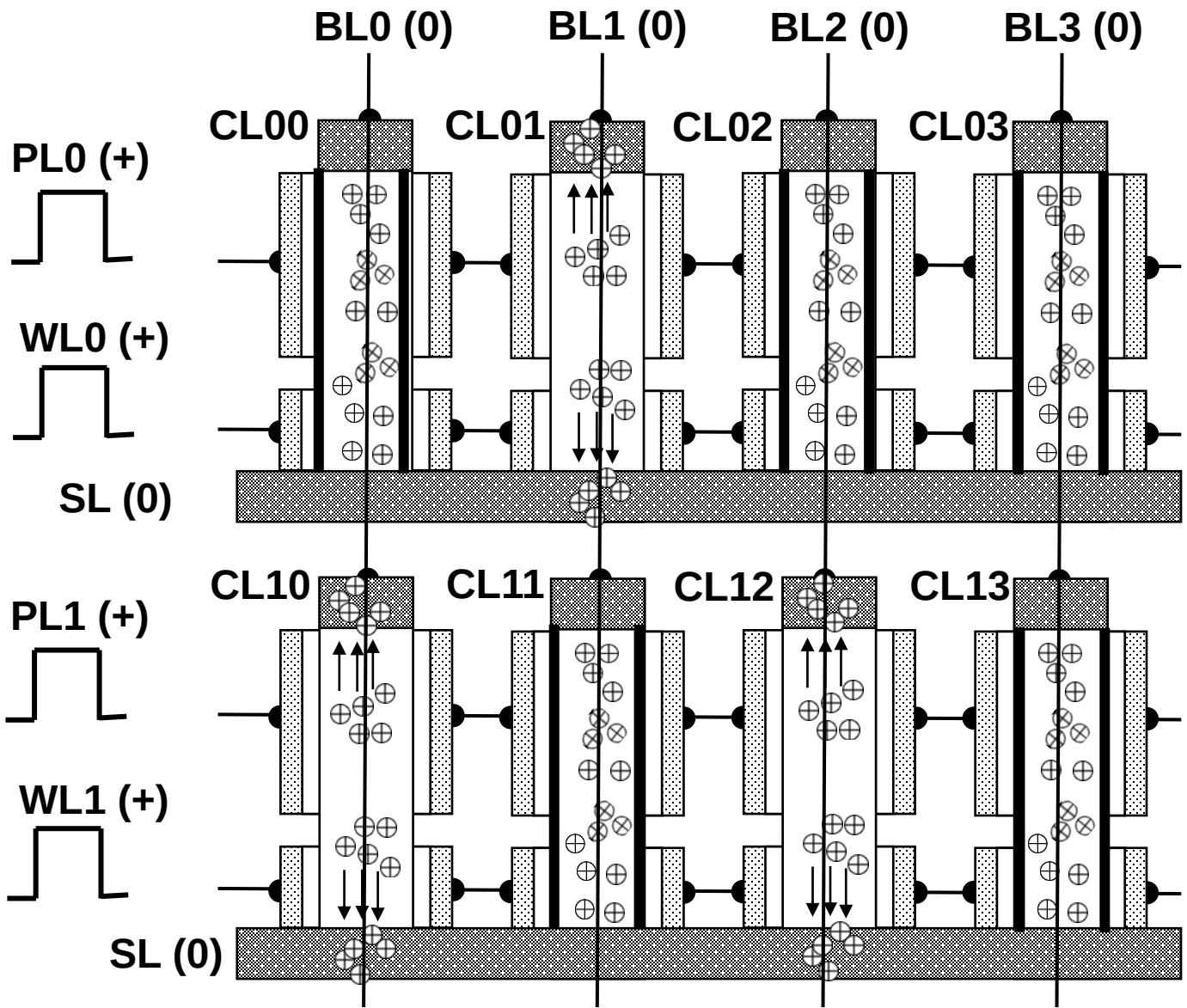
Block Refresh “1”



Without Sense Amplifiers

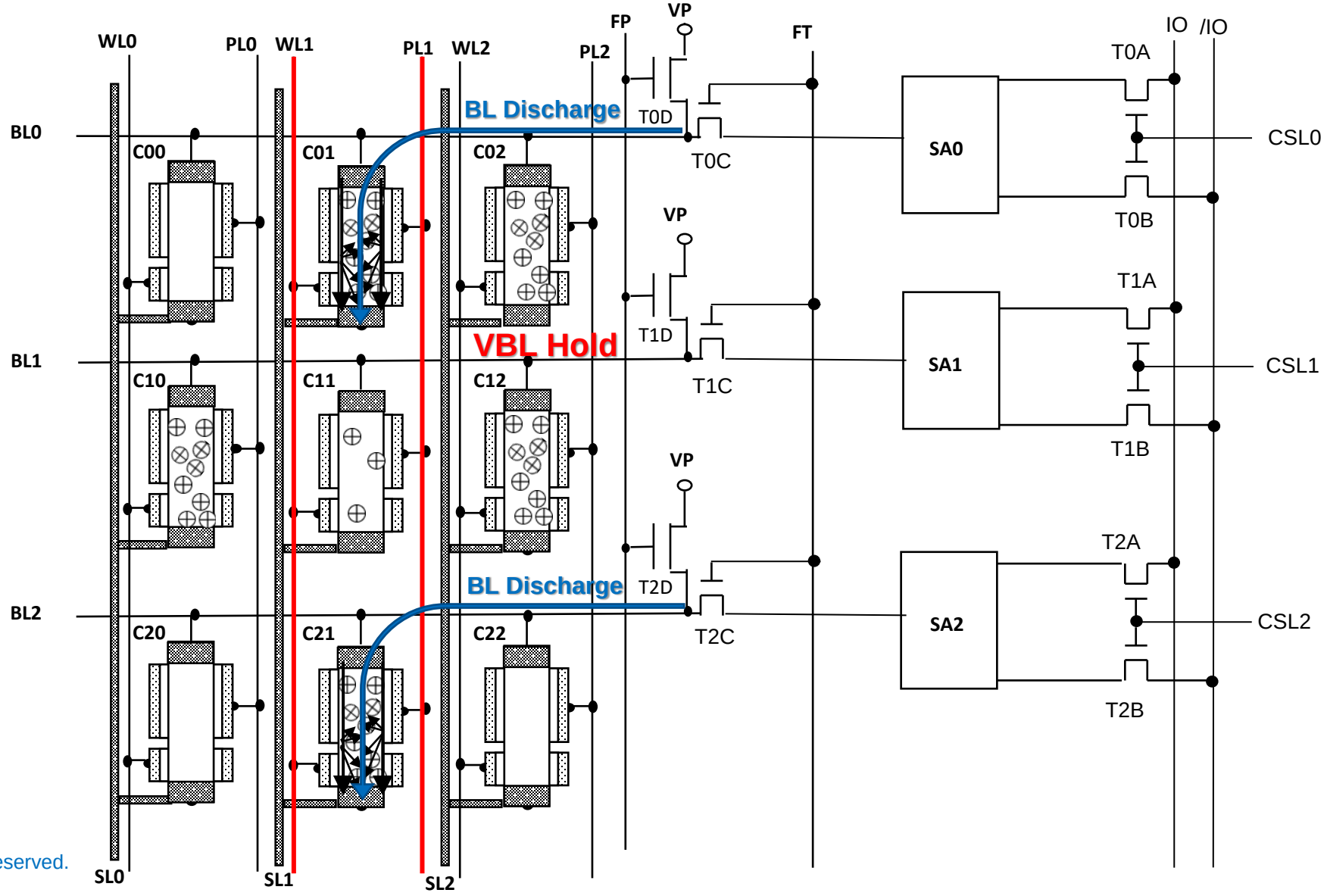
 ©2022 Flash Memory Summit. All Rights Reserved.

Block Refresh “0”



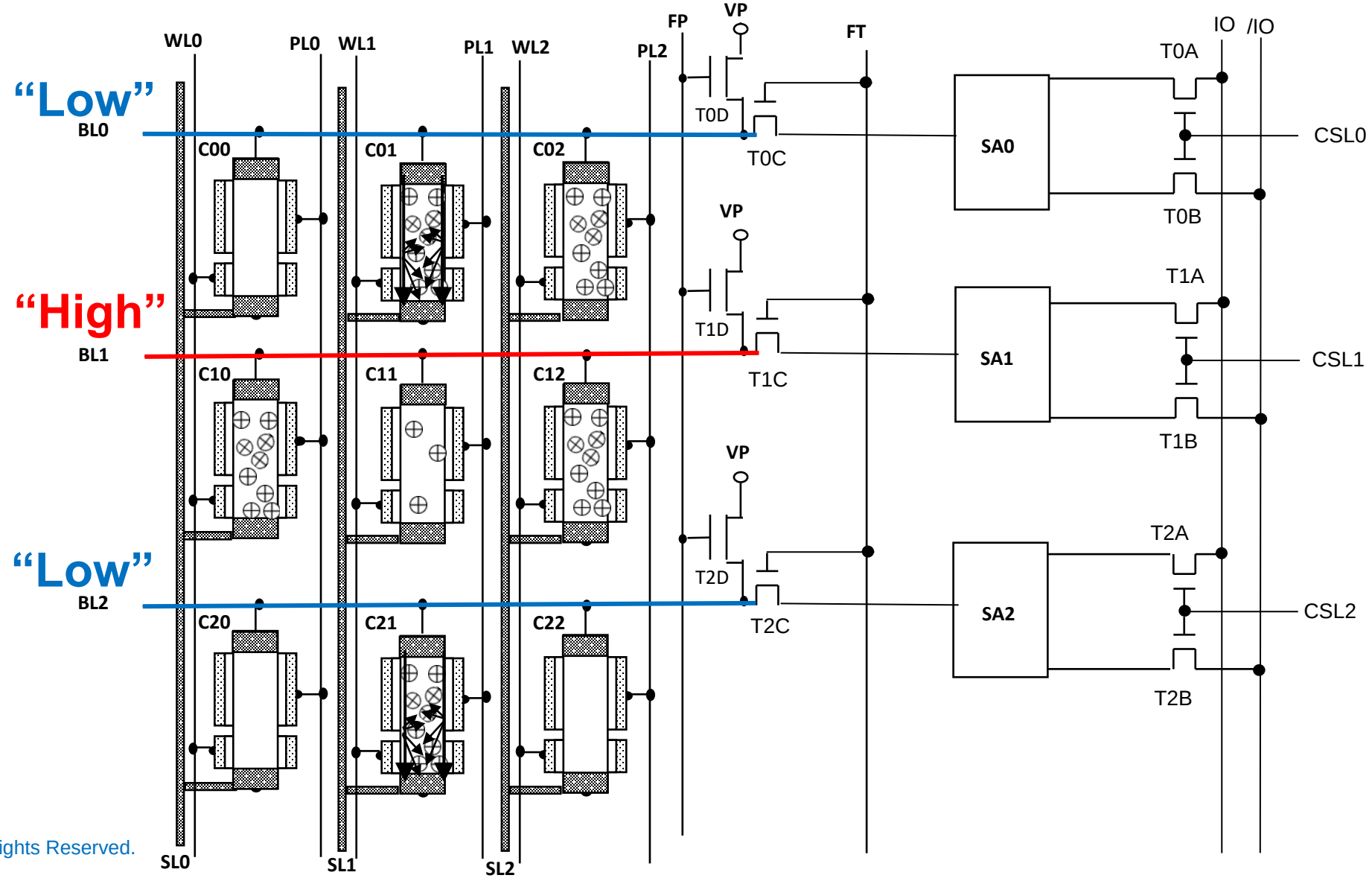
 ©2022 Flash Memory Summit. All Rights Reserved.

Bit by Bit “0” Page Refresh



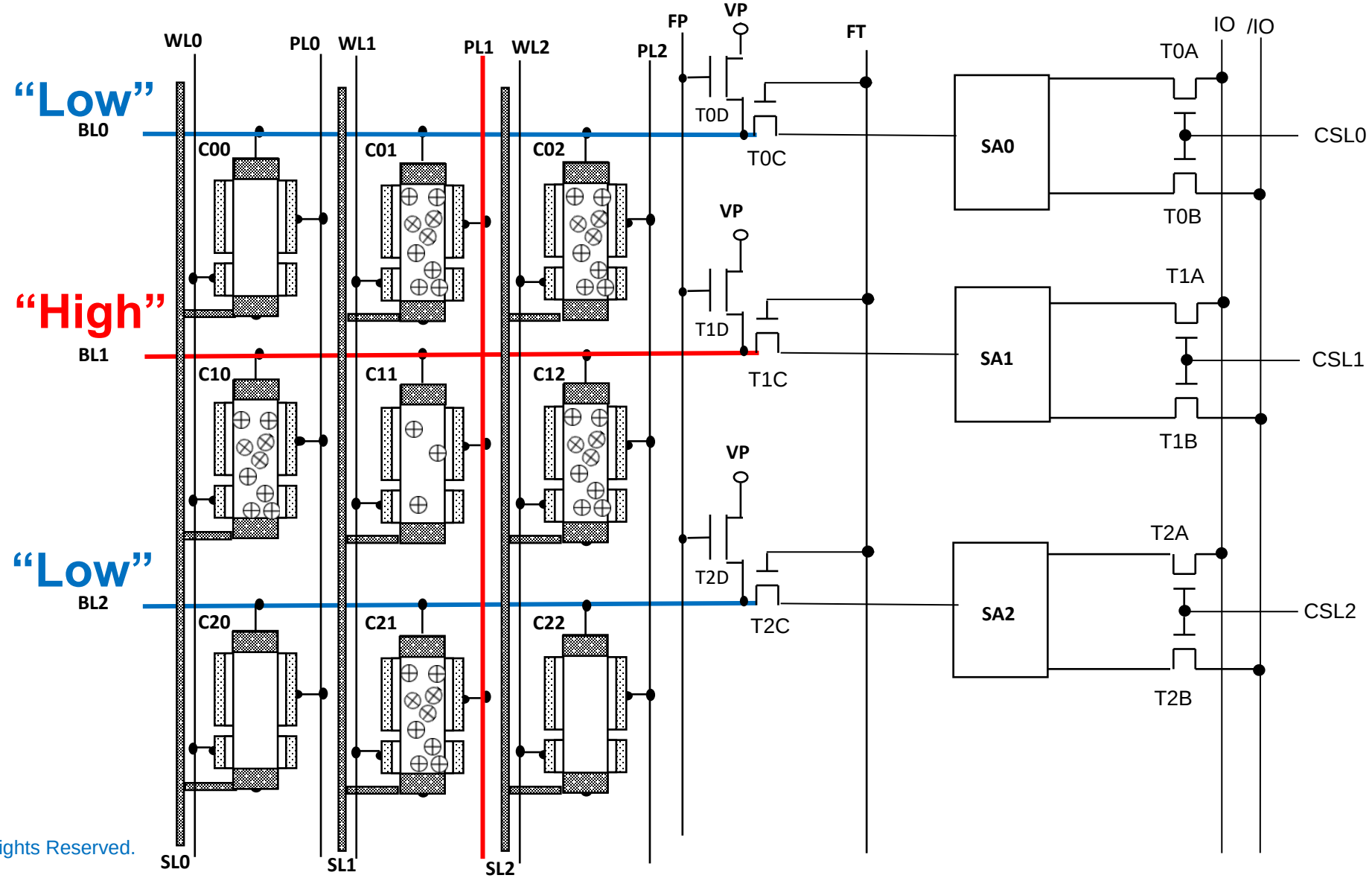
 ©2022 Flash Memory Summit. All Rights Reserved.

Bit by Bit “0” Page Refresh



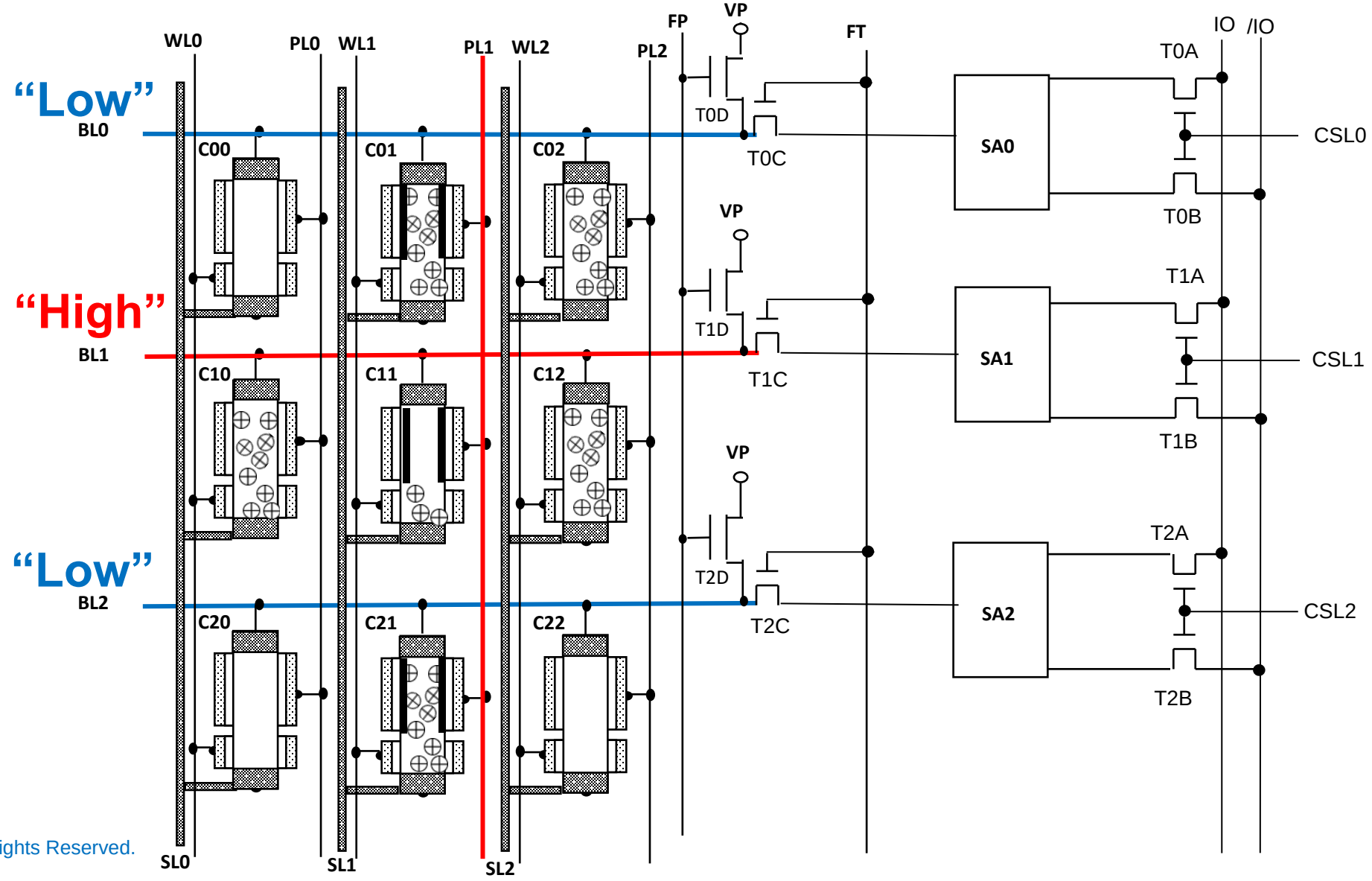
 ©2022 Flash Memory Summit. All Rights Reserved.

Bit by Bit “0” Page Refresh



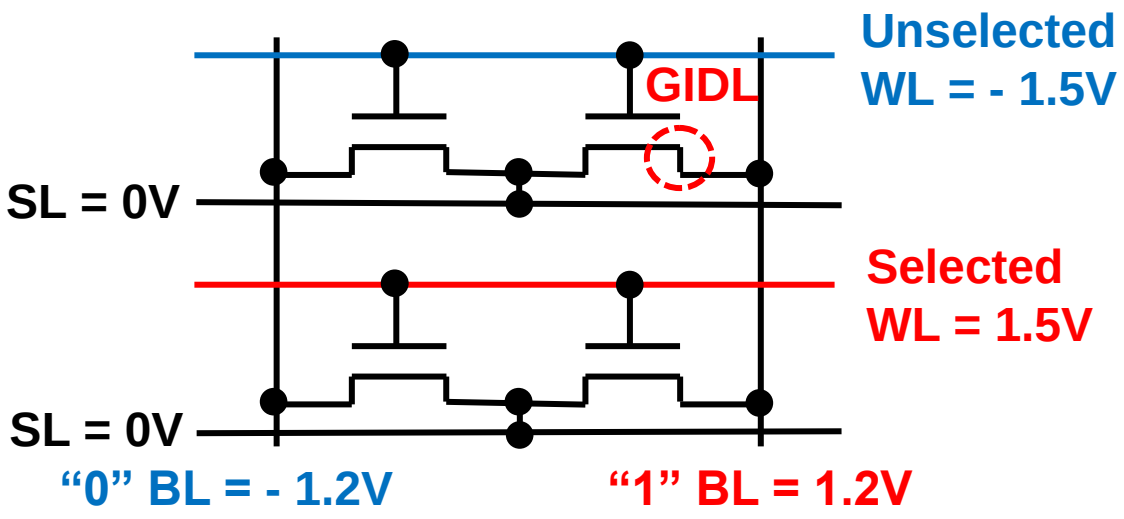
 ©2022 Flash Memory Summit. All Rights Reserved.

Bit by Bit “0” Page Refresh



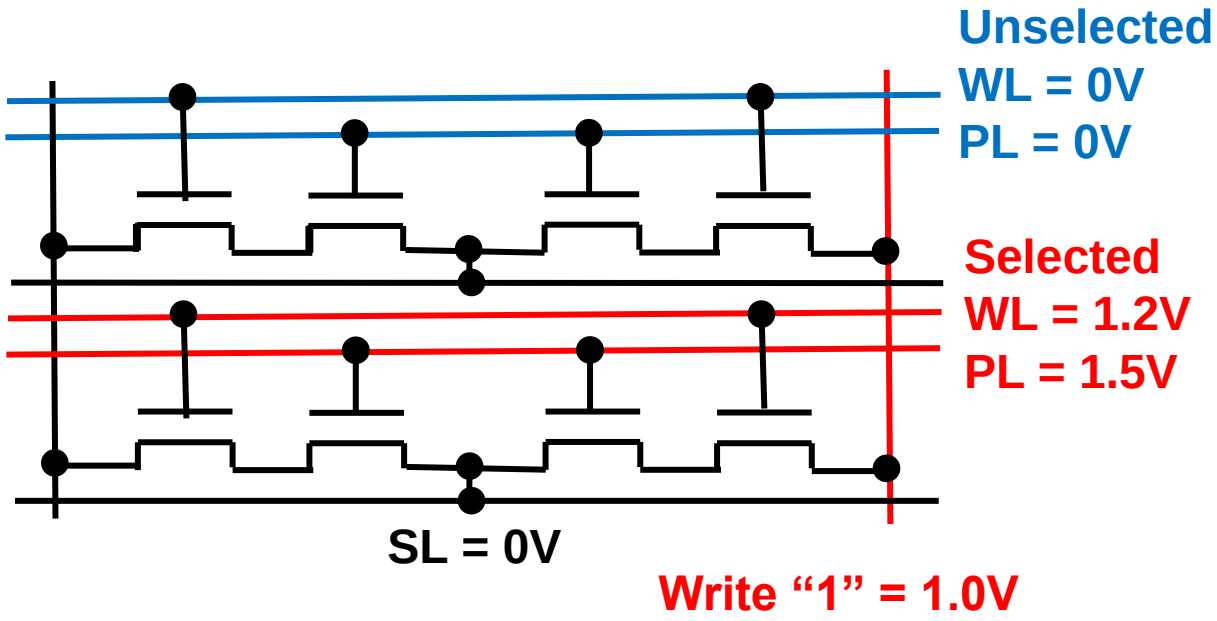
 ©2022 Flash Memory Summit. All Rights Reserved.

Disturbance



Write "0" after Write "1"

1T-DRAM Write/Restore



DFM Write

WL can shield BL disturbance, while PL can shield SL disturbance!

GIDL: Gate Induced Drain Leakage

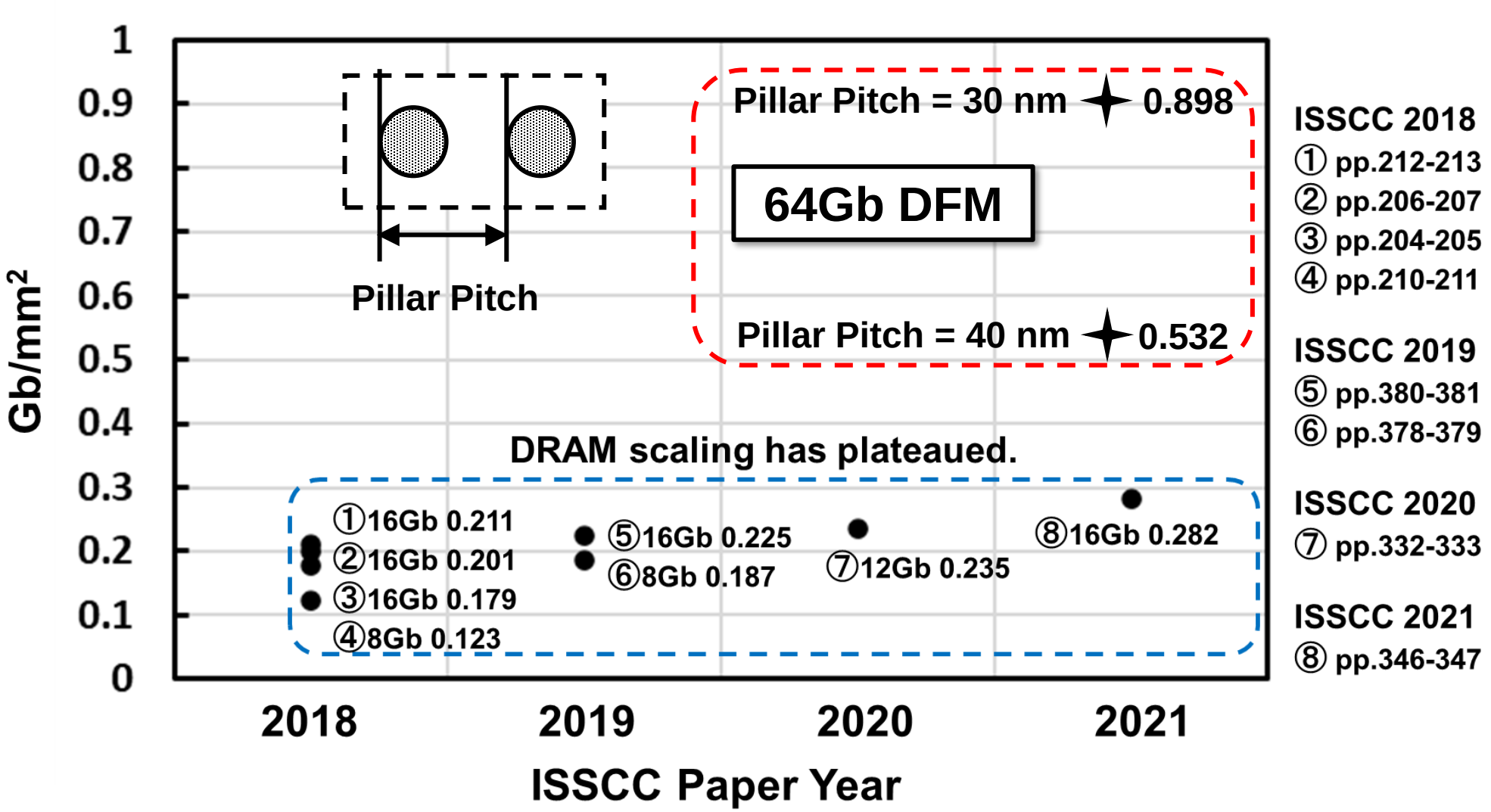
 ©2022 Flash Memory Summit. All Rights Reserved.

Perfect Read Non-Destructive DFM

1. Goal for Creating a DFM and 1T-DRAM Review
2. DFM Concept and Program/Erase/Read Mechanism
3. Block and Bit by Bit “0” Refresh
4. DFM Prospects and Potential
5. Conclusion

 ©2022 Flash Memory Summit. All Rights Reserved.

DFM vs DRAM



 ©2022 Flash Memory Summit. All Rights Reserved.

DFM Prospects and Potential

Speed

1. DFM is a ‘gain cell’, which can drive the BL charges quickly. This means that it can be sensed dynamically (like DRAM) and also statically (like NAND Flash).
2. No restore period with sense amplifiers is needed for every read cycle. DFM can be refreshed by multiple pages of the block simultaneously, which will reduce the allocated refresh duty ratio.
3. We are in the process of obtaining experimental data for a DFM prototype, and believe that the system speed could be improved significantly.

Scalability

1. 3D DFM can be designed and fabricated using several architectures, such as the vertical SGT DFM, and lateral FinFET or stacked GAA DFM.
2. If the pillar pitch of the SGT DFM could be shrunk to 40nm or 30nm, the SGT DFM has a substantial potential to realize a higher density memory than that of DRAM.

 ©2022 Flash Memory Summit. All Rights Reserved.

Volatile Memory Ranking

Flash Memory Summit

Bit Cost

Low Bit Cost

1. DFM
2. DRAM
3. SRAM

Speed

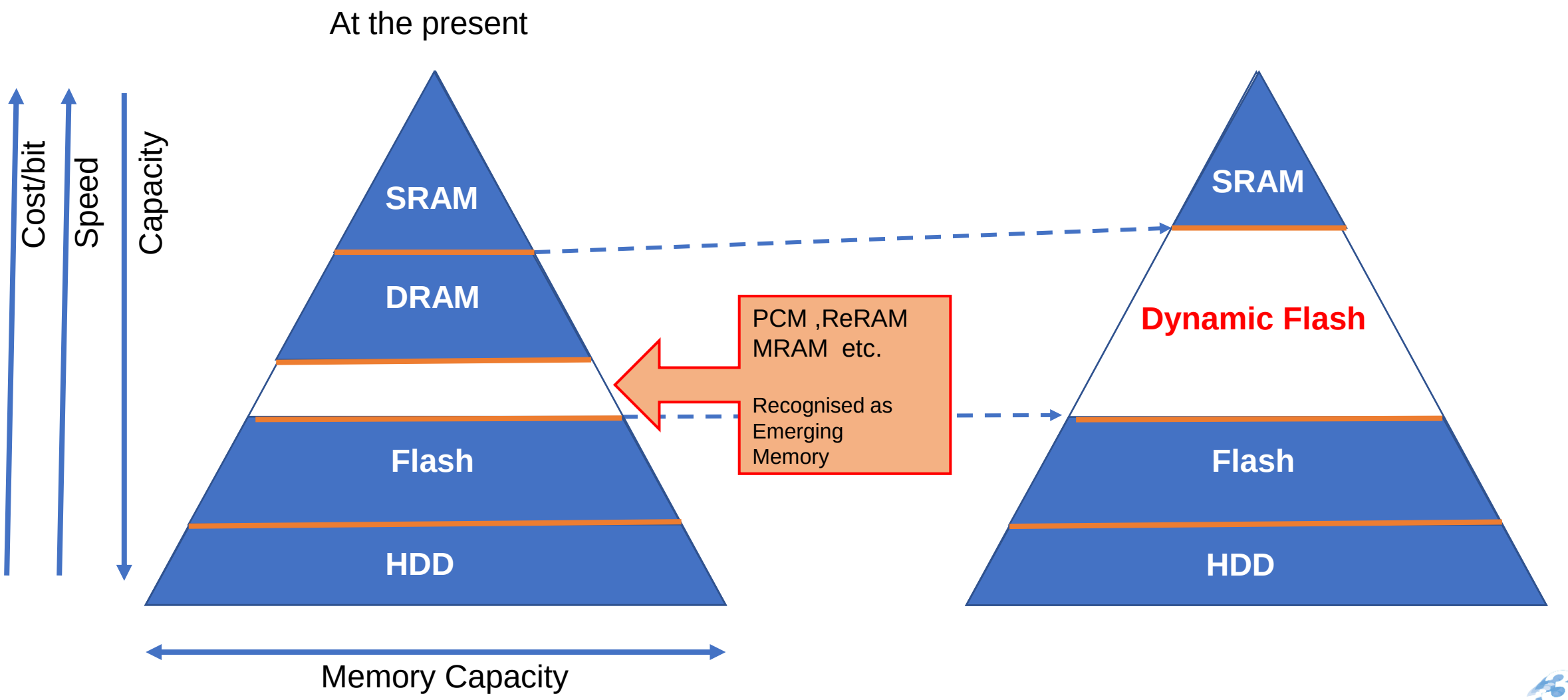
High Speed

1. SRAM
2. DFM
3. DRAM

 ©2022 Flash Memory Summit. All Rights Reserved.

35 YEARS OF NAND FLASH MEMORY INNOVATION

Potential DFM Position



 ©2022 Flash Memory Summit. All Rights Reserved.

Perfect Read Non-Destructive DFM

1. Goal for Creating a DFM and 1T-DRAM Review
2. DFM Concept and Program/Erase/Read Mechanism
3. Block and Bit by Bit “0” Refresh
4. DFM Prospects and Potential
5. Conclusion

 ©2022 Flash Memory Summit. All Rights Reserved.

Conclusion

1. The Dynamic Flash Memory (DFM) is a unique novel device.
2. 3D DFM has possibilities to be fabricated using structures such as the vertical SGT DFM, and lateral FinFET or stacked GAA DFM.
3. Unlike emerging memories, such as ReRAM and MRAM, neither variable resistors nor special materials are needed, which means that DFM can be fabricated with the conventional Si process.
4. A low cost DFM is a promising device positioned to DRAM and NAND in the memory hierarchy.

 ©2022 Flash Memory Summit. All Rights Reserved.