Flash Memory Summit

Teledyne LeCroy: End to End NVMe Debugging

Presented by:
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TELEDYNE LECROY
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35 YEARS OF NAND FLASH MEMORY INNOVATION

About the Presenters

Gordon Getty

About

- Technical Marketing Manager – Solutions Marketing
- 20 years experience in PCI and PCI Express testing and Compliance Programs
- Masters in Information Technology from University of Paisley, Scotland
- Bachelor of Engineering In Electronics with Music from University of Glasgow, Scotland

David Obert

About

- Sales Development Manager with Teledyne LeCroy, OakGate Products
- Prior to Teledyne LeCroy, 30 years experience as a Marketing Specialist with Hewlett-Packard
- MBA from Drucker School of Management, Claremont Graduate School

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Agenda: End to End NVMe Debugging

- Introduction and Quick Overview of NVMe
- Discussion of trigger types
- Hardware Setup
- Capturing NVMe Initialization on the Protocol Analyzer
- Overview of setting triggers in the Teledyne LeCroy OakGate Test Appliances system
- Overview of setting the trigger actions in the Teledyne LeCroy Summit series Protocol Analyzer
- Summary
- **Questions**

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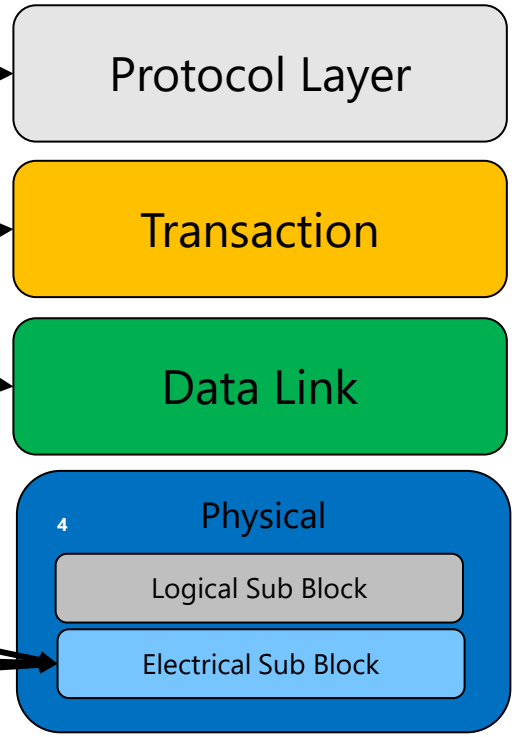
Objective

How do I find the root cause of unclear or intermittent problems when running NVMe Validation tests where the problems might be at any layer of the protocol stack?

- NVMe Protocol

Link and Transaction Layer
- Testing Link Training
- Lane Margining

Electrical
- Link Equalization/De-emphasis testing
- Transmitter Signal Quality
- Receiver Jitter Tolerance



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Quick Basics

Introduction and Overview

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Validating and Debugging NVMe Devices

- NVMe is now the standard protocol used for SSDs both in server and client platforms
- NVMe takes advantage of established transport and data link layers
- Thorough validation of devices helps to avoid post-release corner case issues
- Problems can show up as:
  - Drive failures
  - Performance problems
  - System crashes

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Background: What is NVMe?

- A family of specifications that define how host software communicates with non-volatile memory across multiple transports like PCI Express® (PCIe®)
- An industry standard specification was designed from the ground up for SSDs
- A much more efficient interface, providing lower latency, and is more scalable for SSDs than legacy interfaces
- The NVMe architecture brings a new high performance queuing mechanism that supports 65,535 I/O queues each with 65,535 commands
- The NVMe interface significantly reduces the number of memory-mapped input/output commands and accommodates operating system device drivers running in interrupt or polling modes for higher performance and lower latency
- The NVMe specification also contains host-to-device protocol for SSD commands used by an operating system for: read, write, flush, TRIM, firmware management, temperature, errors and others
- The NVMe Specifications are managed by NVM Express® consortium

Source: NVM Express®

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Types of Validation Tools

- Test Appliances
  - Host based emulation tool that allows the tester to generate a range of scripts with defined IO traffic patterns, admin commands and error injection
  - Allows Validation with complex traffic flows
- Protocol Analyzers and Exercisers
  - Provide insight into all activity on the link from the Logical PHY Layer up to the higher protocol layers including NVMe.
  - With analyzer and exerciser capabilities an ideal early development and debug tool in addition to providing conformance test capabilities
- Combining these Tools
  - Allows you to apply this system level intelligence and error recognition seen in host-based tools with the deep packet capture and granular detail on all levels of protocol analyzers

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Trigger Types

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Triggers

- **What is a trigger?** A trigger is any defined event that causes the Protocol Analyzer to stop overwriting any buffer information. On the OakGate system a trigger is a response to an error event
- **What is the challenge?** If I don't know exactly what problem I am trying to find defining the protocol analyzer trigger can be very challenging
- **Why do I care?** The more general OakGate triggers allows me to capture the areas of interest on the Protocol Analyzer to verify exactly what is happening in the problematic and surrounding transactions
- **Other Trigger Uses?** Yes, the trigger can also be used to place a marker in the analyzer trace and drive logs that can be used as a search key

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Error Trigger Options

- Have the test software mark the drive as having a fatal error so that NVMe traffic will cease and then the recording will stop
- Have the Protocol Analyzer trigger on the error event itself provided that the error pattern is well known and defined and can be configured as an analyzer trigger event
- Create a trigger event within the OakGate Appliance test software upon the introduction of the error and configure the Protocol Analyzer to trigger on the event

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Hardware Setup

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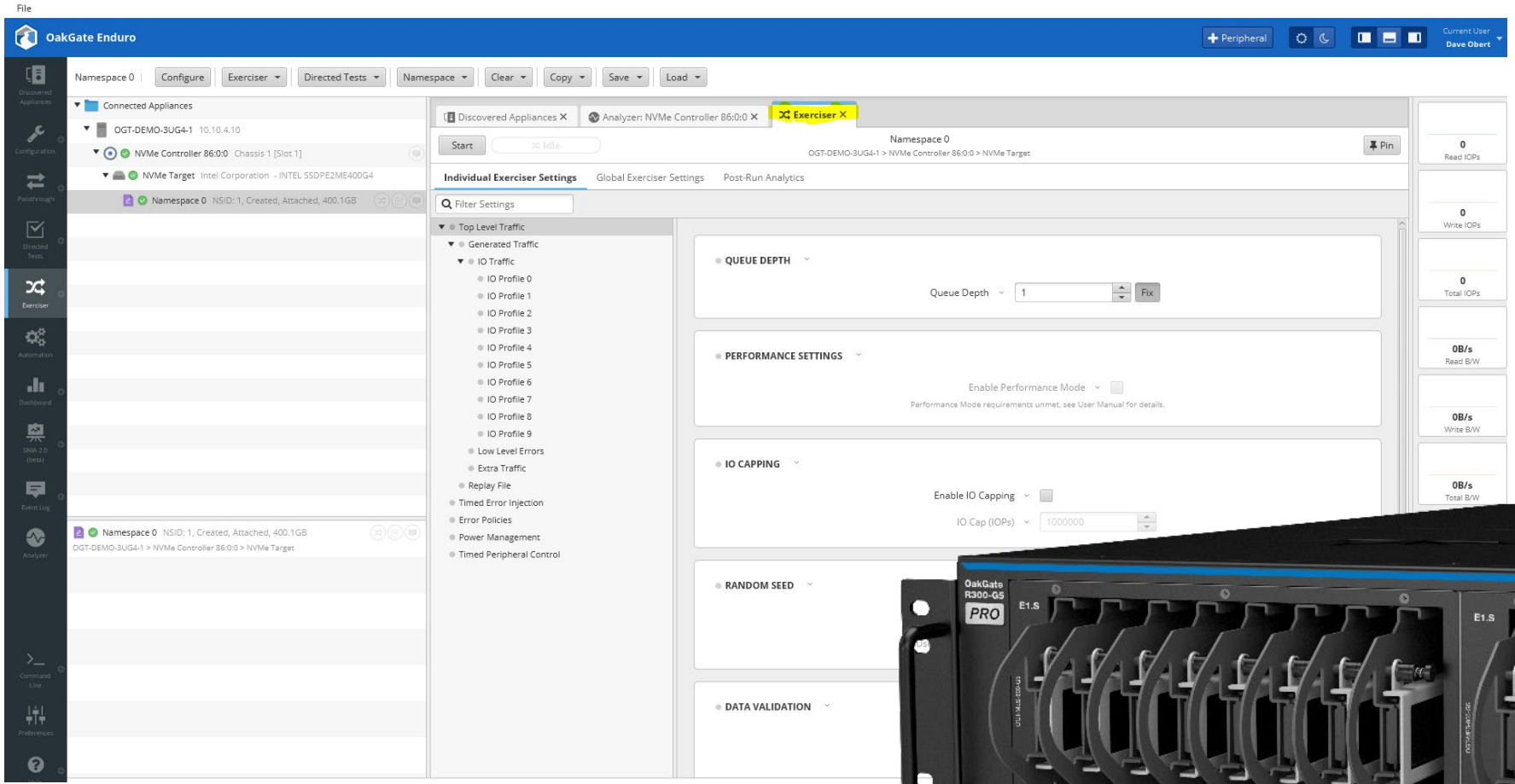
What is the OakGate Test Appliance?



Enduro Client Interface

Gen5 Appliance with Drive Bays

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What is a Teledyne LeCroy Protocol Analyzer?

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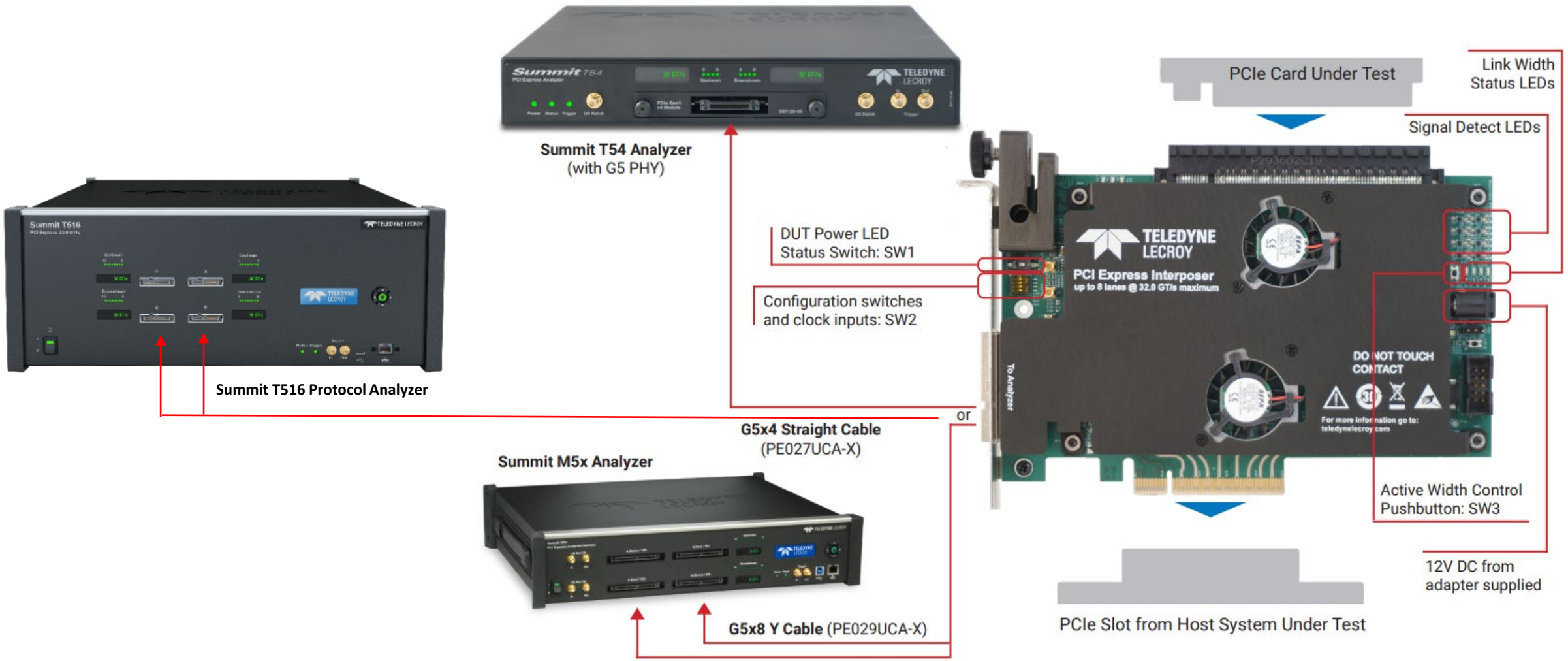
Protocol Analyzers Use Interposers for Probing



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Insert the U.2 Interposer into the U.2 Slot

- Insert SSD into Interposer
- Insert Interposer and SSD into Oakgate Test Appliance

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Process Flow Summary

Connect Hardware

1. Connect Protocol analyzer interposer into OakGate Test Appliance

Capture NVMe Decode

1. Configure Host Memory and NVMe Controllers (DUTs) in the Oakgate software
2. Power on Protocol Analyzer and configure to capture controller/queue initialization
3. Initialize Host Memory and NVMe Controllers within OakGate software

Set-up Triggers

1. Set up OakGate Events
2. Set up Protocol Analyzer Triggers and arm

Run Test and Capture Debug information

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Capturing NVMe Initialization on the Protocol Analyzer

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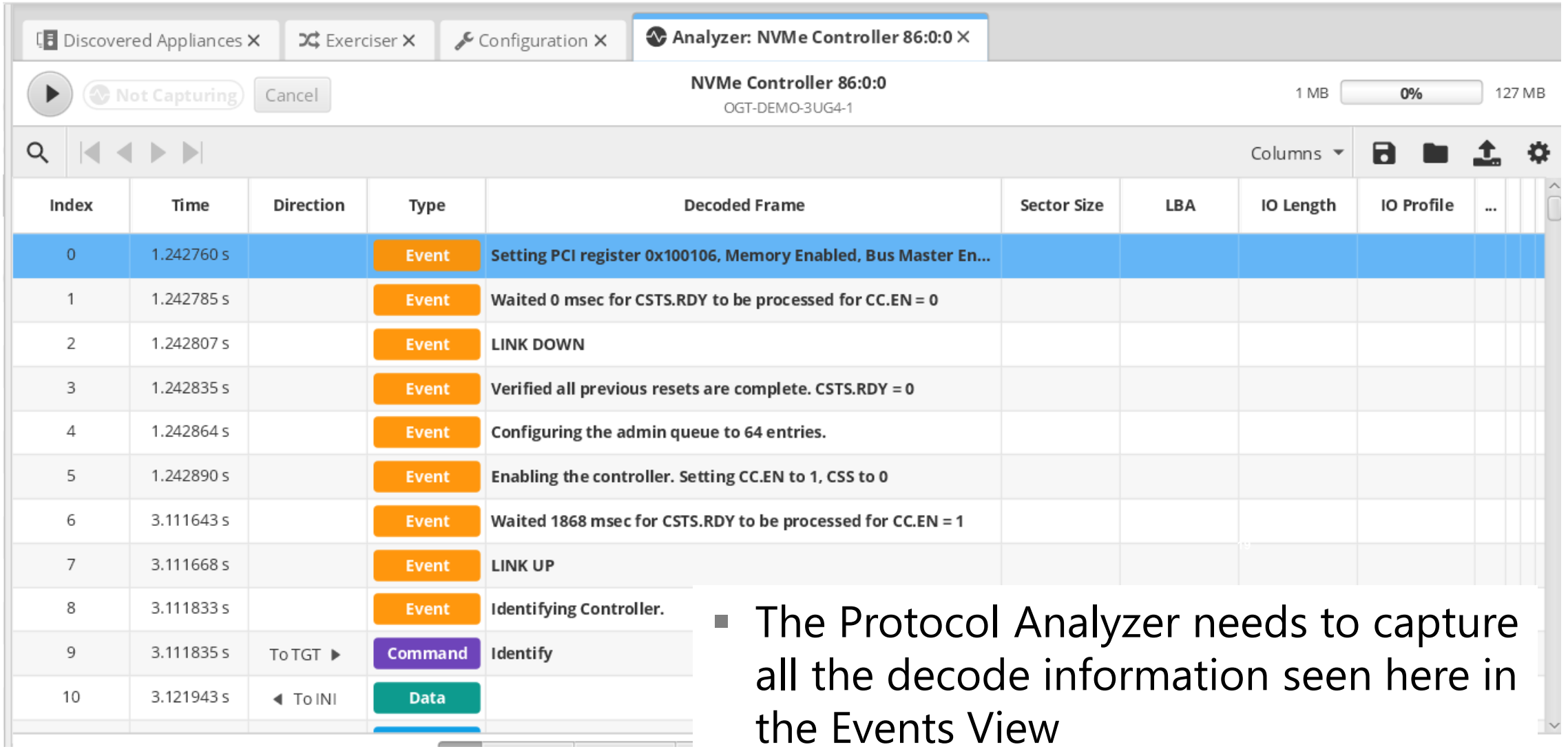
Capturing NVMe Decode Information



Index	Time	Direction	Type	Decoded Frame	Sector Size	LBA	IO Length	IO Profile	...
0	1.242760 s		Event	Setting PCI register 0x100106, Memory Enabled, Bus Master En...					
1	1.242785 s		Event	Waited 0 msec for CSTS.RDY to be processed for CC.EN = 0					
2	1.242807 s		Event	LINK DOWN					
3	1.242835 s		Event	Verified all previous resets are complete. CSTS.RDY = 0					
4	1.242864 s		Event	Configuring the admin queue to 64 entries.					
5	1.242890 s		Event	Enabling the controller. Setting CC.EN to 1, CSS to 0					
6	3.111643 s		Event	Waited 1868 msec for CSTS.RDY to be processed for CC.EN = 1					
7	3.111668 s		Event	LINK UP					
8	3.111833 s		Event	Identifying Controller.					
9	3.111835 s	To TGT ▶	Command	Identify					
10	3.121943 s	◀ To INI	Data						

- The Protocol Analyzer needs to capture all the decode information seen here in the Events View

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Setting up the Protocol Analyzer

- Since the address assignment in NVMe is dynamic – i.e. it may vary from boot to boot, it is necessary to capture the locations of the queues that the system sets up
- This is straightforward and can be done using a simple trigger on the protocol analyzer to capture all the initialization information
- This information will be used when the test is run to allow the protocol analyzer to trigger on the correct NVMe command

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Set up the Protocol Analyzer Trigger

- The Protocol Analyzer can be triggered by:
  - A pattern on the bus/link
  - An external event – such as a trigger input line pulse
- These are both set up using the Recording Options Dialog
- NVMe Triggers can be set as patterns
  - These may require some additional information
  - The information can be extracted from the Oakgate Software
  - NVMe triggers on the Protocol Analyzer are PCIe triggers with defined addresses and payload
  - Recording the system boot or initialization will also allow the Protocol Analyzer to capture this information
  - The trigger could be based on an error event indicated by the Oakgate system

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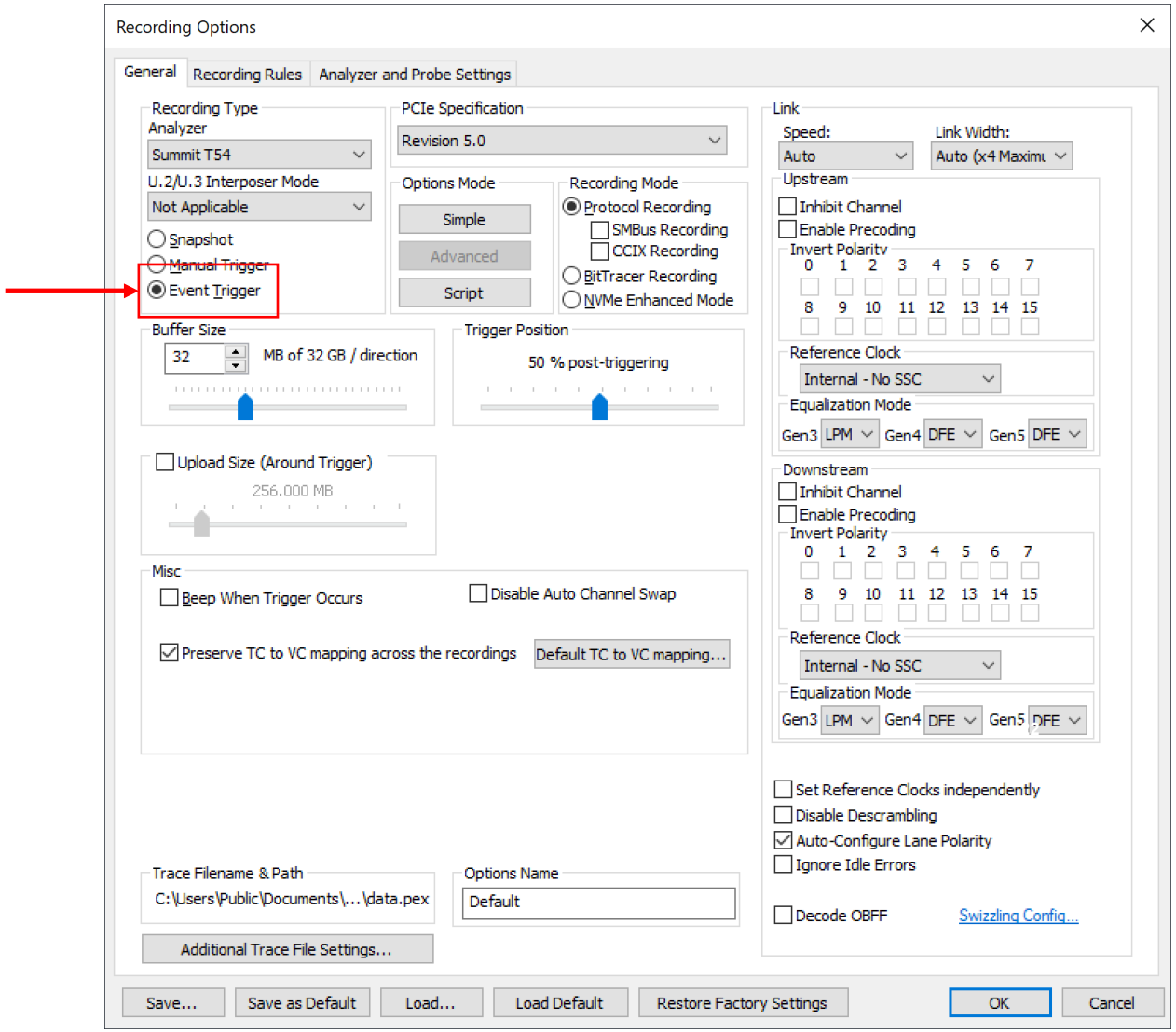
Protocol Analyzer Recording Options

Choose Event Trigger



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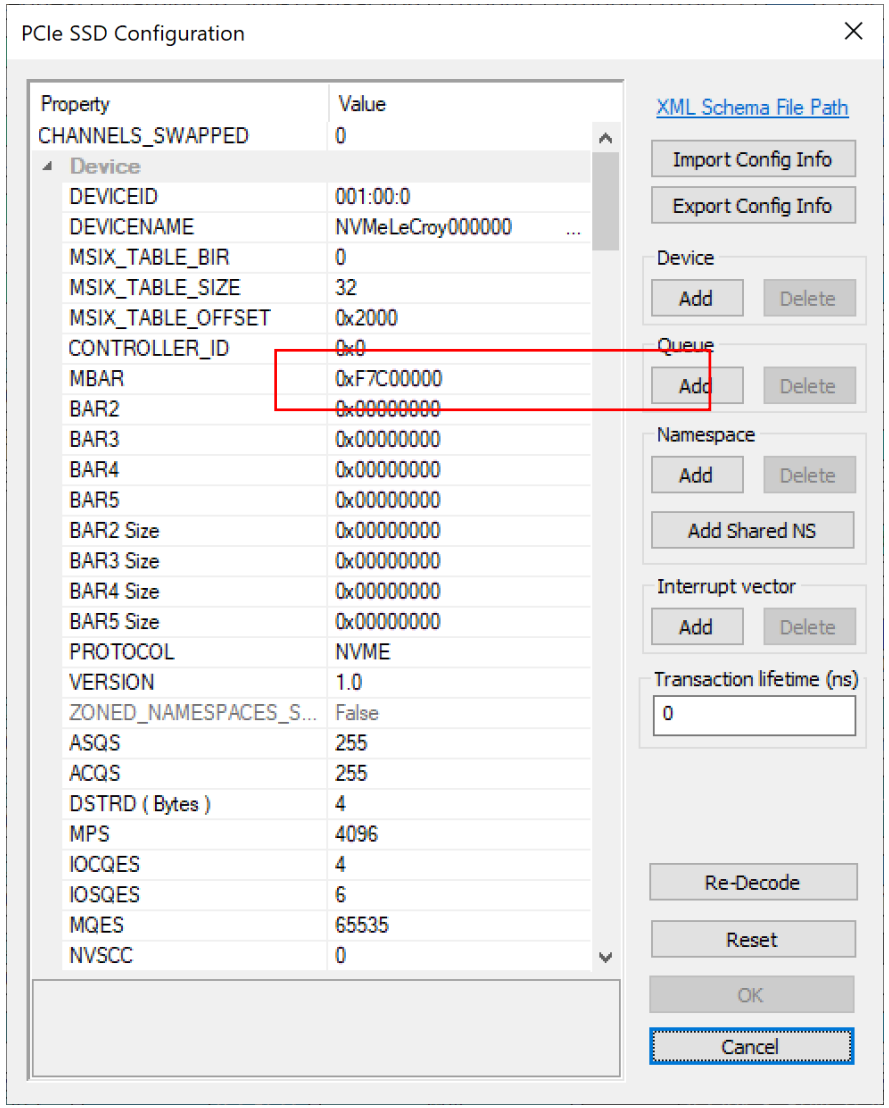
PCIe SSD Base Address Mapping



- When the Protocol Analyzer records the boot/initialization of the Oakgate system, it will enable the decoding of the PCIe Traffic into NVMe Traffic
- The NVMe triggers require this information to be present
- NVMe addresses are mapped from the MBAR address set by the system

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Defining the Trigger in the OakGate Test Appliance

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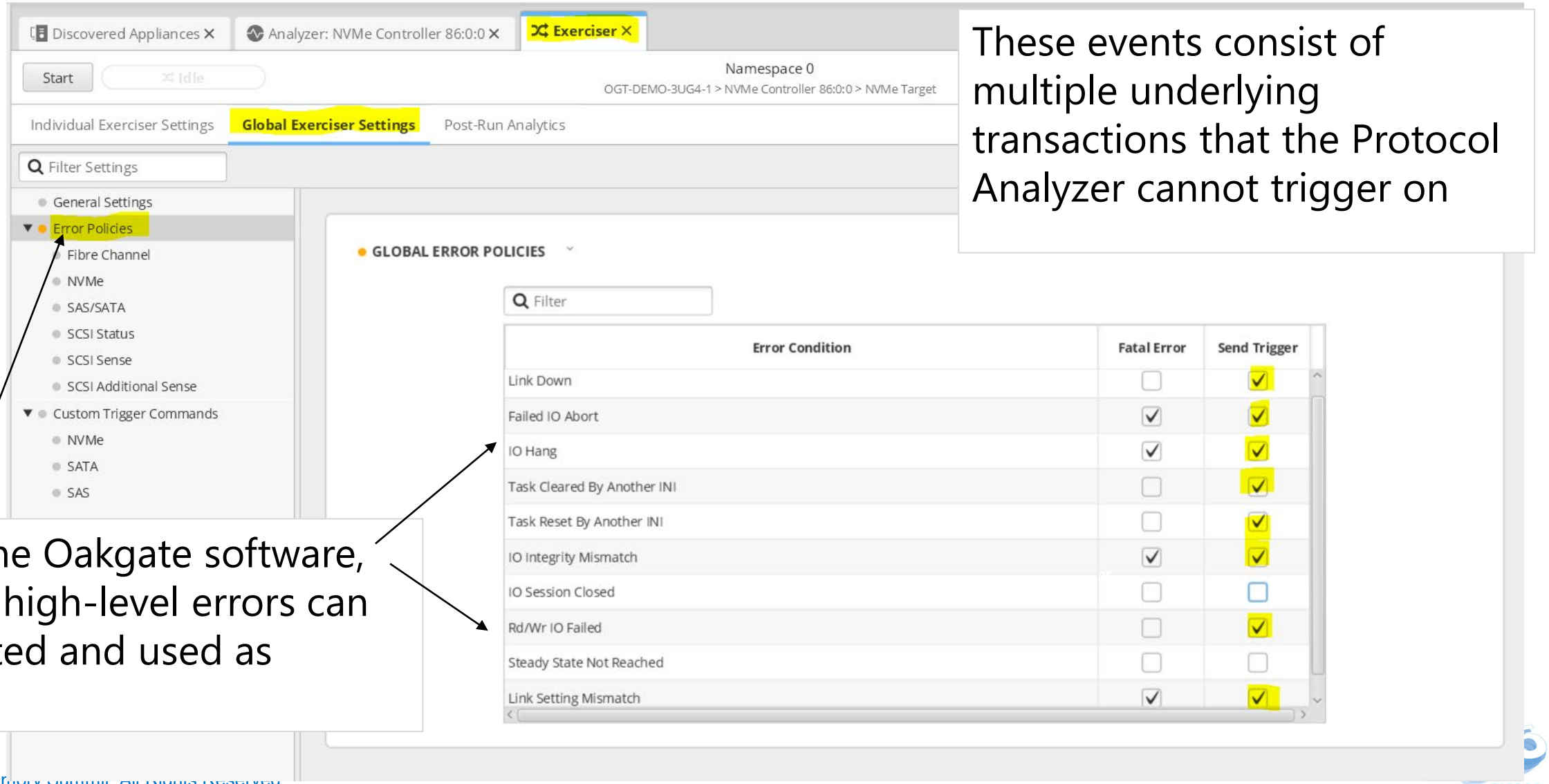
Setting Trigger Events



These events consist of multiple underlying transactions that the Protocol Analyzer cannot trigger on

Within the Oakgate software, multiple high-level errors can be selected and used as triggers

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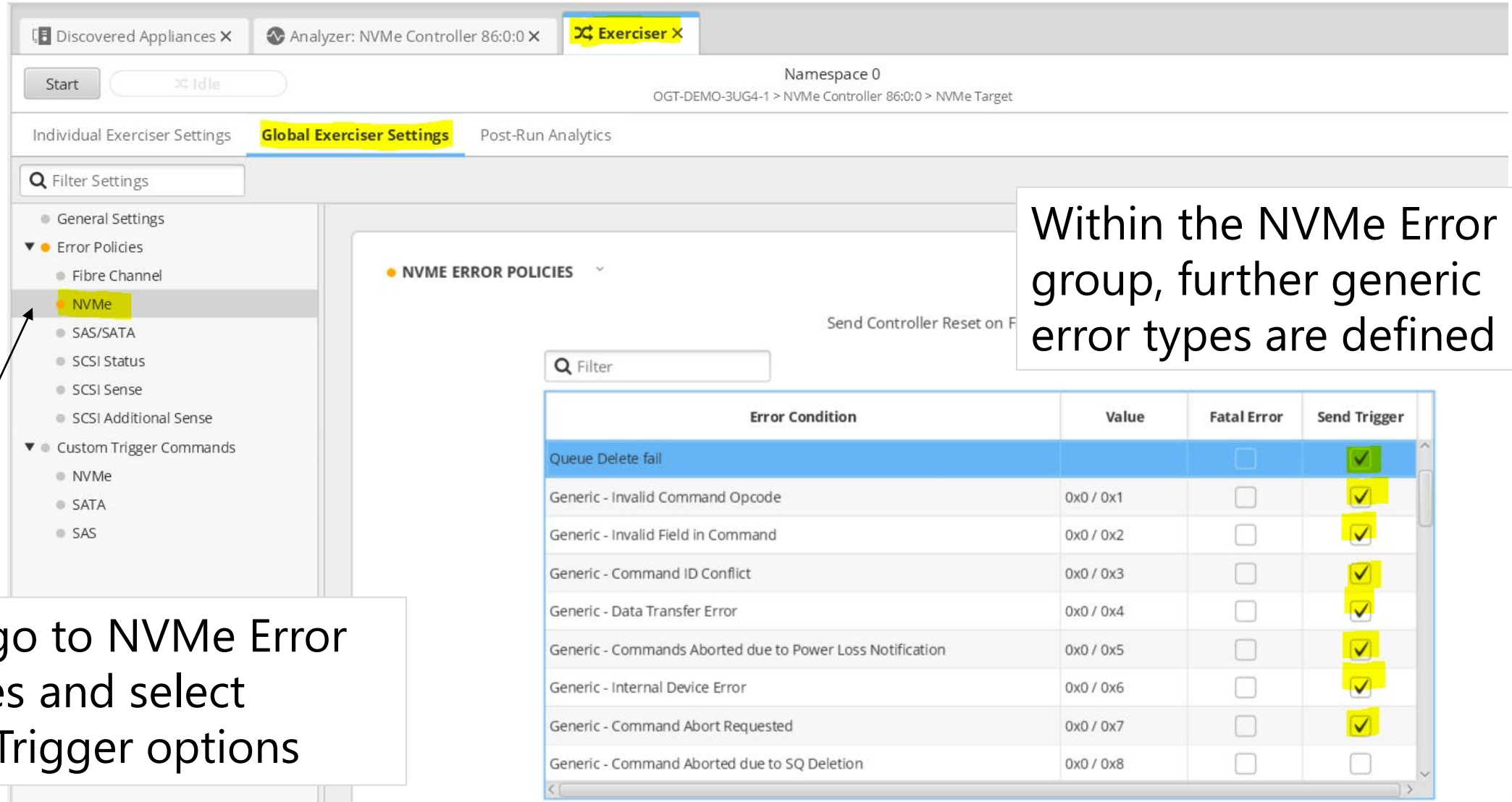
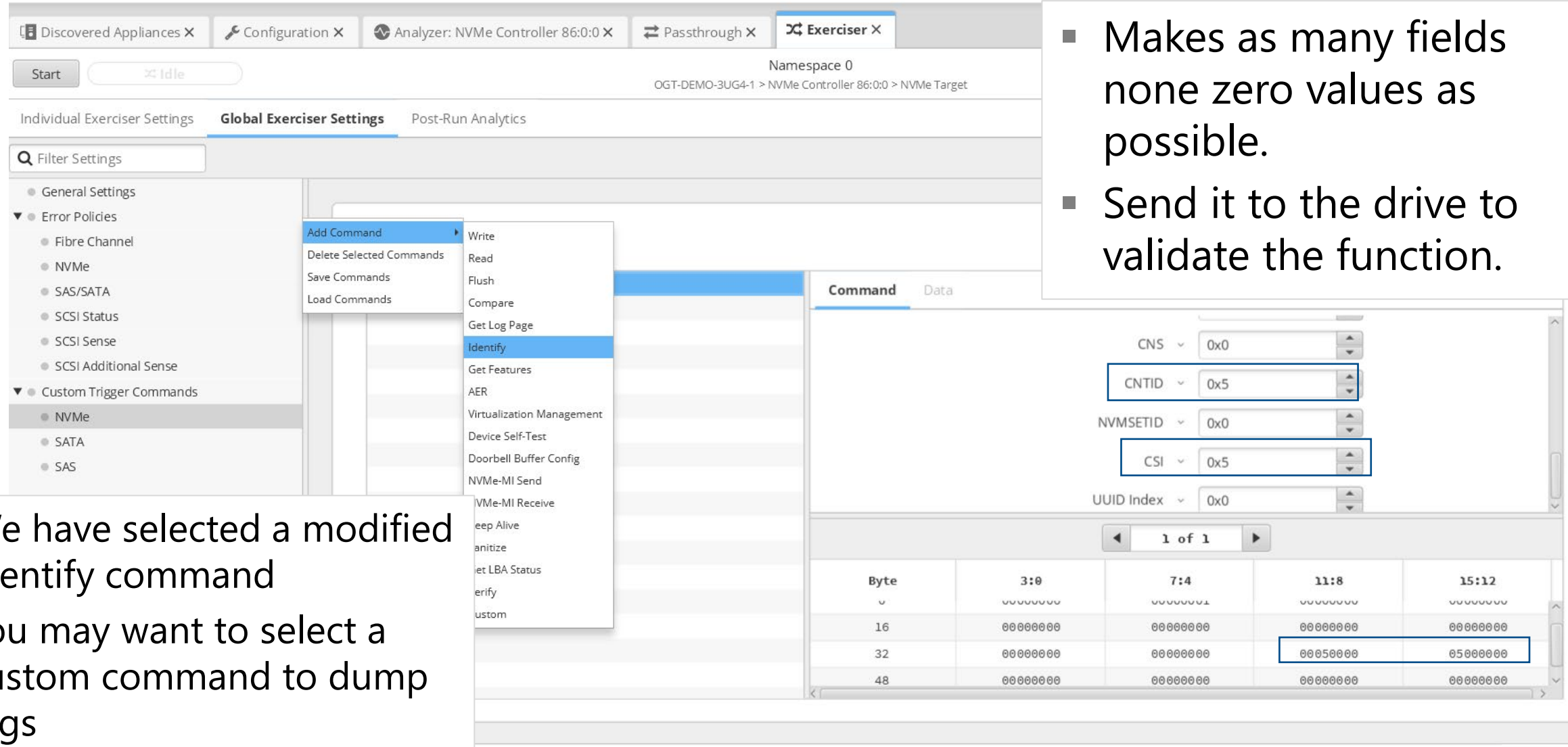
Setting Trigger Events



Within the NVMe Error group, further generic error types are defined

- Next go to NVMe Error Policies and select Send Trigger options

Define your Trigger Event in Oakgate Test Software



- Makes as many fields none zero values as possible.
- Send it to the drive to validate the function.

- We have selected a modified Identify command
- You may want to select a custom command to dump logs

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Defining the Trigger in the Teledyne LeCroy Analyzer

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Defining the trigger on the Protocol Analyzer

- The Protocol Analyzer will look for the event on the PCI Express link
- The NVMe event, is a sequence of PCI Express events
- Once the Protocol Analyzer has the NVMe queue information, either by capturing the boot sequence or providing the information manually from the Oakgate software, the Protocol Analyzer can be armed and wait for the event to happen

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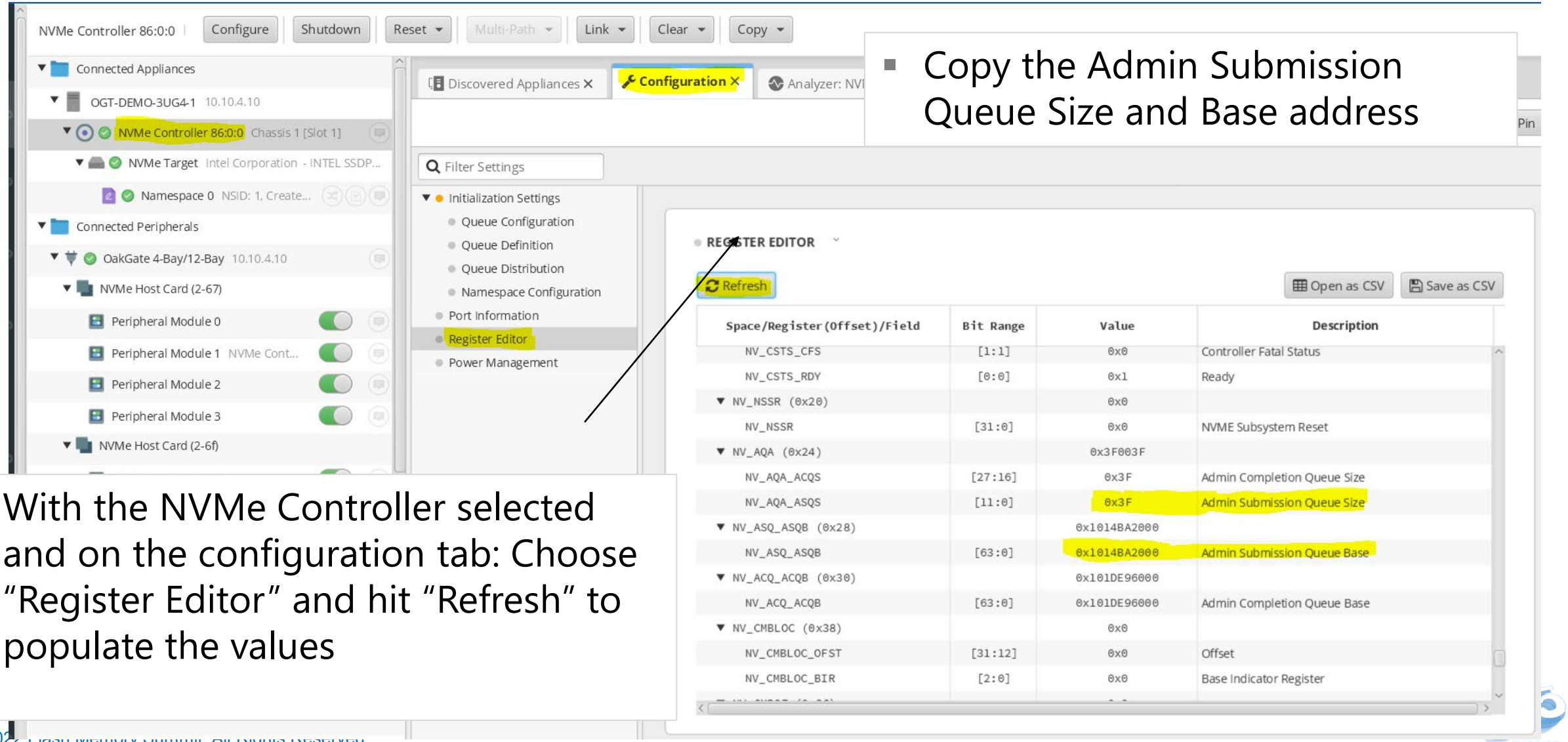
Obtain the Admin Queue Base Address and Size



- Copy the Admin Submission Queue Size and Base address

- With the NVMe Controller selected and on the configuration tab: Choose “Register Editor” and hit “Refresh” to populate the values

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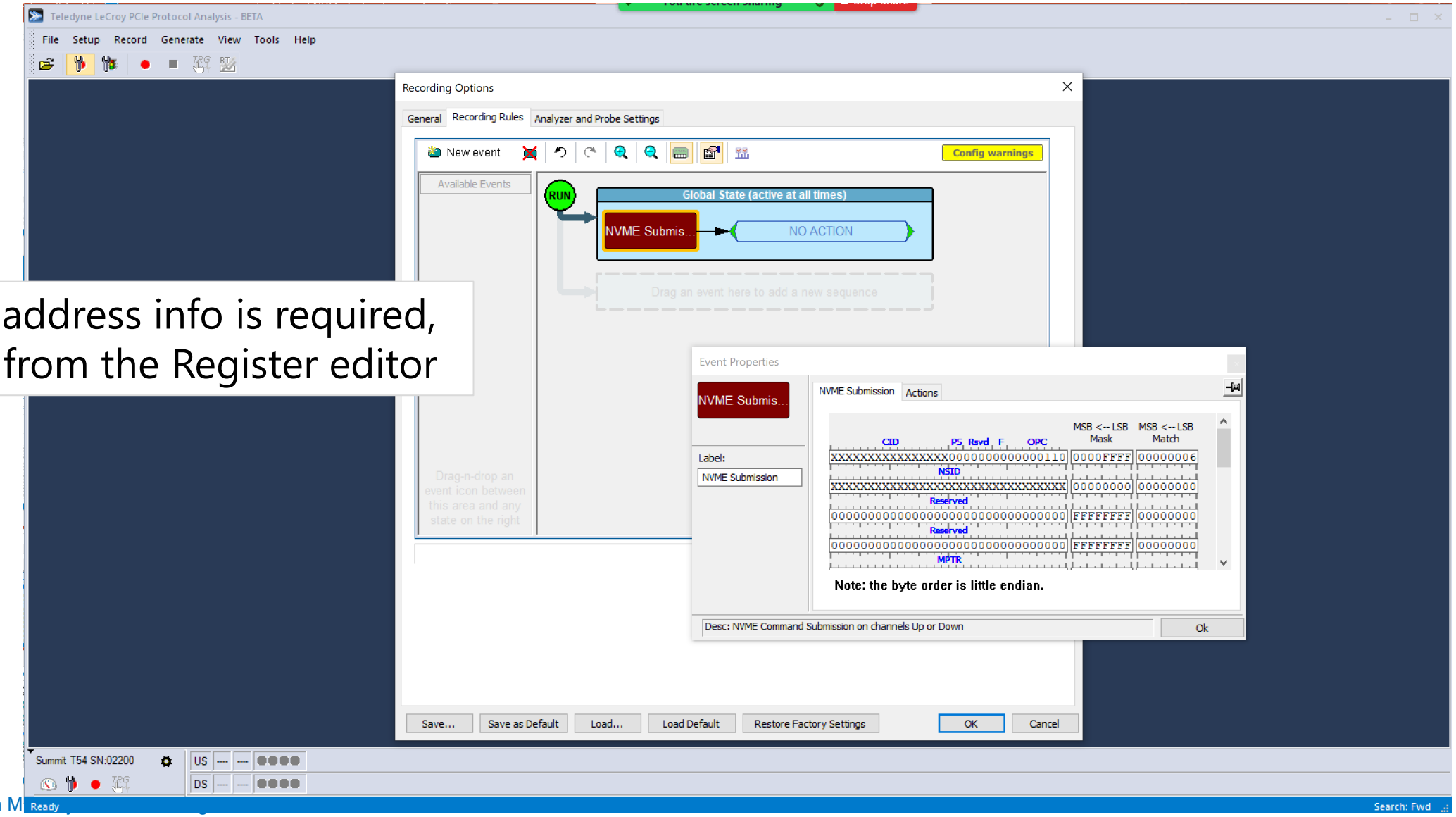
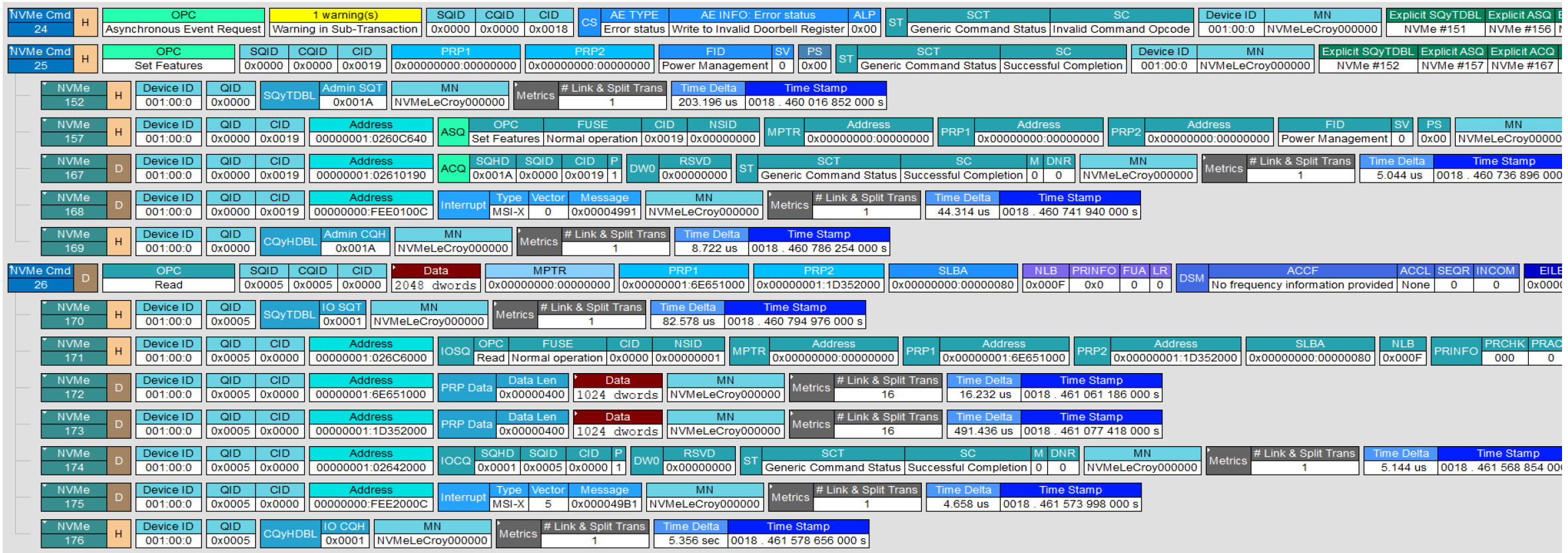
Setting up the Protocol Analyzer for the Error Trigger



If the address info is required, get it from the Register editor

Protocol Analyzer View of NVMe Traffic

The Protocol Analyzer trace can give a very detailed view of the NVMe traffic, all the way down to the PCIe Data Link and Transaction Layers



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Summary

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Summary

- Using Trigger Events on Oakgate Test Appliance to trigger Protocol Analyzer can be a very useful way to root cause errors
- Gives full visibility that might be difficult to find otherwise
- Use Generic triggers to find broader range of errors without needing to define each case specifically
  - Using the Oakgate system will allow the user to select a range of errors without knowing in advance which error may occur
- The Protocol Analyzer will provide the specific details around the error condition
  - Use the same Protocol Analyzer trigger each time, based on the definition from the Oakgate software, saving time and effort

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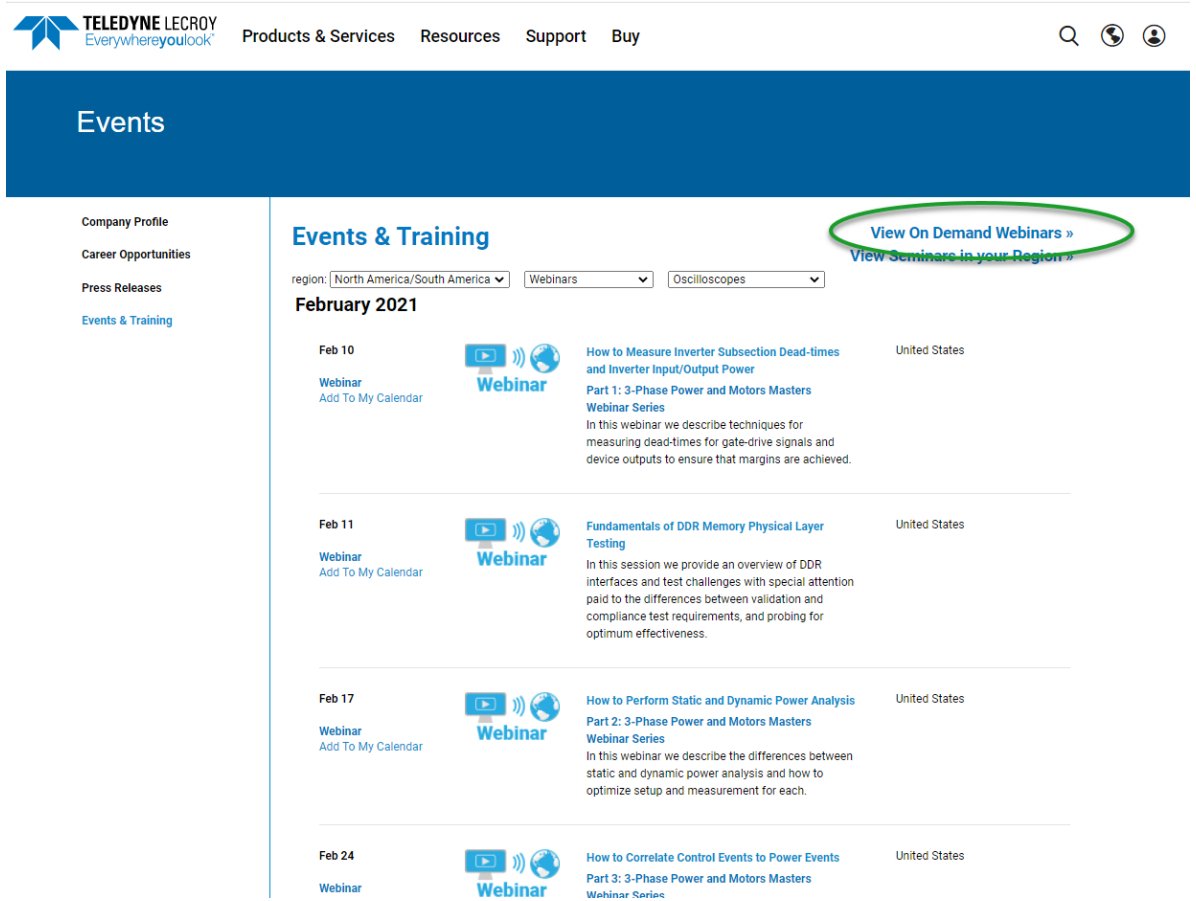

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Questions

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Summit M5x Analyzer/Jammer
Gen 4 up to x16 (Gen 5 Capable up to x8)

Summit T416 Analyzer
Gen 4 up to x16

Summit T516 Analyzer
Gen 5 x16

Summit T3-16 Analyzer

Summit T3-8 Analyzer

Summit T54 Analyzer
Gen 5 up to x4

Summit T28 Analyzer

Summit T48 Analyzer
Gen 4 up to x8

Summit Z416 Exerciser
Gen 4 up to x16

Summit Z58 5.0 Exerciser/Analyzer
Gen 5 up to x8

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