Ferroelectric FET

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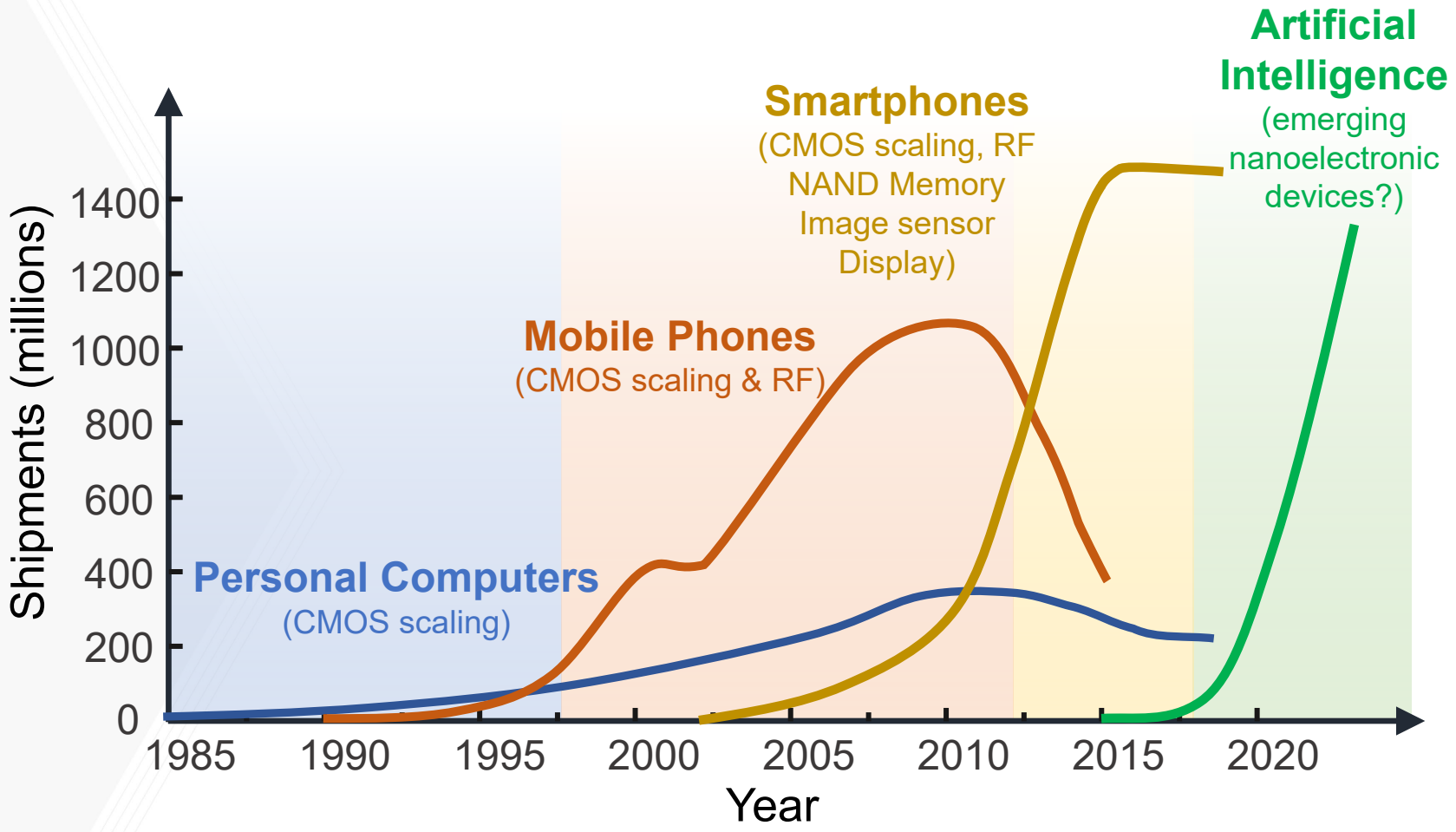
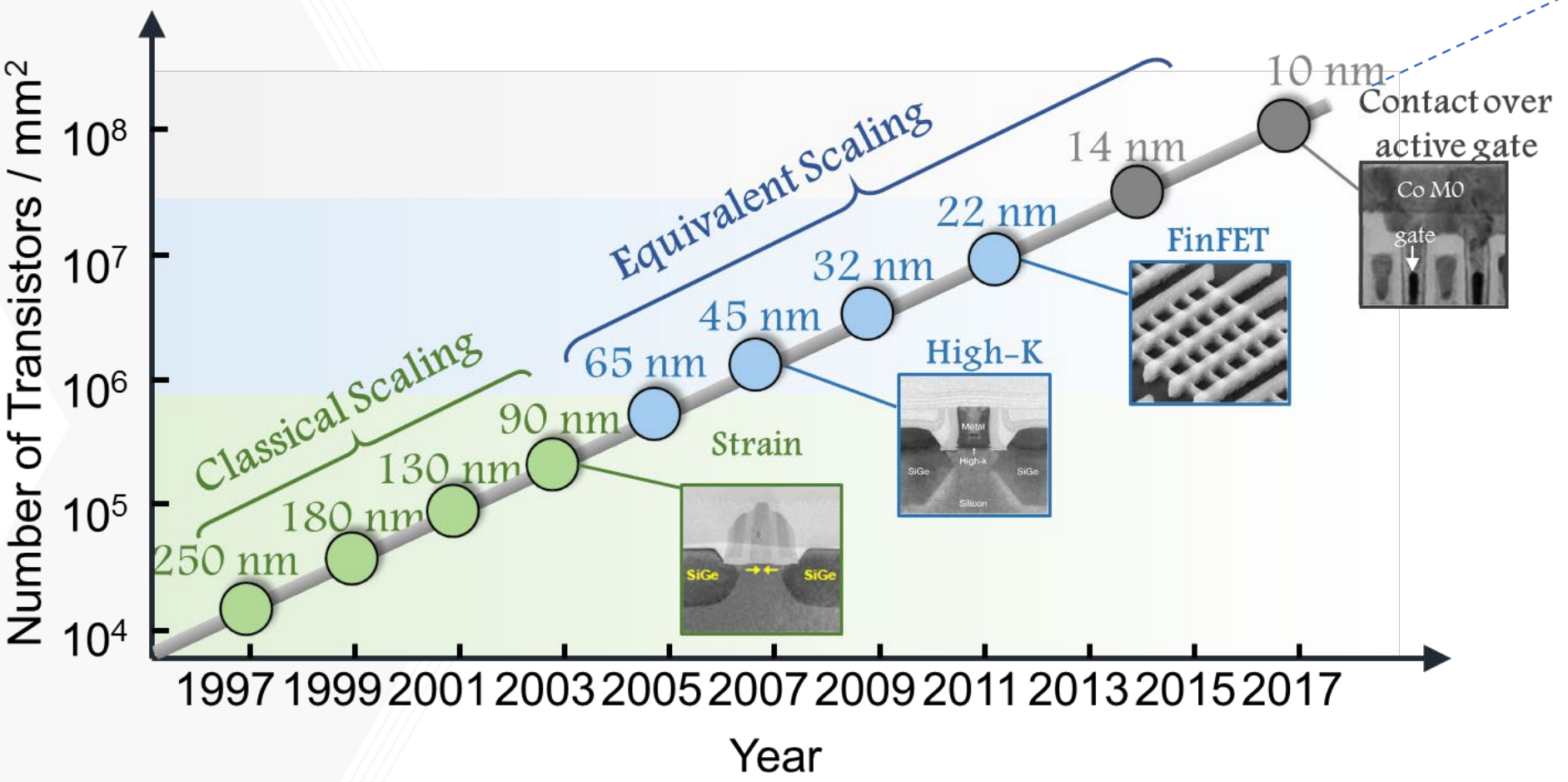
Waves of Computing

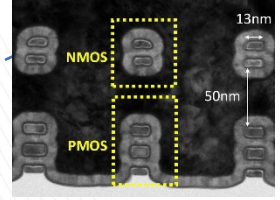


AI hardware accelerators are poised to be embedded in future computing devices.

Source: https://www.economist.com/briefing/2015/02/26/the-truly-personal-computer
https://www.statista.com/chart/12798/global-smartphone-shipments/

Logic and SRAM Scaling





Logic scaling continues enabled by innovation in materials, devices, process integration & DTCO

S. Salahuddin, K. Ni and S. Datta, "The era of hyper-scaling in electronics," Nature Electronics, 2018

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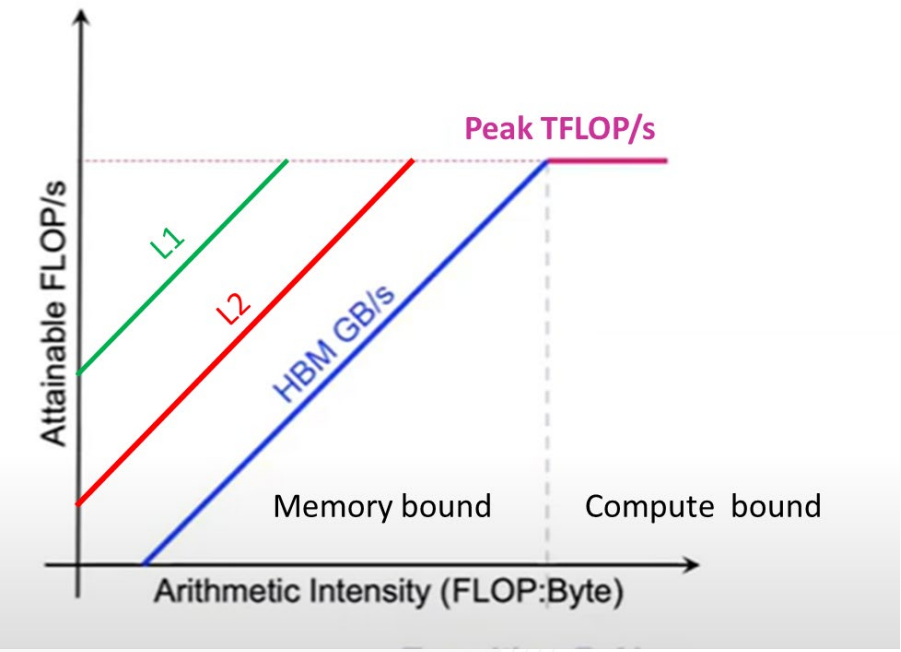
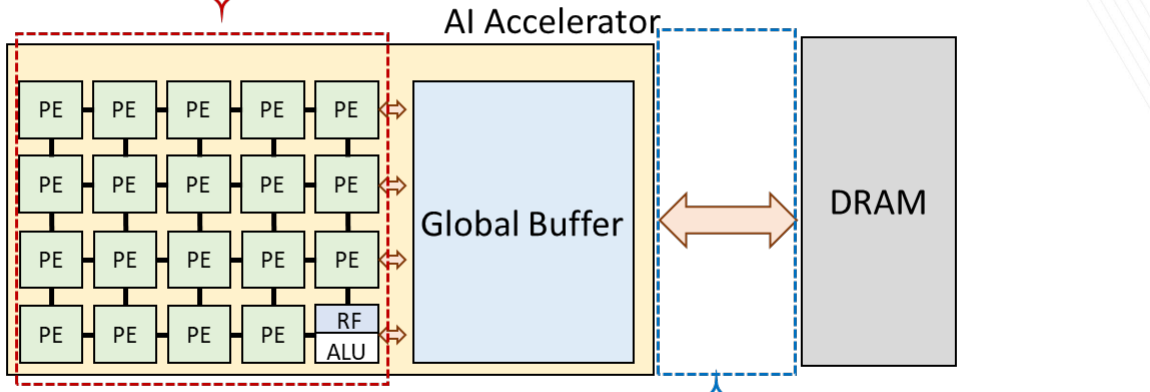
Roofline Performance



$$\text{Peak throughput} = N_{cores} \times F_{cores} \times \frac{OP}{cycle}$$



$$\text{Memory bandwidth} = Width_{bus} \times F_{bus} \times \text{Data Rate}$$

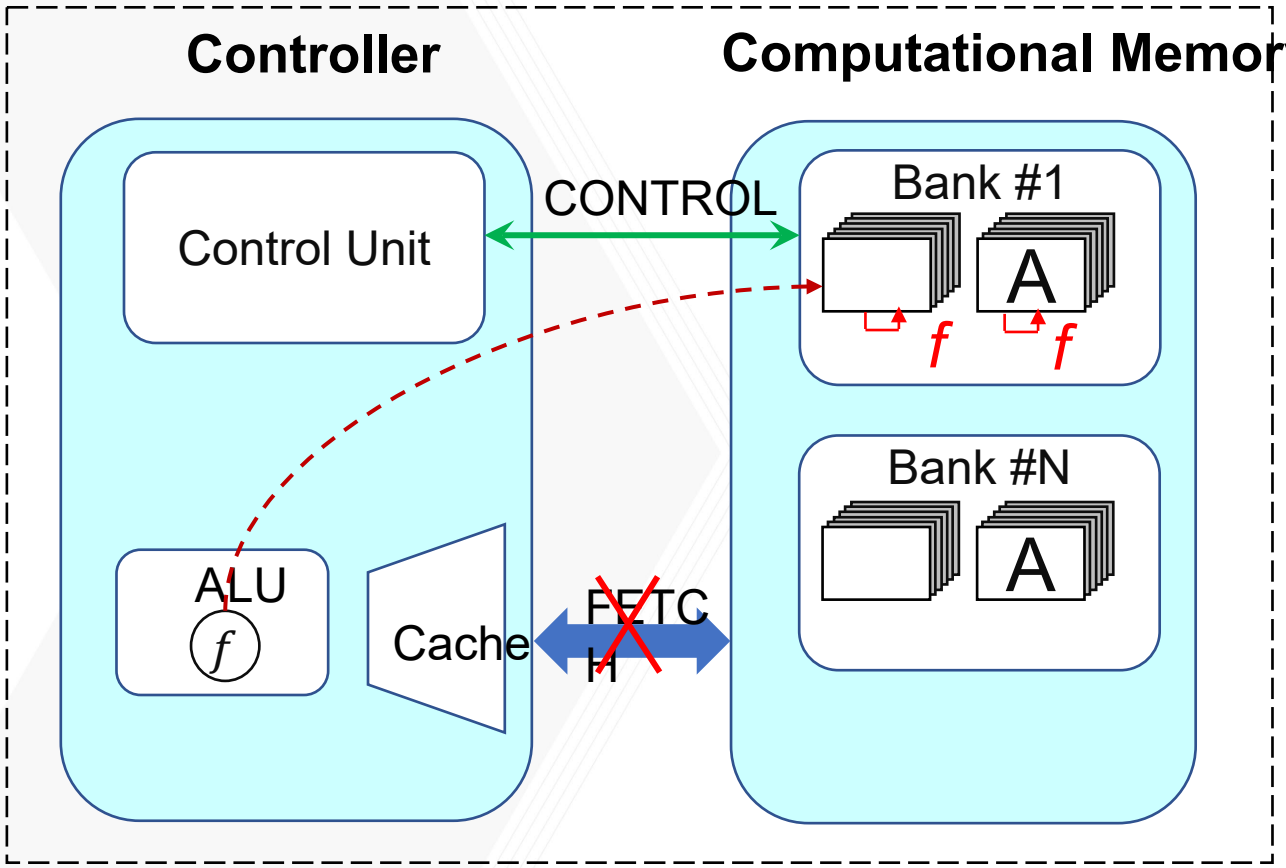
Arithmetic Intensity = FLOPS / Bytes (moved)

- **Compute Bound**: logic transistor performance, improve wire RC, stack more layers with high intertier via density
- **Memory bandwidth Bound**: Internal: Memory layer stacking with high TSV density, External: core to HBM interconnect using Si interposer

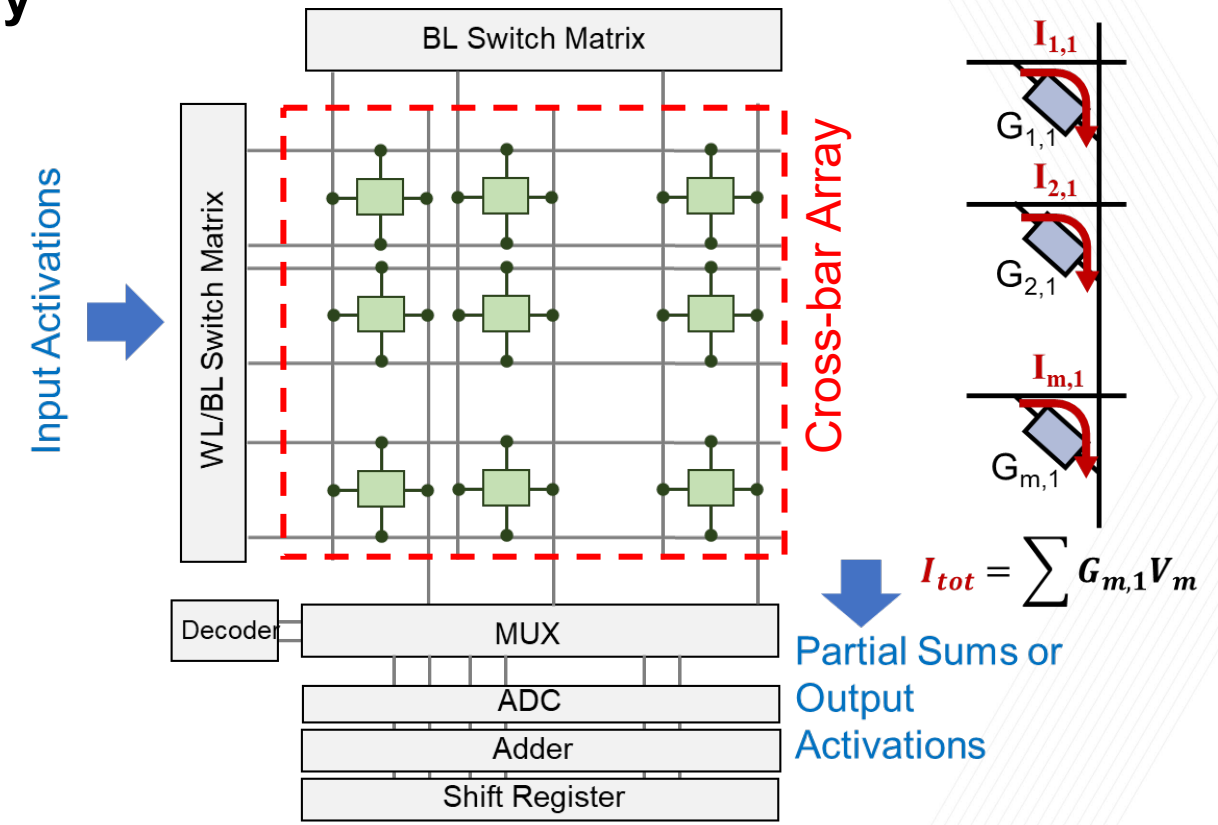
C Yang, T Kurth, S Williams "Hierarchical Roofline analysis for GPUs:….. ", Concurrency and Computation: Practice and Experience (CCPE), Aug 2019

In-memory Compute

In-memory Computing



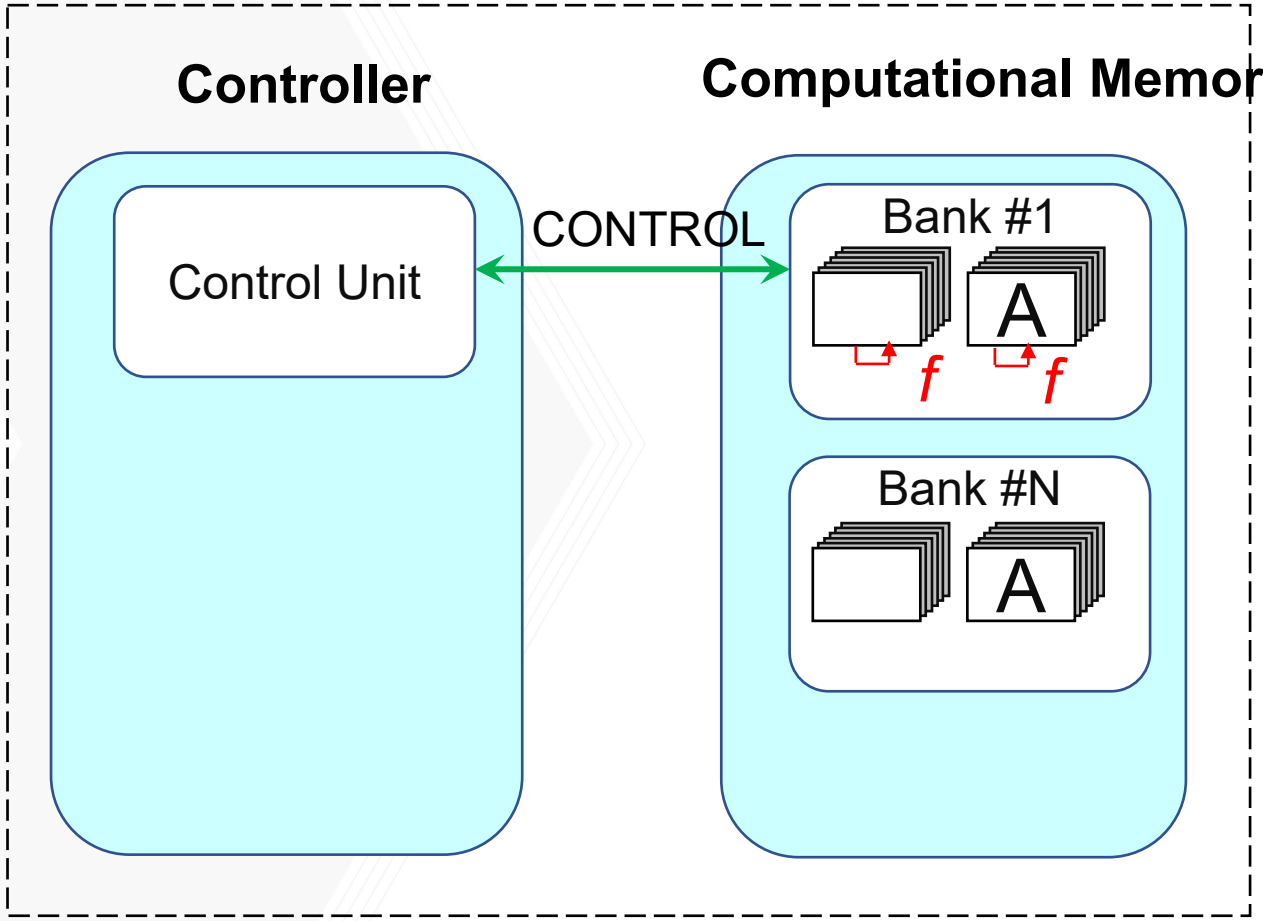
Example: Synaptic Core

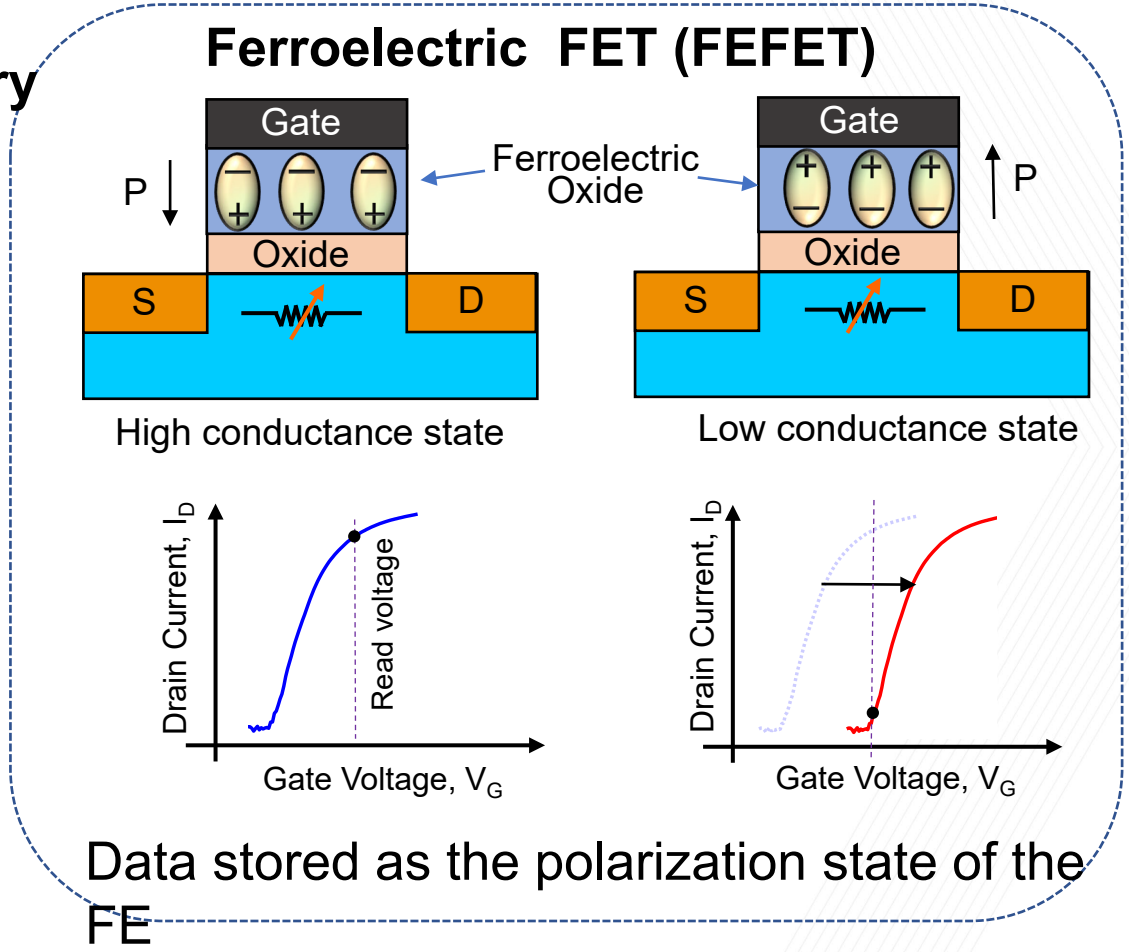


- Perform computational tasks within the memory itself
- Alleviates the memory bottleneck

Ferroelectric FET as Computational Memory

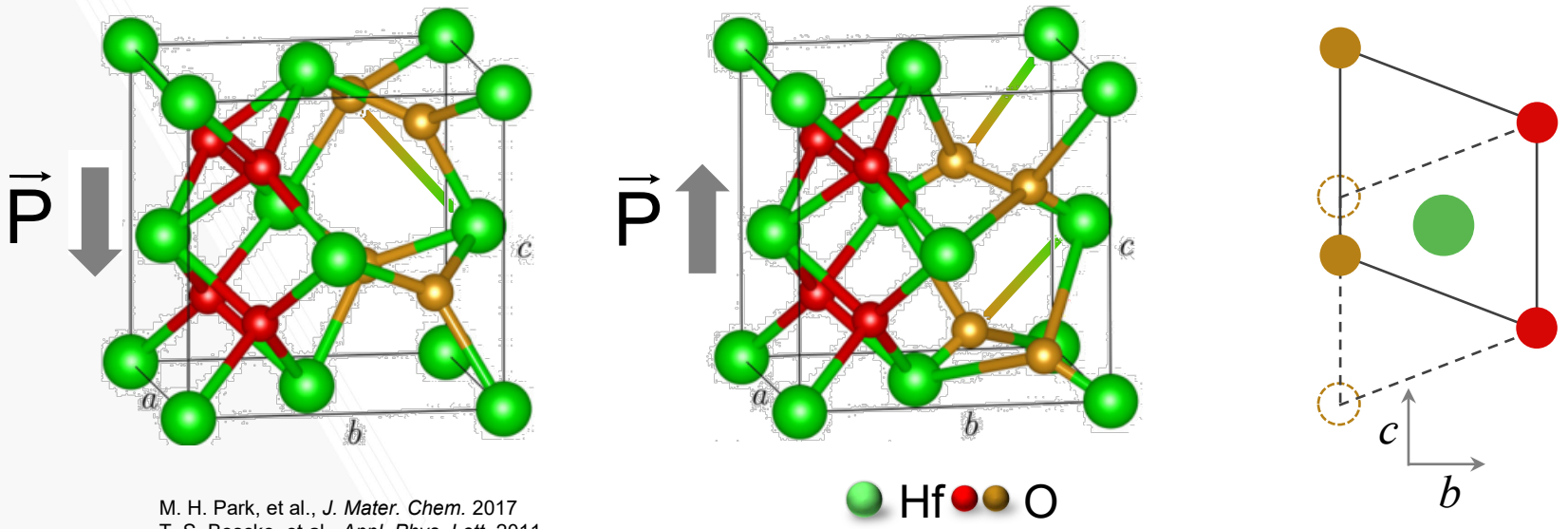
In-memory Computing



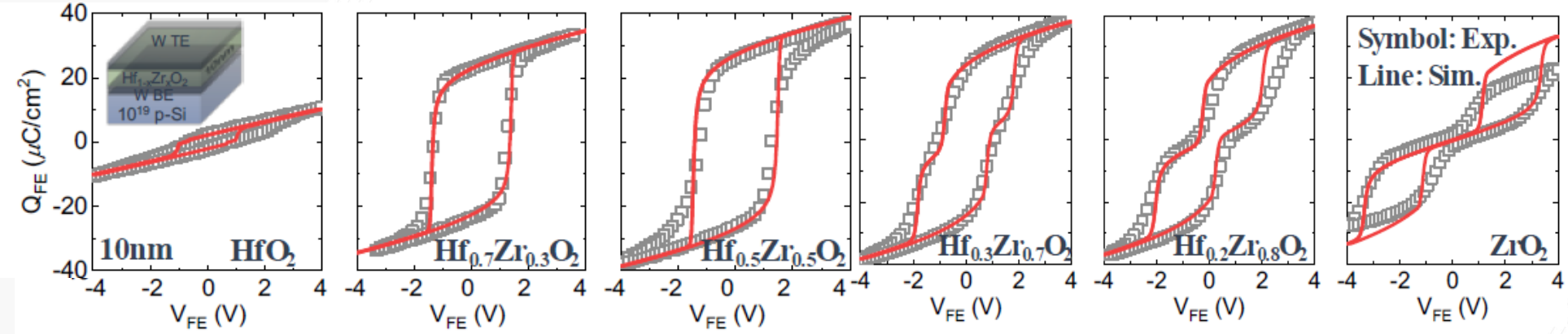


- FEFET stores information by means of polarization charge within the FE film.
- Polarization charge is translated into channel conductance and read as drain current

Ferroelectricity in doped HfO_2

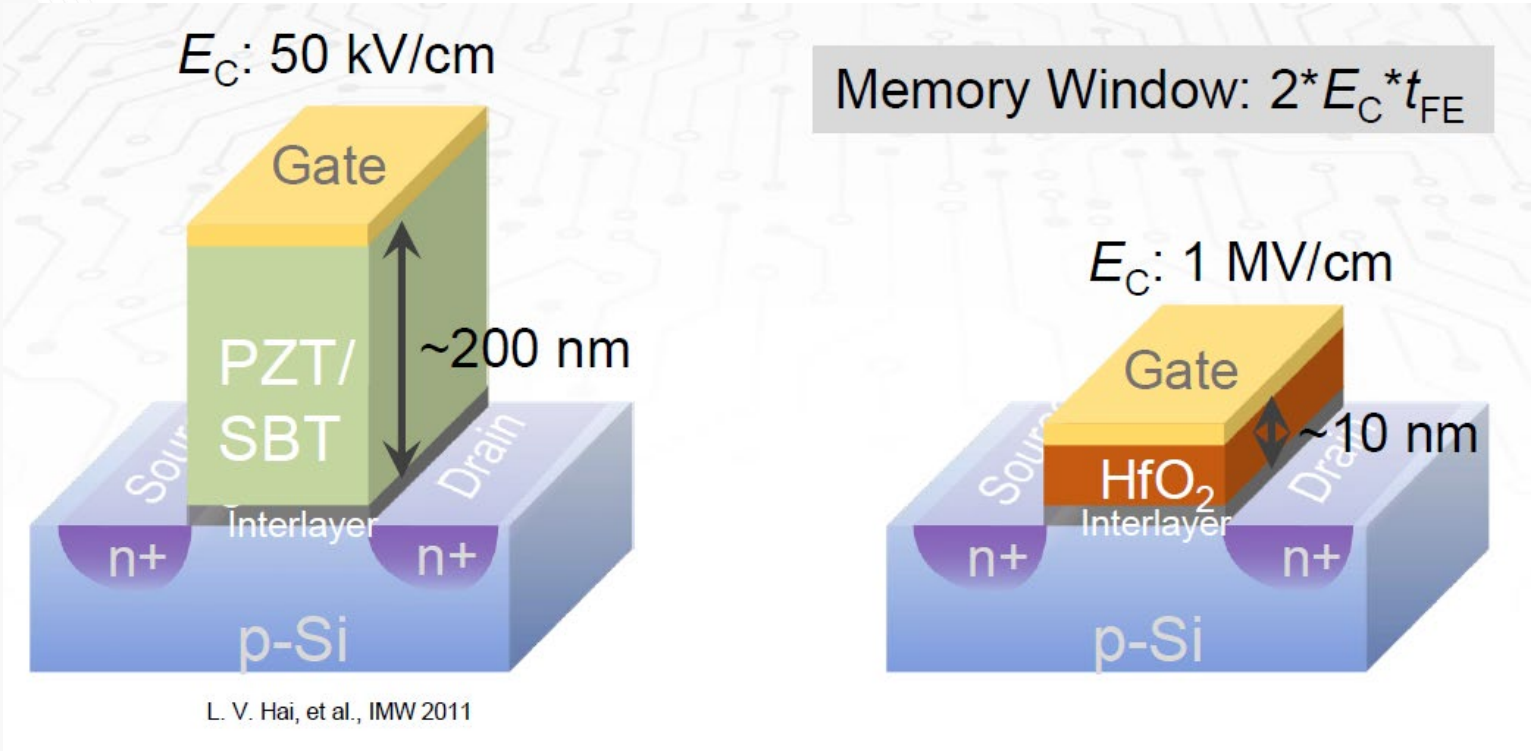


M. H. Park, et al., *J. Mater. Chem.* 2017
T. S. Boscke, et al., *Appl. Phys. Lett.* 2011



Orthorhombic phase HfO_2 exhibits ferroelectricity and is CMOS compatible, scalable down to 5nm

HfO_2 FerroFET

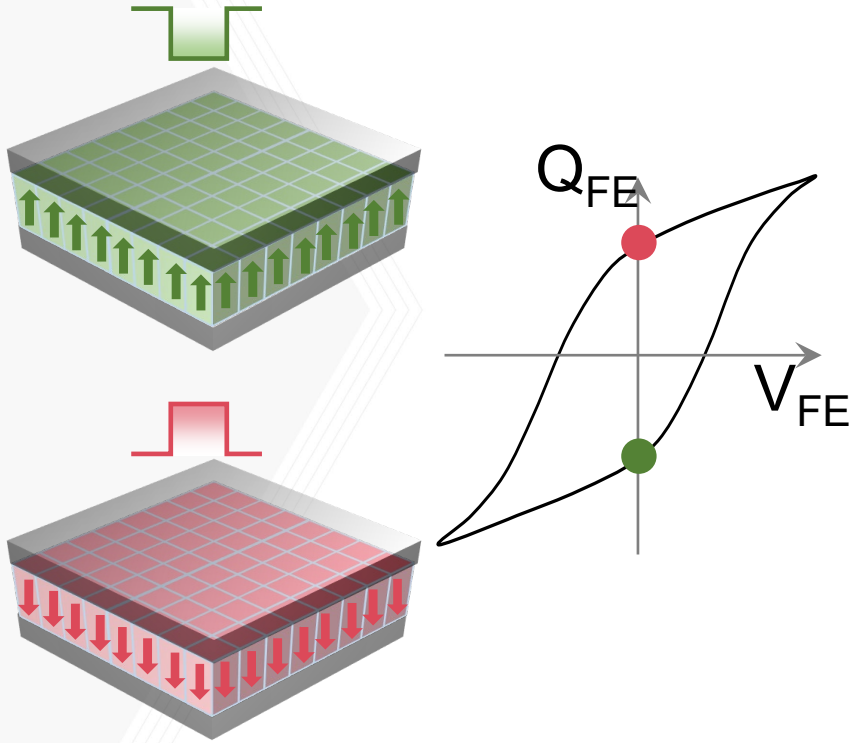


L. V. Hai, et al., IMW 2011

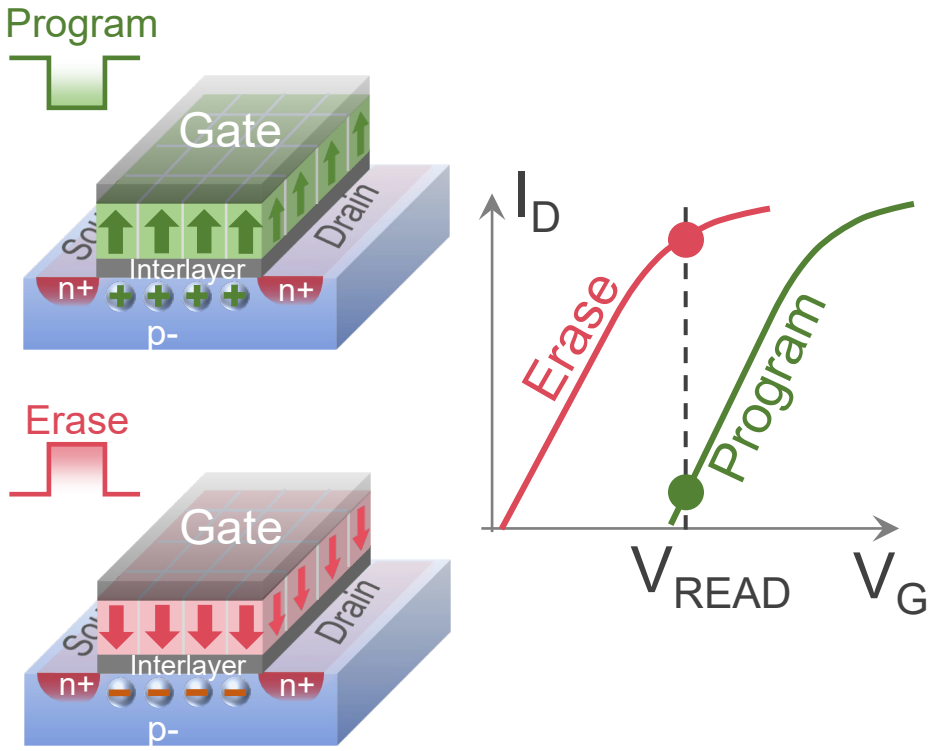
HfO_2 based FeFET is amenable to scaling

Ferroelectric FET

MFM Capacitor

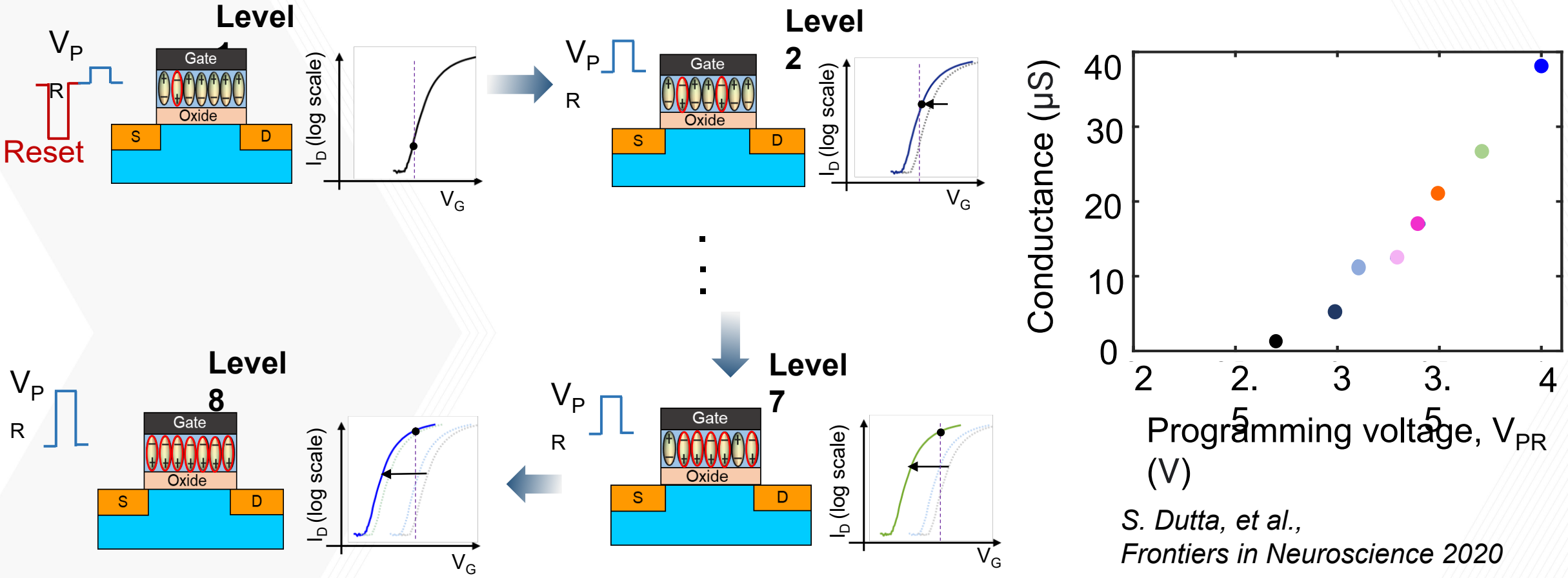


Ferroelectric FET (FeFET)



Polarization states in FeFET can be used to store information.

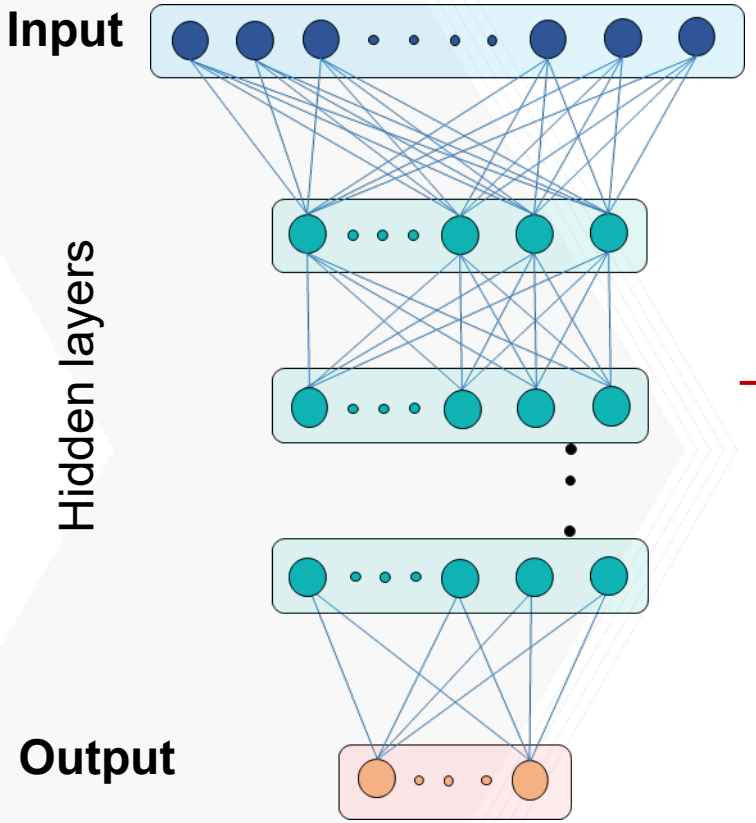
Multi-level FeFET as Computational Memory



S. Dutta, et al.,
Frontiers in Neuroscience 2020

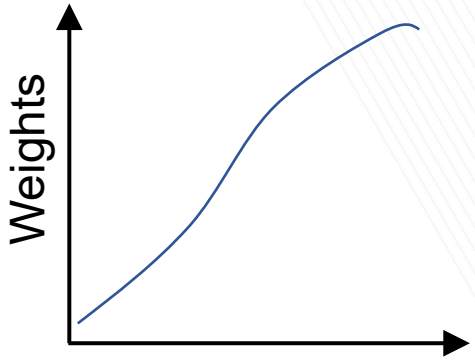
- Partial polarization enables multi level conductance in FerroFET
- Exact requirements of FerroFET as computational memory depend on applications (for example inference vs training)

Precision of Weights & Granularity of Updates



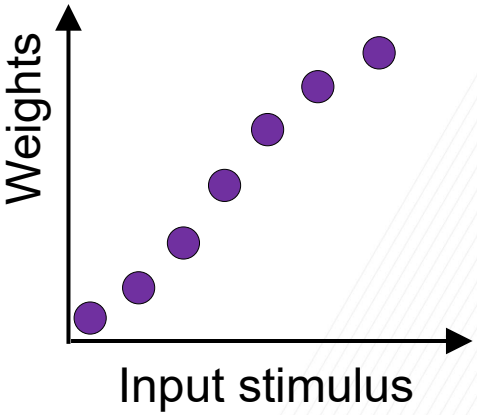
Training

- *Fine granularity in weights*
- *High Write and Read Endurance*
- *Variation tolerance*



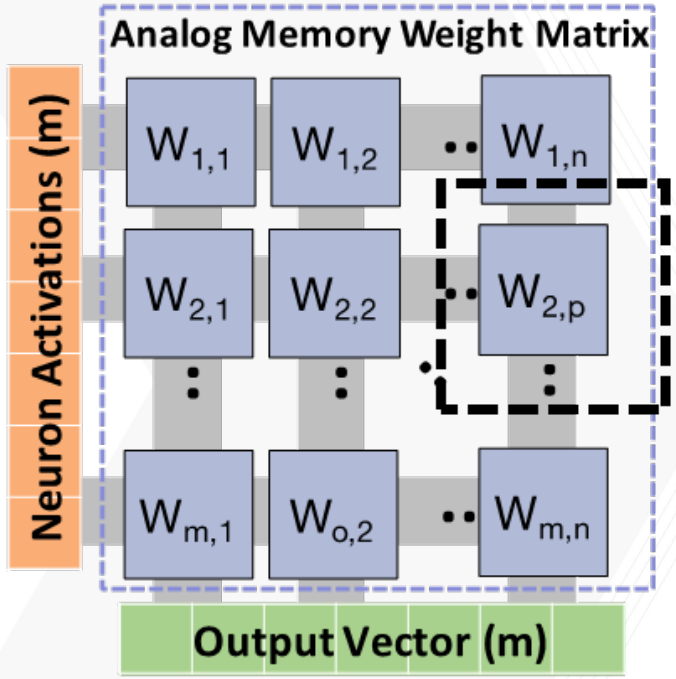
Inference

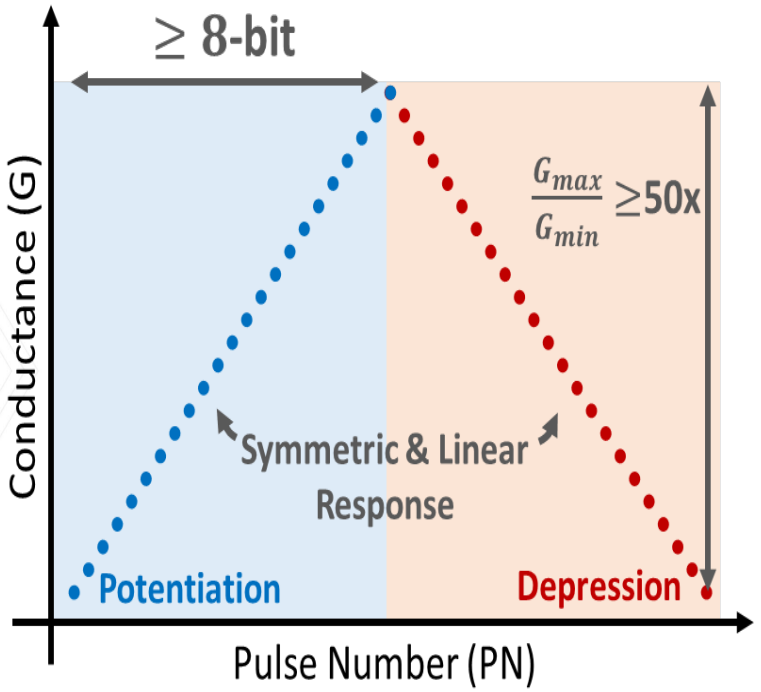
- *Coarse granularity in weights*
- *Precise and few weight transfer*
- *Retention and drift tolerance*



➢ Precision, write latency, endurance requirements more stringent for *in situ* training

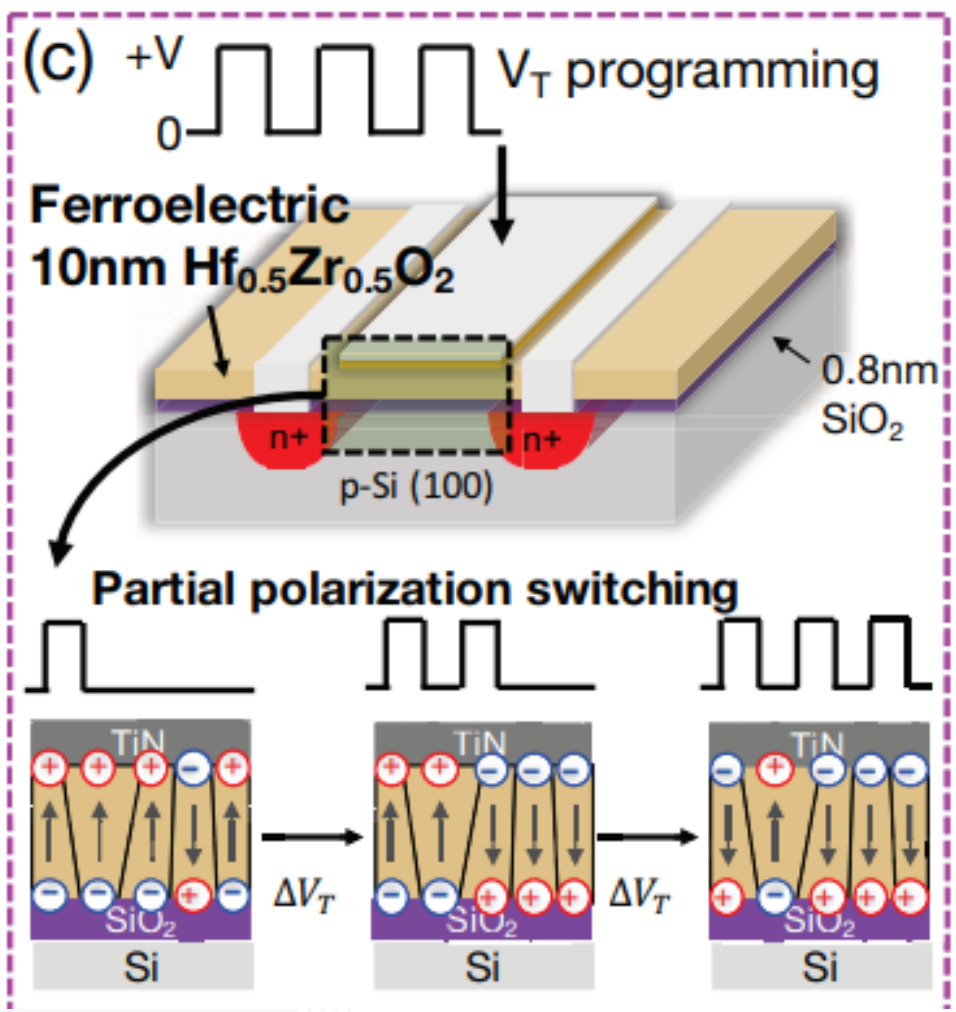
Device Requirement for On-chip Training

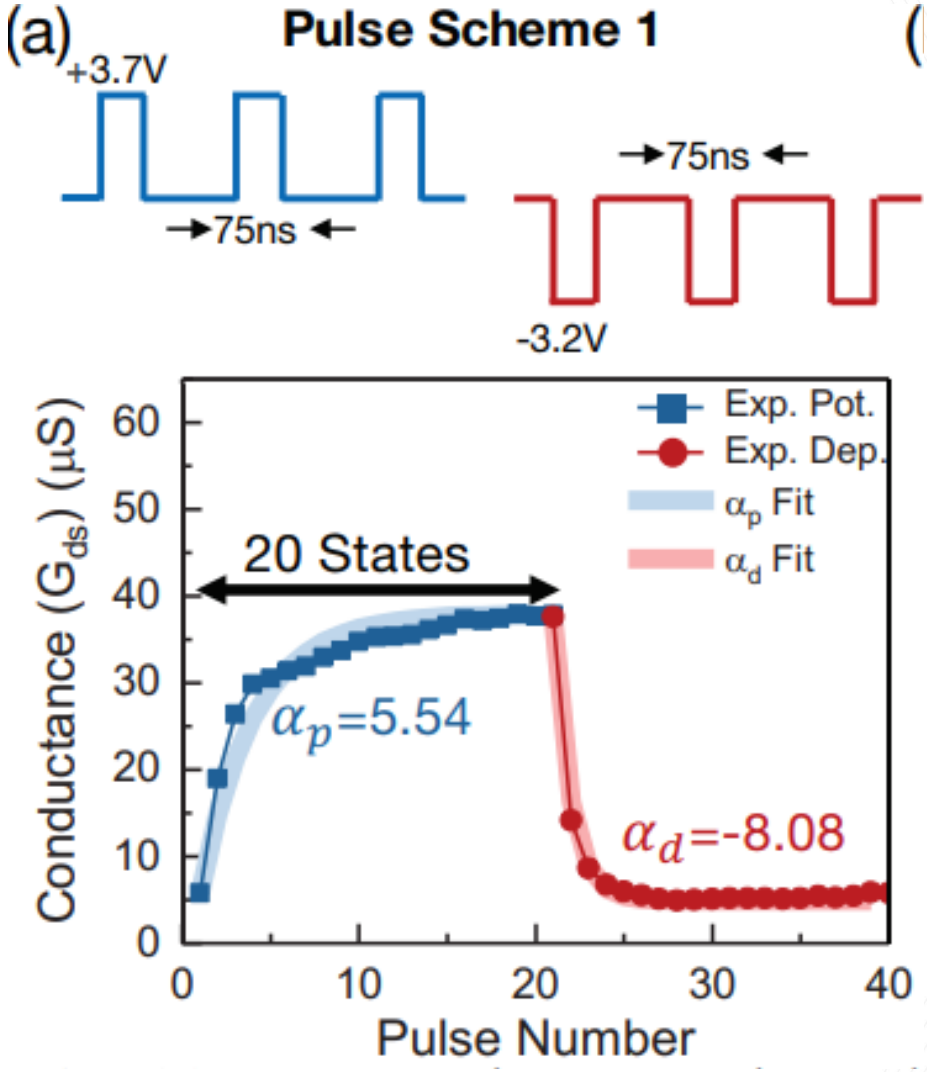




- Linear conductance profile
- High-level of symmetry of potentiation/depression
- High bit precision (>8-bit)
- High dynamic range ($DR=G_{max}/G_{min}>50$)
- High write endurance (>10^{12})
- Identical input pulse (<50ns)
- CMOS compatibility enabling monolithic 3D integration

FeFET not an Analog Synapse





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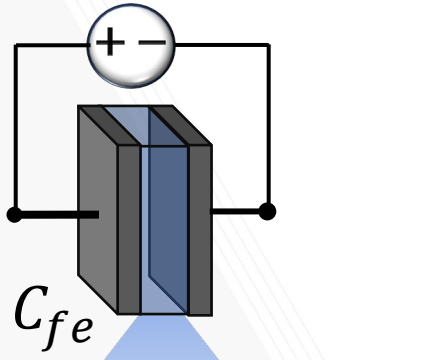
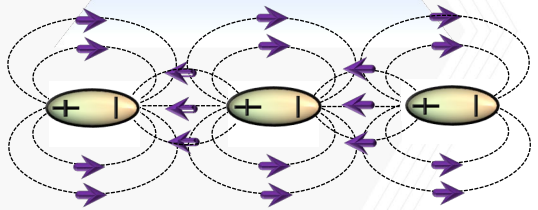
Physics of Stand-alone Ferroelectric Switching

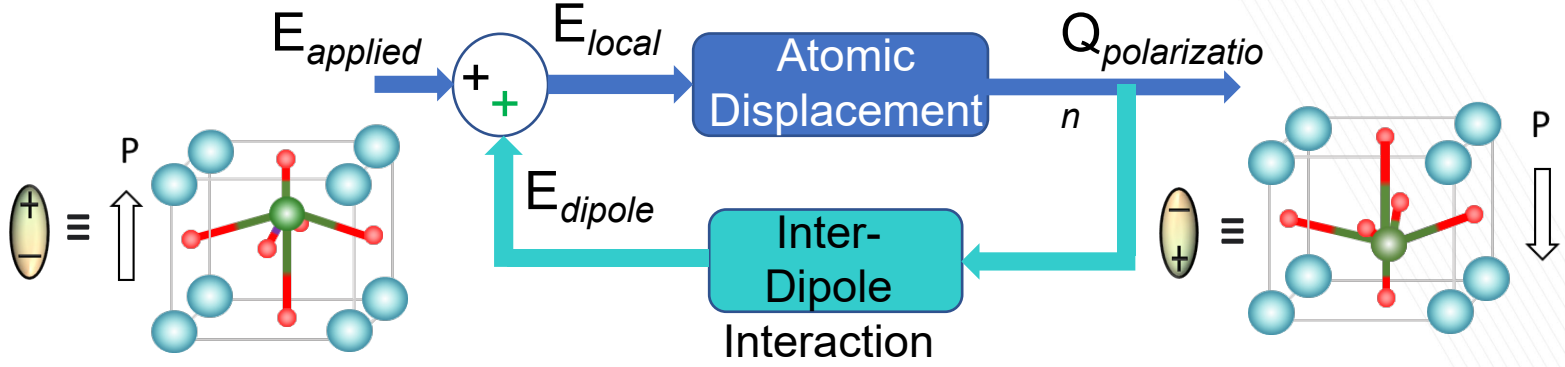


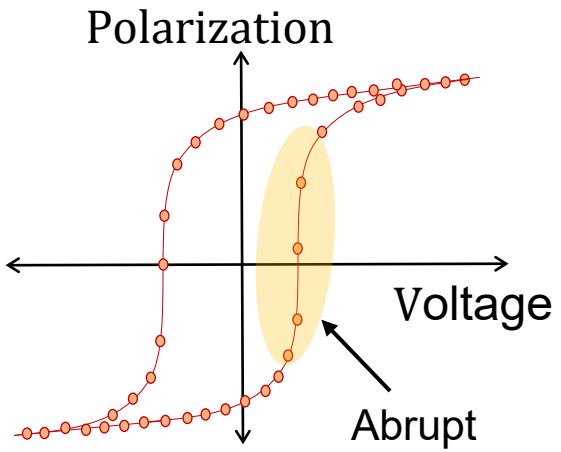


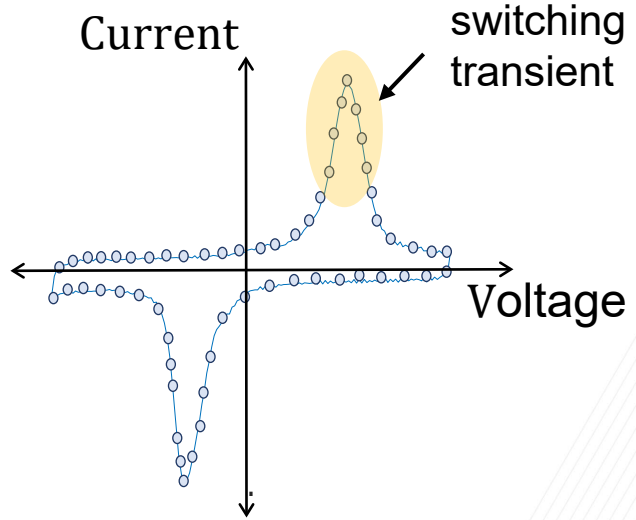
$$E_{local} = E_{FE} + E_{dipole}$$

E_{FE}

E_{dipole}



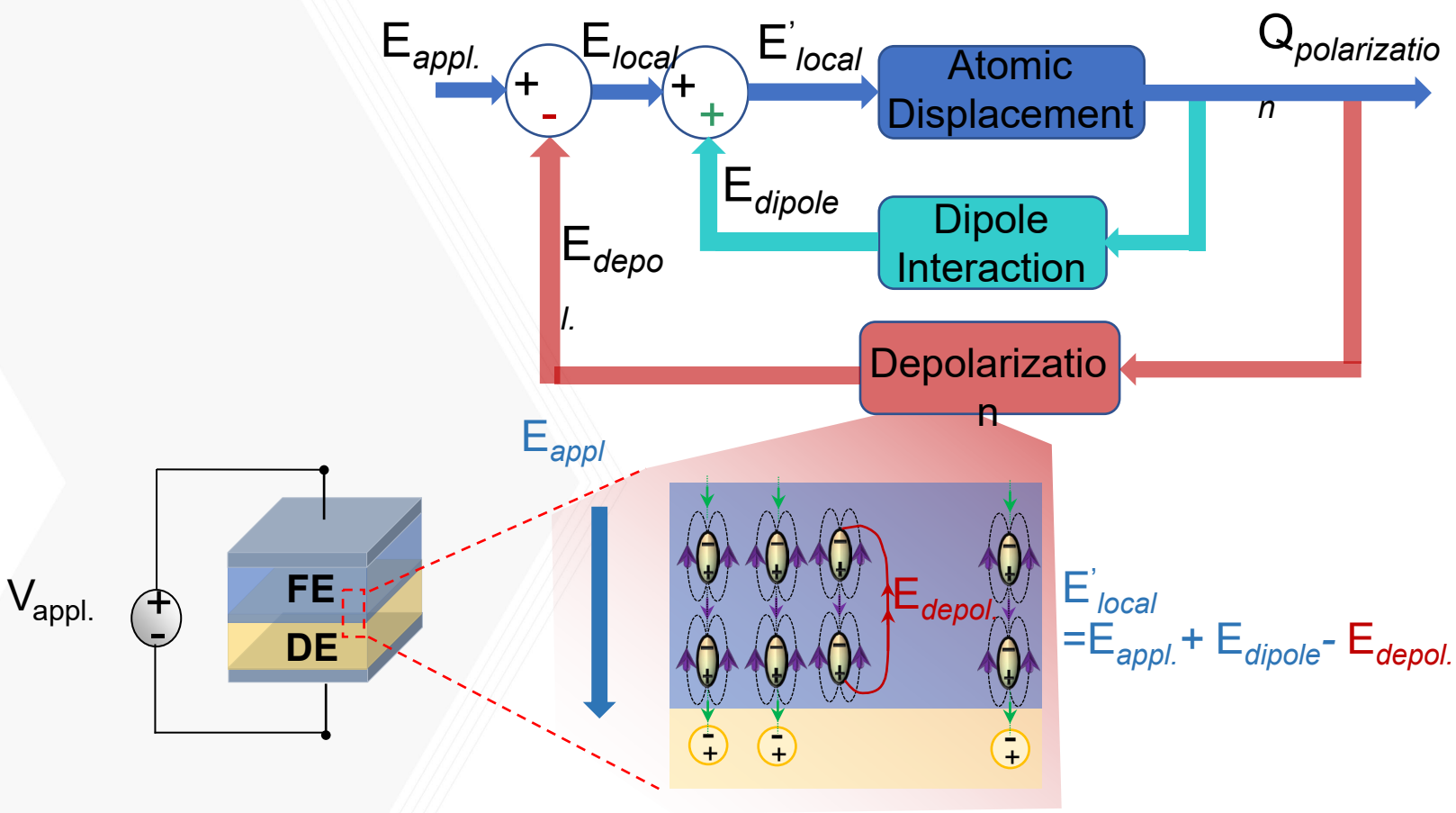


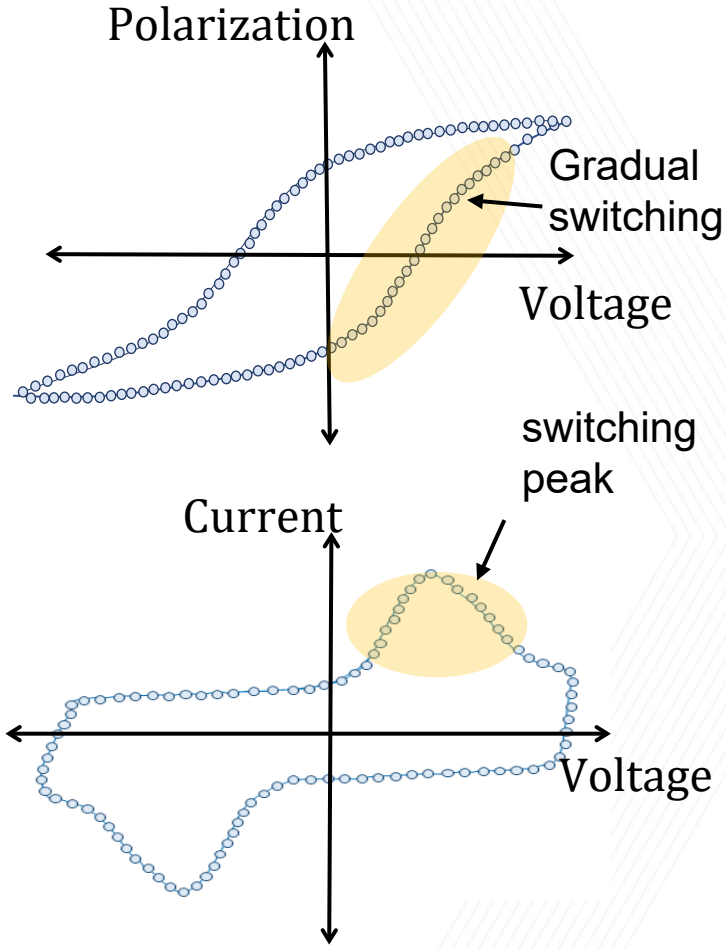


Al. Khan, *IEDM*, 2018
J. Gomez et al., *DRC*, 2019

- Positive feedback due to inter-dipole interaction causes abrupt polarization switching in FE
- Abrupt switching behavior is not favorable for analog weight update operation

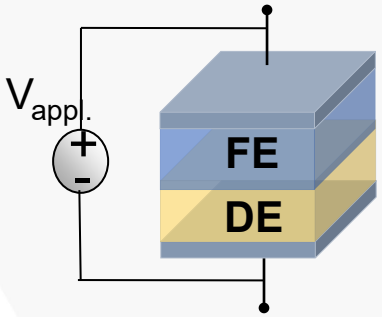
Physics of Ferroelectric-Dielectric Superlattice



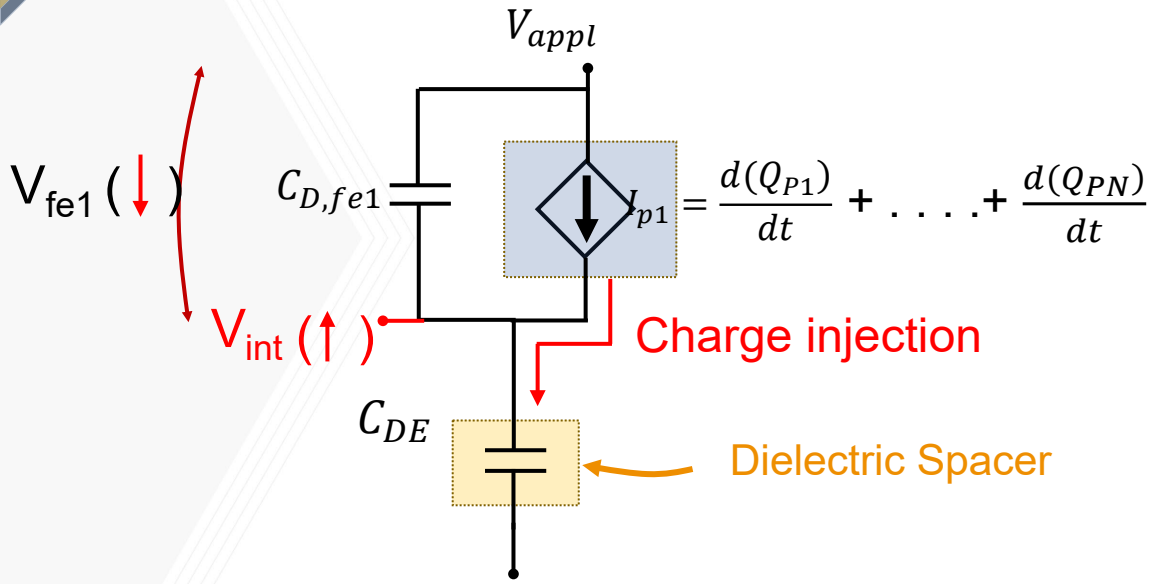


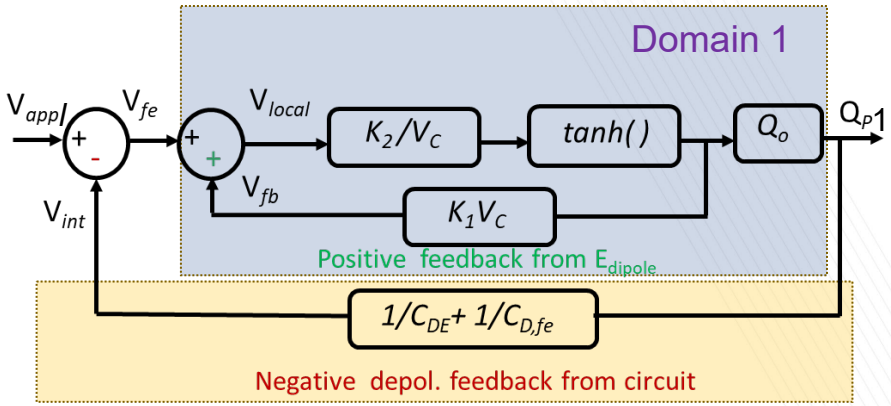
➢ -ve feedback from depolarization field ($E_{depol.}$) tilts the PV loop and prevents abrupt switching

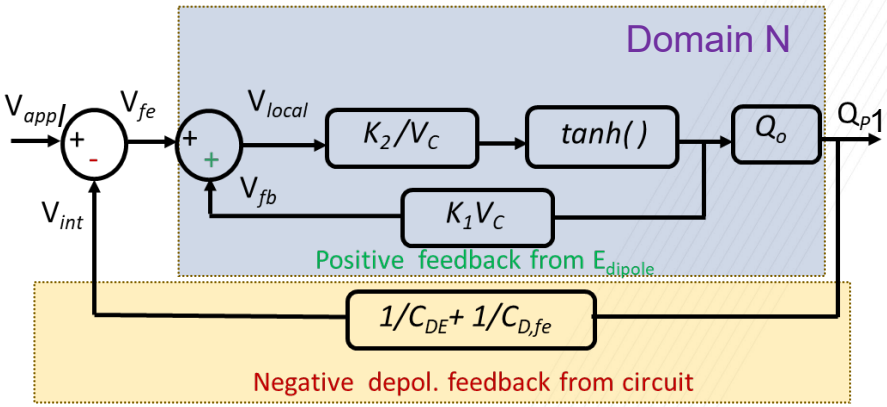
Equivalent Circuit for FE-DE SL Switching



Ferroelectric/Dielectric Capacitor







- Domains require higher E-field to switch due to the –ve feedback from DE spacer

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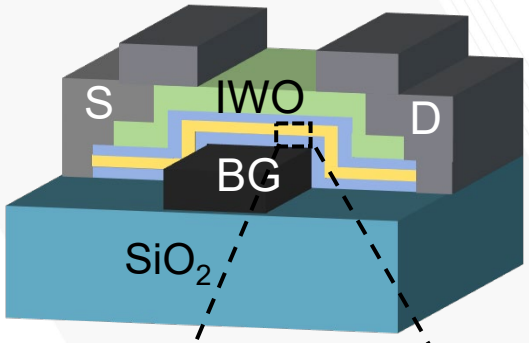
SL FeFET Fabrication

Schematic View of the FEFET Structure



Conv. Gate Stack

(10nm HZO)

10nm(FE)

SL Gate Stack

(6-6-5)

5nm(FE)

5nm(DE)

5nm(FE)

SiO

Tungsten (W)

HZO

Pd

HfO_2

W doped In_2O_3

1. Formation of Patterned Tungsten(W) Back

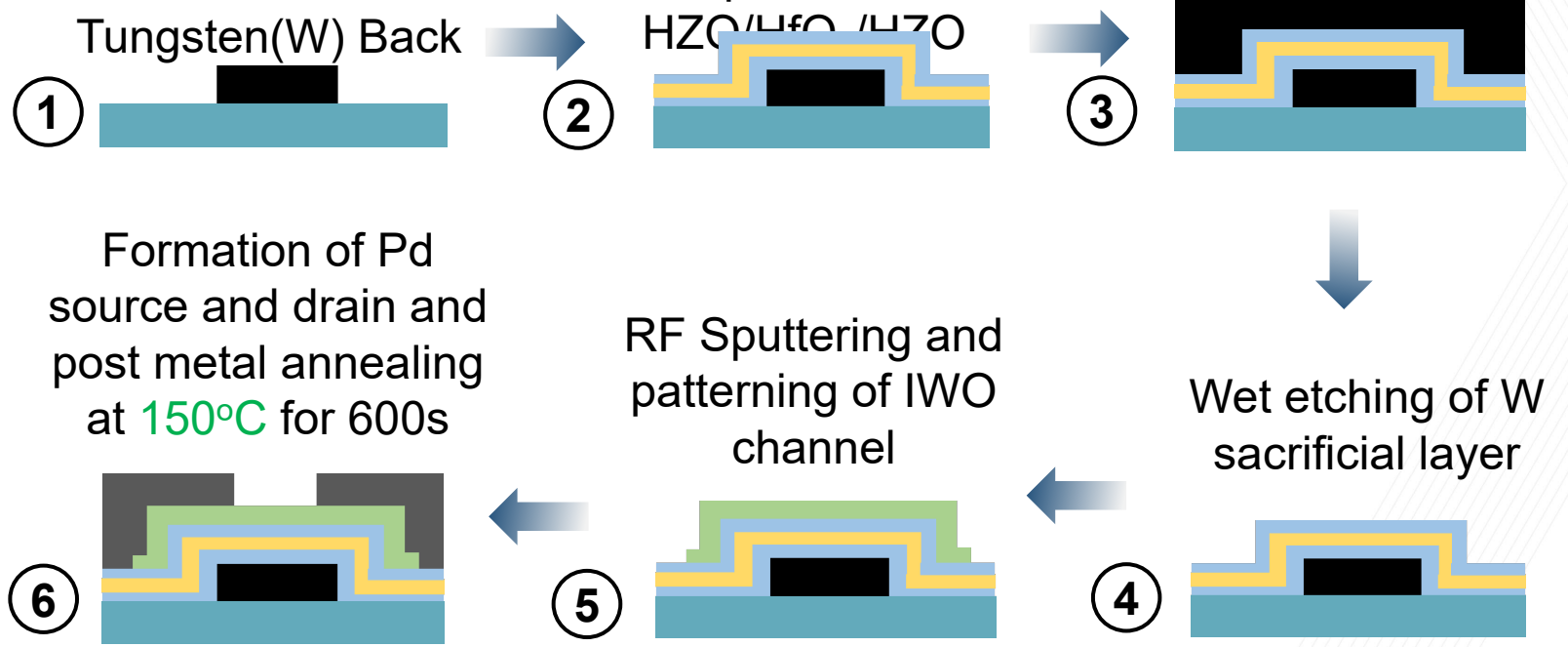
2. Back-to-back Plasma ALD deposition of HZO/HfO_2/HZO

3. Sputtering of W sacrificial layer and RTA at 400°C for 60s in N_2

4. Wet etching of W sacrificial layer

5. RF Sputtering and patterning of IWO channel

6. Formation of Pd source and drain and post metal annealing at 150°C for 600s



- All process steps takes place under back-end-of-line compatible thermal budget (400°C)

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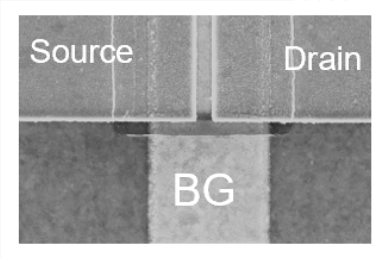
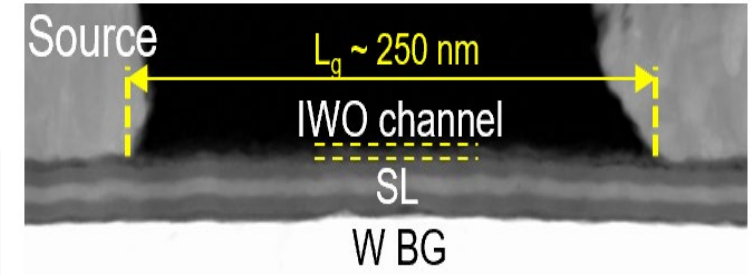
SL FEFET: Fabrication & Characterization

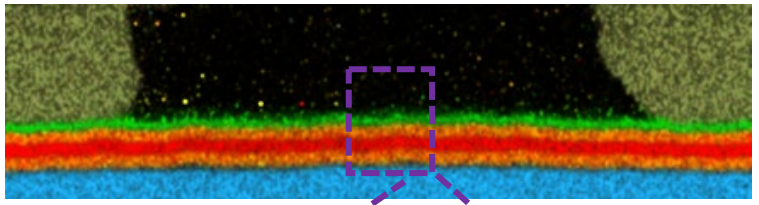
Top view



Cross-sectional TEM

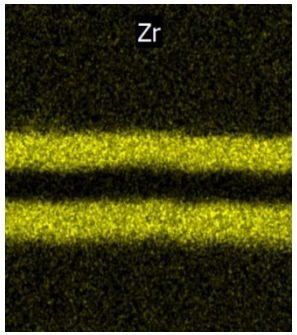


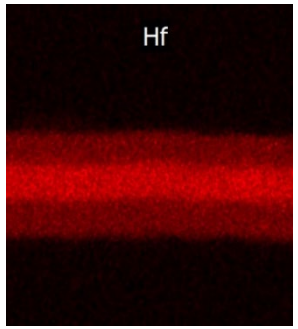
STEM-EDX of SL FEFET



H
In
Z
r
P
Hf/Z
r
W

Highlighted Zr and Hf map





- The SL (FE/DE/FE) gate stack do not intermix after undergoing all process steps of the FEFET

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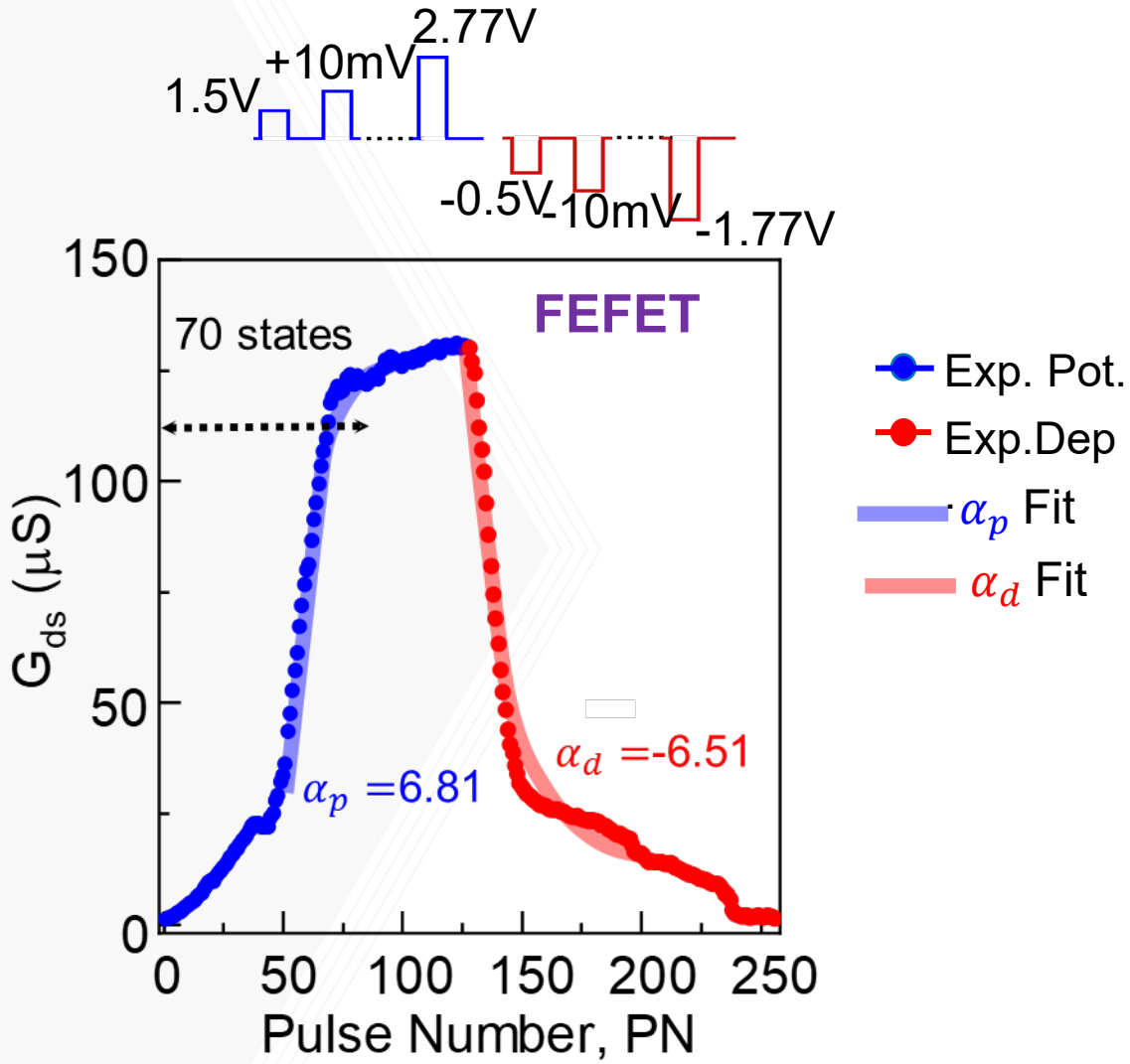
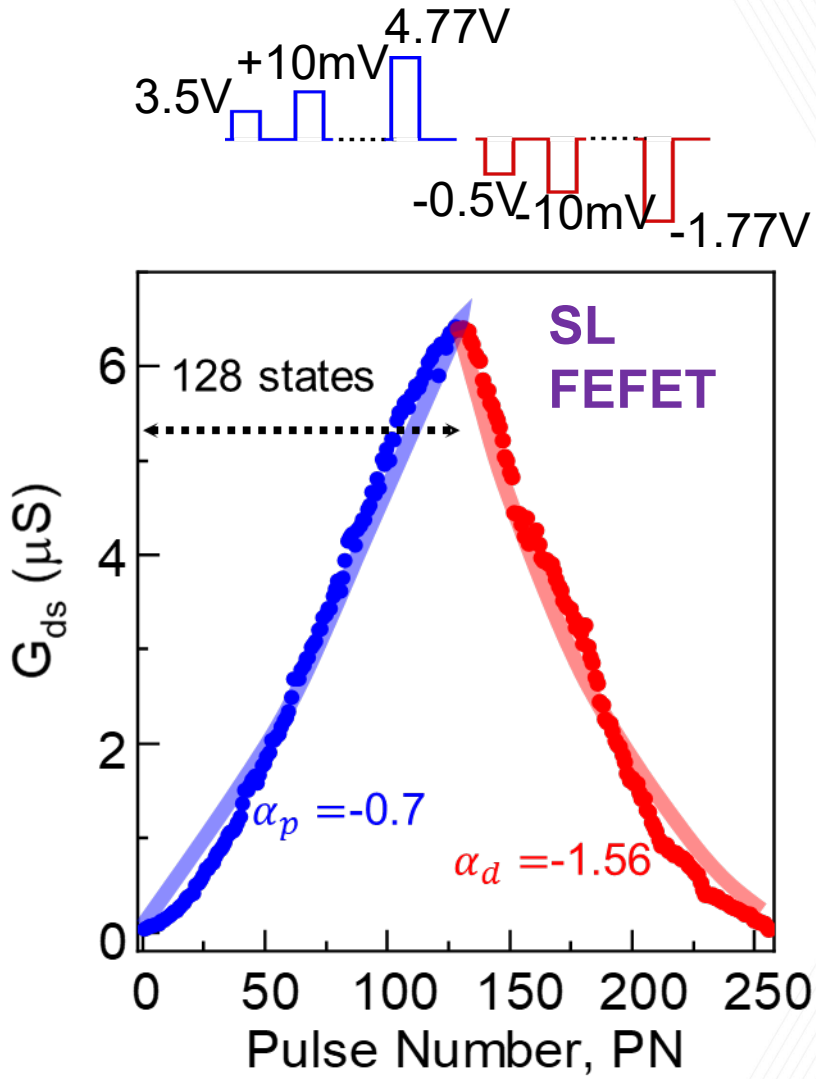
FEFET: Analog Synapse Characteristics

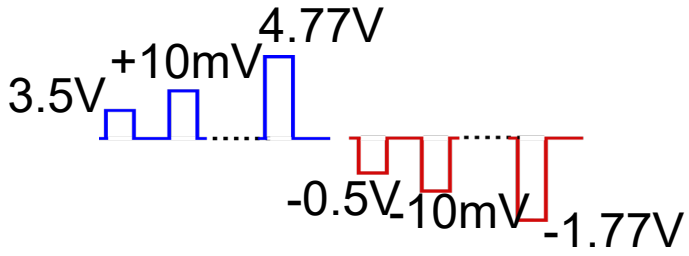


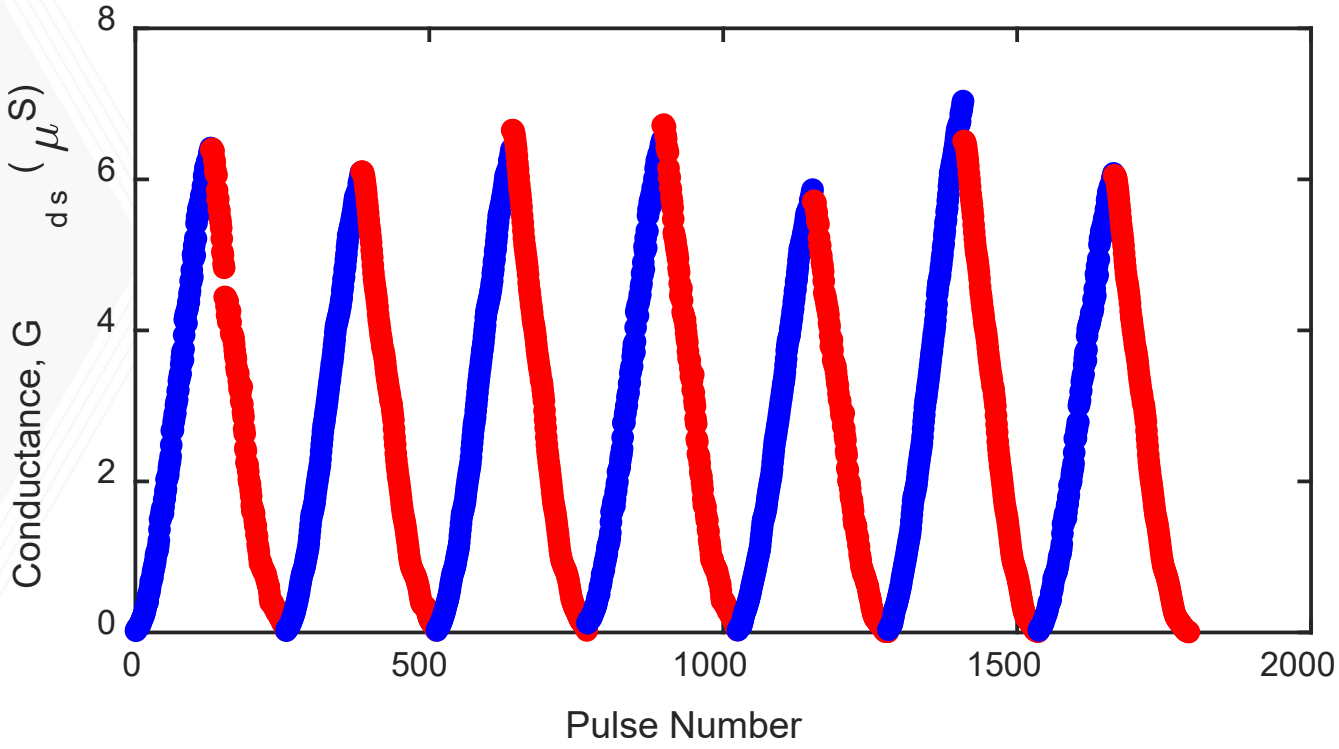


➢The SL FEFET exhibits 128 states with linear and symmetric conductance profile for pot/dep

FEFET: Cycle-to-Cycle Variation

Pulse Scheme:

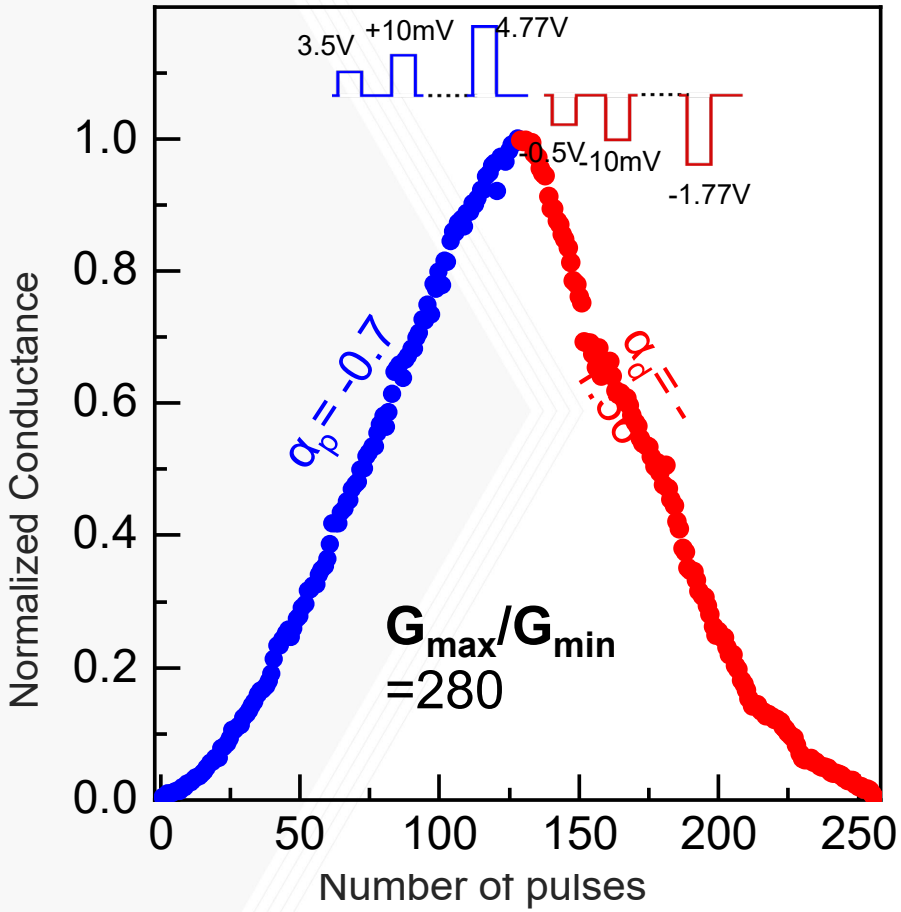




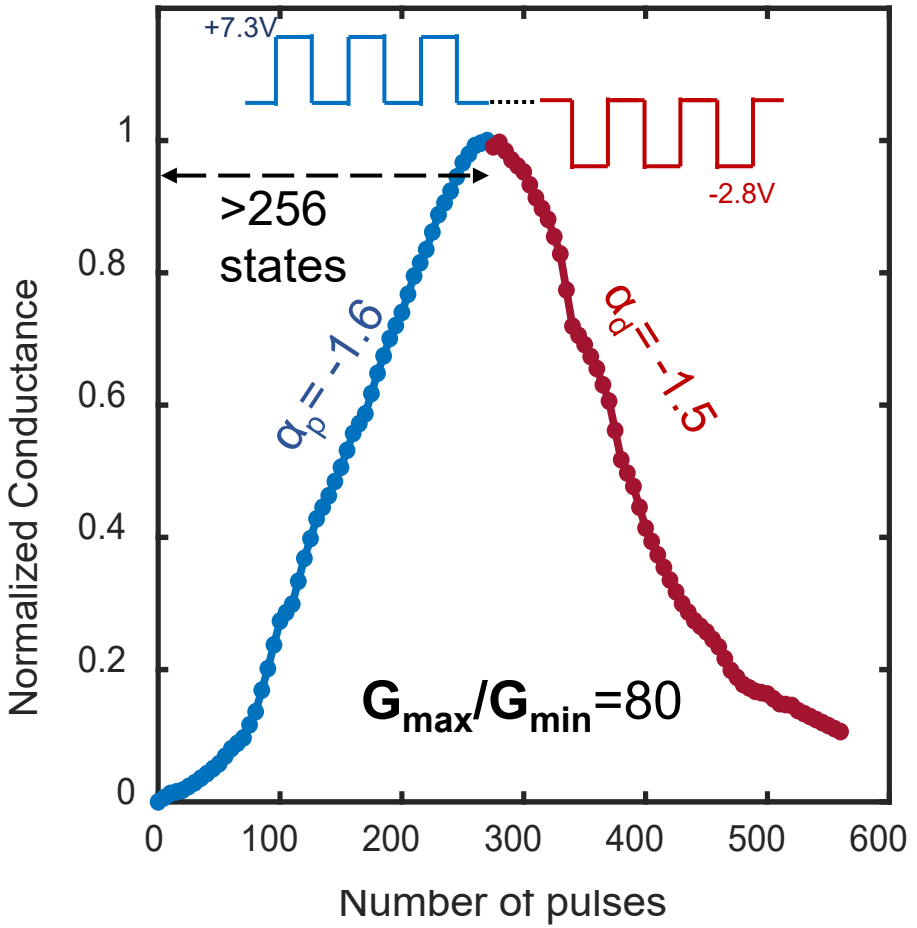
- 7 consecutive cycles show repetitive conductance profiles without serious distortion

FEFET: Identical Pulse Scheme

Non-identical Pulse Scheme



Identical Pulse Scheme



- The SL FEFET shows linear and symmetric conductance profile for both non-identical and identical pulse schemes.

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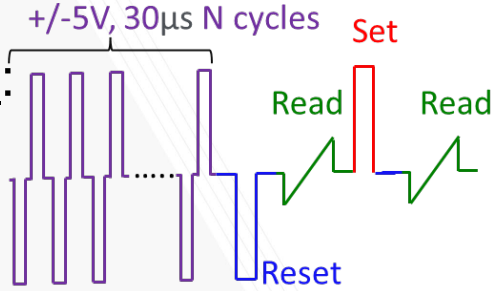
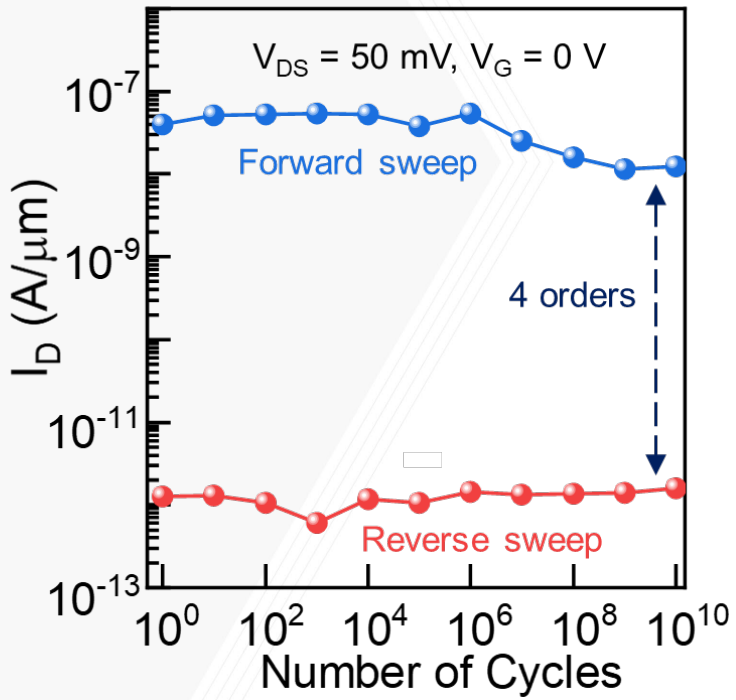
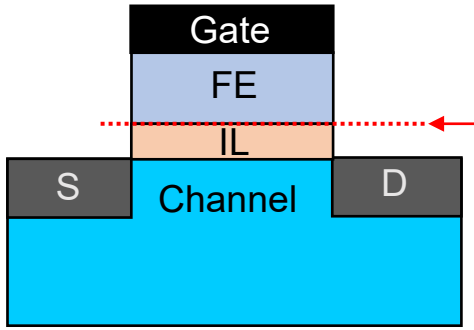
Endurance

Pulse Scheme:



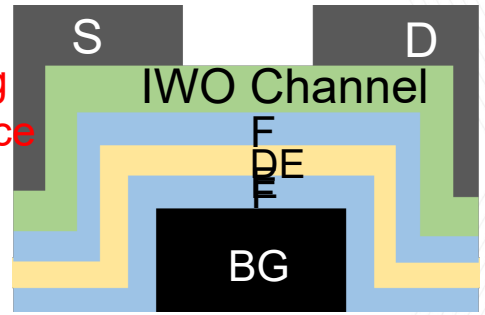


Si-FEFET



Charge trapping @ FE-IL interface

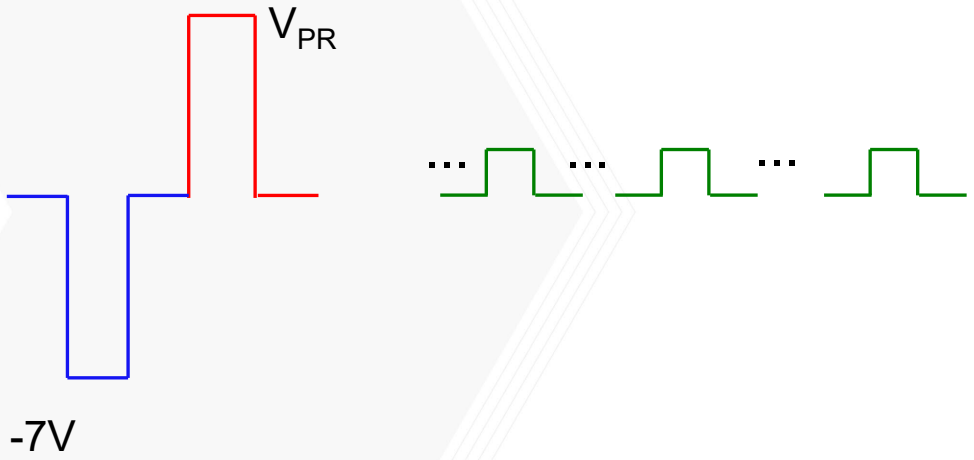
BEOL SL FEFET

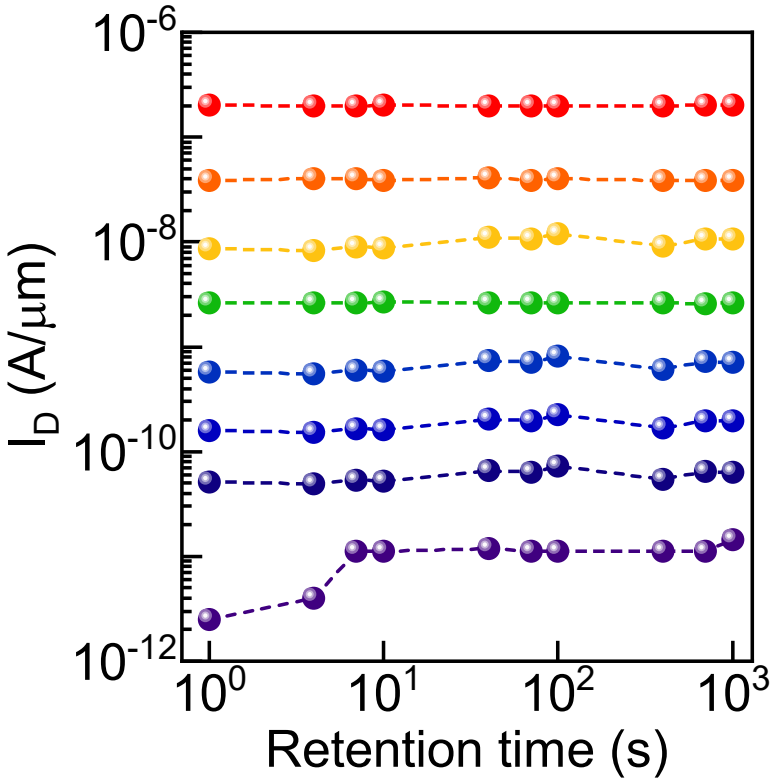


➢High endurance (>10^{10} cycles) of BEOL SL FEFET due to absence of low-k interfacial layer (IL)

Retention

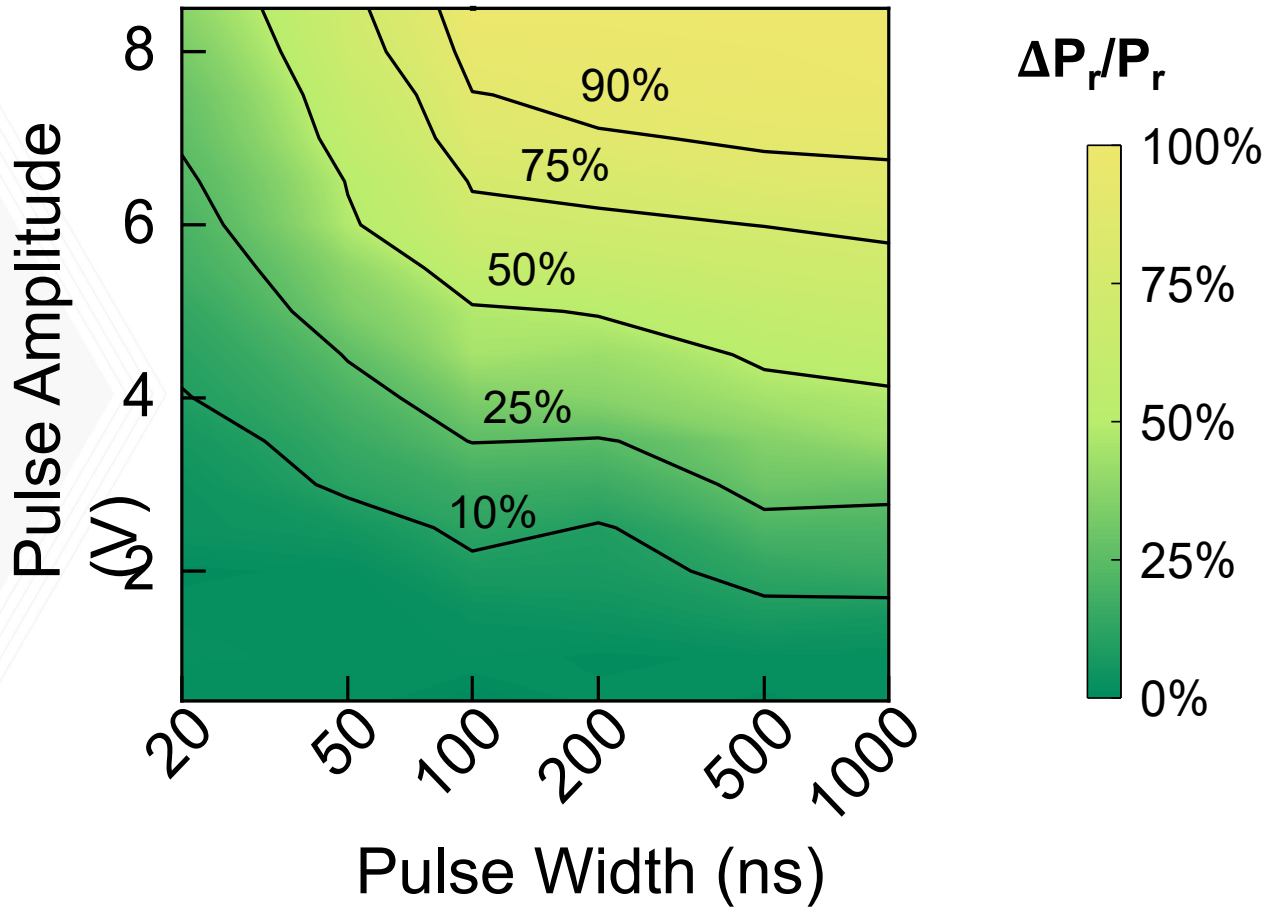
Pulse Scheme:





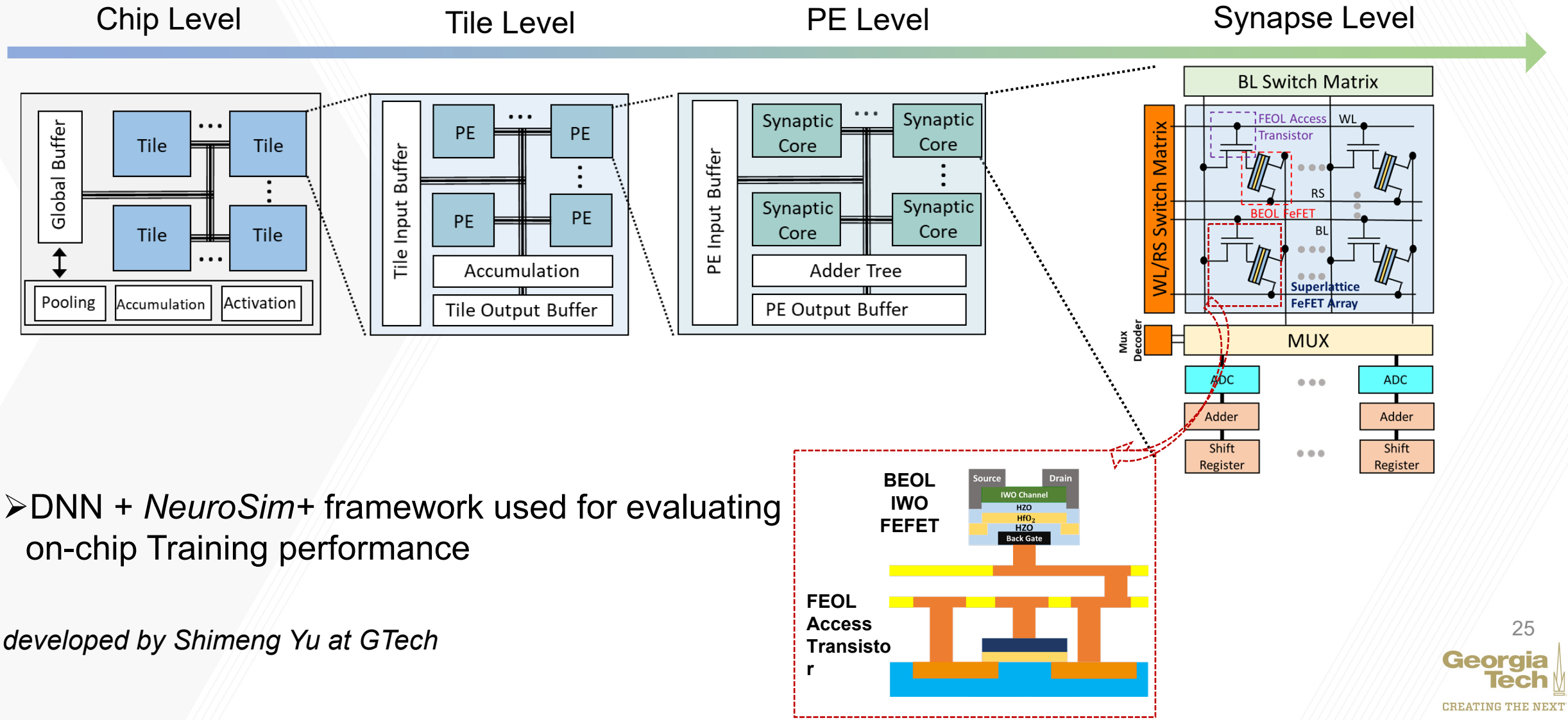
➢Retention >10^3s measured for intermediate states at 25°C

Switching Speed



- The 5/5/5 SL stack shows switching capability at 100ns pulse width.

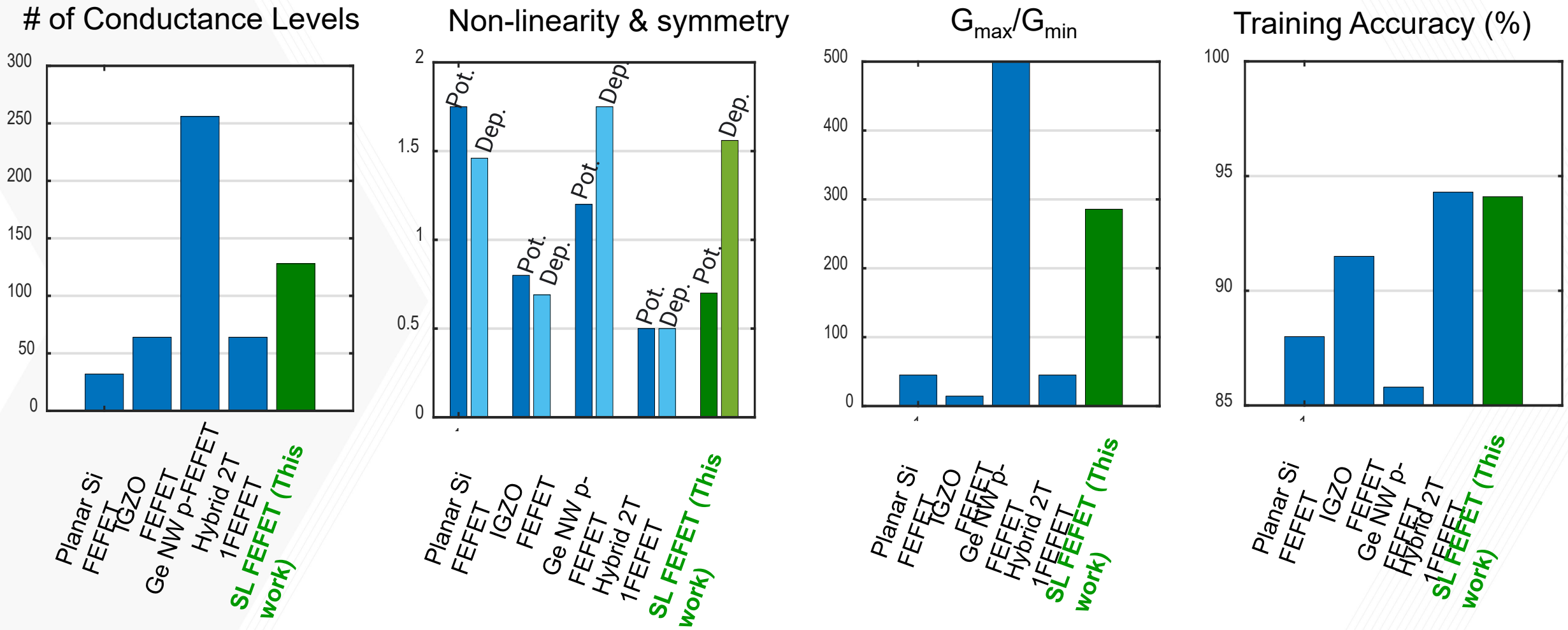
FEFET Analog Weight Cell: Benchmarking



- DNN + *NeuroSim+* framework used for evaluating on-chip Training performance

developed by Shimeng Yu at GTech

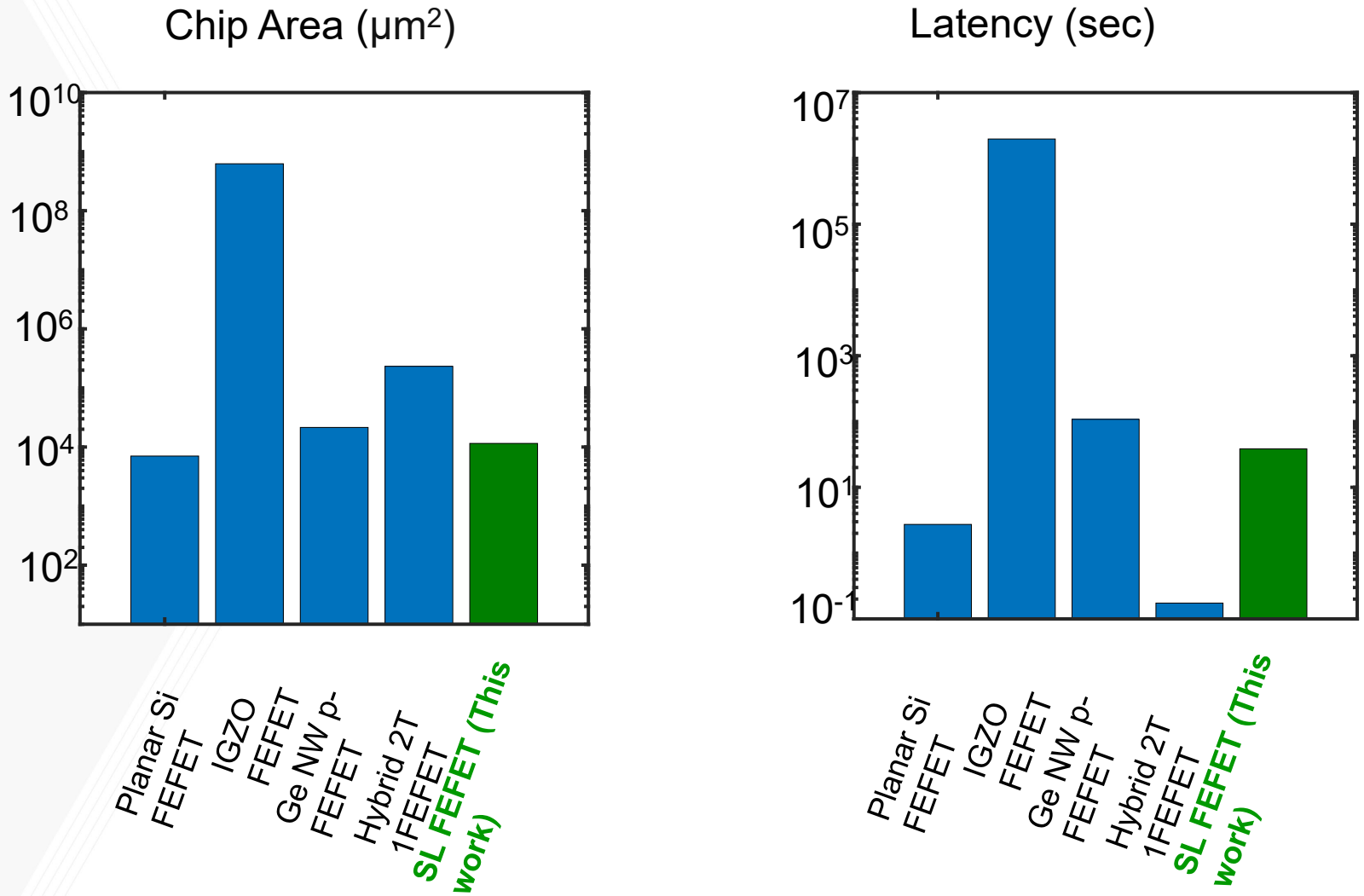
FEFET Analog Synapse: Benchmarking



➢SL FEFET yields a higher number of states, linearity and symmetry leading to 94.1% Training accuracy

Georgia Tech
CREATING THE NEXT

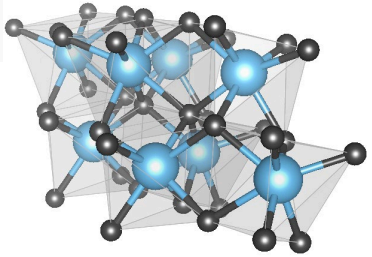
FEFET Analog Synapse: Benchmarking



- SL FEFET maintains a small chip area and latency

Ferroelectronics

Fluorite structure Ferroelectrics (HfO_2 and ZrO_2 based)



Front-end

Back-end

Conventional Logic Transistor (MOSFET)

Ferroelectric Field-Effect Transistor (FEFET)

Ferroelectric-Metal Field-Effect Transistor (FEMFET)

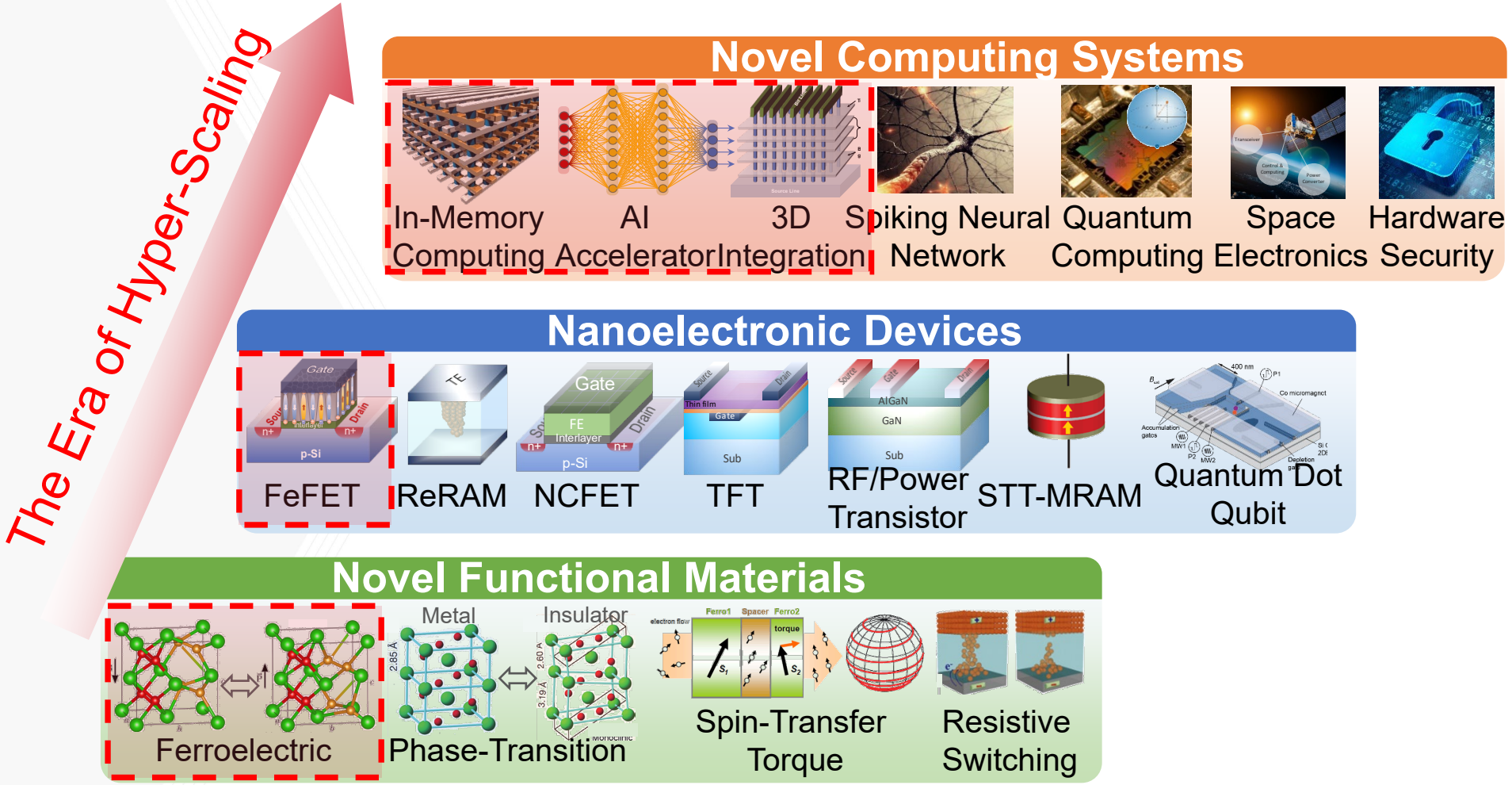
Ferroelectric Random Access Memory (FRAM)

Ferroelectric Field-Effect Transistor (FEFET)

Ferroelectric FET memory for embedded memory (cache) and for in-memory-compute applications

(Datta/Khan) The future of ferroelectric field-effect transistor technology, 2020 Nature Electronics

Materials-Device-System Co-Design



Sayeef Salahuddin, Kai Ni, and Suman Datta, "The era of hyper-scaling in electronics," Nature Electronics, 2018