



Flash Memory Summit

# Teledyne LeCroy: End to End NVMe Debugging

## Presented by:

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Gordon Getty, Teledyne LeCroy



**TELEDYNE LECROY**  
Everywhereyoulook™

# About the Presenters



Gordon Getty

## About

- Technical Marketing Manager – Solutions Marketing
- 20 years experience in PCI and PCI Express testing and Compliance Programs
- Masters in Information Technology from University of Paisley, Scotland
- Bachelor of Engineering In Electronics with Music from University of Glasgow, Scotland



David Obert

## About

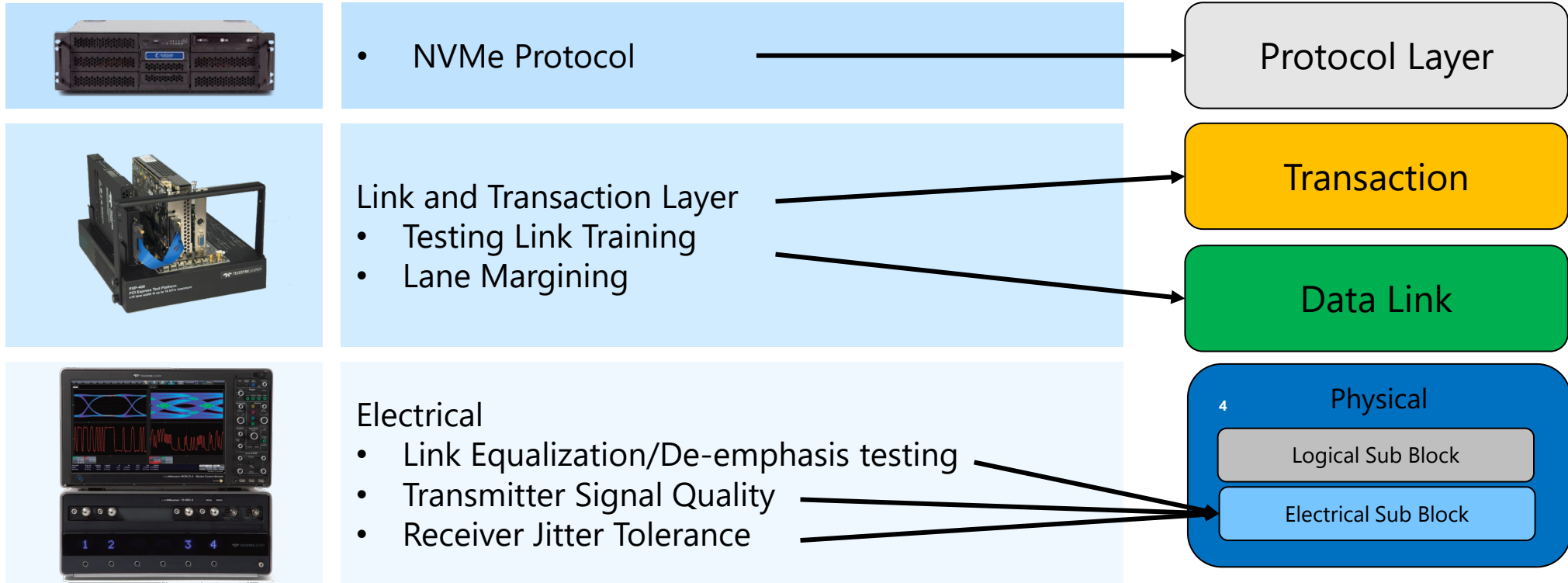
- Sales Development Manager with Teledyne LeCroy, OakGate Products
- Prior to Teledyne LeCroy, 30 years experience as a Marketing Specialist with Hewlett-Packard
- MBA from Drucker School of Management, Claremont Graduate School

# Agenda: End to End NVMe Debugging

- Introduction and Quick Overview of NVMe
- Discussion of trigger types
- Hardware Setup
- Capturing NVMe Initialization on the Protocol Analyzer
- Overview of setting triggers in the Teledyne LeCroy OakGate Test Appliances system
- Overview of setting the trigger actions in the Teledyne LeCroy Summit series Protocol Analyzer
- Summary
- **Questions**

# Objective

How do I find the root cause of unclear or intermittent problems when running NVMe Validation tests where the problems might be at any layer of the protocol stack?



# Quick Basics

## Introduction and Overview

# Validating and Debugging NVMe Devices

- NVMe is now the standard protocol used for SSDs both in server and client platforms
- NVMe takes advantage of established transport and data link layers
- Thorough validation of devices helps to avoid post-release corner case issues
- Problems can show up as:
  - Drive failures
  - Performance problems
  - System crashes



# Background: What is NVMe?

- A family of specifications that define how host software communicates with non-volatile memory across multiple transports like PCI Express® (PCIe®)
- An industry standard specification was designed from the ground up for SSDs
- A much more efficient interface, providing lower latency, and is more scalable for SSDs than legacy interfaces
- The NVMe architecture brings a new high performance queuing mechanism that supports 65,535 I/O queues each with 65,535 commands
- The NVMe interface significantly reduces the number of memory-mapped input/output commands and accommodates operating system device drivers running in interrupt or polling modes for higher performance and lower latency
- The NVMe specification also contains host-to-device protocol for SSD commands used by an operating system for: read, write, flush, TRIM, firmware management, temperature, errors and others
- The NVMe Specifications are managed by NVM Express® consortium



# Types of Validation Tools

- **Test Appliances**
  - Host based emulation tool that allows the tester to generate a range of scripts with defined IO traffic patterns, admin commands and error injection
  - Allows Validation with complex traffic flows
- **Protocol Analyzers and Exercisers**
  - Provide insight into all activity on the link from the Logical PHY Layer up to the higher protocol layers including NVMe.
  - With analyzer and exerciser capabilities an ideal early development and debug tool in addition to providing conformance test capabilities
- **Combining these Tools**
  - Allows you to apply this system level intelligence and error recognition seen in host-based tools with the deep packet capture and granular detail on all levels of protocol analyzers



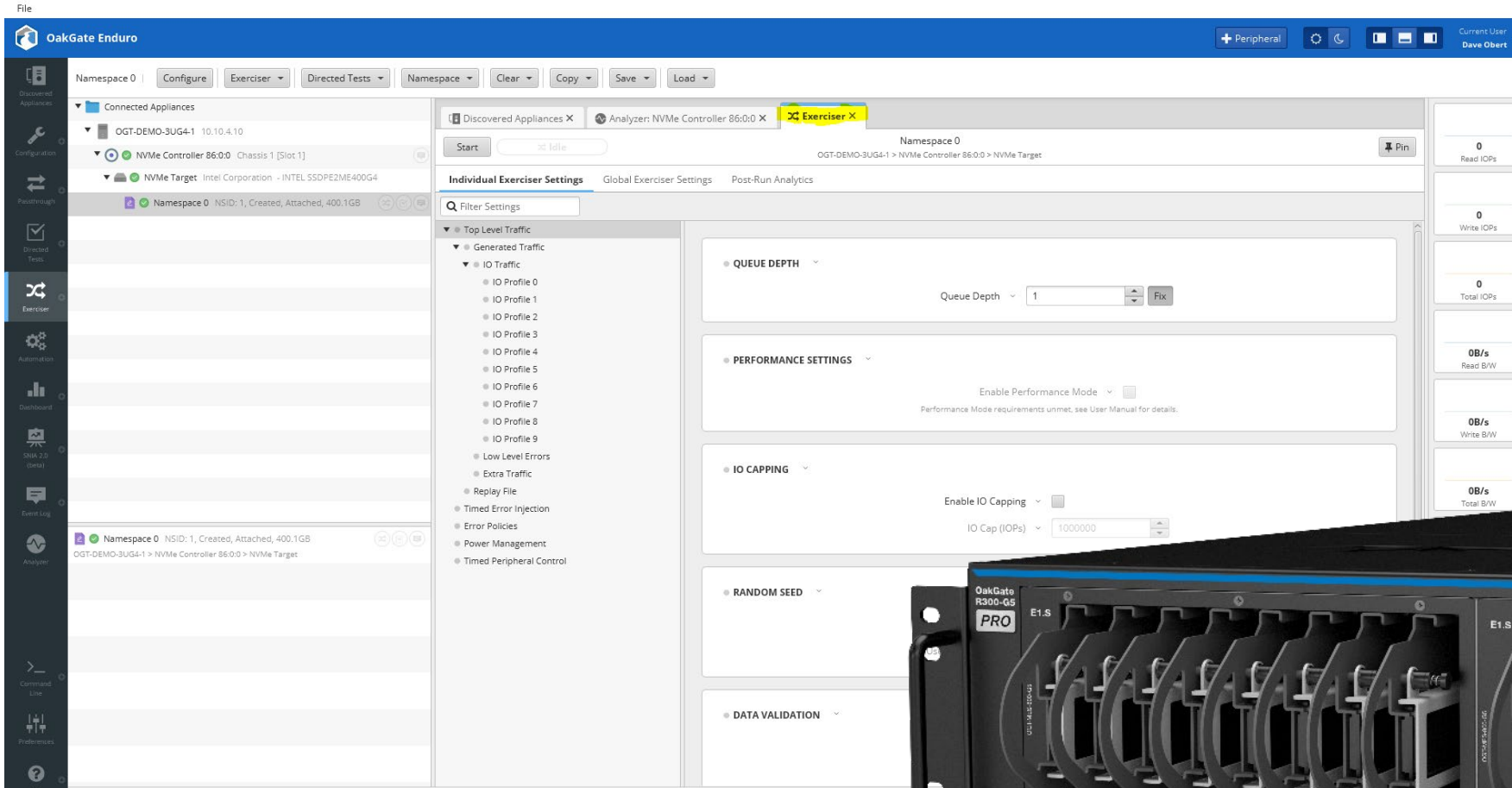
# Trigger Types

- **What is a trigger?** A trigger is any defined event that causes the Protocol Analyzer to stop overwriting any buffer information. On the OakGate system a trigger is a response to an error event
- **What is the challenge?** If I don't know exactly what problem I am trying to find defining the protocol analyzer trigger can be very challenging
- **Why do I care?** The more general OakGate triggers allows me to capture the areas of interest on the Protocol Analyzer to verify exactly what is happening in the problematic and surrounding transactions
- **Other Trigger Uses?** Yes, the trigger can also be used to place a marker in the analyzer trace and drive logs that can be used as a search key

- Have the test software mark the drive as having a fatal error so that NVMe traffic will cease and then the recording will stop
- Have the Protocol Analyzer trigger on the error event itself provided that the error pattern is well known and defined and can be configured as an analyzer trigger event
- Create a trigger event within the OakGate Appliance test software upon the introduction of the error and configure the Protocol Analyzer to trigger on the event

# Hardware Setup

# What is the OakGate Test Appliance?



Gen5 Appliance  
with Drive Bays

Enduro Client Interface



# What is a Teledyne LeCroy Protocol Analyzer?

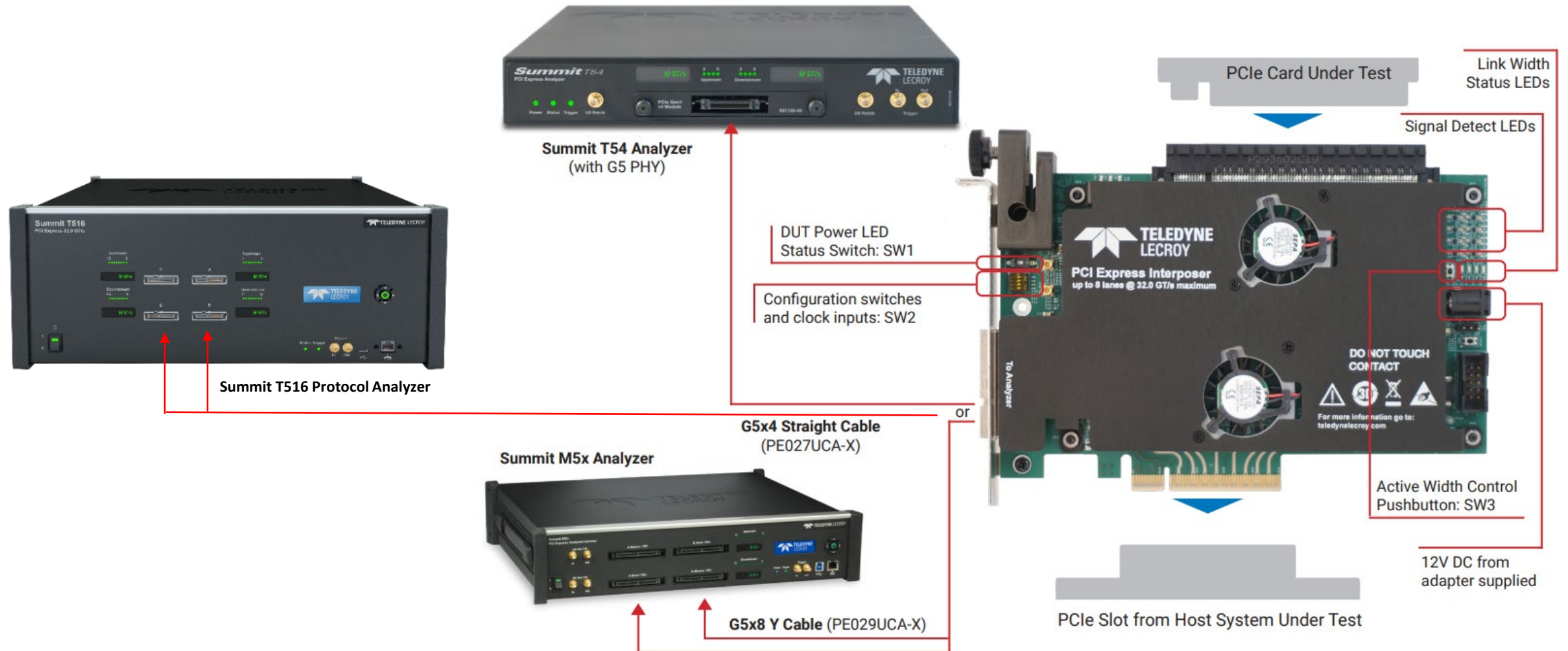
Teledyne LeCroy PCIe Protocol Analysis - BETA - [C:\Users\Public\Documents\LeCroy\PCIe Protocol Suite\Sample Files\NVMe\_Z4DriveEmulation.pxi]

FileSetupRecordGenerateReportSearchViewToolsWindowHelp

<



# Protocol Analyzers Use Interposers for Probing





# Insert the U.2 Interposer into the U.2 Slot

- Insert SSD into Interposer
- Insert Interposer and SSD into Oakgate Test Appliance





# Process Flow Summary

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## Connect Hardware

1. Connect Protocol analyzer interposer into OakGate Test Appliance

## Capture NVMe Decode

1. Configure Host Memory and NVMe Controllers (DUTs) in the Oakgate software
2. Power on Protocol Analyzer and configure to capture controller/queue initialization
3. Initialize Host Memory and NVMe Controllers within OakGate software

## Set-up Triggers

1. Set up OakGate Events
2. Set up Protocol Analyzer Triggers and arm

## Run Test and Capture Debug information

# Capturing NVMe Initialization on the Protocol Analyzer

# Capturing NVMe Decode Information

Discovered Appliances X Exerciser X Configuration X **Analyzer: NVMe Controller 86:0:0 X**

**NVMe Controller 86:0:0**  
OGT-DEMO-3UG4-1

1 MB 0% 127 MB

Not Capturing Cancel

Columns

Index	Time	Direction	Type	Decoded Frame	Sector Size	LBA	IO Length	IO Profile	...
0	1.242760 s		Event	Setting PCI register 0x100106, Memory Enabled, Bus Master En...					
1	1.242785 s		Event	Waited 0 msec for CSTS.RDY to be processed for CC.EN = 0					
2	1.242807 s		Event	LINK DOWN					
3	1.242835 s		Event	Verified all previous resets are complete. CSTS.RDY = 0					
4	1.242864 s		Event	Configuring the admin queue to 64 entries.					
5	1.242890 s		Event	Enabling the controller. Setting CC.EN to 1, CSS to 0					
6	3.111643 s		Event	Waited 1868 msec for CSTS.RDY to be processed for CC.EN = 1					
7	3.111668 s		Event	LINK UP					
8	3.111833 s		Event	Identifying Controller.					
9	3.111835 s	To TGT ▶	Command	Identify					
10	3.121943 s	◀ To INI	Data						

- The Protocol Analyzer needs to capture all the decode information seen here in the Events View

# Setting up the Protocol Analyzer

- Since the address assignment in NVMe is dynamic – i.e. it may vary from boot to boot, it is necessary to capture the locations of the queues that the system sets up
- This is straightforward and can be done using a simple trigger on the protocol analyzer to capture all the initialization information
- This information will be used when the test is run to allow the protocol analyzer to trigger on the correct NVMe command

# Set up the Protocol Analyzer Trigger

- The Protocol Analyzer can be triggered by:
  - A pattern on the bus/link
  - An external event – such as a trigger input line pulse
- These are both set up using the Recording Options Dialog
- NVMe Triggers can be set as patterns
  - These may require some additional information
  - The information can be extracted from the Oakgate Software
  - NVMe triggers on the Protocol Analyzer are PCIe triggers with defined addresses and payload
  - Recording the system boot or initialization will also allow the Protocol Analyzer to capture this information
  - The trigger could be based on an error event indicated by the Oakgate system

# Protocol Analyzer Recording Options

Choose Event Trigger



Recording Options

General | Recording Rules | Analyzer and Probe Settings

Recording Type  
Analyzer: Summit T54  
U.2/U.3 Interposer Mode: Not Applicable  
☐ Snapshot  
☒ Manual Trigger  
☒ Event Trigger

PCIe Specification  
Revision 5.0

Options Mode  
Simple  
Advanced  
Script

Recording Mode  
☒ Protocol Recording  
☐ SMBus Recording  
☐ CCIX Recording  
☐ BitTracer Recording  
☐ NVMe Enhanced Mode

Buffer Size  
32 MB of 32 GB / direction

Trigger Position  
50 % post-triggering

☐ Upload Size (Around Trigger)  
256,000 MB

Misc  
☐ Beep When Trigger Occurs  
☐ Disable Auto Channel Swap  
☒ Preserve TC to VC mapping across the recordings  
Default TC to VC mapping...

Trace Filename & Path  
C:\Users\Public\Documents\...\data.pex  
Additional Trace File Settings...

Options Name  
Default

Link  
Speed: Auto  
Link Width: Auto (x4 Maximum)

Upstream  
☐ Inhibit Channel  
☐ Enable Precoding  
Invert Polarity  
0 1 2 3 4 5 6 7  
8 9 10 11 12 13 14 15

Reference Clock  
Internal - No SSC

Equalization Mode  
Gen3 LPM Gen4 DFE Gen5 DFE

Downstream  
☐ Inhibit Channel  
☐ Enable Precoding  
Invert Polarity  
0 1 2 3 4 5 6 7  
8 9 10 11 12 13 14 15

Reference Clock  
Internal - No SSC

Equalization Mode  
Gen3 LPM Gen4 DFE Gen5 DFE

☐ Set Reference Clocks independently  
☐ Disable Descrambling  
☒ Auto-Configure Lane Polarity  
☐ Ignore Idle Errors  
☐ Decode OBFF [Swizzling Config...](#)

Save... Save as Default Load... Load Default Restore Factory Settings OK Cancel

# PCIe SSD Base Address Mapping

PCIe SSD Configuration

Property	Value
CHANNELS_SWAPPED	0
Device	
DEVICEID	001:00:0
DEVICENAME	NVMeLeCroy000000
MSIX_TABLE_BIR	0
MSIX_TABLE_SIZE	32
MSIX_TABLE_OFFSET	0x2000
CONTROLLER_ID	0x0
MBAR	0xF7C00000
BAR2	0x00000000
BAR3	0x00000000
BAR4	0x00000000
BAR5	0x00000000
BAR2 Size	0x00000000
BAR3 Size	0x00000000
BAR4 Size	0x00000000
BAR5 Size	0x00000000
PROTOCOL	NVME
VERSION	1.0
ZONED_NAMESPACES_S...	False
ASQS	255
ACQS	255
DSTRD ( Bytes )	4
MPS	4096
IOCQES	4
IOSQES	6
MQES	65535
NVSCC	0

XML Schema File Path

Import Config Info

Export Config Info

Device

Add Delete

Queue

Add Delete

Namespace

Add Delete

Add Shared NS

Interrupt vector

Add Delete

Transaction lifetime (ns)

0

Re-Decode

Reset

OK

Cancel

- When the Protocol Analyzer records the boot/initialization of the Oakgate system, it will enable the decoding of the PCIe Traffic into NVMe Traffic
- The NVMe triggers require this information to be present
- NVMe addresses are mapped from the MBAR address set by the system

# Defining the Trigger in the OakGate Test Appliance



# Setting Trigger Events



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Discovered Appliances X Analyzer: NVMe Controller 86:0:0 X Exerciser X

Start Idle Namespace 0  
OGT-DEMO-3UG4-1 > NVMe Controller 86:0:0 > NVMe Target

Individual Exerciser Settings **Global Exerciser Settings** Post-Run Analytics

Filter Settings

General Settings

**Error Policies**

- Fibre Channel
- NVMe
- SAS/SATA
- SCSI Status
- SCSI Sense
- SCSI Additional Sense
- Custom Trigger Commands
  - NVMe
  - SATA
  - SAS

**GLOBAL ERROR POLICIES**

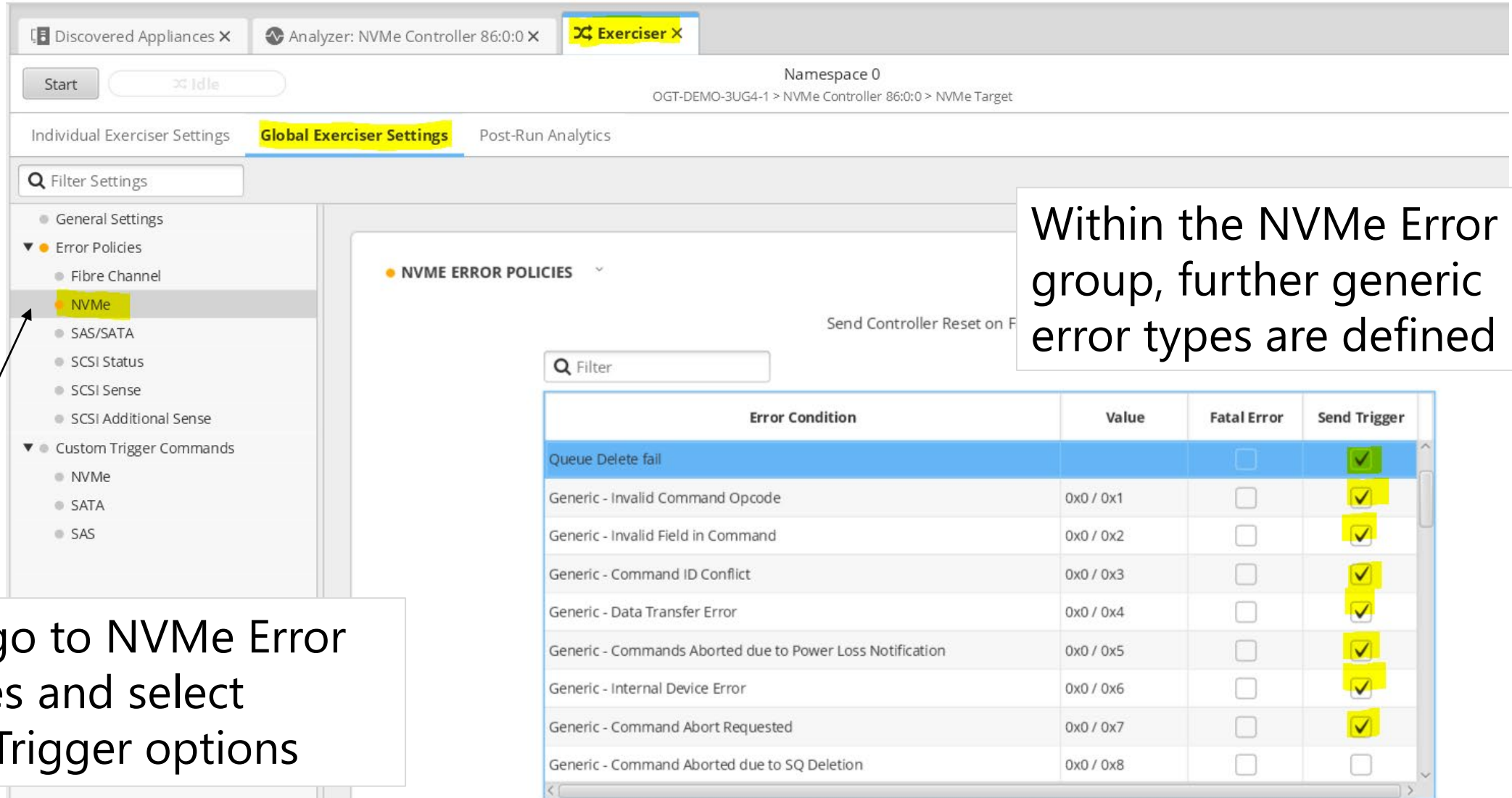
Filter

Error Condition	Fatal Error	Send Trigger
Link Down	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Failed IO Abort	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IO Hang	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Task Cleared By Another INI	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Task Reset By Another INI	<input type="checkbox"/>	<input checked="" type="checkbox"/>
IO Integrity Mismatch	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
IO Session Closed	<input type="checkbox"/>	<input type="checkbox"/>
Rd/Wr IO Failed	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Steady State Not Reached	<input type="checkbox"/>	<input type="checkbox"/>
Link Setting Mismatch	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

These events consist of multiple underlying transactions that the Protocol Analyzer cannot trigger on

Within the Oakgate software, multiple high-level errors can be selected and used as triggers

# Setting Trigger Events



Within the NVMe Error group, further generic error types are defined

Error Condition	Value	Fatal Error	Send Trigger
Queue Delete fail		<input type="checkbox"/>	<input checked="" type="checkbox"/>
Generic - Invalid Command Opcode	0x0 / 0x1	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Generic - Invalid Field in Command	0x0 / 0x2	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Generic - Command ID Conflict	0x0 / 0x3	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Generic - Data Transfer Error	0x0 / 0x4	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Generic - Commands Aborted due to Power Loss Notification	0x0 / 0x5	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Generic - Internal Device Error	0x0 / 0x6	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Generic - Command Abort Requested	0x0 / 0x7	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Generic - Command Aborted due to SQ Deletion	0x0 / 0x8	<input type="checkbox"/>	<input type="checkbox"/>

- Next go to NVMe Error Policies and select Send Trigger options

# Define your Trigger Event in Oakgate Test Software



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- Makes as many fields none zero values as possible.
- Send it to the drive to validate the function.

Discovered Appliances X Configuration X Analyzer: NVMe Controller 86:0:0 X Passthrough X Exerciser X

Start Idle Namespace 0  
OGT-DEMO-3UG4-1 > NVMe Controller 86:0:0 > NVMe Target

Individual Exerciser Settings **Global Exerciser Settings** Post-Run Analytics

Filter Settings

- General Settings
- Error Policies
  - Fibre Channel
  - NVMe
  - SAS/SATA
  - SCSI Status
  - SCSI Sense
  - SCSI Additional Sense
- Custom Trigger Commands
  - NVMe**
    - SATA
    - SAS

Add Command

- Write
- Read
- Flush
- Compare
- Get Log Page
- Identify**
- Get Features
- AER
- Virtualization Management
- Device Self-Test
- Doorbell Buffer Config
- NVMe-MI Send
- NVMe-MI Receive
- Keep Alive
- Sanitize
- Get LBA Status
- Verify
- Custom

Command Data

CNS 0x0

CNTID 0x5

NVMSETID 0x0

CSI 0x5

UUID Index 0x0

1 of 1

Byte	3:0	7:4	11:8	15:12
16	00000000	00000000	00000000	00000000
32	00000000	00000000	00050000	05000000
48	00000000	00000000	00000000	00000000

- We have selected a modified Identify command
- You may want to select a custom command to dump logs

# Defining the Trigger in the Teledyne LeCroy Analyzer

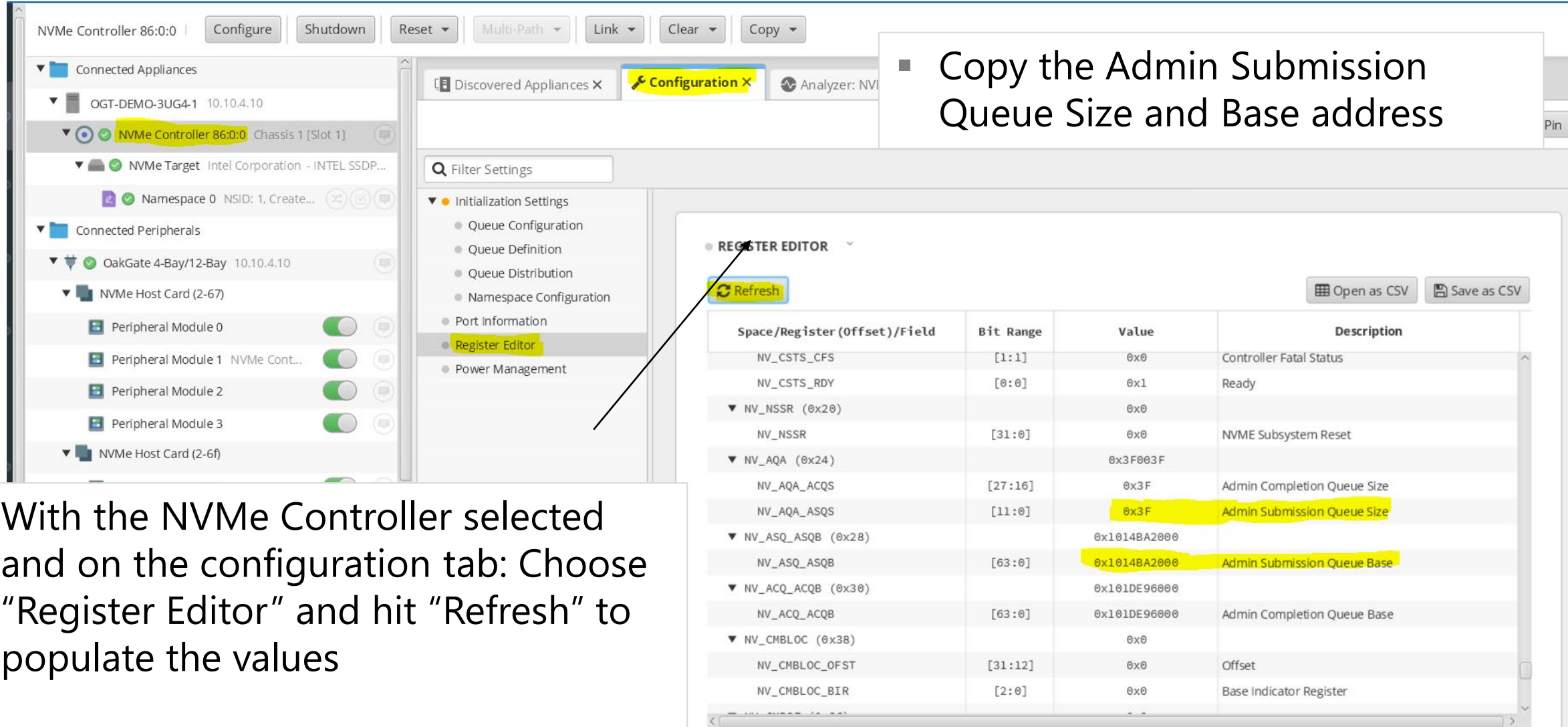
# Defining the trigger on the Protocol Analyzer

- The Protocol Analyzer will look for the event on the PCI Express link
- The NVMe event, is a sequence of PCI Express events
- Once the Protocol Analyzer has the NVMe queue information, either by capturing the boot sequence or providing the information manually from the Oakgate software, the Protocol Analyzer can be armed and wait for the event to happen

# Obtain the Admin Queue Base Address and Size

- Copy the Admin Submission Queue Size and Base address

- With the NVMe Controller selected and on the configuration tab: Choose "Register Editor" and hit "Refresh" to populate the values



Filter Settings

Initialization Settings

- Queue Configuration
- Queue Definition
- Queue Distribution
- Namespace Configuration
- Port Information
- Register Editor**
- Power Management

**REGISTER EDITOR**

Refresh

Open as CSV Save as CSV

Space/Register (Offset)/Field	Bit Range	Value	Description
NV_CSTS_CFS	[1:1]	0x0	Controller Fatal Status
NV_CSTS_RDY	[0:0]	0x1	Ready
▼ NV_NSSR (0x20)		0x0	
NV_NSSR	[31:0]	0x0	NVME Subsystem Reset
▼ NV_AQA (0x24)		0x3F003F	
NV_AQA_ACQS	[27:16]	0x3F	Admin Completion Queue Size
NV_AQA_ASQS	[11:0]	0x3F	Admin Submission Queue Size
▼ NV_ASQ_ASQB (0x28)		0x1014BA2000	
NV_ASQ_ASQB	[63:0]	0x1014BA2000	Admin Submission Queue Base
▼ NV_ACQ_ACQB (0x30)		0x101DE96000	
NV_ACQ_ACQB	[63:0]	0x101DE96000	Admin Completion Queue Base
▼ NV_CMBLOC (0x38)		0x0	
NV_CMBLOC_OFST	[31:12]	0x0	Offset
NV_CMBLOC_BIR	[2:0]	0x0	Base Indicator Register





# Protocol Analyzer View of NVMe Traffic

The Protocol Analyzer trace can give a very detailed view of the NVMe traffic, all the way down to the PCIe Data Link and Transaction Layers

NVMe Cmd 24		H	OPC		Asynchronous Event Request		1 warning(s)		Warning in Sub-Transaction		SQID	CQID	CID	CS	AE TYPE		AE INFO: Error status		ALP	ST	SCT		SC		Device ID		MN		Explicit SQyTDBL		Explicit ASQ	
											0x0000	0x0000	0x0018		Error status		Write to Invalid Doorbell Register		0x00		Generic Command Status		Invalid Command Opcode		001:00:0		NVMeLeCroy000000		NVMe #151		NVMe #156	

NVMe Cmd 25		H	OPC		SQID	CQID	CID	PRP1			PRP2			FID		SV	PS	ST	SCT		SC		Device ID		MN		Explicit SQyTDBL		Explicit ASQ		Explicit ACQ	
			Set Features		0x0000	0x0000	0x0019	0x00000000:00000000			0x00000000:00000000			Power Management		0	0x00		Generic Command Status		Successful Completion		001:00:0		NVMeLeCroy000000		NVMe #152		NVMe #157		NVMe #167	

NVMe 152

H

Device ID

QID

SQyTDBL

Admin SQT

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0000

0x001A

NVMeLeCroy000000

1

203.196 us

0018 . 460 016 852 000 s

NVMe 157

H

Device ID

QID

CID

Address

ASQ

OPC

FUSE

CID

NSID

MPTR

Address

PRP1

Address

PRP2

Address

FID

SV

PS

MN

001:00:0

0x0000

0x0019

00000001:0260C640

Set Features

Normal operation

0x0019

0x00000000

0x00000000:00000000

0x00000000:00000000

0x00000000:00000000

0x00000000:00000000

Power Management

0

0x00

NVMeLeCroy000000

NVMe 167

D

Device ID

QID

CID

Address

ACQ

SQHD

SQID

CID

P

DW0

RSVD

ST

SCT

SC

M

DNR

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0000

0x0019

00000001:02610190

0x001A

0x0000

0x0019

1

0x00000000

Generic Command Status

Successful Completion

0

0

NVMeLeCroy000000

1

5.044 us

0018 . 460 736 896 000 s

NVMe 168

D

Device ID

QID

CID

Address

Interrupt

Type

Vector

Message

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0000

0x0019

00000000:FEE0100C

MSI-X

0

0x00004991

NVMeLeCroy000000

1

44.314 us

0018 . 460 741 940 000 s

NVMe 169

H

Device ID

QID

CQyHDBL

Admin CQH

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0000

0x001A

NVMeLeCroy000000

1

8.722 us

0018 . 460 786 254 000 s

NVMe Cmd 26		D	OPC		SQID	CQID	CID	Data	MPTR		PRP1		PRP2		SLBA		NLB	PRINFO	FUA	LR	DSM	ACCF		ACCL	SEQR	INCOM	EILE
			Read		0x0005	0x0005	0x0000	2048 dwords	0x00000000:00000000		0x00000001:6E651000		0x00000001:1D352000		0x00000000:00000080		0x000F	0x0	0	0		No frequency information provided		None	0	0	0x0000

NVMe 170

H

Device ID

QID

SQyTDBL

IO SQT

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0005

0x0001

NVMeLeCroy000000

1

82.578 us

0018 . 460 794 976 000 s

NVMe 171

H

Device ID

QID

CID

Address

IOSQ

OPC

FUSE

CID

NSID

MPTR

Address

PRP1

Address

PRP2

Address

SLBA

NLB

PRINFO

PRCHK

PRAC

001:00:0

0x0005

0x0000

00000001:026C6000

Read

Normal operation

0x0000

0x00000001

0x00000000:00000000

0x00000001:6E651000

0x00000001:1D352000

0x00000000:00000080

0x000F

0x0

0

0

NVMe 172

D

Device ID

QID

CID

Address

PRP Data

Data Len

Data

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0005

0x0000

00000001:6E651000

0x000000400

1024 dwords

NVMeLeCroy000000

16

16.232 us

0018 . 461 061 186 000 s

NVMe 173

D

Device ID

QID

CID

Address

PRP Data

Data Len

Data

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0005

0x0000

00000001:1D352000

0x000000400

1024 dwords

NVMeLeCroy000000

16

491.436 us

0018 . 461 077 418 000 s

NVMe 174

D

Device ID

QID

CID

Address

IOCC

SQHD

SQID

CID

P

DW0

RSVD

ST

SCT

SC

M

DNR

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0005

0x0000

00000001:02642000

0x0001

0x0005

0x0000

1

0x00000000

Generic Command Status

Successful Completion

0

0

NVMeLeCroy000000

1

5.144 us

0018 . 461 568 854 000 s

NVMe 175

D

Device ID

QID

CID

Address

Interrupt

Type

Vector

Message

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0005

0x0000

00000000:FEE2000C

MSI-X

5

0x000049B1

NVMeLeCroy000000

1

4.658 us

0018 . 461 573 998 000 s

NVMe 176

H

Device ID

QID

CQyHDBL

IO CQH

MN

Metrics

# Link & Split Trans

Time Delta

Time Stamp

001:00:0

0x0005

0x0001

NVMeLeCroy000000

1

5.356 sec

0018 . 461 578 656 000 s

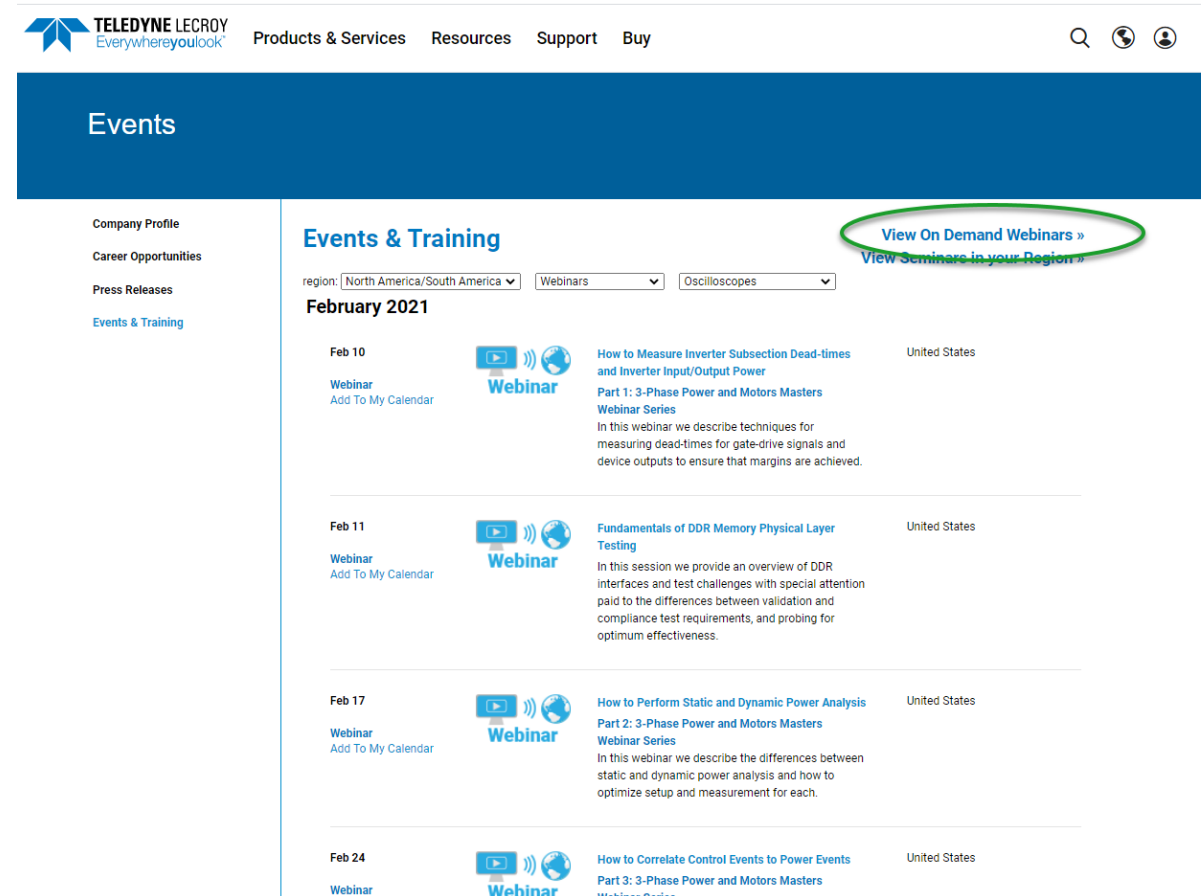


# Summary

- Using Trigger Events on Oakgate Test Appliance to trigger Protocol Analyzer can be a very useful way to root cause errors
- Gives full visibility that might be difficult to find otherwise
- Use Generic triggers to find broader range of errors without needing to define each case specifically
  - Using the Oakgate system will allow the user to select a range of errors without knowing in advance which error may occur
- The Protocol Analyzer will provide the specific details around the error condition
  - Use the same Protocol Analyzer trigger each time, based on the definition from the Oakgate software, saving time and effort

# Live Webinar, Events and Training Schedule

- <https://teledynelecroy.com/events/>
- View upcoming live events by date
  - Select to register for the event
- View On Demand Webinars
  - Select in upper right corner



The screenshot shows the Teledyne Lecroy website's 'Events & Training' section. The header includes the company logo and navigation links: Products & Services, Resources, Support, and Buy. A search icon and user profile icon are also present. The main content area is titled 'Events & Training' and features a sidebar with links to Company Profile, Career Opportunities, Press Releases, and Events & Training. The main content area displays a list of events for February 2021, filtered by region (North America/South America) and category (Webinars). The events listed are:

- Feb 10:** Webinar titled 'How to Measure Inverter Subsection Dead-times and Inverter Input/Output Power Part 1: 3-Phase Power and Motors Masters Webinar Series'. Description: 'In this webinar we describe techniques for measuring dead-times for gate-drive signals and device outputs to ensure that margins are achieved.' Location: United States.
- Feb 11:** Webinar titled 'Fundamentals of DDR Memory Physical Layer Testing'. Description: 'In this session we provide an overview of DDR interfaces and test challenges with special attention paid to the differences between validation and compliance test requirements, and probing for optimum effectiveness.' Location: United States.
- Feb 17:** Webinar titled 'How to Perform Static and Dynamic Power Analysis Part 2: 3-Phase Power and Motors Masters Webinar Series'. Description: 'In this webinar we describe the differences between static and dynamic power analysis and how to optimize setup and measurement for each.' Location: United States.
- Feb 24:** Webinar titled 'How to Correlate Control Events to Power Events Part 3: 3-Phase Power and Motors Masters Webinar Series'. Location: United States.

In the top right corner of the 'Events & Training' section, there are two links: 'View On Demand Webinars »' and 'View Seminars in your Region »', both of which are circled in green.

# Questions

# Contact Teledyne LeCroy



Flash Memory Summit



Summit M5x Analyzer/Jammer  
Gen 4 up to x16 (Gen 5 Capable up to x8)



Summit T416 Analyzer  
Gen 4 up to x16



Summit T516 Analyzer  
Gen 5 x16



Summit T3-16 Analyzer



Summit T54 Analyzer  
Gen 5 up to x4



Summit T3-8 Analyzer



Summit T28 Analyzer



Summit T48 Analyzer  
Gen 4 up to x8



Summit Z416 Exerciser  
Gen 4 up to x16



Summit Z516 PCIe 5.0/CXL Exerciser  
Gen 5 up to x16



Summit T3-16 Exerciser  
with Test Platform



Summit Z58 5.0 Exerciser/Analyzer  
Gen 5 up to x8

PCI   
**EXPRESS**®

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