



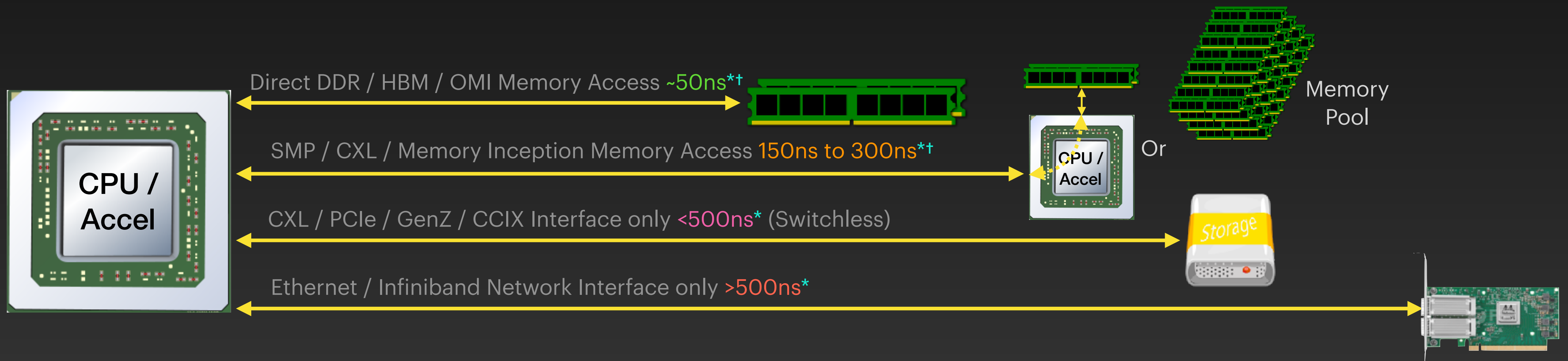
Open Memory Interface Overview

Allan Cantle - 03/27/2022

Today's Processor interface Choices

From a Latency / Power Perspective

- Processor Designers must allocate % beachfront for each interface
- Choices are increasing at the moment making the decision harder!



*Latencies are round trip approximations only : † Includes DDR Memory Read access time

OMI DDIMM Overview

Performance & Latency Optimized Serial Memory Interface

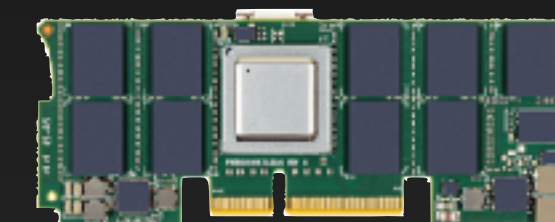
- 8 lane Serial Interface running at 25G & 32G
 - NRZ interface with No FEC
 - BER = 1E-12 with 20% Margin over a 30dB channel : Replays are rare
 - 4ns Loaded Latency Adder over a DDR4 LRDIMM Channel
- In production from Samsung, Smart & Micron
- Jedec Differential DIMM, DDIMM, Format
- Memory Technology Agnostic
 - Easy processor migration from DDR4 to DDR5
 - Other memories - LPDDR5x, MRAM etc.
- 512GB Dual OMI E3.S Memory in Development

To Scale



32GB 3200 DDR4 DIMM (reference)

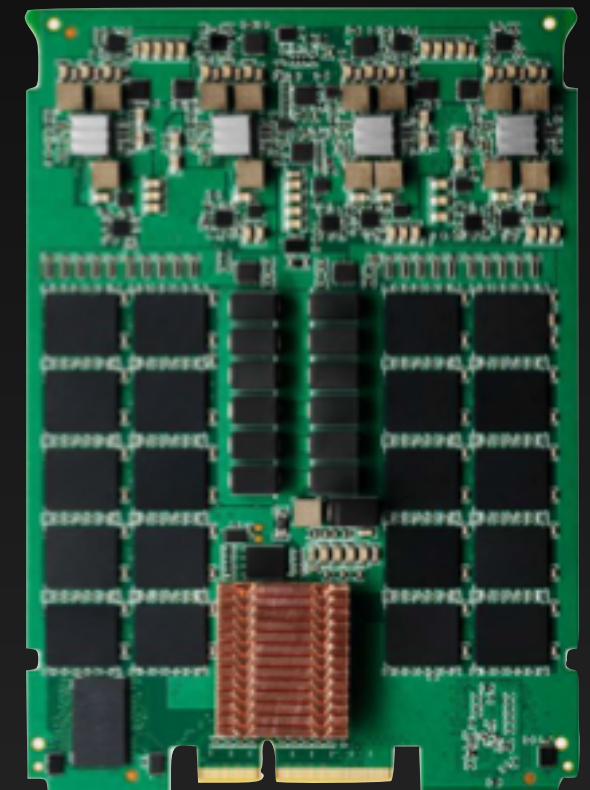
OMI DDIMMs Formats



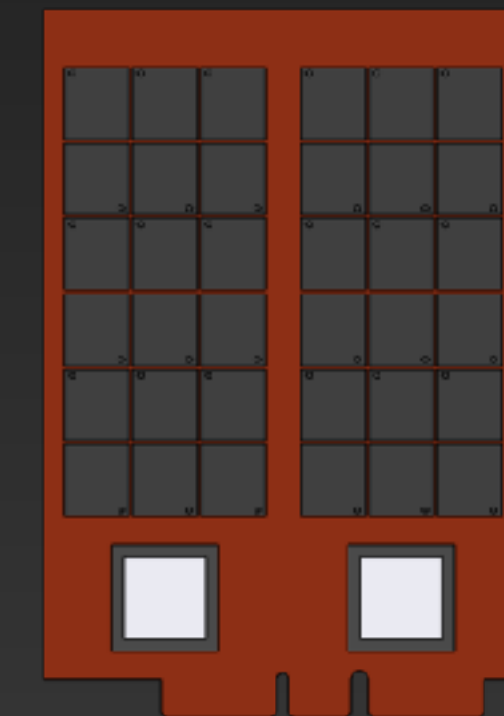
16GB / 32GB - 1U High
DDIMM



64GB / 128GB - 2U High
DDIMM



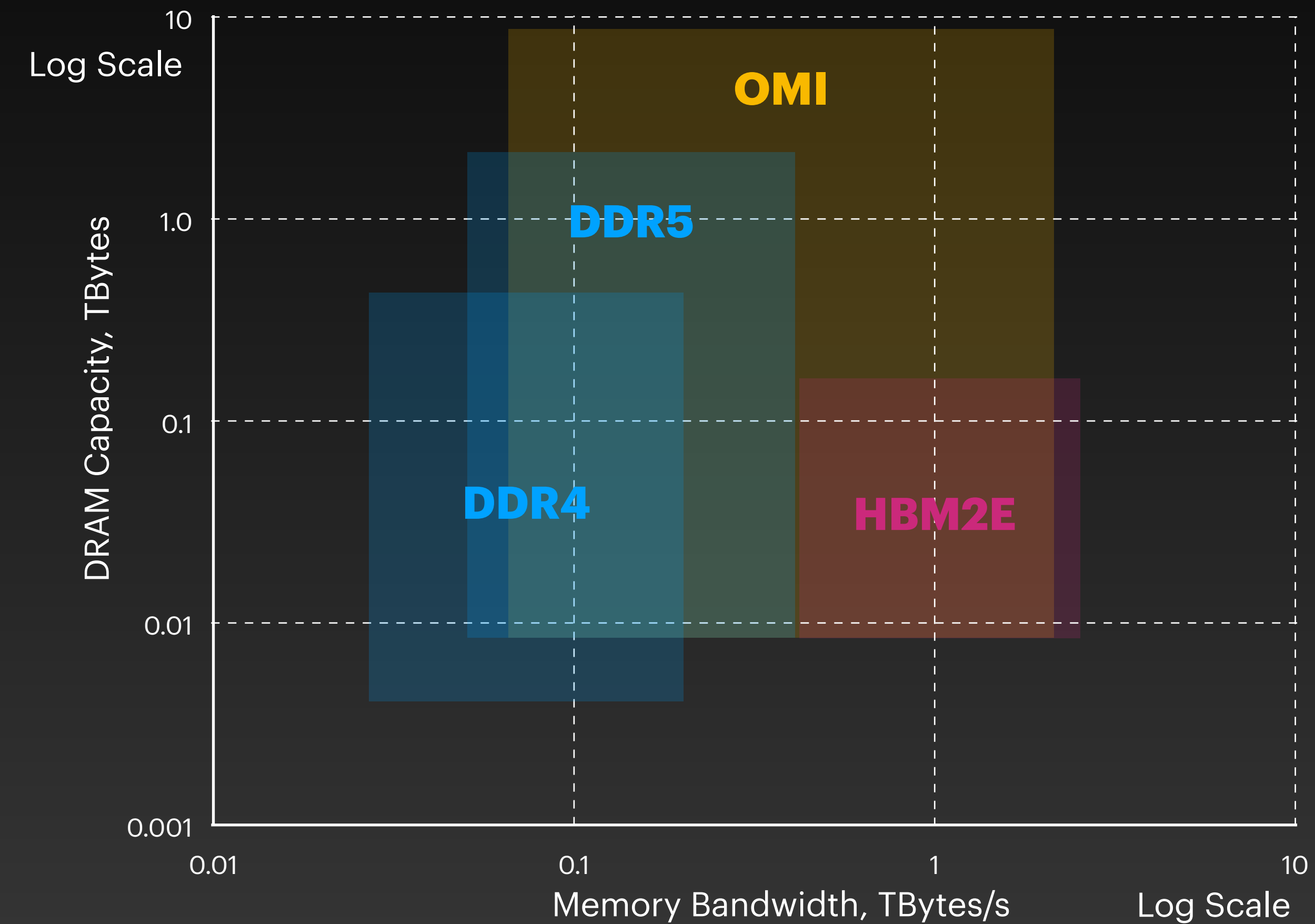
128GB - 4U High
DDIMM



512GB - Dual OMI
E3.S Module (In development)

Memory Interface Comparison

OMI - Bandwidth of HBM at DDR Latency, Capacity & Cost

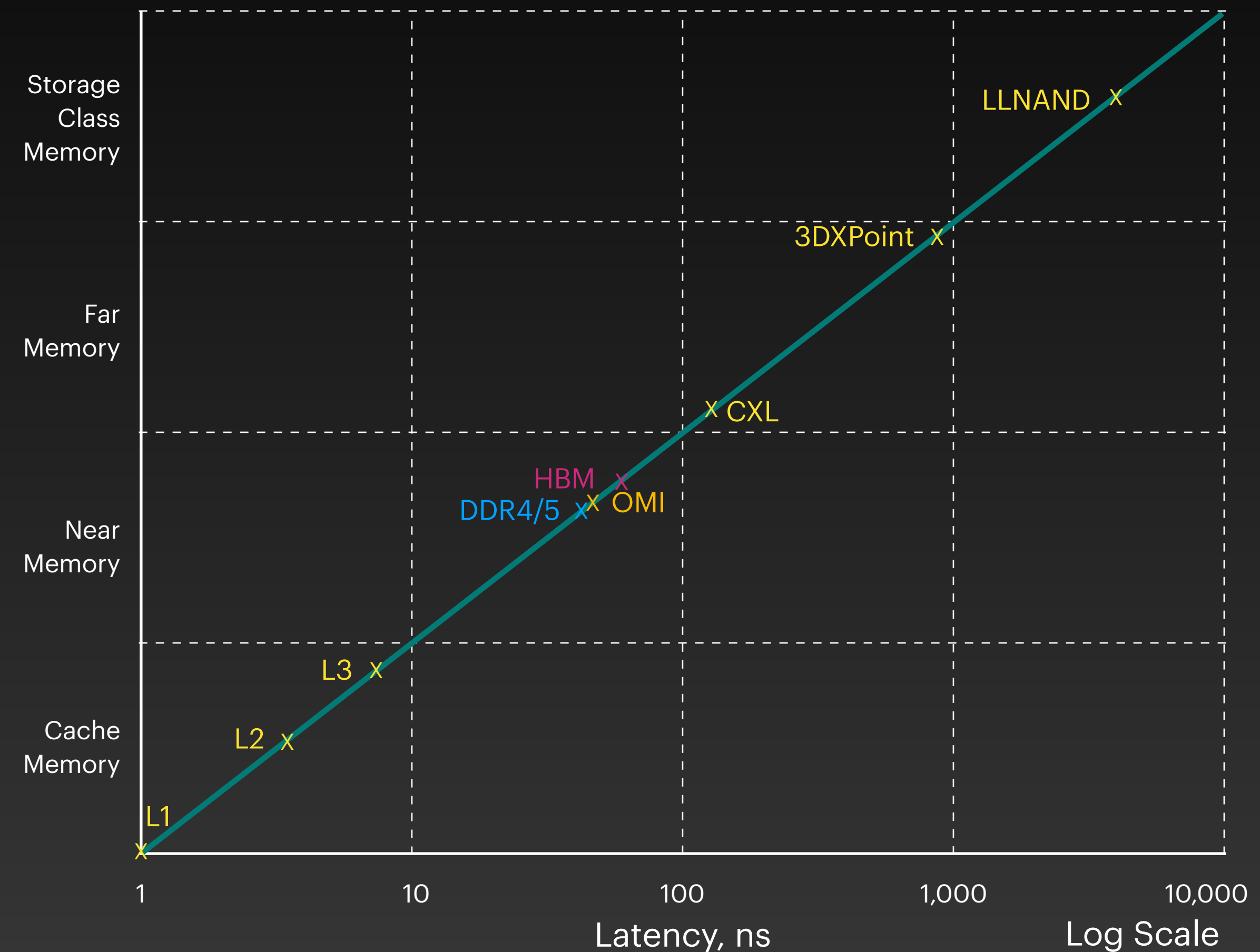


Graph depicts Practical Minimum : Maximum Channels per Processor

DDR = 1 : 8

OMI = 1 : 32

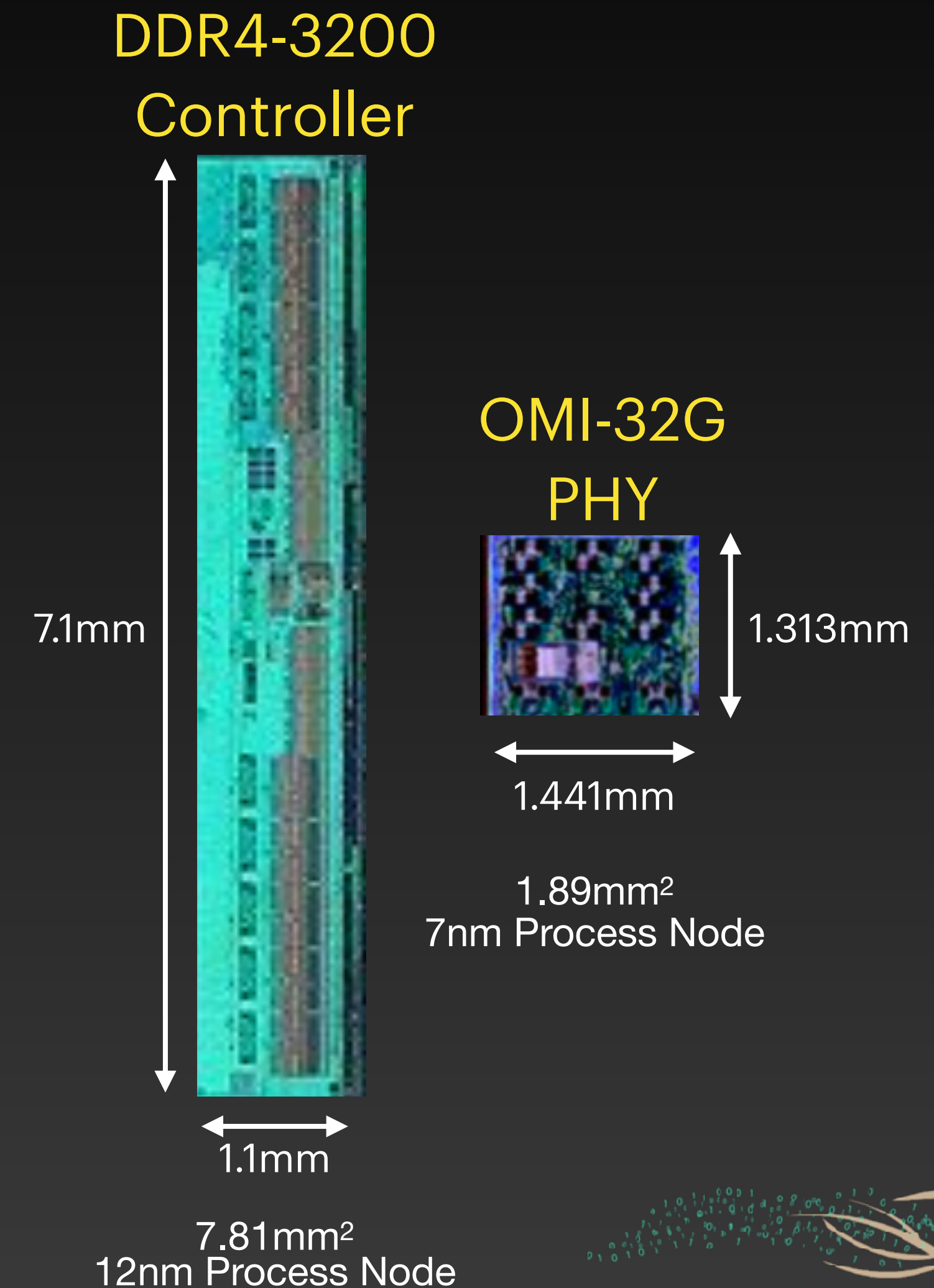
HBM = 1 : 6



Minimized Area & Beachfront for Memory IO

Smaller Processors OR Larger external Memory Bandwidth

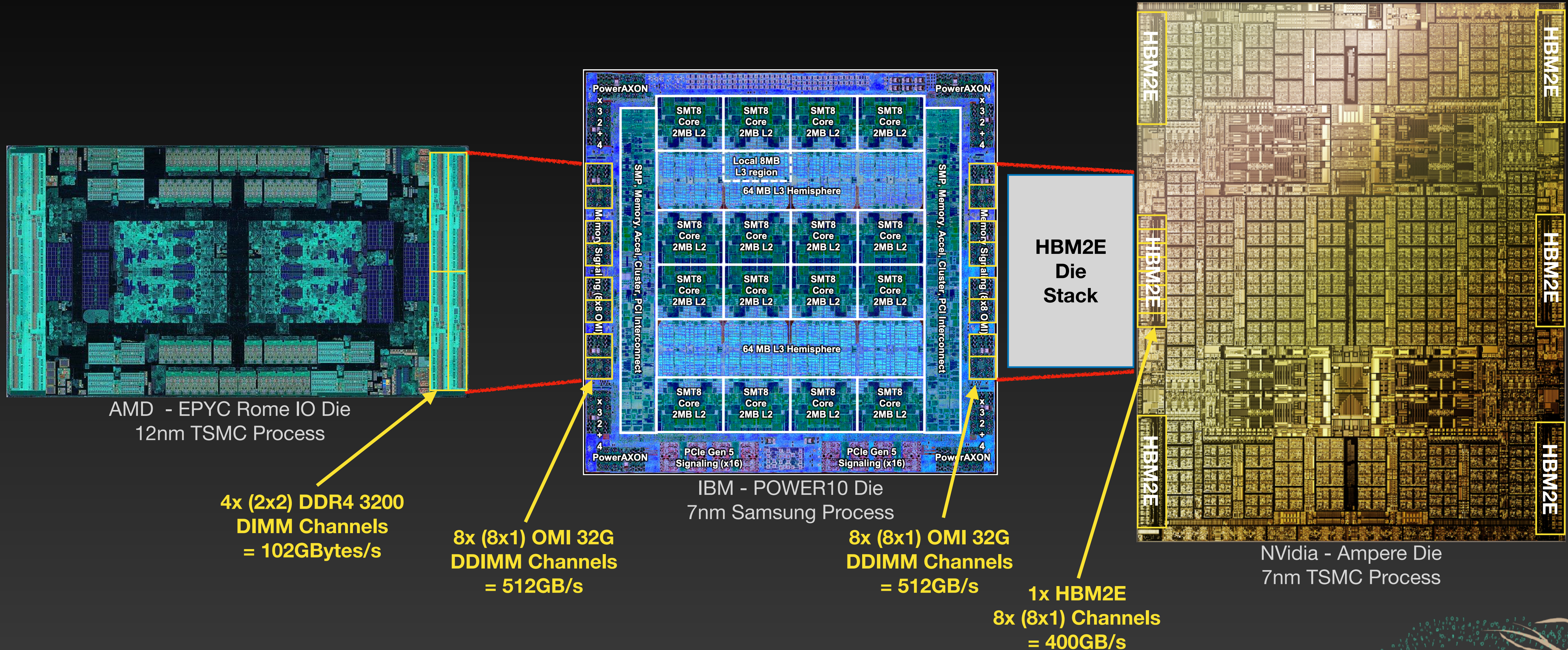
- OMI-32G Comparison to DDR4-3200
 - 2x Bandwidth Improvement per Channel
 - 6 : 1 Bandwidth / Silicon Area improvement*
 - ~10 : 1 Bandwidth / Beachfront improvement
- Processor Design Choices
 - Smaller better yielding lower power processor
 - Higher memory bandwidth with more channels
 - More area for more processor performance



* IBM POWER10 Processor - Hotchips 2020 - Slide 7

Actual Memory Technology Comparison

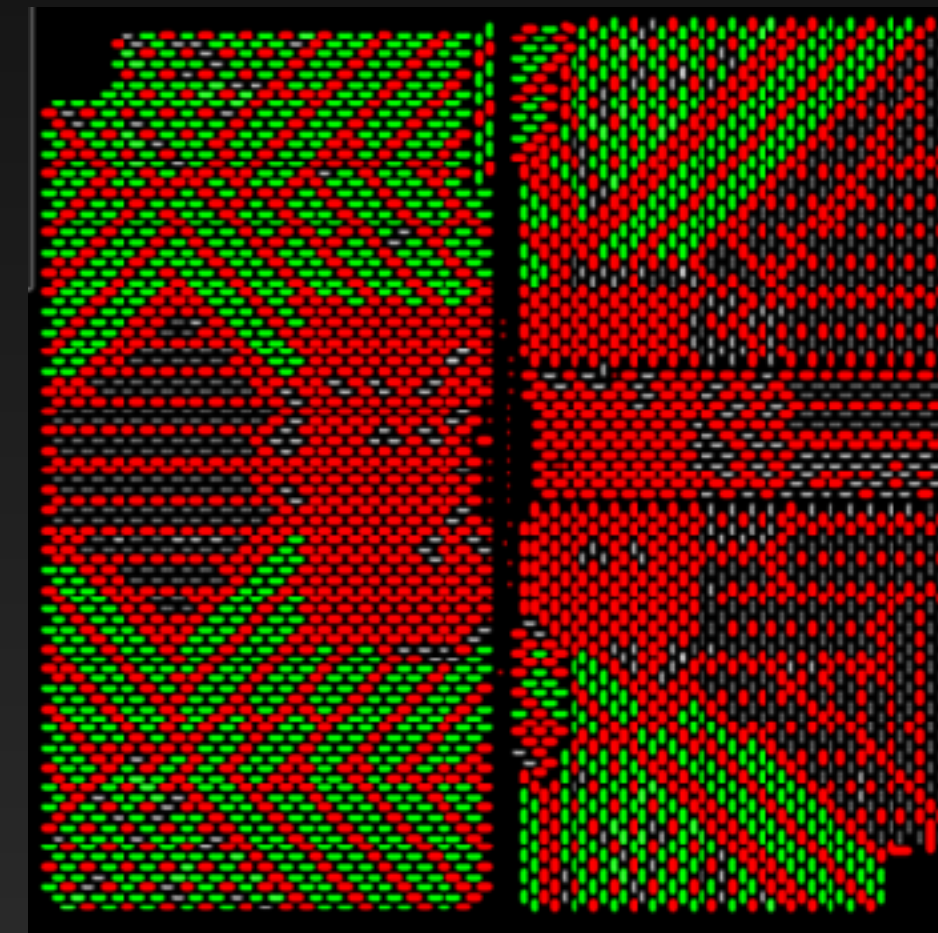
DDR4, OMI & HBM2E Bandwidth / Real Beachfront Comparison



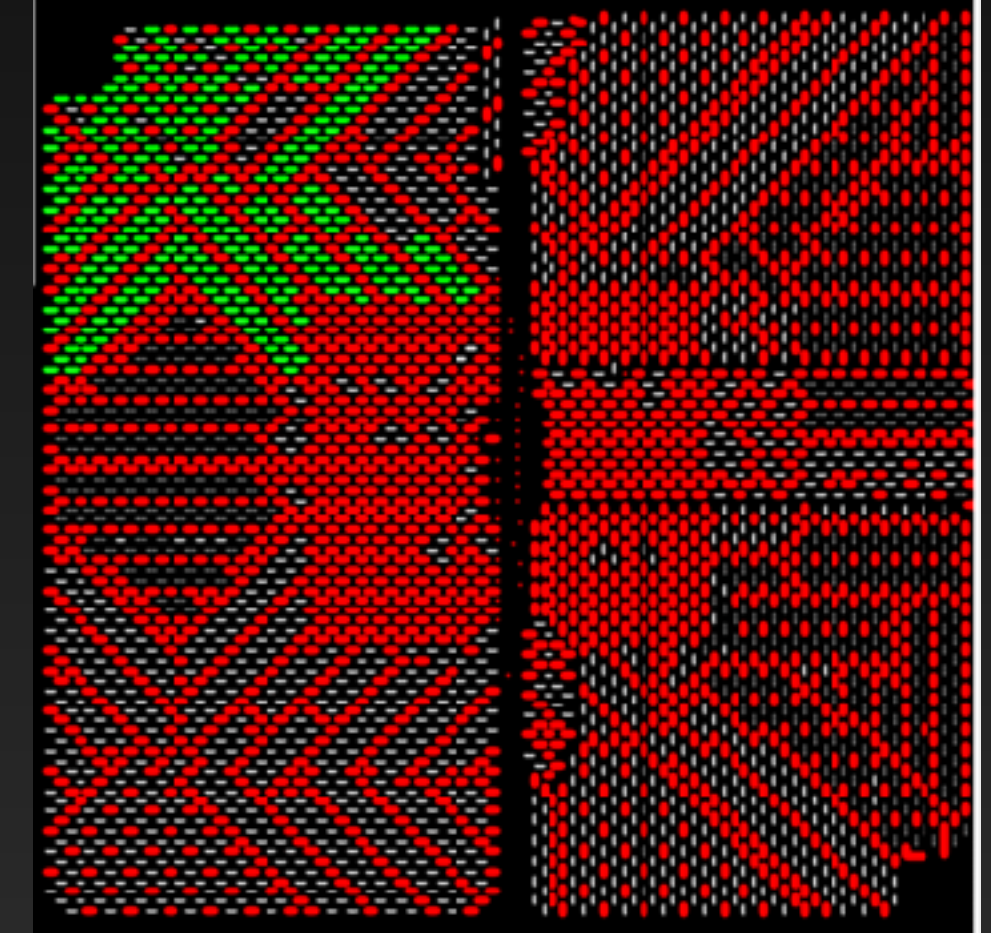
Reduced Processor Package Footprint

Simpler, Lower Cost Packages and Motherboards

- DDR4/5 Channels require 170+ Package pins
 - Memory Channels increasing rapidly
 - Processor Pin counts are ballooning
 - Processor Package sizes becoming untenable
 - Motherboard Complexity & Costs increasing
- OMI Channels require <40 Package Pins
 - 4x OMI Channels for Same Package Size
 - 8x Memory Bandwidth / Same Package Size



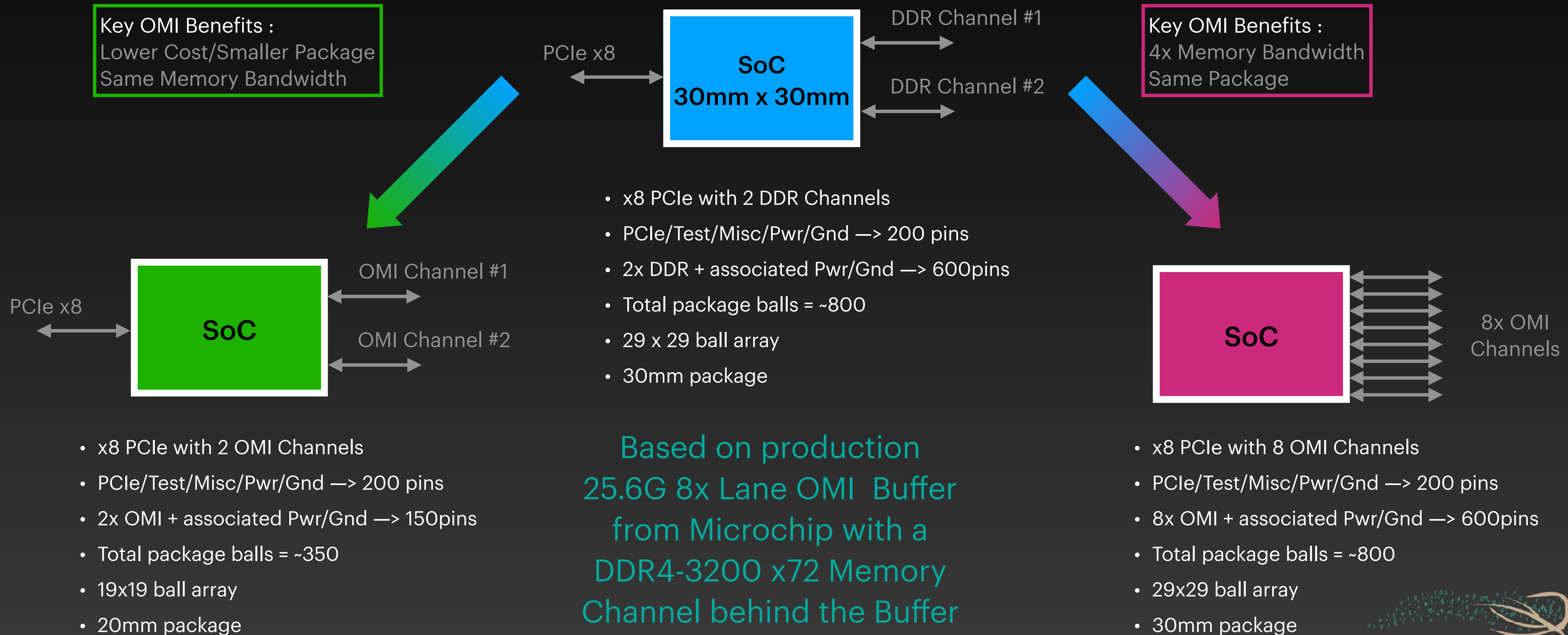
8 Industry Standard
DDR4 Channels



8 OMI Channels
(Equivalent Pin
Comparison)

OMI Serial Memory Example

No Memory Controller License Fees & seamless Transition from DDR4 to DDR5



OMI Development Platform

In Collaboration : AMD, IBM, Smart Modular & OpenCAPI Members

- Free, Open Sourced OMI Transaction and Data Link Layer IP
 - Two versions available for both FPGAs and ASICs
 - Includes both Host Controller and Memory Buffer IP
- FPGA Functional and Memory Traffic Generator IP
 - For evaluation and Testing purposes
- Hardware Platform Includes
 - Xilinx(AMD) VCU128 PCIe Development Platform
 - OpenCAPI FMC+ to two OMI DDIMM Sockets Adapter
 - DDIMM Memory Modules from Smart Modular
 - Compiled Ready to run FPGA IP



Why OMI - Summary

- OMI dramatically increases Memory Capacity & Bandwidth
 - for a given Processor Die size and Package size
 - without sacrificing Latency
- OMI ASIC Transaction and Data Link Layer RTL IP is Open and Royalty Free
 - For both Host and Buffer devices
 - Memory Controller Royalties are removed from the Processor
- Removes the technology transfer burden from DDR4 to DDR5
- In Production today from all major memory manufacturers
- Developer Ecosystem & Tools available through OpenCAPI Membership