

Challenges of Testing PCIe Gen. 4 SSDs and Beyond

Justin Treon Advantest

Santa Clara, CA August 2019





- MPT3000 SSD Tester
- Implementing PCIe Gen. 4 Early
- Specification Issues
- Testing Issues
- Test Compliance Issues
- PCIe Gen. 5 and 6
- SAS-4 and SAS-5



Our PCIe Gen. 4 Product

- The MPT3000 is a multi-protocol SSD tester
 - FPGA based implementation allows for the protocol switches





Risking Early Development

- Hardware developed for the 0.7 physical layer of the PCIe Gen. 4 specification
- By using the FPGA we were able to test before the Gen. 4 devices became available



Testing the Link

- No devices to test the link available
 - ... so we made our own
 - To be an early adopter you need to build you own test equipment
- Test board has many debug features to test the link





Eye Diagram

- Eye Diagram tool added to debug the link
 - Similar to Rx Margin (a.k.a. Lane Margining)
- Adding eye diagram to SSD controllers is suggested

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	192.0mv	#####	*****	******	****	******	******	*****	*******	******	*****	##
	179.2mv	#####	*****	******	****	******	#######	######	*******	******	*****	##
	166.4mv	#####	*****	******	****	******	#######	######	*******	******	*****	##
	153.6mv	#####	*****	******	*****	******	******	*****	*******	******	*****	##
	140.8mv	#####	*****	******	****	****~~~	**###**	~	~ ~%%	******	*****	##
	128.0mv	#####	*****	####***	~~~		: ~			**#####	*****	##
	115.2mv	#####	*****	##%~~			:			~%####	*****	##
	102.4mv	#####	*****	*~~			:			~~%###	******	##
	89.6mv	#####	*****	~~			:			~%##	*****	##
	76.8m v	#####	#### <i>*~</i>	~			:			~%#	*****	##
	64.0mv	#####	###%~				:			%#	*****	##
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	-166.4mv	#####	######	******	****	******	******	######	*******	******	******	##
	-179.2mv	#####	*****	******	*****	******	******	######	*******	******	******	##
	-192.0mv	#####	""""""	******	*****	******	******	######	*******	******	******	# #

Maximum Eve Width = 0.75 UI



Changes to the Specification

- The optional lane margining feature was made mandatory at the last moment ... surprise
- Causing implementation mismatch requiring rearchitecting
 - Budget time and resources for specification changes



Testing the Performance

- No SSD available to test with ... so we made our own
- DMA transfers simulated the NVMe command
 - Setting data engine speed
 - Determining performance with NVMe command overhead

Gen. 4 x4 Performance vs Payload Size



Advantest Gen. 4 x4 with NVMe command overhead

- - Link Limit Gen. 4 x4



PCI SIG Compliance

- Test systems were not ready
 - False positives for pass and fail
 - Engineering resources used to correct tests
- Test specification as of last plug fest
 - Not possible to obtain PCI SIG certification



Hurry Up and Wait

- PCIe Gen. 4 market intercept pushed out from original expectations
- Extra time allowed for feature development and stability improvements



TCDT (Traffic Capture and Debug Tool)

- Traffic Capture and Debug Tool
 - Suite of user friendly graphical tools for parsing and debugging captures
 - LTSSM Rules Checker
 - Tools allow users to parse and analyze logs in a quick and user friendly manner

🔣 LTS	iM Rules Checker - [tlp_capt_20190	0506_134919_dn_dut0_0_0.srt]								
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Searc	h List			Re	esult List					
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3	Recovery.RcvrLock	Detect.Quiet	na							
4	Polling.Active	Any	24							
5	Recovery.RcvrLock	Any	24							
6	Polling.Configuration	Detect.Quiet	na	E						
7	Recovery.RcvrCfg	Detect.Quiet	na							
8	Recovery.Idle	Detect.Quiet	na							
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7284	ctype=LS, time=20190506_13:4	8:18.685698843 , add= 390, delta=	0.131 us, Itssm=[Of Rcv_Idle] Ipmsm	=[1 L0], 1pmsm=[[0 L10]]. TxEI=0, RxEI=0, Clkreq=1, SpdCh=0, Spd=Gen3, perst=F, NAKtx=0, NA	4Knx=0, RxAct=00000			
7285	ctype=LS, time=20190506_13:4	8:18.685698855 , add= 391, delta=	0.012 us, Itssm=[0f Rcv_Idle], Ipmsm	=[1 L0], l1pmsm=[[0 L10] TxEI=0, RxEI=1, Clkreq=1, SpdCh=0, Spd=Gen3, perst=F, NAKtx=0, NA	VKrx=0, RxAct=00000			
7285	ctype=LS, time=20190506_13:40	8:18.085099024, add= 392, delta=	0.159 us, Itssmillof Rcv_Idle], Ipmsm	=[1 L0], l1pmsm=[ULLO J, TXLEO, KXLEO, CIKreq I, SpdChio, Spdillens, perstiif, NAKtxio, NA	Krx=0, RxAct=00000			
7288	ctupe=15, time=20190506_13:40	8:18.687115062 adds 204 daltas	1416 925 us Iterm=10b Roy PLos 1 Jon	=[1 L0] items	m=10110] TxE1=0, RxE1=1, Cikren=1, SpdCh=0, Spd=Gen3, perst=F, NAKX=0, NA	NAKer=0, React=00000			
7289	ctype=15, time=20190506_13:4	8:18.711215968 add= 395 delta=	24100.006 us itssm=10d Rev Speci 1 In	msm=[110	1110ms	sm=10.110 1 TyFI=0 RyFI=1 Clkreq=1 SndCh=0 Snd=Gen3 perst=F NAKty=0	0 NAKrx=0 RxArt=0			
7290	ctype=LS. time=20190506 13:41	8:18.711215993 add= 396 delta=	0.025 us. Itssm=[0d Rcv Sped 1. Ipms	m=[1 L0	1. l1pmsm:	=10 L10 1 TxEI=1 RxEI=1 Clkreg=1 SpdCh=0 Spd=Gen3 perst=F. NAKtx=0. N	NAKrx=0. RxAct=0000			
7291	ctype=LS, time=20190506_13:4	8:18.711217968 , add= 397, delta=	1.975 us, Itssm=[0d Rcv_Sped], Ipms	m=[1 L0], I1pmsm:	=[0 L10], TxEI=1, RxEI=1, Clkreg=1, SpdCh=0, Spd=Gen1, perst=F, NAKtx=0, P	NAKrx=0, RxAct=0000			
7292	ctype=LS, time=20190506_13:48	8:18.711217974 , add= 398, delta=	0.006 us, Itssm=[0d Rcv_Sped], Ipms	m=[1 L0], I1pmsm:	=[0 L10], TxEI=1, RxEI=1, Clkreq=1, SpdCh=1, Spd=Gen1, perst=F, NAKtx=0, M	NAKrx=0, RxAct=000			
7293	ctype=LS, time=20190506_13:48	8:18.711217980 , add= 399, delta=	0.006 us, Itssm=[0d Rcv_Sped], Ipms	im=[1 L0], I1pmsm:	=[0 L10], TxEI=1, RxEI=1, Clkreq=1, SpdCh=0, Spd=Gen1, perst=F, NAKtx=0, M	NAKrx=0, RxAct=0000			
7294	ctype=LS, time=20190506_13:4	8:18.712216005 , add= 400, delta=	998.025 us, Itssm=[0b Rcv_RLoc], Ipm	sm=[1 L0], I1pmsm	n=[0 L10], TxEI=1, RxEI=1, Clkreq=1, SpdCh=0, Spd=Gen1, perst=F, NAKtx=0,	NAKrx=0, RxAct=000			
7295	ctype=LS, time=20190506_13:4	8:18.712216043 , add= 401, delta=	0.038 us, Itssm=[0b Rcv_RLoc], Ipms	m=[1 L0], I1pmsmi	=[0 L10], TxEI=0, RxEI=1, Clkreq=1, SpdCh=0, Spd=Gen1, perst=F, NAKtx=0, N	VAKrx=0, RxAct=0000			
7296	ctype=LS, time=20190506_13:4	8:18.736316012 , add= 402, delta= 1	24099.969 us, Itssm=[00 DetQuiet], Ipn	nsm=(1 LO], l1pmsr	m=[0 L10], TxEI=0, RxEI=1, Clkreq=1, SpdCh=0, Spd=Gen1, perst=F, NAKtx=0	NAKrx=0, RxAct=00			
7297	ctype=LS, time=20190506_13:4	8:18.736316049 , add= 403, delta=	0.037 us, Itssm=[00 DetQuiet], Ipmsi	m=[1 L0], l1pmsm=	=[U L10], TxEI=1, RxEI=1, Clkreq=1, SpdCh=0, Spd=Gen1, perst=F, NAKtx=0, N	IAKnx=0, RxAct=0000			
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- TLP Capture
 - Packet capture at the TLP layer and above
- PCIe Protocol Decoder
 - Protocol Decoder allows the user to graphically analyze the traffic





TLP Capture Example (1)

- PCIe link framing
 - Test Log

Minimize Voltage and disconnect!

Example of link framing failure

*********** PCIE Link St. LinkUp LO LTSSM LinkWidth LinkSped ActiveLanes ValidLanes LinkUpCount LinkRetrainC(****** = = = = = = = =	true 0x10, LTSSN x4 8.0G 00001111 (0 00001111 (0 1 22	******** M_LO DxOf) DxOf)														
Sun Jan 27 2 Error in con	8:54:4 nectir	47 2019 E	lin	c r	etr	ai	n c	oun	t	22	> 2	20.					
Power up PCI	e leve	els! ERROR i	in settin	g the PC	Ie Powe	r Level											
- Log	fr	om	TLF	> C	Cap	otu	re										
delta=473746.780	us,	ltssm=[Ob Rc	v_RLoc]	, lpmsm=[1 L0	1,	l1pmsm=[0 I	10],	TxEI=0,	RxEI=0,	Clkreq=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc
delta= 0.005	us,	ltssm=[0b Rc	v_RLoc]	, lpmsm=[1 L0	1,	l1pmsm=[0 I	10],	TxEI=0,	RxEI=0,	Clkreq=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc
delta= 0.005	us,	ltssm=[0b Rc	v_RLoc]	, lpmsm=[1 L0	1,	l1pmsm=[0 I	10],	TxEI=0,	RxEI=0,	Clkreg=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc
delta= 0.005	us,	ltssm=[0b Rc	v_RLoc]	, lpmsm=[1 L0	1,	l1pmsm=[0 I	10],	TxEI=0,	RxEI=0,	Clkreg=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc
delta= 0.945	us,	ltssm=[0e Rc	v_RCfg]	, lpmsm=[1 L0	1,	l1pmsm=[0 I	10],	TxEI=0,	RxEI=0,	Clkreg=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc
delta= 0.240	us,	ltssm=[0f Rc	v_Idle]	, lpmsm=[1 L0	1,	l1pmsm=[0 I	10],	TxEI=0,	RxEI=0,	Clkreg=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc
delta= 0.340	us,	ltssm=[10	L0]	, lpmsm=[1 L0	1,	l1pmsm=[0 I	10],	TxEI=0,	RxEI=0,	Clkreg=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc
delta=122430.750	us,	ltssm=[0b Rc	v_RLoc]	, lpmsm=[1 L0	1,	l1pmsm=[0 I	10],	TxEI=0,	RxEI=0,	Clkreq=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc
delta= 0.005	us,	ltssm=[0b Rc	v RLoc]	, lpmsm=[1 L0	1.	l1pmsm=[0 I	10 1,	TxEI=0.	RxEI=0,	Clkreg=0,	SpdCh=0,	Gen3,	perst=F,	NAKtx=0,	NAKrx=0,	RxAc

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August 2019

delta=

delta=

delta=

delta=

deltas

delta=

delta=

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delta=

delta=

delta=

0.005 us.

0.005 us,

0.940 us.

0.245 us,

0.335 us.

0.005 us.

0.005 us,

0.005 us.

0.970 us.

0.240 us,

0.340 us.

delta= 38072.200 us,

delta= 38072.180 us.

ltssm=[0b Rcv RLoc

ltssm=[Ob Rcv RLoc

ltssm=[0e Rcv RCfg

ltssm=[0f Rcv Idle

ltssm=[0b Rcv RLoc

ltssm=[0b Rcv RLoc

ltssm=[0b Rcv RLoc

ltssm=[0b Rcv RLoc

ltssm=[0e Rcv RCfg

ltssm=[Of Rcv Idle

ltssm=[Ob Rcv RLoc

0.005 us, ltssm=[0b Rcv RLoc], lpmsm=[1 L0

ltssm=[10 --L0--

0.005 us. ltssm=[0b Rcv RLoc

ltssm=[10 --L0--



TLP Capture Example (2)

No block device not ready •

Test Log Minimize Voltage and disconnect!

PCIe Link Status : LinkUp L0 = true LISSM = 0x10, LTSSM_L0 LinkWidth = x4 LinkSpeed = 8.0G = 00001111 (0x0f) ActiveLanes = 00001111 (0x0f) ValidLanes LinkUpCount = 1 LinkRetrainCot = 3 Sun Mar 24 01:55:04 2019 ERROR : Block Device is not present. find protocol fpga virtual ep: ---> bus (number=14 primarv=12 nvme_wait_ready: Error: device not ready after 20500 nvme probe: nvme configure admin queue failed, result Block Device is not present.

Log from TLP

Example of device ready failure

20190324_01:54:12.277536572 [142]:>DN1[Mem32 RdReq] 'b00000001 'b0000000f 'bca01001c 20190324_01:54:12.277537080 [138]: <dn1['h0000001c="" 'h0e000004="" 'h4a000001="" 0x0<=""]="" cpl="" data="" th="" w=""><th></th></dn1[>	
[many lines reporting the same status deleted]	
20190324_01:54:32.585139616 [337]:>DN1[Mem32 RdReq]	(3:11,0,1.12) LEN=4 CPU
20190324_01:54:32.585140124 [333]: <dn1['h0000001c="" 'h0e000004="" 'h4a000001="" 0x0<=""]="" cpl="" data="" td="" w=""><td>0000000 (4:11,0,0.02) LEN=4 CPU</td></dn1[>	0000000 (4:11,0,0.02) LEN=4 CPU
20190324 01:54:32.689161116 [338]:>DN1[Mem32 RdReq]	
20190324_01:54:32.689161616 [334]: <dn1['h0000001c="" 'h0e000004="" 'h4a000001="" 0x0<=""]="" cpl="" data="" td="" w=""><td>0000000 (4:11,0,0.02) LEN=4 CPU</td></dn1[>	0000000 (4:11,0,0.02) LEN=4 CPU

NVMe controller status register CSTS.RDY reports not ready

Santa Clara, CAQ August 2019



August 2019

PCIe Gen. 5 and Beyond

- PCIe Gen. 5 is almost the same as Gen. 4
 - Early adopters will need to make their own tools
- Gen. 6 specification in 2021
 - Significant changes
 - 64 GT/s
 - Pulse Amplitude Modulation
 - Forward Error Correction
- PCI SIG on three year cycle, Gen. 7 in 2024





SAS-4 and SAS-5

- There may be a SAS-4 market ... maybe
 - SAS-4 demand is limited to companies that do not want to update/upgrade databases
 - SAS optimized databases do not make good use of potential performance gains
- Will there even be a SAS-5?





- Making your own tools is crucial as an early implementor
- Starting early allows the product to mature, but is costly ... and frustrating
- Beware supply chain issues
 - High speed components may be in short supply
 - Resin for high speed PCBs will be costly and is in short supply







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TLP Capture Example (3)

], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=00001111

], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=00001111

], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=00001111

], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=00001111, l0recovery=[rcvd ts]

Flash Memory Summit

- PCIe link rcvd_ts
- **Test Log** •

ActiveLanes ValidLanes TxElecIdle TxDetectRx RxElecIdle RxPolarity LINK Width Link Width Link Up ReTrain LinkUp	Test: Display = 00001111 (0x0f) = 10100111 (0x0f) = 10100111 (0x0f) = 0000111 (0x0f) = 010000 (0x00) = 00000000 (0x00) = x4 Changed = 5.0G Changed = 1 = 0 = 1	Link LO	Status,	Wed	Mar
ReTrain	Count	=	655	3!	5

on from TLP Canture

], lpmsm=[1 L0

], lpmsm=[1 L0

], 1pmsm=[1 L0

lpmsm=[1 L0

Time since last ReTrain: 1.1e-05 seconds

0.512 us, ltssm=[10 --L0--

13.996 us, ltssm=[10 --L0--

0.016 us, ltssm=[10 --L0--

0.016 us, ltssm=[Ob Rcv_RLoc

Example of link training failure

	9				
delta=	0.000 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreg=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
delta=	0.000 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
delta=	0.016 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
ielta=	0.016 us,	ltssm=[0b Rcv_RLoc], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
ielta=	1.332 us,	ltssm=[0e Rcv_RCfg], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
delta=	0.448 us,	ltssm=[0f Rcv_Idle], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
ielta=	0.504 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
ielta-	14.004 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
ielta=	0.016 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
ielta=	0.016 us,	ltssm=[0b Rcv_RLoc], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
ielta=	1.340 us,	ltssm=[0e Rcv_RCfg], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
delta=	0.448 us,	ltssm=[0f Rcv_Idle], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
delta=	0.496 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
ielta=	14.012 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
delta=	0.016 us,	ltssm=[10L0], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
delta=	0.016 us,	ltssm=[0b Rcv_RLoc], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
delta=	1.332 us,	ltssm=[0e Rcv_RCfg], lpmsm=[1 L0], l1pmsm=[0 L10], TxEI=0, RxEI=0, Clkreq=0, SpdCh=0, Spd=Gen2, perst=F, NAKtx=0, NAKrx=0, RxAct=000
4-1	0 449	langer [Of Des Table	1 1mmmm [1 T.0	1 11mmm 10 T10	1 TyFI-0 PyFI-0 Clkrage0 SndCh=0 Snd-Gan2 narst-F NAVty=0 NAVty=0 PyAct=000

], l1pmsm=[0 L10

], l1pmsm=[0 L10

], l1pmsm=[0 L10

], l1pmsm=[0 L10

10recovery=[rcvd_ts	1
10recovery=[rcvd_ts	1

1, 10recovery=[rcvd ts]

1, 10recovery=[rcvd_ts]

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delta= delta=

delta= delta=



PCIe Gen. 4 Changes

- 1. Speed change to 16GT/s
- 2. Equalization updates for 4.0 (8 GT/s to 16 GT/s)
- 3. TSx OS changes
- 4. 16 GT/s EIEOS
- 5. SKP OS changes (CTRL SKP)
- 6. Polling.Compliance update
- 7. 10-Bit Tag
 - Allowing for greater token count
- 8. Data Link Feature Exchange
- 9. Flow Control Scaling
- 10. Rx Margining (a.k.a. Lane Margining)
 - Host cabling feature
 - Pushed through as a requirement by Intel
- 11. Retimer
- 12. Configuration space register updates