Hyperdimensional Computing | Cognitive Memory of the Pattern Kind and Computing with Vague and Ambiguous Information

Gil Russell

WebFeet Research Inc.

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Research | Vision | Knowledge

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View "Hello Computer" from "Startrek IV" here:

https://www.youtube.com/watch?v=v9kTVZiJ3Uc

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Natural, Synthetic & Artificial

- Some Semantic Variations

Natural

Found in Nature => "Natural Intelligence"

Artificial

Not Found in Nature => "Unnatural Intelligence?"

Synthetic

Man Made => "Synthetic Intelligence"

On the road to Synthetic Intelligence

- Trends on What we've learned (so far)

Machine Learning ≠Intelligence Deep Learning Promise

Has entered the trough of disillusionment

Sequences are mandatory

Prediction absolutely required

Fast "One-shot" learning required for anomalous conditions

Broad span solution – one algebra for all

Embedded Controllers through High-Performance Computing

Cognitive Database compatibilities

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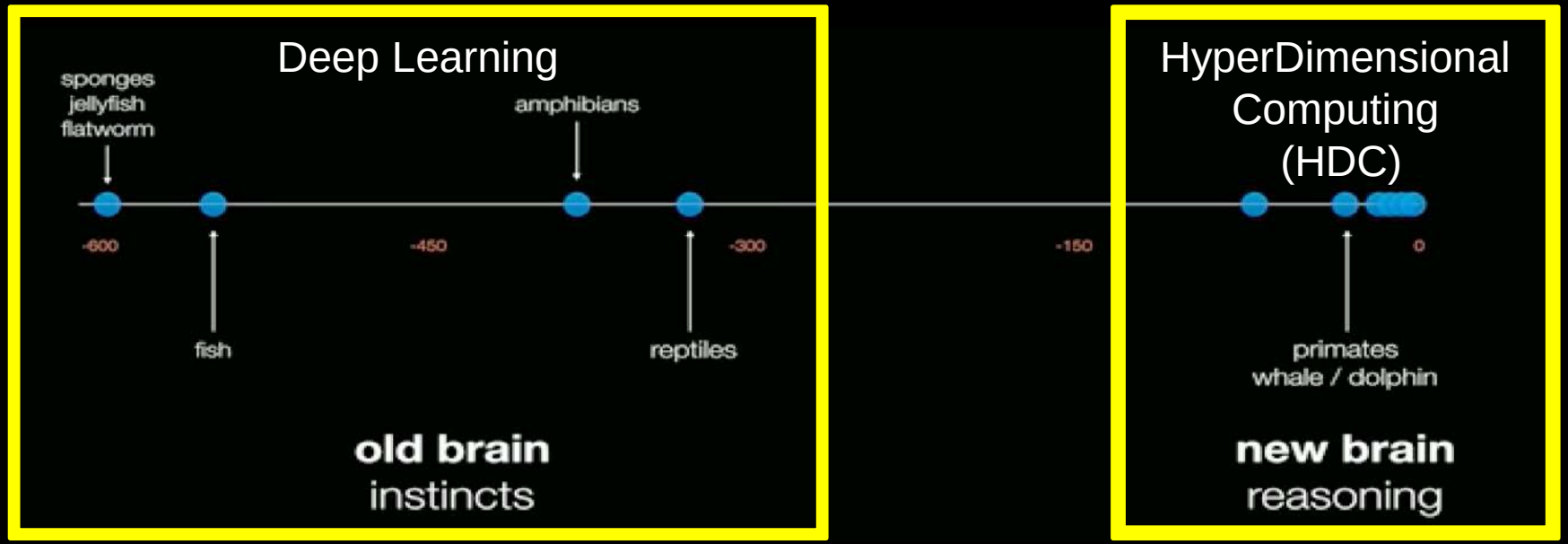
New vs. Old Brain



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"Brain Inspired"

Hyper-Dimensional Computing (HDC)
Google: Visualizing High Dimensional Space

View "A.I. Experiments: Visualizing High-Dimensional Space" here:

https://www.youtube.com/watch?v=wvsE8jm1GzE

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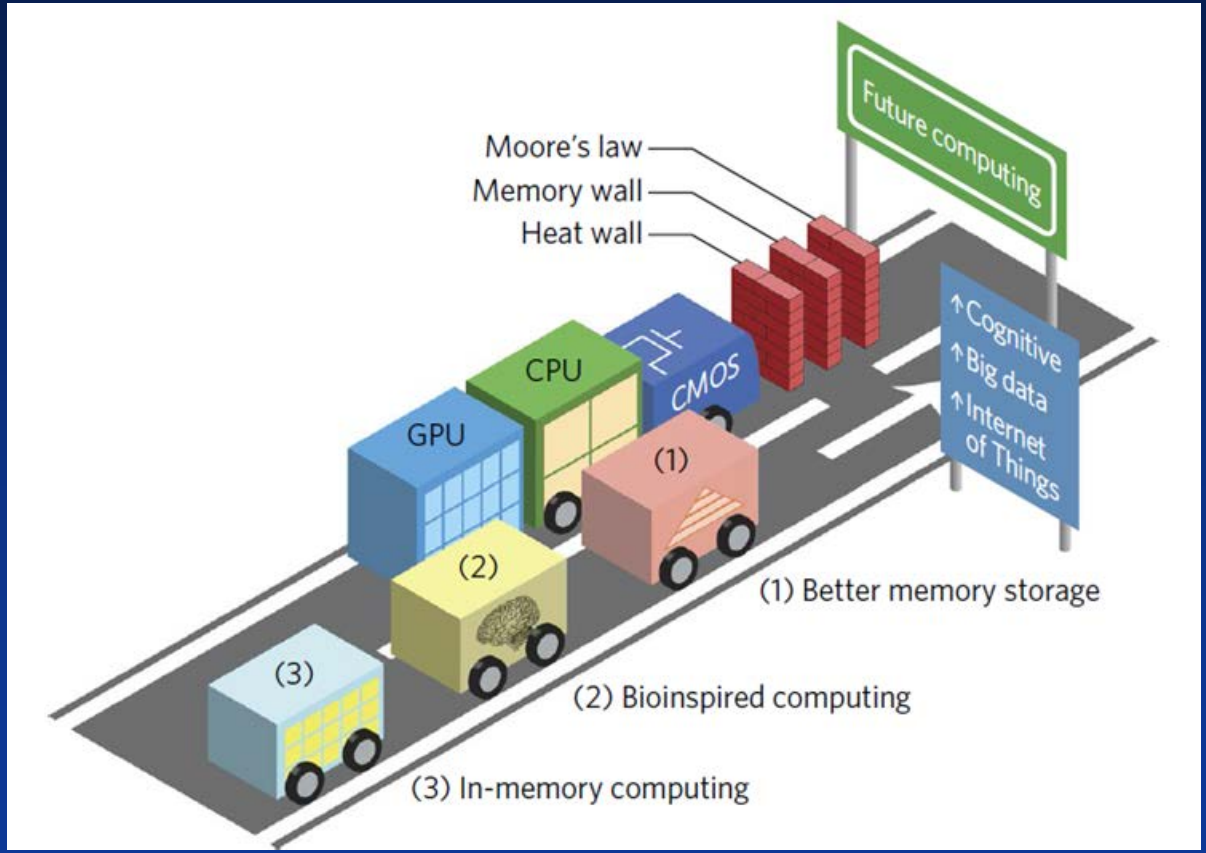
Future of the Cognitive Computing Highway



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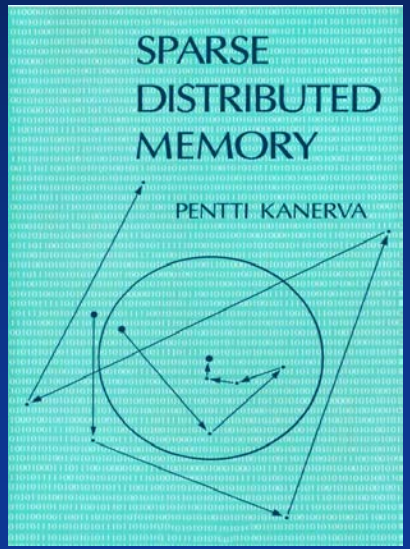
Sparse Distributed Memory + Hyperdimensional Computing

Pentti Kanerva, UC Berkeley
Redwood Center for Theoretical Neuroscience

"Sparse, Distributed Memory", MIT Press, 1988



"Hyperdimensional Computing: An Introduction to Computing in Distributed Representation with High-Dimensional Random Vectors", Pentti Kanerva, January 2009

https://redwood.berkeley.edu/

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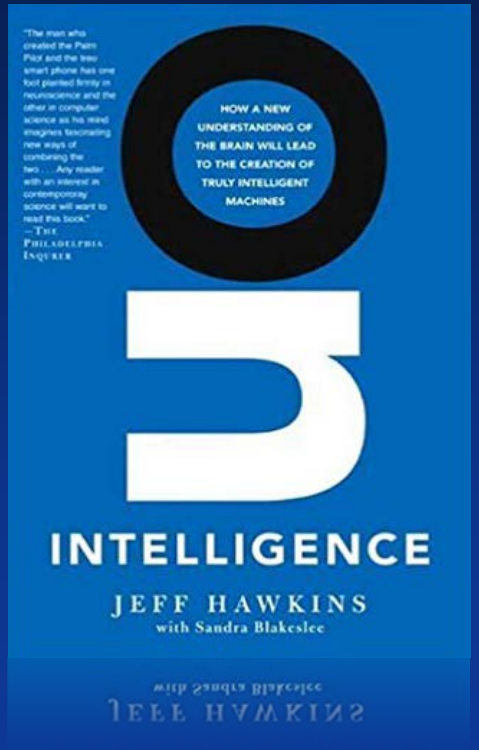
Sparse Distributed Memory + Thousand Brains Theory of Intelligence



Jeff Hawkins
Founder: Redwood Center for Theoretical Neuroscience (2002), Founder & CEO Numenta (2005)

“On Intelligence, How a New Understanding of the Brain Will Lead to the Creation of Truly Intelligent Machines”, 2004

“Thousand Brains Theory of Intelligence”, 2019

https://numenta.com/

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Hyper-Dimensional Computing – What is it?

An advanced algebra memory based framework for building a general cognitive system with the associative qualities of the human brain's neo-cortex:

- Robust and noise-tolerant
- Learns from data/example, learns by analogy
- Can learn fast: "One-shot" learning
- Integrates signals from disparate senses
- Allows simple algorithms that scale to large problems efficiently
- Allows high degree of parallelism
- Has been implemented on extremely low power electronics

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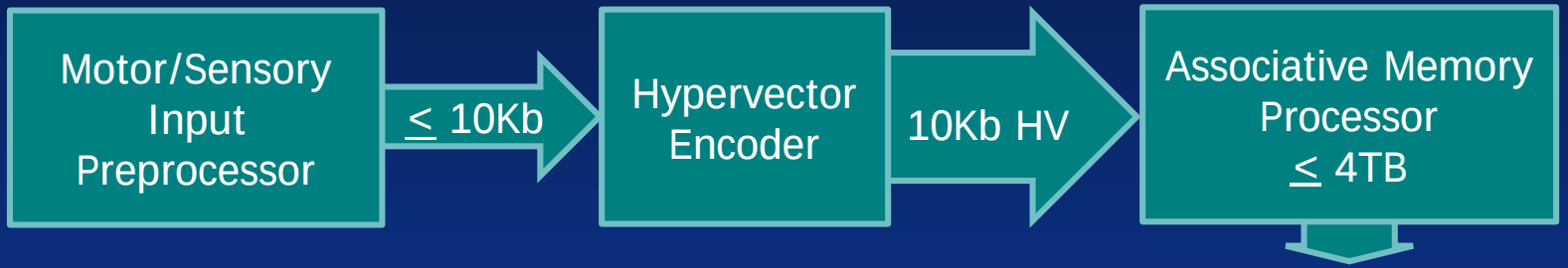
Hyperdimensional Computing (Block Diagram)



HV Address space ($2^{10,000}$ = 1.995063116880758384883742162 6 e+3010)

Associative Memory Processor (Training + Experiential ~ 4 to 8 TB)

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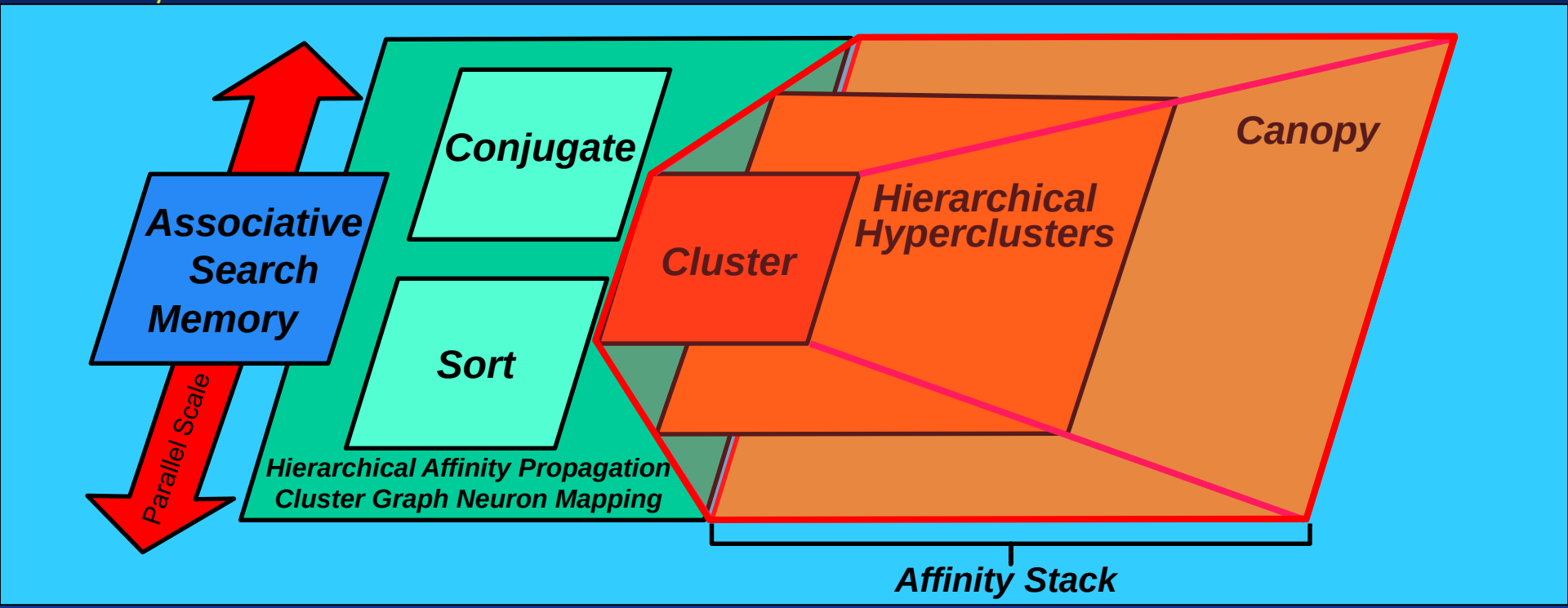
Hyperdimensional Cognitive Computing Conceptual Architecture



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Europe – IMEC, CEA-Leti & Fraunhofer Group

- *Decision to fund a 3 year program called Tempo*
- *Plan to develop process technology and hardware platforms leveraging emerging memory technologies for neuromorphic computing*
- *Goal is to develop a new way to support applications in mobile computing devices that require complex machine-learning algorithms*
- *IBM/ETH Zurich Paper "In-memory hyperdimensional computing" thought to have highly influential to this decision (https://arxiv.org/pdf/1906.01548.pdf)*

https://www.eetimes.com/document.asp?doc_id=1334886#

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IBM Research /ETH Zurich

In-memory hyperdimensional computing

Geethan Karunaratne,1, 2 Manuel Le Gallo,1 Giovanni Cherubini,1 Luca Benini,2 Abbas Rahimi,2, a) and Abu Sebastian1, b)
1)IBM Research – Zurich, S ¨aumerstrasse 4, 8803 R ¨uschlikon, Switzerland.
2)Department of Information Technology and Electrical Engineering, ETH Zurich, Gloriastrasse 35, 8092 Zurich, Switzerland.
(Dated: 5 June 2019)

(https://arxiv.org/pdf/1906.01548.pdf)

[WebFeet Research highly recommends this source material]

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In-Memory Computing SUMMIT NORTH AMERICA 2018

High-Dimensional Computing

SDM Memory & Hyperscaling

A session on the Cloud's missing AI component

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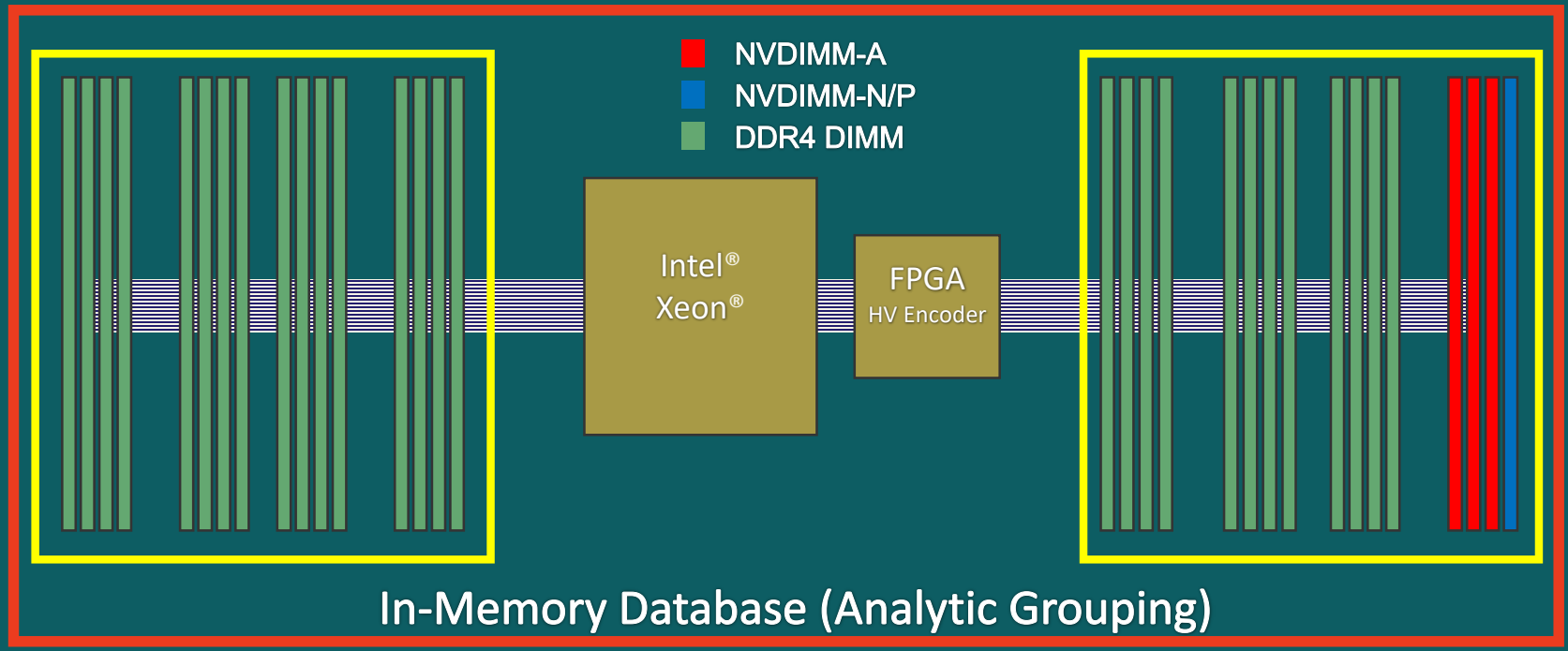
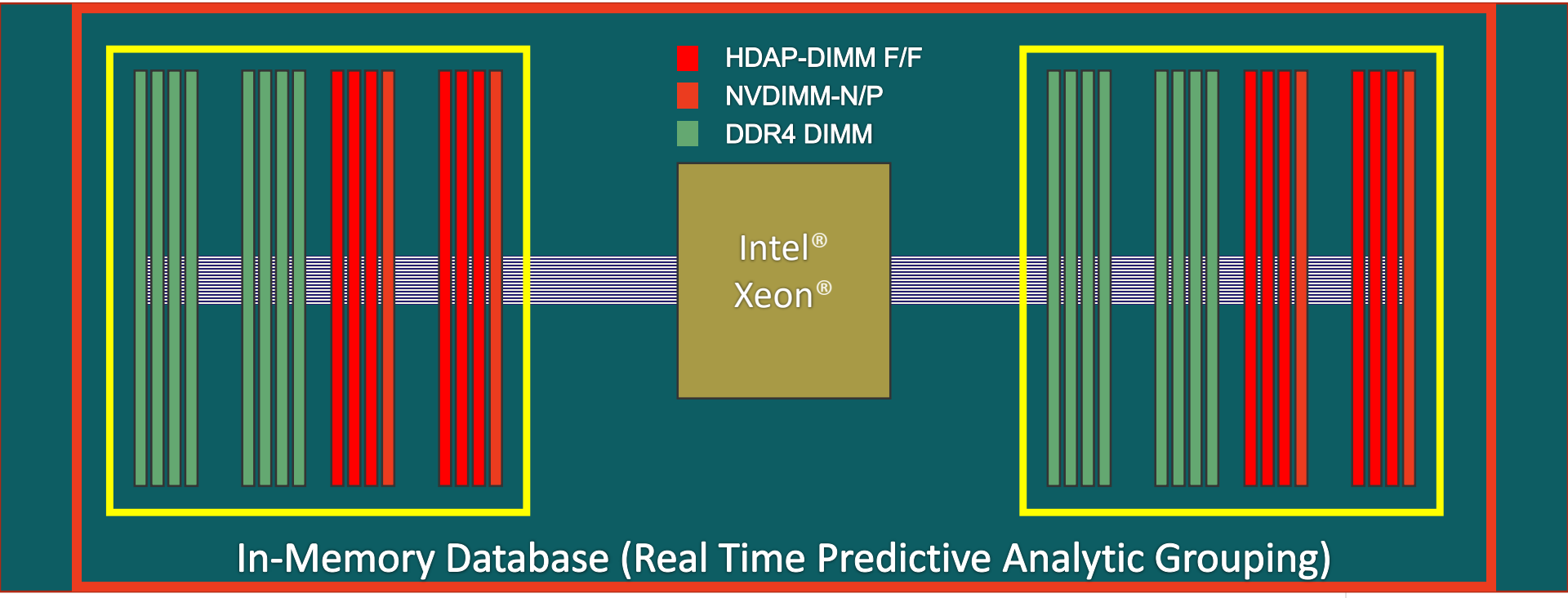
The Kanerva Partition (Database Intersect)
In-Memory Hypothetical System Implementation



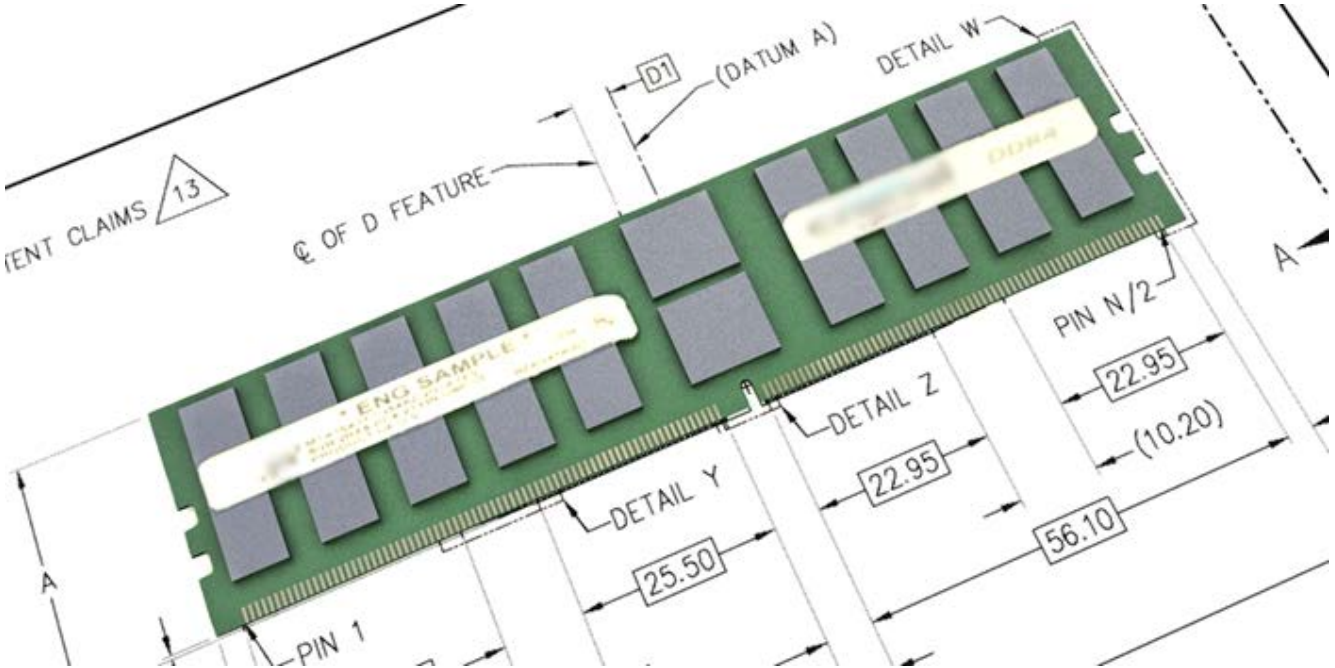
The Kanerva Partition

(RT-PA Grouping)

In-Memory Hyperdimensional Associative Processor (Hypothetical)



Hyperdimensional Computing
Associative Processor - NVDIMM-X Form Factor



288 Pin NVDIMM Form Factor

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Patent Applications of Note:

US 20190227981A1

(19) **United States**

(12) **Patent Application Publication**

Tomishima et al.

(10) **Pub. No.: US 2019/0227981 A1**

(43) **Pub. Date: Jul. 25, 2019**

(54) **TECHNOLOGIES FOR PROVIDING A SCALABLE ARCHITECTURE FOR PERFORMING COMPUTE OPERATIONS IN MEMORY**

(71) Applicant: **Intel Corporation**, Santa Clara, CA (US)

(72) Inventors: **Shigeki Tomishima**, Portland, OR (US); **Srikanth Srinivasan**, Portland, OR (US); **Chetan Chauhan**, Folsom, CA (US); **Rajesh Sundaram**, Folsom, CA (US); **Jawad B. Khan**, Portland, OR (US)

(21) Appl. No.: **16/368,983**

(22) Filed: **Mar. 29, 2019**

Publication Classification

(51) **Int. Cl.**

G06F 15/78	(2006.01)
G06F 17/16	(2006.01)
G06F 15/80	(2006.01)

(52) **U.S. Cl.**

CPC ***G06F 15/7867*** (2013.01); ***G06F 15/803*** (2013.01); ***G06F 17/16*** (2013.01); ***G06F 15/7842*** (2013.01)

(57) **ABSTRACT**

Technologies for providing a scalable architecture to efficiently perform compute operations in memory include a memory having media access circuitry coupled to a memory media. The media access circuitry is to access data from the memory media to perform a requested operation, perform, with each of multiple compute logic units included in the media access circuitry, the requested operation concurrently on the accessed data, and write, to the memory media, resultant data produced from execution of the requested operation.

US 2019/0227981 A1
Filed: Mar. 29, 2019
Published: July 25, 2019:

"TECHNOLOGIES FOR PROVIDING A SCALABLE ARCHITECTURE FOR PERFORMING COMPUTE OPERATION IN MEMORY"

Applicant: Intel Corporation, Santa Clara, CA

Enables "Computational Memory" on the Memory Channel

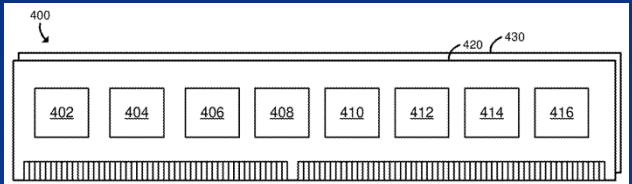

FIG. 4

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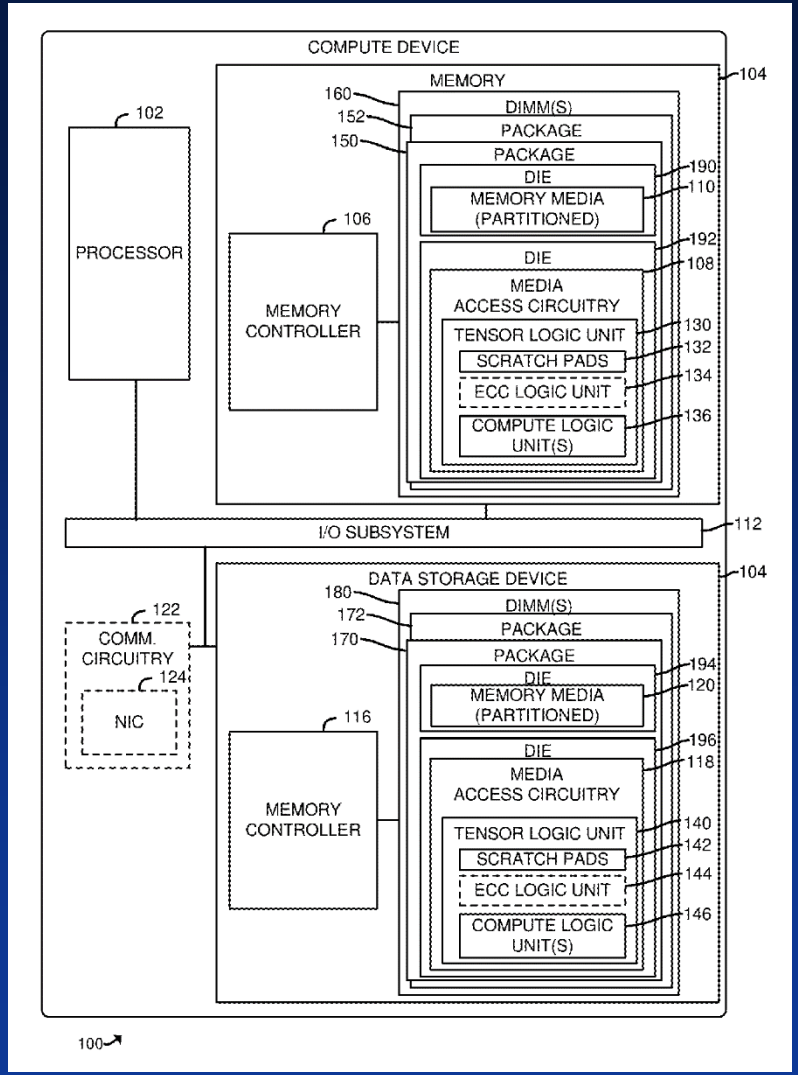

Patent Applications of Note:

US 2019/0227981 A1
Filed: Mar. 29, 2019
Published: July 25, 2019:

"TECHNOLOGIES FOR PROVIDING A SCALABLE ARCHITECTURE FOR PERFORMING COMPUTE OPERATION IN MEMORY"

Applicant: Intel Corporation, Santa Clara, CA

Optane DIMM & Drive covered

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Patent Applications of Note:

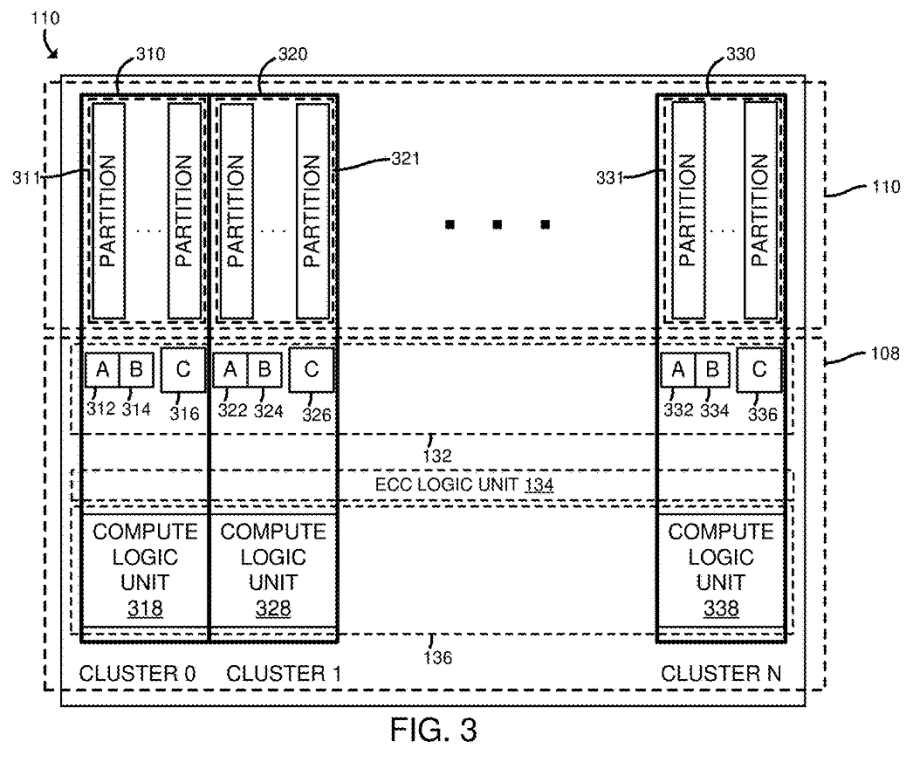

FIG. 3

US 2019/0227981 A1
Filed: Mar. 29, 2019
Published: July 25, 2019:

"TECHNOLOGIES FOR PROVIDING A SCALABLE ARCHITECTURE FOR PERFORMING COMPUTE OPERATION IN MEMORY"

Applicant: Intel Corporation, Santa Clara, CA

Enables Bit Level Addressable Persistent Memory:

- 3DXPoint
- Chalcogenide (memresistive)
- FeTRAM
- Nanowire-based Non-volatile
- STT-RAM
- MRAM

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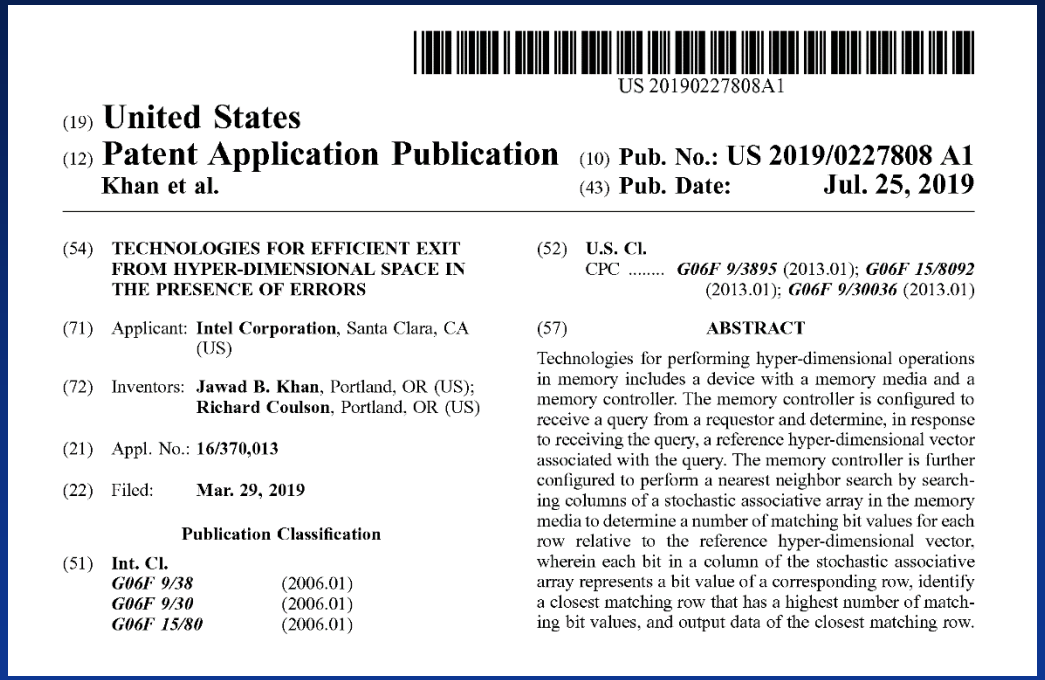
Patent Applications of Note:

US 2019/0227808 A1
Filed: Mar. 29, 2019
Published: July 25, 2019:

"TECHNOLOGIES FOR EFFICIENT EXIT FROM HYPER-DIMENSIONAL SPACE IN PRESENSE OF ERRORS"

Applicant: Intel Corporation, Santa Clara, CA

Enables "Hyperdimensional" operations



US 20190227808A1

(19) **United States**

(12) **Patent Application Publication**
Khan et al.

(10) **Pub. No.: US 2019/0227808 A1**
(43) **Pub. Date: Jul. 25, 2019**

(54) **TECHNOLOGIES FOR EFFICIENT EXIT FROM HYPER-DIMENSIONAL SPACE IN THE PRESENCE OF ERRORS**

(71) Applicant: **Intel Corporation**, Santa Clara, CA (US)

(72) Inventors: **Jawad B. Khan**, Portland, OR (US); **Richard Coulson**, Portland, OR (US)

(21) Appl. No.: **16/370,013**

(22) Filed: **Mar. 29, 2019**

Publication Classification

(51) **Int. Cl.**

G06F 9/38	(2006.01)
G06F 9/30	(2006.01)
G06F 15/80	(2006.01)

(52) **U.S. Cl.**
CPC ***G06F 9/3895*** (2013.01); ***G06F 15/8092*** (2013.01); ***G06F 9/30036*** (2013.01)

(57) **ABSTRACT**

Technologies for performing hyper-dimensional operations in memory includes a device with a memory media and a memory controller. The memory controller is configured to receive a query from a requestor and determine, in response to receiving the query, a reference hyper-dimensional vector associated with the query. The memory controller is further configured to perform a nearest neighbor search by searching columns of a stochastic associative array in the memory media to determine a number of matching bit values for each row relative to the reference hyper-dimensional vector, wherein each bit in a column of the stochastic associative array represents a bit value of a corresponding row, identify a closest matching row that has a highest number of matching bit values, and output data of the closest matching row.

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Related Intel Patent Applications:

CONDUCTIVE BRIDGE RANDOM ACCESS MEMORY (CBRAM) DEVICES WITH LOW THERMAL CONDUCTIVITY ELECTROLYTE SUBLAYER

Patent Application Publication No.: US 2019/0229264 Al

Applicant: Intel Corporation, Santa Clara, CA

KARPOV et al

Pub. Date: Jul. 25, 2019

PCT Filed: Sep. 30, 2016

TECHNOLOGIES FOR EFFICIENT STOCHASTIC ASSOCIATIVE SEARCH OPERATIONS

Patent Application Publication No.: US 2019/0220230 Al

Applicant: Intel Corporation, Santa Clara, CA

Khan et al.

Pub. Date: Jul. 18, 2019

Filed: Mar. 28, 2019

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Hyperdimensional Computing | Robotic Application

"Learning sensorimotor control with neuromorphic sensors: Toward hyperdimensional active perception"

A. Mitrokhin*, P. Sutor*†, C. Fermüller, Y. Aloimonos

Department of Computer Science, University of Maryland, College Park, MD., 20742, USA

- Dynamic Sensor Fusion – Perception to Motoric output
- Hyperdimensional Binary Vectors (HBVs) and the notion of facilitating Hyperdimensional Active Perception (HAP)
- image, video, motion sequence, control sequence, concept, word, or sound, the "center" is represented by an associated HBV

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MemComputing - (MemCPU)
Digital MemComputing Machines

Massimiliano Di Ventra, UCSD: Memcomputing: leveraging memory and physics to compute efficiently

https://www.youtube.com/watch?v=eN-4aO6TLZQ

(UC Berkeley EECS Events Streamed live on Apr 24, 2019)

- Universal MemComputing Machines
- Working on the concept of a "Quantum Memristor"
- "Self Organizing Logic Gates"
- Solutions to NP (Hard) Problems in Poly Time
- Topologically robust due to use of Instantons in Phase Space
- Experimenting with ML Optimization of Quantum Hamiltonians

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Thank You…,

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