

Exploiting Managed Language Semantics to Mitigate Wear-out in Persistent Memory

Shoaib Akram Ghent University, Belgium



Main memory capacity expansion

Charge storage in **DRAM** a scaling limitation

ડ્ર 0.9 Manufacturing complexity makes Price/Gb 0.8 **DRAM** pricing 0.7 volatile Source: WSTS, IC Insights 0.6 Jan'17 Jan'18



Phase change memory (PCM)

Scalable \rightarrow More Gb for the same price

Byte addressable like DRAM

Latency closer to DRAM

🕑 Low write endurance



Why PCM has low write endurance?

Electric pulses to program PCM cells wear them out over time temperature



time



Hybrid DRAM-PCM memory

PCM alone as a DRAM replacement wears out in a few months for popular Java applications



Capacity Persistence		





Wear-leveling to spread writes across PCM This talk \rightarrow Use DRAM to limit PCM writes



OS to limit PCM writes



DRAM

PCM

Coarse-grained page migrations hurt application performance and PCM lifetime



Managed runtimes

Platform independence Abstract hardware/OS → Aka Virtual Machine

Ease programmer's burden Garbage collection Security





GC to limit PCM writes

GC understands memory semantics

GC approaches are *pro-active* and *fine-grained*

Application





Operating System

Hardware



Write Distribution in GC heap



70% of writes



Write Distribution in GC heap



70% of writes





Write-Rationing Garbage Collection

Limit PCM writes by discovering highly written objects



Kingsguard dynamically monitor writes



Kingsguard-Nursery (KG-N)















PCM





Overhead of dynamic monitoring

Limited time window to predict write intensity

Excessive & fixed DRAM consumption



Write-Rationing Garbage Collection

Limit PCM writes by discovering highly written objects



Kingsguard dynamically monitor writes



Crystal Gazer statically profiles objects



Allocation site as a write predictor



Uniform distribution 😟 Skewed distribution 🙂



Santa Clara, CA

Write distribution by allocation site

Few sites capture majority of writes





Crystal Gazer operation







Goal: Generate <alloc-site, advice> pairs advice → DRAM or PCM input is a write-intensity trace

Two heuristics to classify allocation sites as DRAM or PCM



Freq: A *threshold* % of objects from a site get more than a *threshold* # writes \rightarrow DRAM

Aggressively limits PCM writes No distinction based on object size

No distinction based on object size



Write density \rightarrow Ratio of # writes to object size

Dens: A *threshold* % of objects from a site have more than a *threshold* write density \rightarrow DRAM



Classification thresholds

Homogeneity threshold $\rightarrow 1\%$

- Frequency threshold $\rightarrow 1$
- Density threshold $\rightarrow 1$



Frequency threshold = 1 PCM writes = ?, DRAM bytes = ?

Object Identifier	# Writes	# Bytes	Allocation site
01	0	4	A() + 10
02	0	4	A() + 10
03	128	4	A() + 10
04	128	4096	B() + 4



Frequency threshold = 1 PCM writes = ?, DRAM bytes = ?

	Object Identifier	# Writes	# Bytes	Allocation site
	01	0	4	A() + 10
	02	0	4	A() + 10
>	03	128	4	A() + 10
>	04	128	4096	B() + 4



Frequency threshold = 1 PCM writes = 0/256, DRAM bytes = 5008

	Object Identifier	# Writes	# Bytes	Allocation site
	01	0	4	A() + 10
	02	0	4	A() + 10
>	03	128	4	A() + 10
>	04	128	4096	B() + 4



Density threshold = 1 PCM writes = ?, DRAM bytes = ?

Object Identifier	# Writes	# Bytes	Allocation site
01	0	4	A() + 10
02	0	4	A() + 10
03	128	4	A() + 10
04	128	4096	B() + 4



Density threshold = 1 PCM writes = ?, DRAM bytes = ?

Object Identifier	# Writes	# Bytes	Allocation site	
01	0	4	A() + 10	
02	0	4	A() + 10	
03	128	4	A() + 10	→ 32
04	128	4096	B() + 4	



Density threshold = 1 PCM writes = ?, DRAM bytes = ?

Object Identifier	# Writes	# Bytes	Allocation site	
01	0	4	A() + 10	
02	0	4	A() + 10	
03	128	4	A() + 10	
04	128	4096	B() + 4] –



Density threshold = 1 PCM writes = 128/256, DRAM bytes = 12

Object Identifier	# Writes	# Bytes	Allocation site
01	0	4	A() + 10
02	0	4	A() + 10
03	128	4	A() + 10
04	128	4096	B() + 4



Object placement in Crystal Gazer

new_dram() → Set a bit in the object header

$GC \rightarrow$ Inspect the bit on nursery collection to copy object in DRAM or PCM





Key features of Crystal Gazer

Eliminates overhead of dynamic monitoring

Less mispredictions due to pro-active nature

Pareto optimal trade-offs b/w capacity and lifetime



Evaluation methodology

15 Applications → DaCapo, GraphChi, SpecJBB

Medium-end server platform

Different inputs for production and advice

Jikes **RVM**



Emulation platform









PCM-Only write rate is above 1 GB/s on average

Safe operation is 200 MB/s



PCM write rates KG-N KG-W Dens Freq Write rate in MB/s 800 600 400 200 0 Average usaldb talar productipse Page Rant comp Fact *6.100*



Execution time





KG-W versus Crystal Gazer





KG-W versus Crystal Gazer

writes

 \sum

Crystal Gazer opens up Pareto-optimal trade-offs

DRAM capacity in MB

250



Write-rationing garbage collection

Hybrid memory is inevitable

All layers can contribute to manage hybrid memory



DRAM

Write-rationing GC is pro-active and fine-grained

