

# Update XP ReRAM Technology

# Amigo Tsutsui Sony Semiconductor Solutions Corp

Santa Clara, CA August 2019



### **Cross Point ReRAM**



#### <u>ReRAM</u>

- Mechanism
- Program
- On/Off state
- Endurance
- Retention
- Scaling

### <u>Selector</u>

- Mechanism
- On/Off current :
- Endurance
- Scaling

- : Conductive Bridge type
- : 50uA
- : LRS Low R State ~10kohm
- : HRS High R State >10Mohm
- : 1M cyc
- :>10 yrs @55C
- : Confirmed down to 10nm

- : OTS (Ovonic Threshold Switch)
- rrent : 50uA / ~5nA@75% bias
  - : 100M cyc
  - : Confirmed down to 10nm



### **Memory Cell IV-Curve**





## **Memory Cell Operation**



Santa Clara, CA August 2019



Santa Clara, CA August 2019

Vset

7

Set fail



# **Read-induced Overset**

ReRAM LRS		Data	Effect
	Weak Set ~100Kohm	0 or 1	Somewhere in between HRS and LRS due to poor set. This failure can be detected by voltage sense amp.
	Normal Set ~10Kohm	1	
	Overset ~Kohm	1	Deeply overset by multiple read stress which lead to Reset failure. Prevention scheme such as "Reset and Set after multiple read" is needed.







Need a special controller technology

- Selector Drift
- Read-induced overset