The Composable Platform: Enabling Innovation Through Flexible Infrastructure

FREEDOM TO INNOVATE

Andrew Dieckmann, VP Marketing & Applications
Data Center Solutions Division

microchip.com

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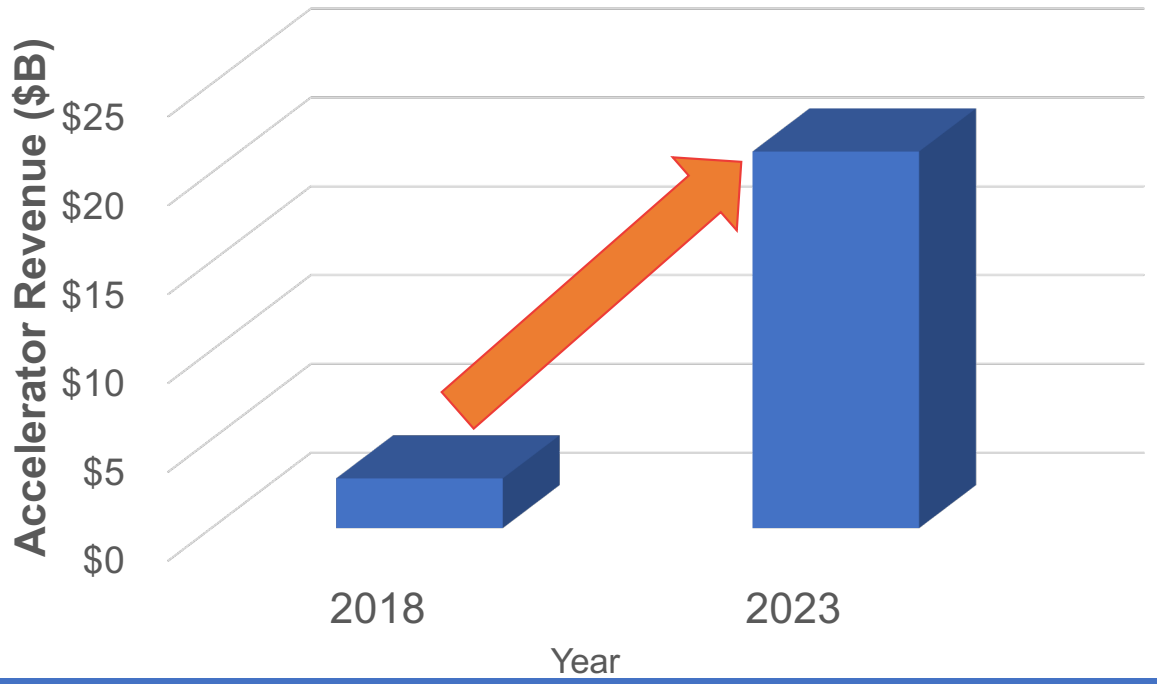
one size fits
NONE

2018: >$140B

Accelerator Spending is Exploding



50% CAGR end-market growth; >$20B market in 2023

Accelerator Efficiency Challenges

IO Bandwidth Constrained

Workload-dependent optimizations for resources

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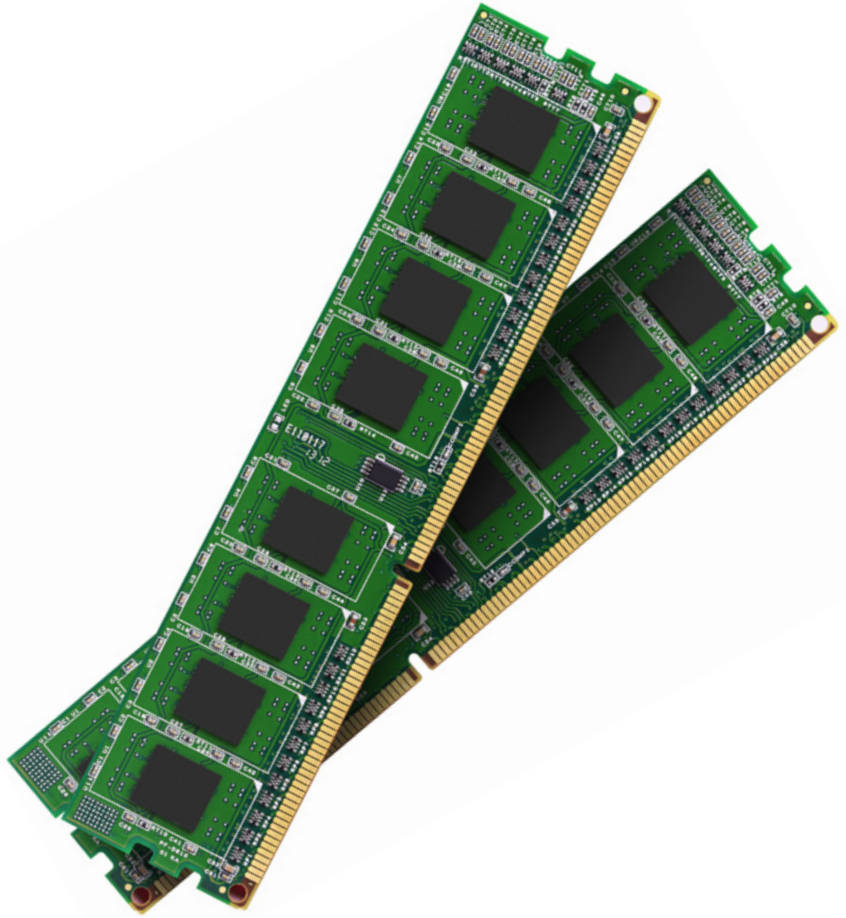
Workload-dependent optimizations for resources

The Cost of Memory

- > $20B in DRAM purchased by data centers in 2019…
- Much of this DRAM is.. **not being used**… stranded in machines with workloads not requiring it
- Not only a capex problem; DRAM consumes 15-20% of the data center power!



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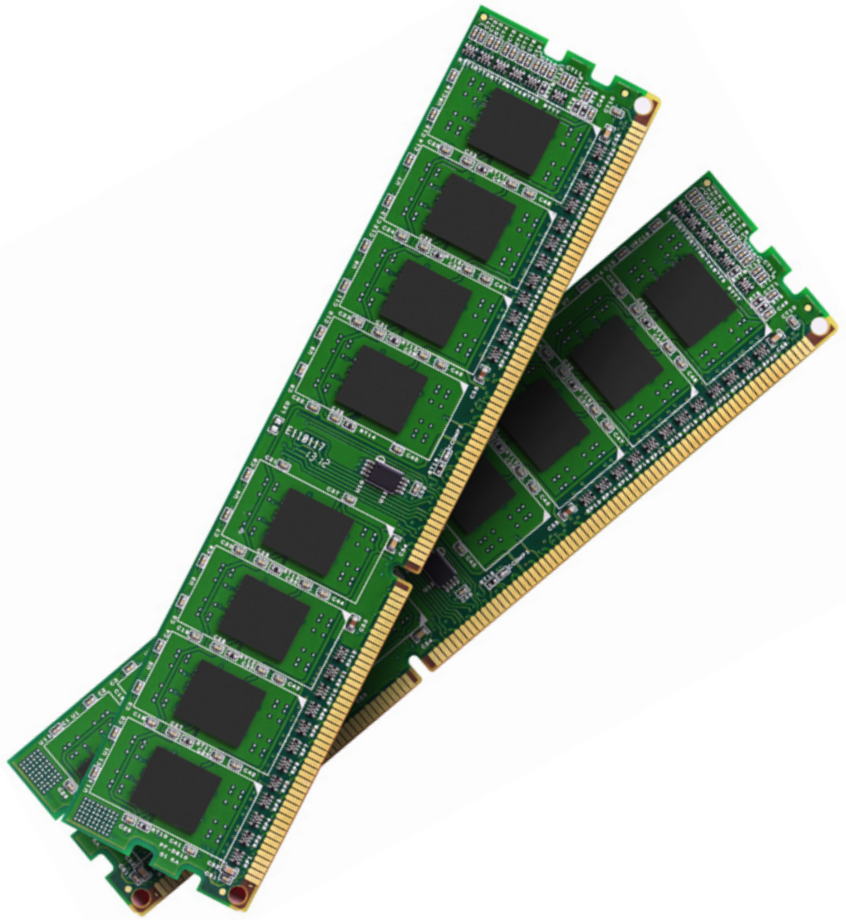
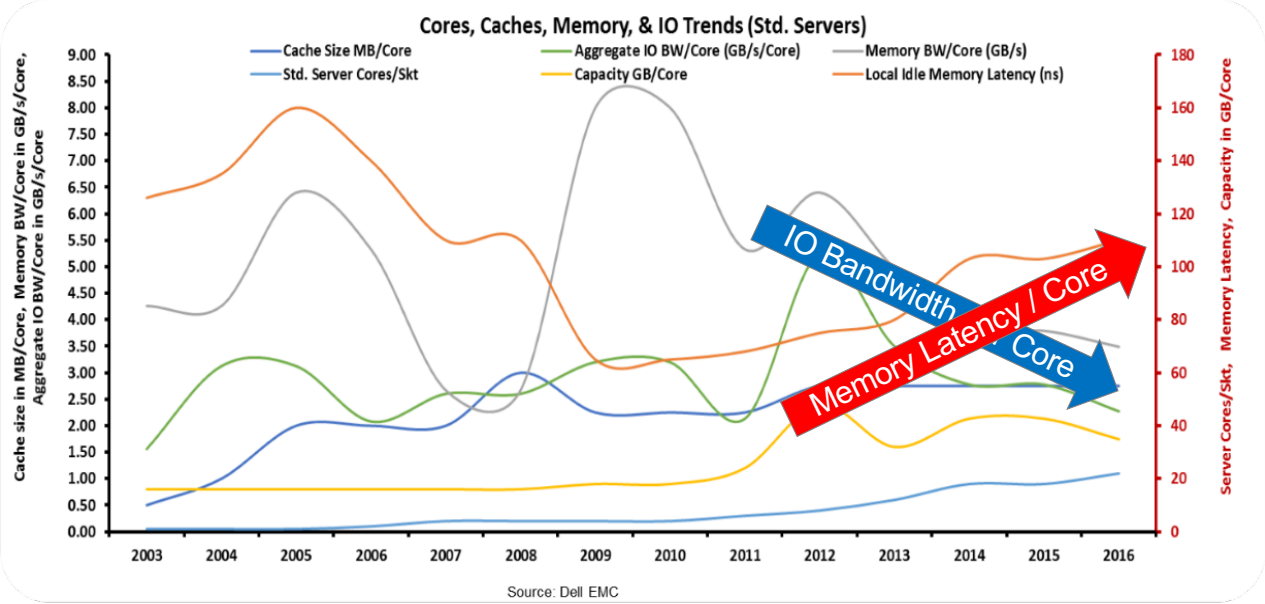


Memory Bandwidth & Latency Bottlenecks

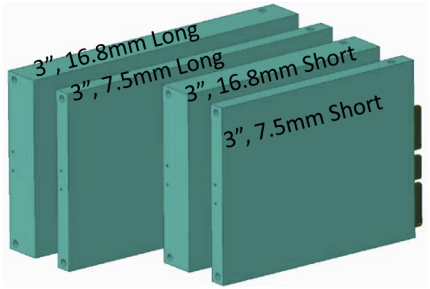


https://blog.dellemc.com/en-us/memory-centric-architecture-vision/

CPU DRAM buses are limited in quantity and performance
Multi-core processor memory latency is increasing

Many Types of Storage Media

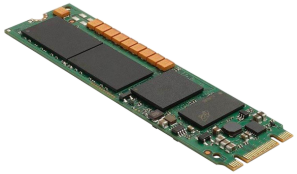
PCIe Cards



EDSFF

U.2 & U.3

Enterprise 3.5" HDD



M.2

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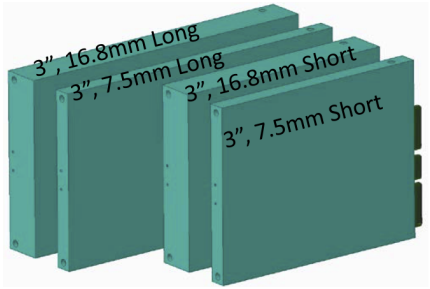

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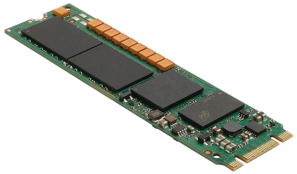

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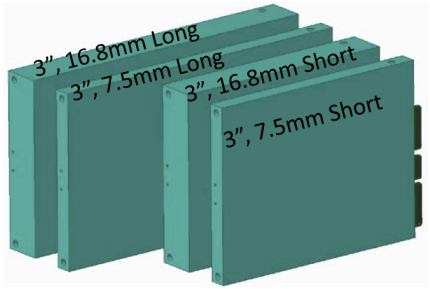

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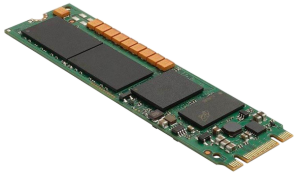

M.2

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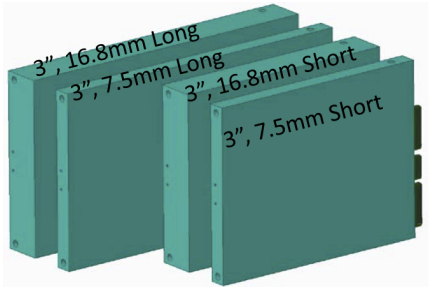

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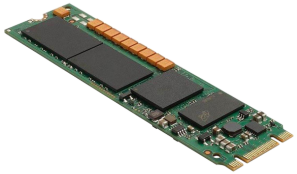

M.2

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Drive Capacities are Growing

1. We are wasting Billons of dollars on **under-utilized** storage, memory and compute resources

2. Rapid innovation in the data center requires **flexible infrastructure**

Flexible Infrastructure

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Flexible Infrastructure


Stop the Madness!!
There must be a better way!

Agile Infrastructure

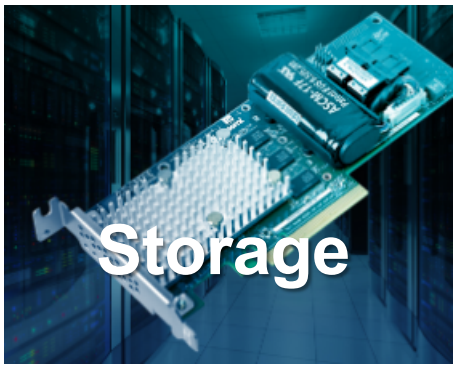
Composable ←→ Flexible

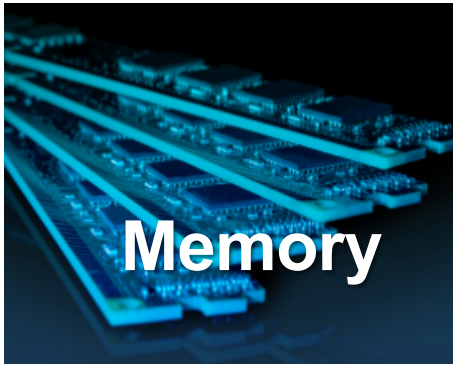
Agile Infrastructure

Composable ←→ Flexible

Innovation Required for Agile Infrastructure

- ***Composable*** storage accelerators & memory
- Optimized resources by workload
- No resource stranding
- Remove BW bottlenecks





Innovation Required for Agile Infrastructure

- ***Composable*** storage accelerators & memory
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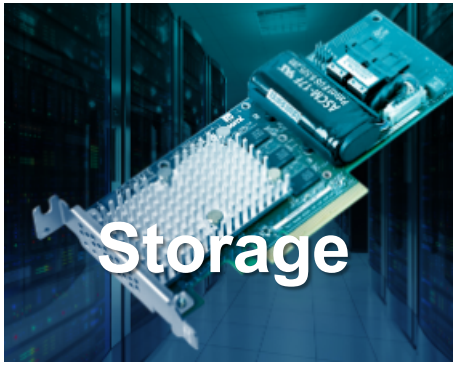
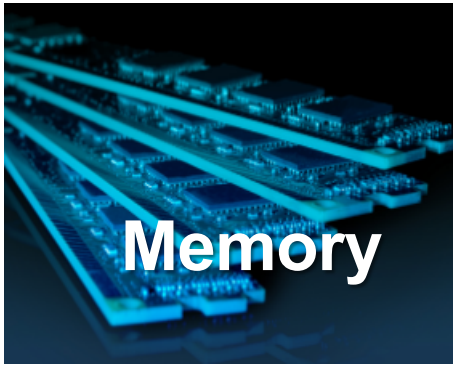
- ***Adaptable*** memory and storage technology
- Memory bandwidth scaling



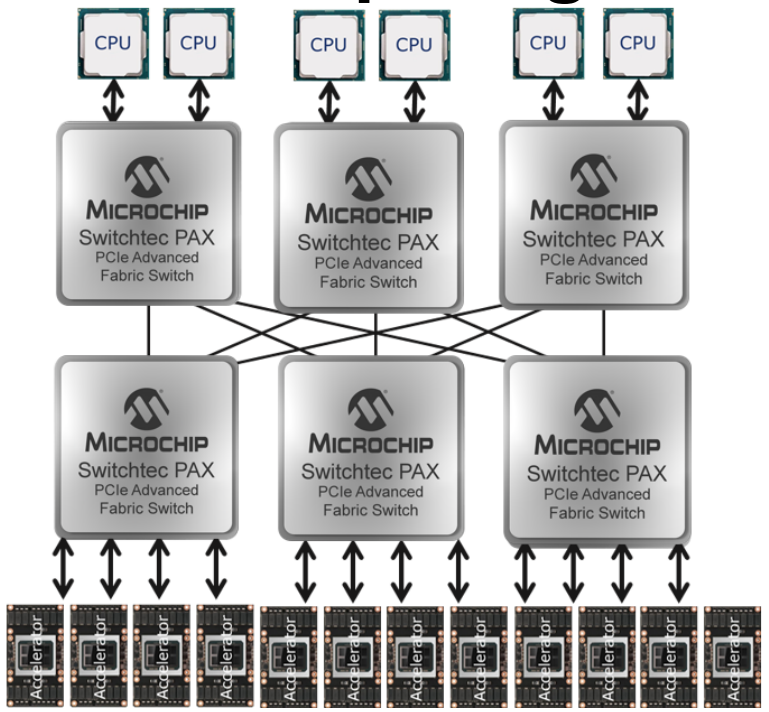


Increased GPU Utilization

Switchec™ PAX Advanced Fabric Switches enable

Composable Heterogeneous Computing

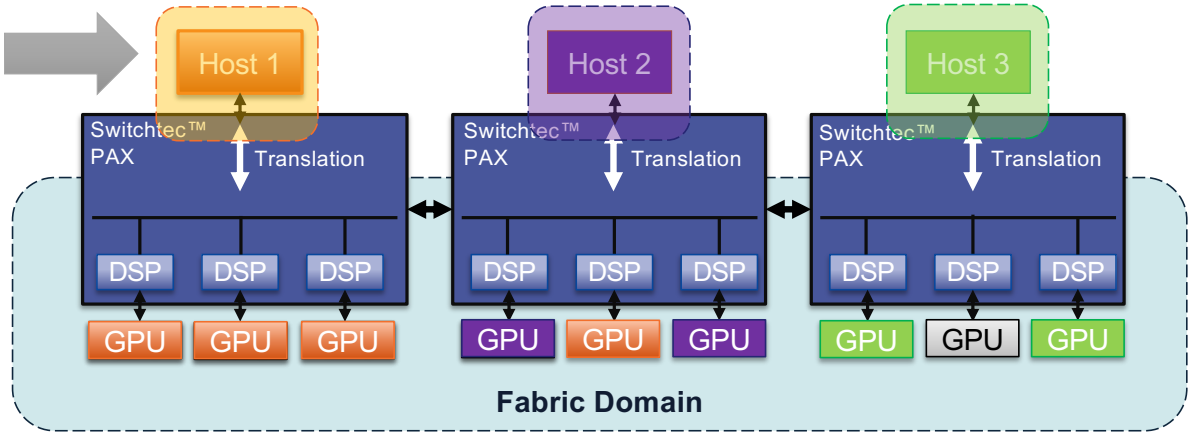
- **Scalable non-hierarchical fabric**
- **Dynamic end-point allocation**
- **Low latency data transfers**
- **..using standard drivers**



Switchtec™ PCIe Fabrics

The Switchtec PCIe fabric is built on the concept of **virtual domains**

Firmware-Virtualized Host Domains



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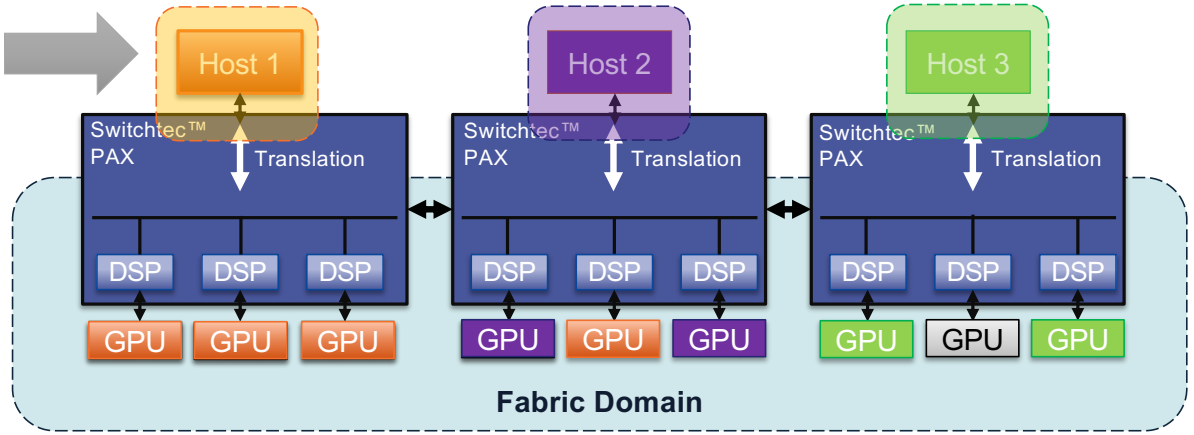

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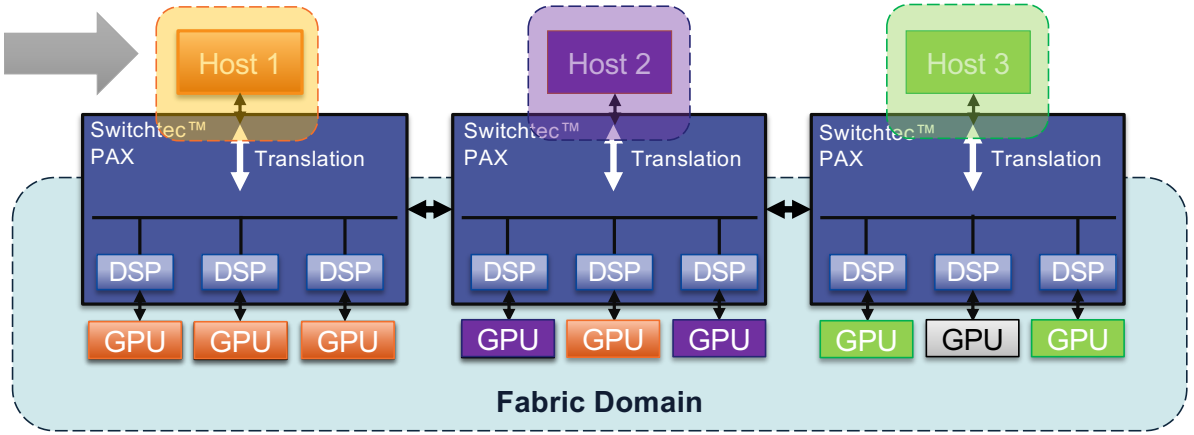
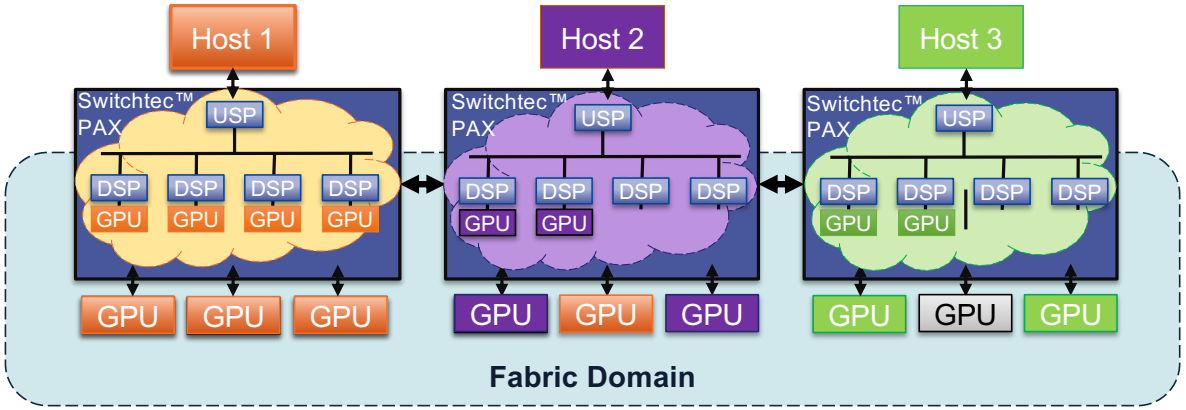


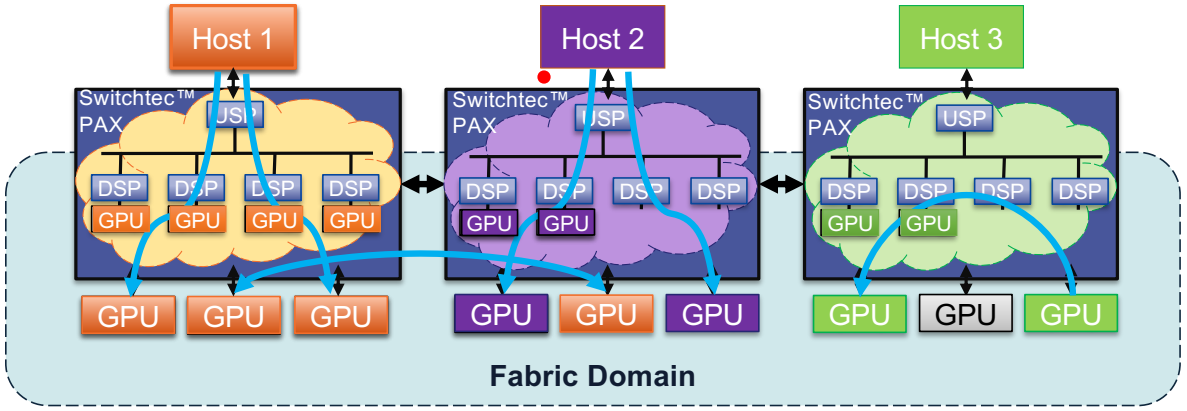
Increased GPU Utilization with PCIe Fabrics

- Embedded CPUs in each fabric element are the virtualizers
  - Each virtual domain is a **PCIe-compliant virtual switch**



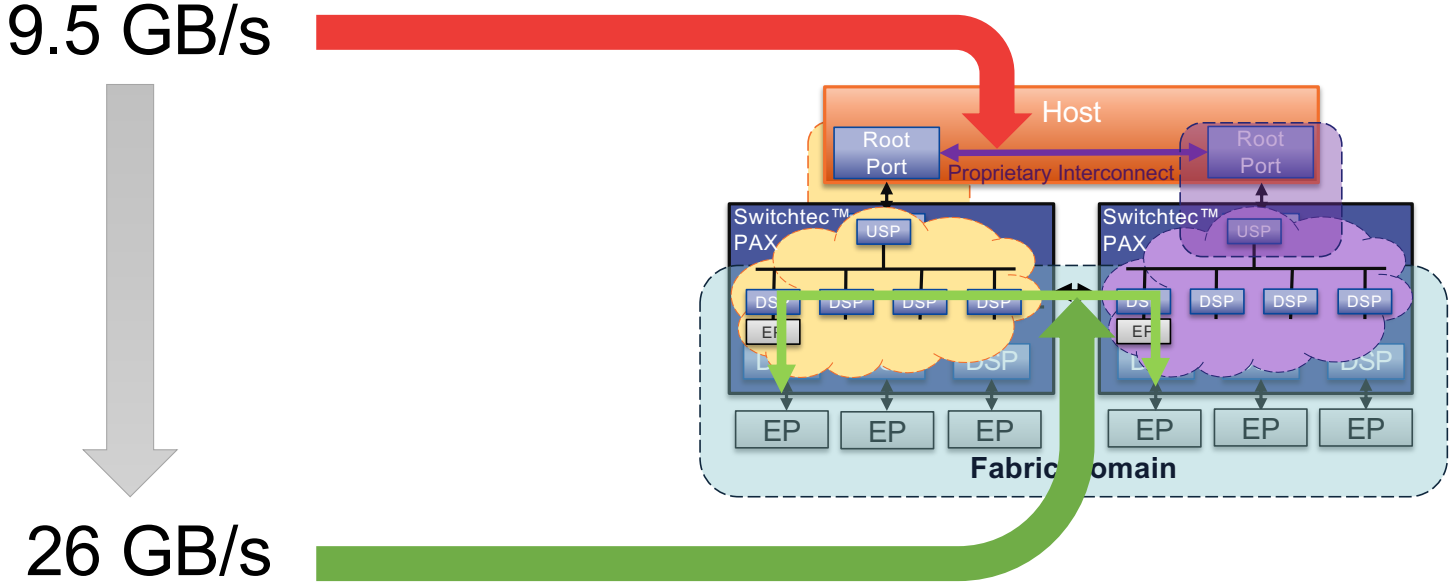
Increased GPU Utilization with PCIe Fabrics

- Data is routed directly by switch hardware
- **Peer-to-peer transfers** supported through the fabric



Removing IO Bottlenecks with Switchtec™

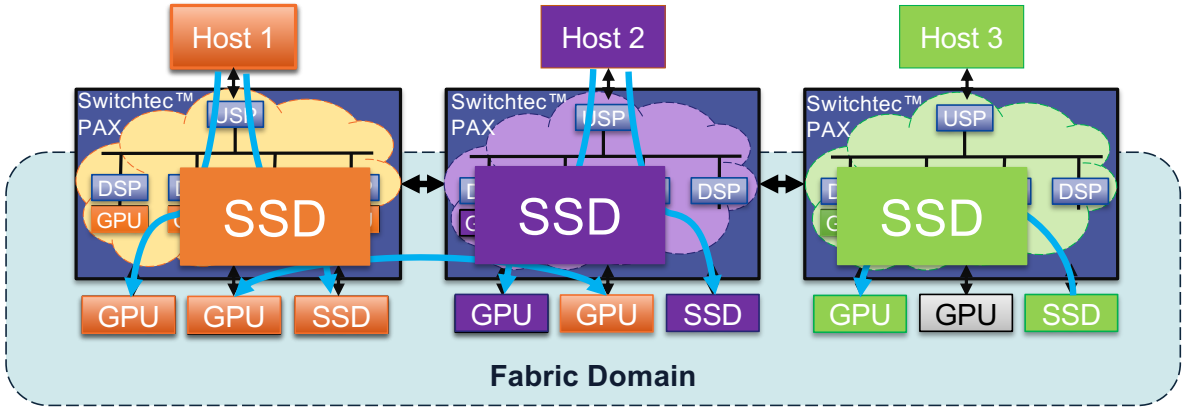
Peer-to-peer traffic through a fabric decreases congestion due to bypass of CPU to CPU interconnect



2.5x increase in bandwidth in 2 socket system

Composable Storage with PCIe Fabrics

- PCIe Fabric model is extensible to NVMe SSDs & other PCIe endpoints
  - End points are added to the fabric just like a spec-compliant GPU
    - Storage is now a flexible resource



Switchtec™ PAX enables

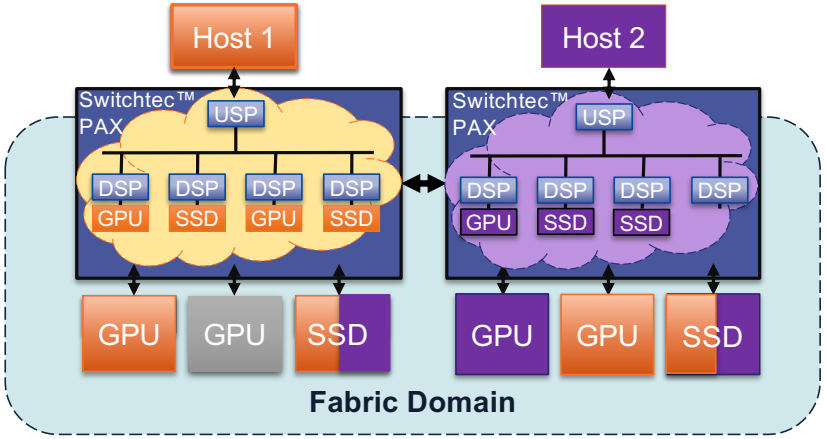
Composable Heterogenous Compute & Storage

No More Stranded Storage

SR-IOV and multi-host sharing provide for new granularity in composable heterogenous compute and storage

Switchtec™ + Flashtec™ provide end-to-end
Multi-Host IO Virtualization with off-the-shelf drivers

- >8 NVMe SR-IOV vendors
- Leading GPU vendors support SR-IOV
- NVMe SR-IOV standardization complete



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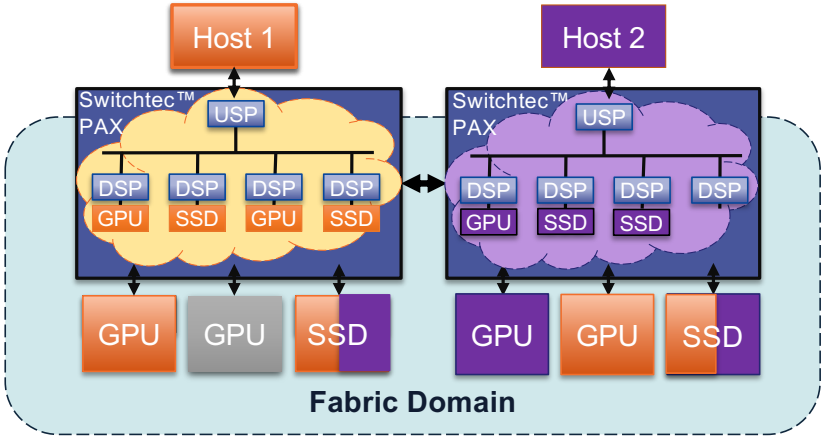
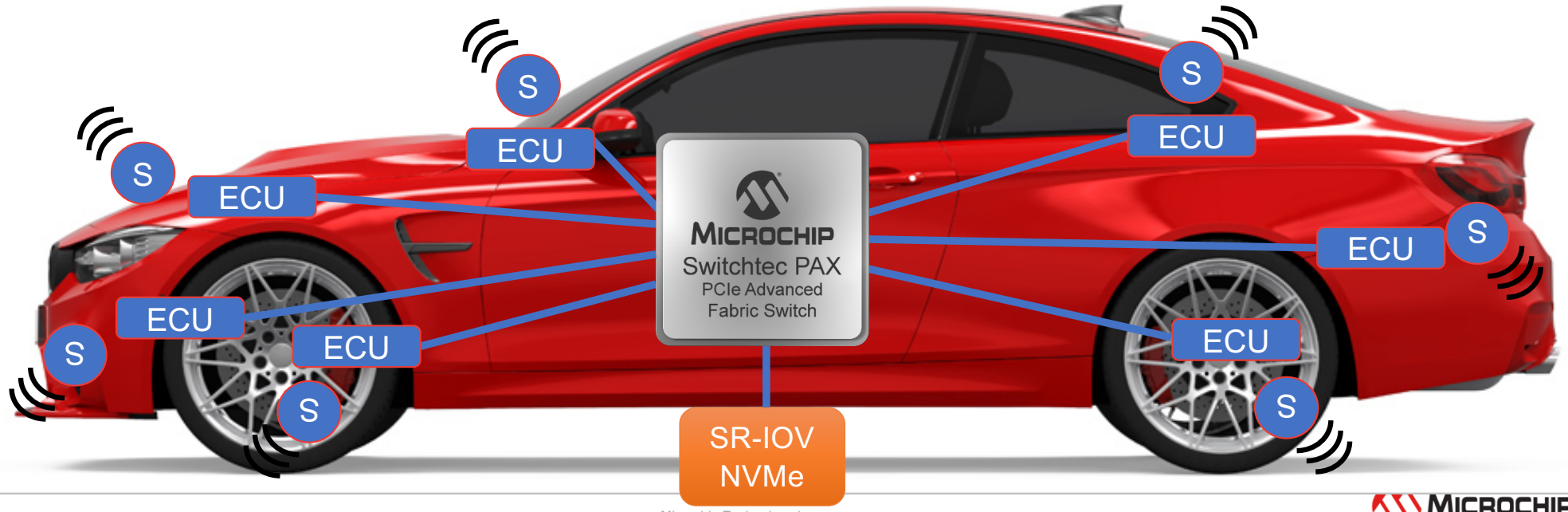
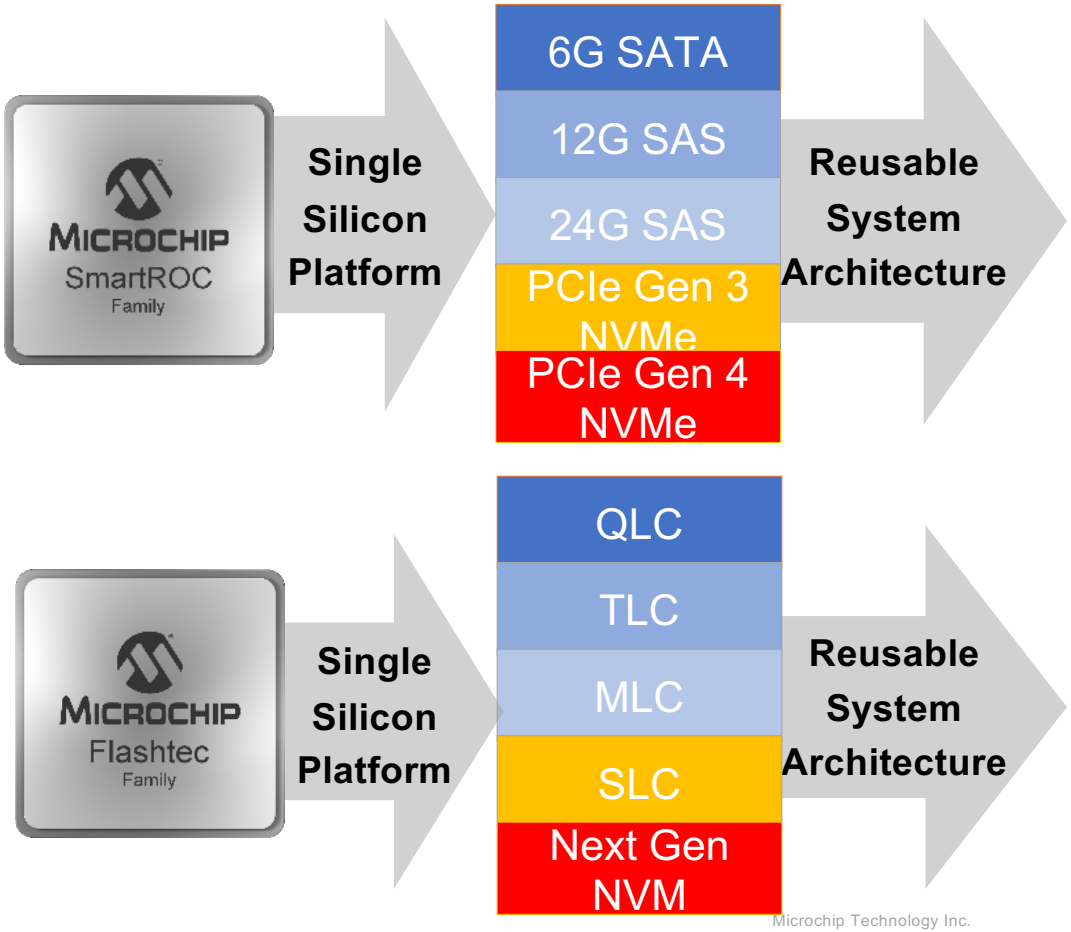


Virtualization Will Be Everywhere

- Many use cases even beyond the Data Center
- Example: Autonomous Driving



Flexibility Building Block Platforms



Hyperscale:

- Compute Servers (NVMe)
- Balanced Servers (Mix)
- Cold Storage (SAS/SATA)

Enterprise:

- Universal Bay Servers (Mix)

Many form factors, many performance points:

- U.2, M.2, EDSFF, Custom
- Performance & Mainstream
- Up to 8GB/s+ bandwidth
- Up to 200TB+ capacity

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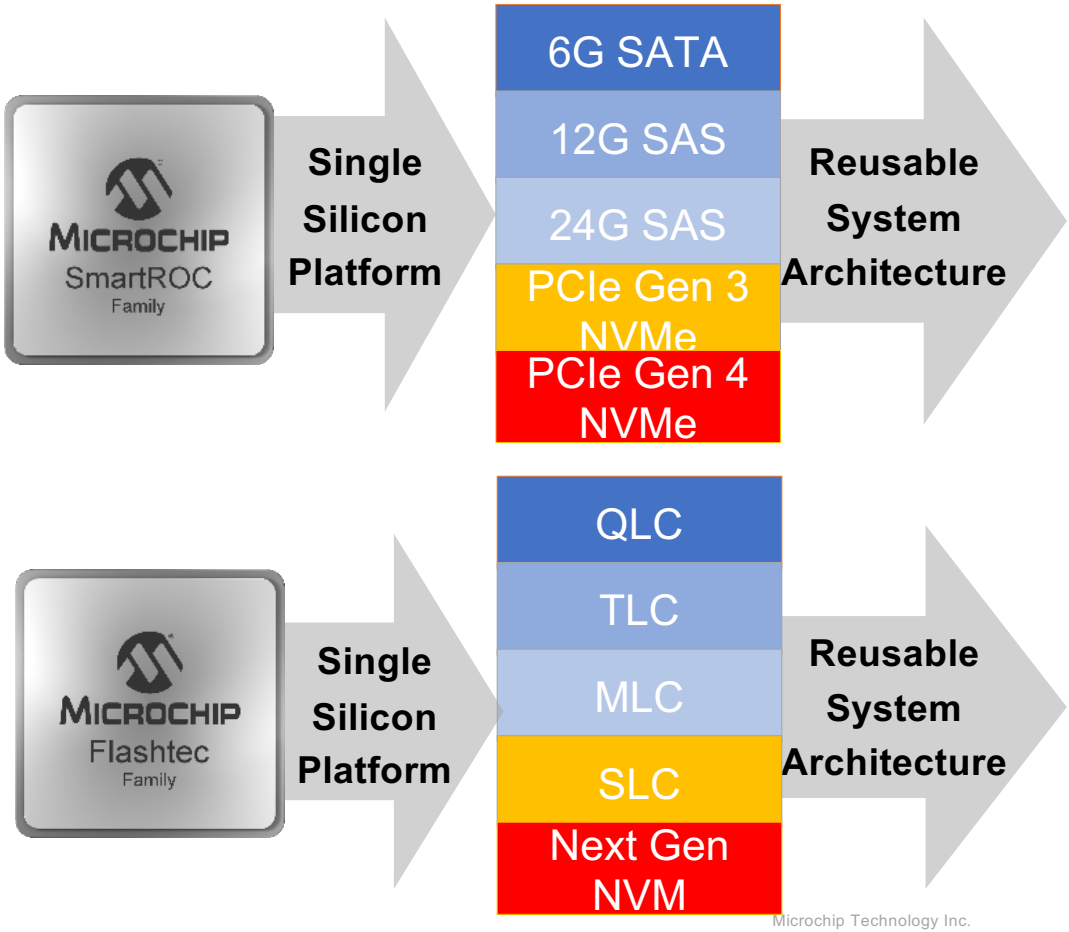

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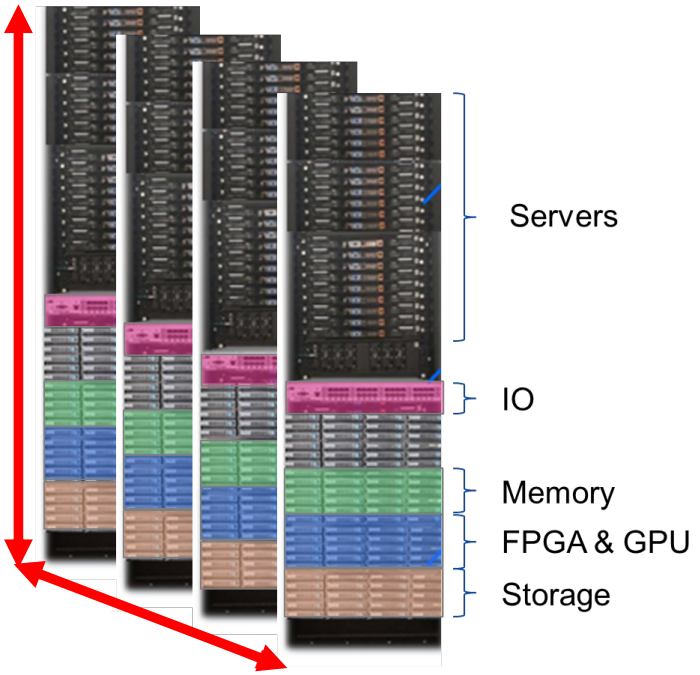
Composable Memory Infrastructure

- **Near memory innovation**
  - Serialization of the memory
- **Far memory innovation**
  - Sharing pools of resources to reduce stranding
- **New open load/store standards** provide the low-latency connectivity required



CXL Compute Express Link GEN Z OpenCAPI™

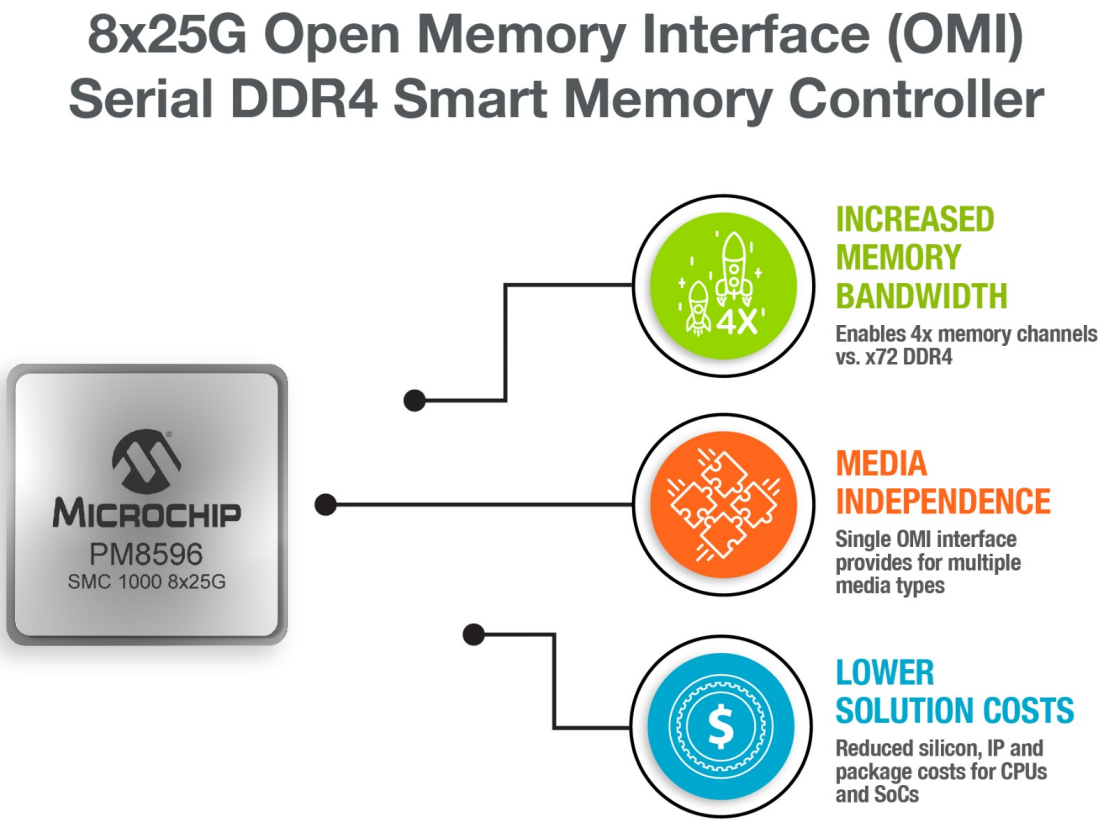
High-Bandwidth Memory Solution – SMC 1000

Microchip Enters Memory Infrastructure Market with Serial Memory Controller for High-performance Data Center Computing

SMC 1000 8x25G enables high memory bandwidth required by next-generation CPUs and SoCs for AI and machine learning

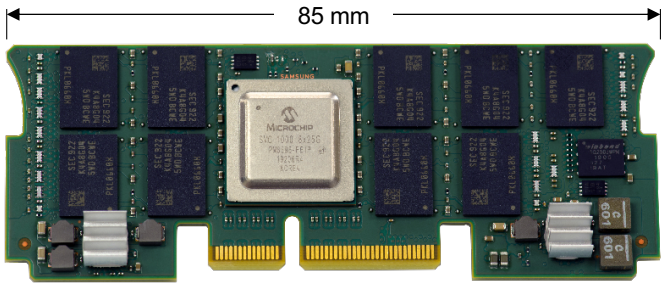
PRESS RELEASE

SMC 1000 Smart Memory Controller

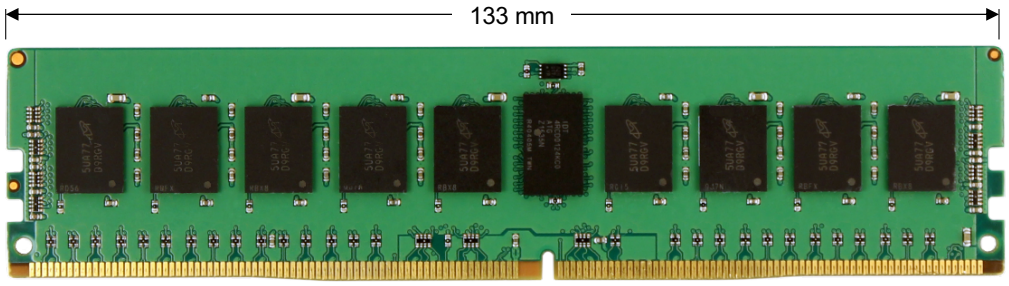


OMI-Enabled DDIMMs are Here!

The SMC 1000 8x25G available on standards-based DDIMMs in 1U and 2U:



1U DDIMM



Traditional RDIMM

Available from Micron, Samsung Electronics, and SMART Modular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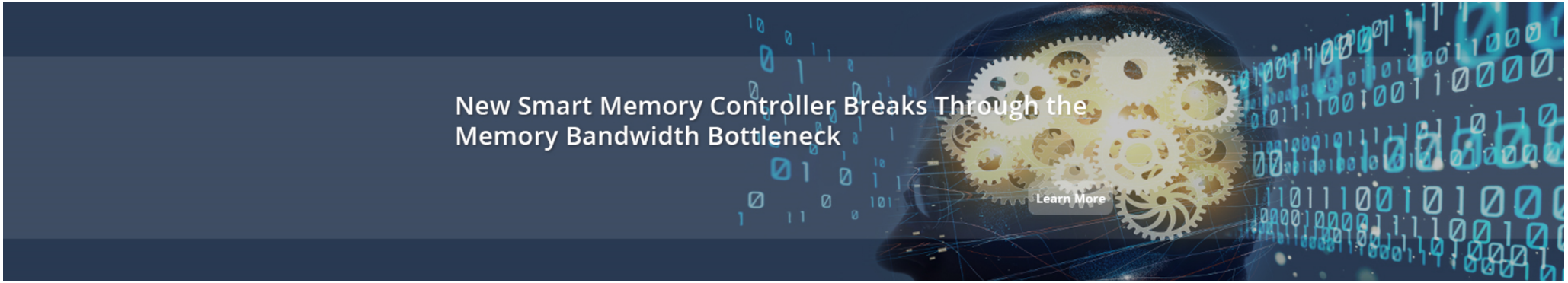
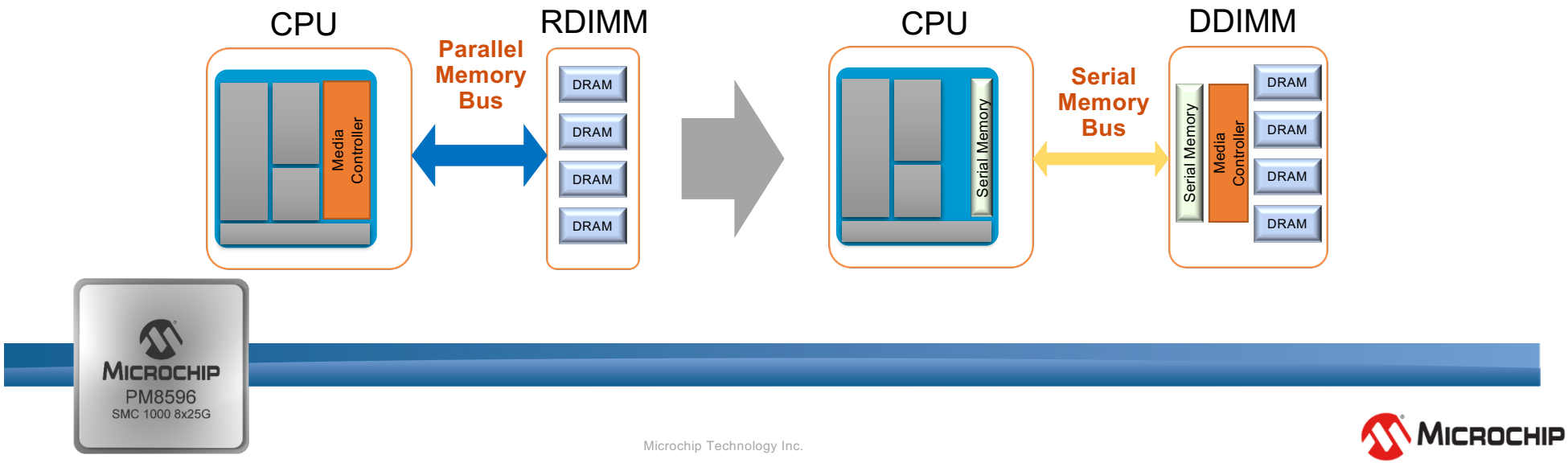
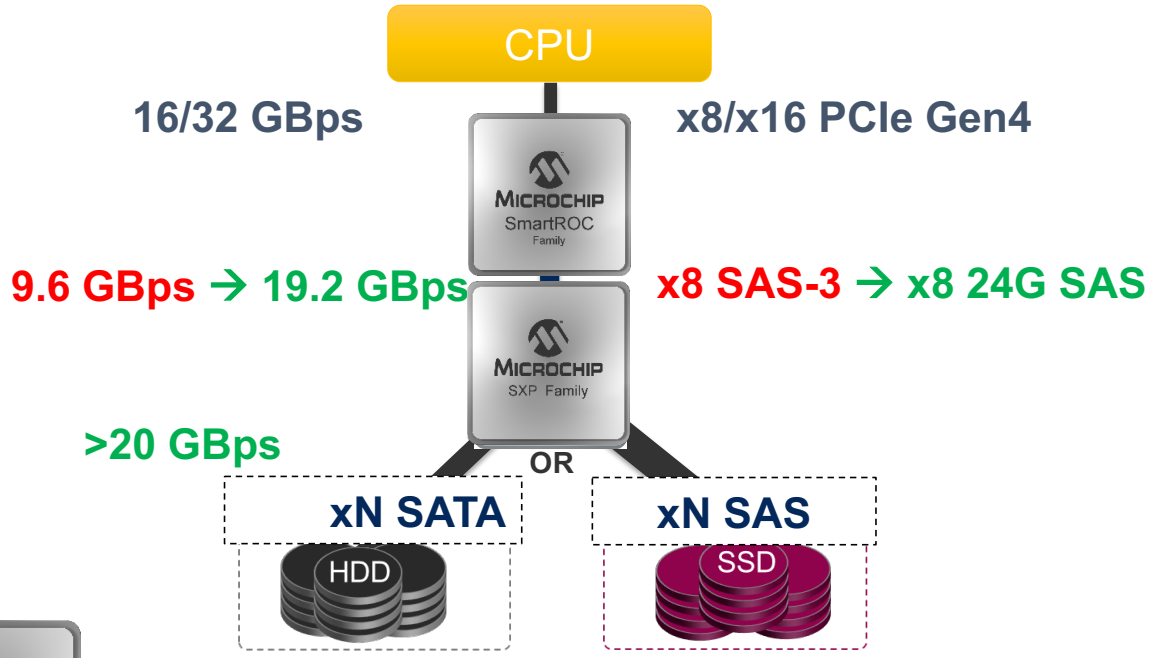
See a Live Demo of the Future of Memory

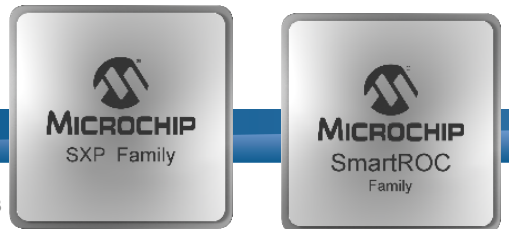




Live Demo: 24G SAS + Dynamic Channel Multiplexing

Unleash the Bandwidth of PCIe Gen 4 Infrastructure

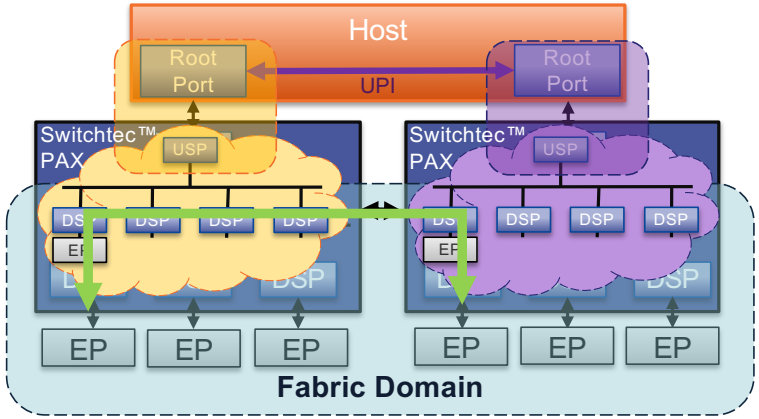




Boost GPU to Storage Transfer Rates with PAX

7x

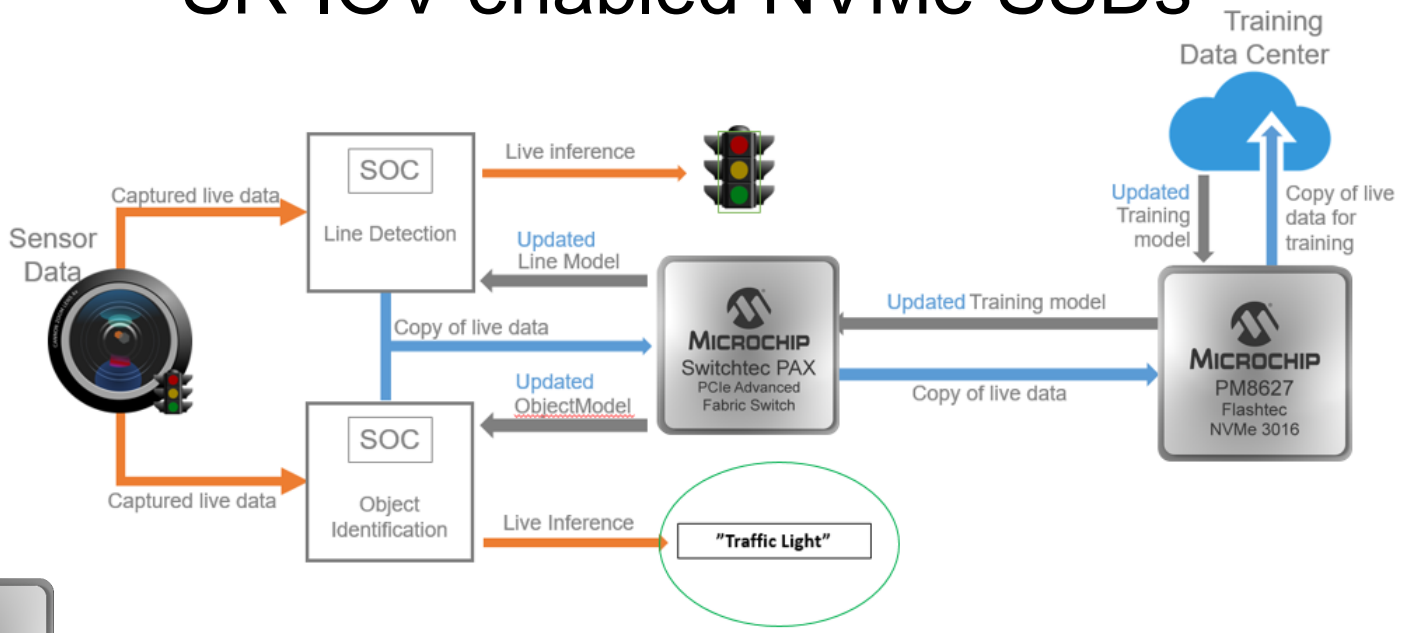
Increase in GPU to Storage Transfer Rates



MICROCHIP
Switchtec PAX
PCIe Advanced
Fabric Switch

Machine Learning Benefits from Shared Storage

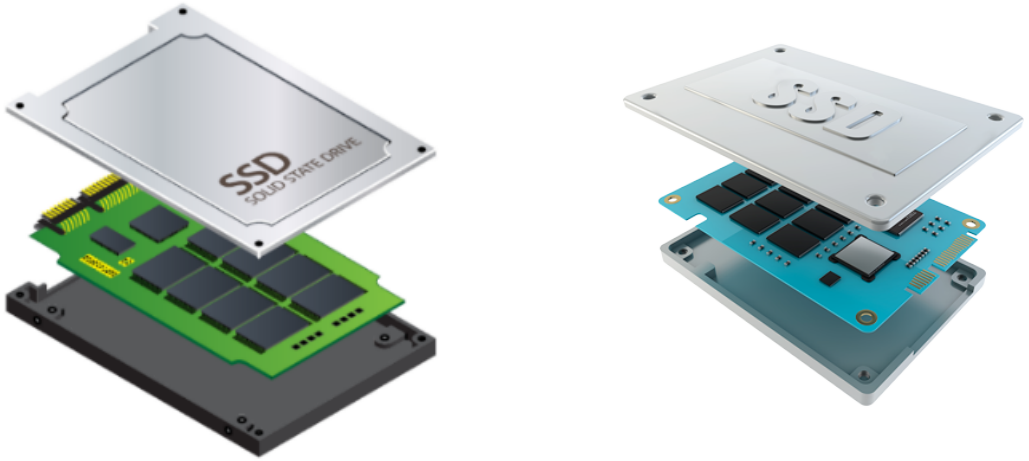
Machine Inference with Switchtec™ and SR-IOV enabled NVMe SSDs



MICROCHIP
Switchtec PAX
PCIe Advanced
Fabric Switch

Flashtec™ PCIe Gen 4 NVMe Controller

The world's highest performance and most flexible PCIe Gen 4 NVMe SSD controller family



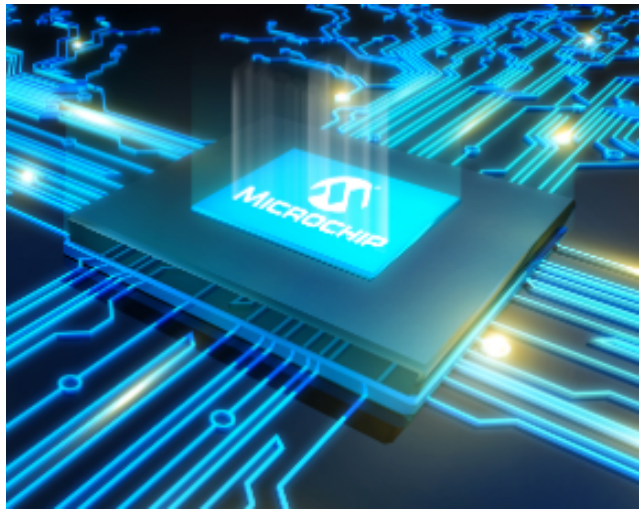
MICROCHIP
PM8627
Flashtec
NVMe 3016

Microchip Data Center Solutions

Connecting, managing and securing the world's information

Storage

Memory



Compute

Thank You