Accelerating Converged System Performance with FPGA-Based Switches

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Acknowledgment

This represents work done by many people within Achronix, especially from the Strategy and Planning organization

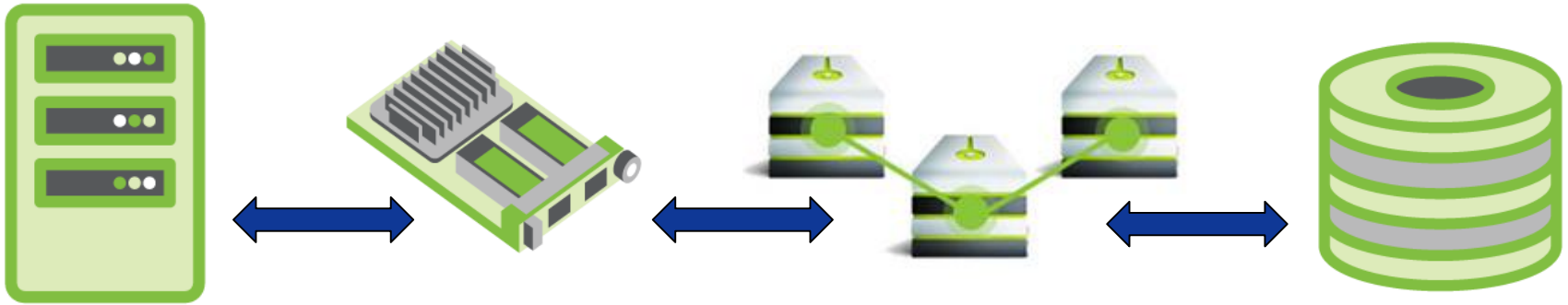
Motivation

- Data center storage demand is growing exponentially
  - Capacity, bandwidth, flexibility
- Storage moving out into the network
  - NVMe-oF, FC-NVMe
- Computational storage gaining momentum
  - Moving work from the server to storage

Network and Storage Convergence

- Look for opportunities to optimize in the evolving storage ecosystem
- To continue TCO scaling, requires holistic approach

System Architecture

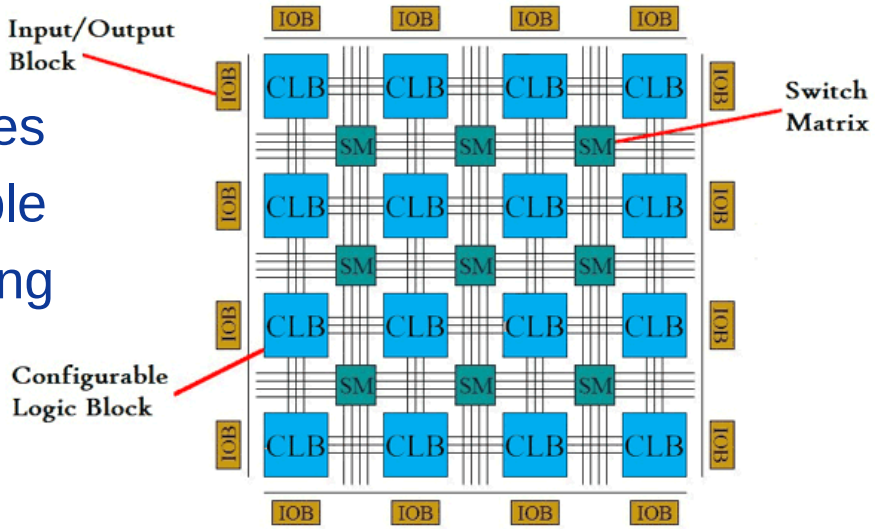


Opportunities for Optimization

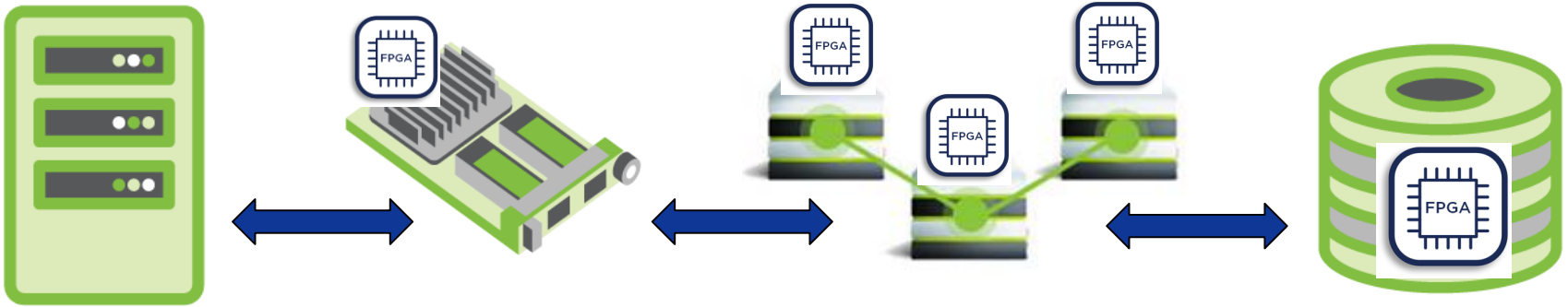
- NICs
  - More work offloading from server processors to NIC
- Network switches
  - Opportunities while all the data is moving through
- Storage nodes
  - More computational capacity
  - Move work to the data

FPGAs for Dataplane Acceleration

- FPGAs provide a flexible building block for dataplane accelerators
  - Efficient direct dataflow pipelines
  - Reconfigurable and upgradeable
  - Partial reconfiguration for loading accelerator cores on demand

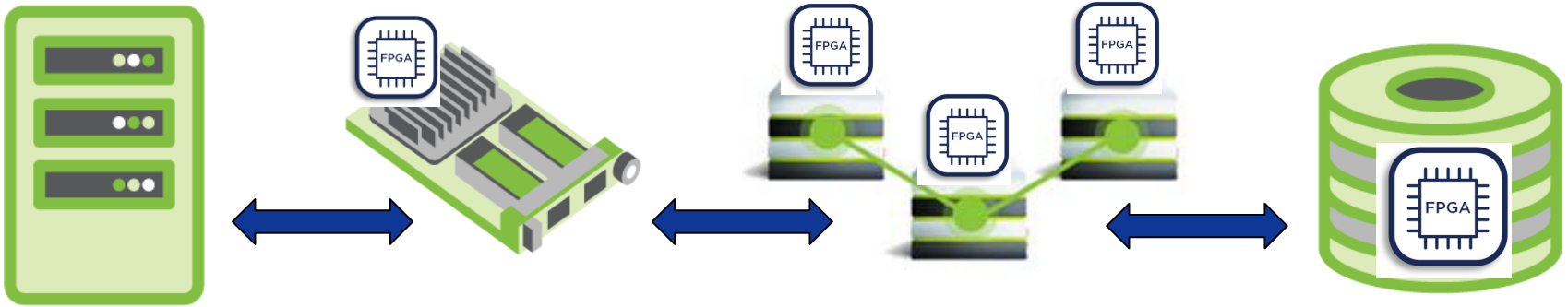


Converge Compute/Network/Storage



Line rate dataplane acceleration available throughout the system

Converge Compute/Network/Storage



Server Processors

NIC

Encryption/ Compression

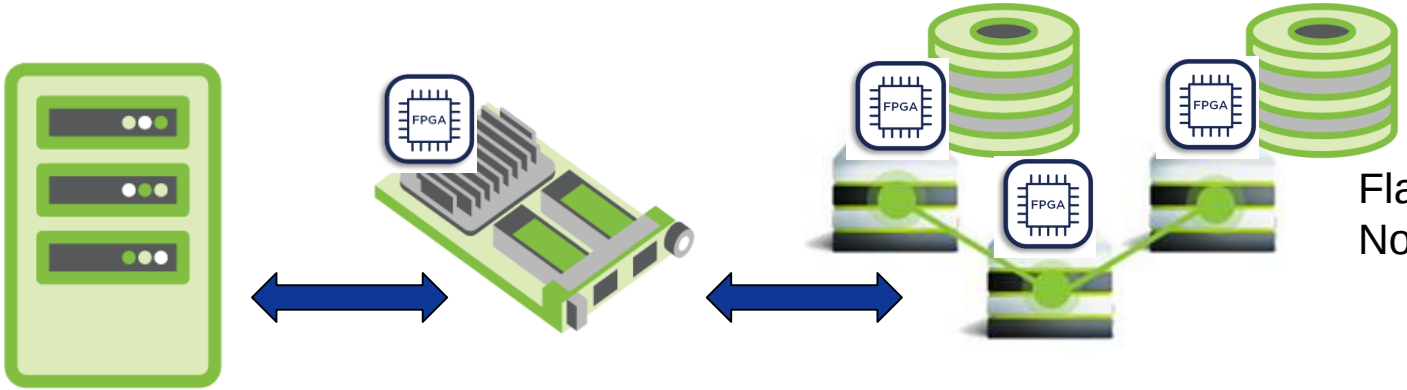
Network Switches

Reduction

Flash Storage Node

Regular Expression

Converge Compute/Network/Storage



Further Convergence

Challenges for FPGAs to Meet

- Networking capacity
  - Many high-speed Ethernet links
- Connectivity to host and storage
  - Multiple PCIe Gen 5 connections
- Ability to move bits around efficiently
  - Keep up with these massive pipes

Architecting an FPGA+

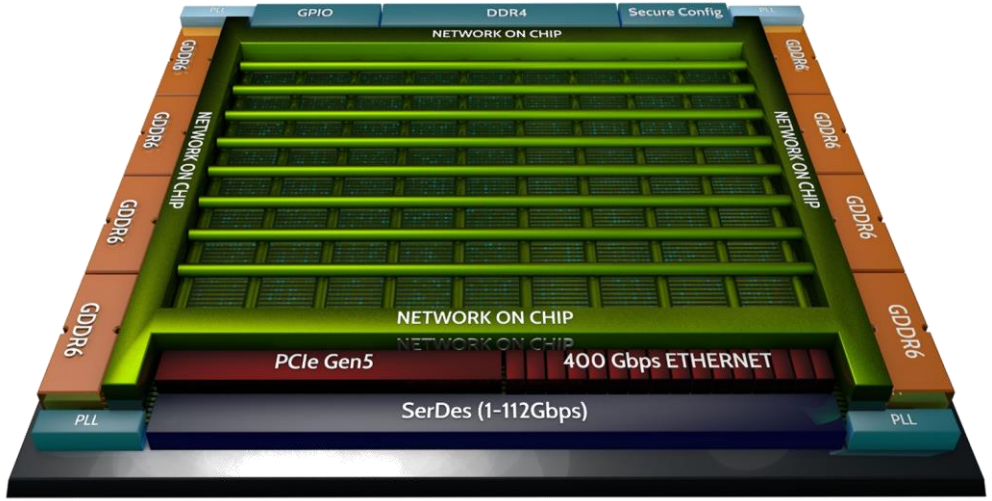
- Achronix has developed a new family of FPGAs
  - Leveraging TSMC's new 7nm technology
  - Multiple PCIe Gen5 ports (768Gbps PCIe bandwidth)
  - 4 x 400G or 16 x 100G Ethernet (1.6Tbps Ethernet)
  - 16 GDDR6 memory channels (4Tbps DRAM)

Network-on-chip (NoC) to tie it all together

FPGA NoC for Converged Solutions

Achronix Speedster7t

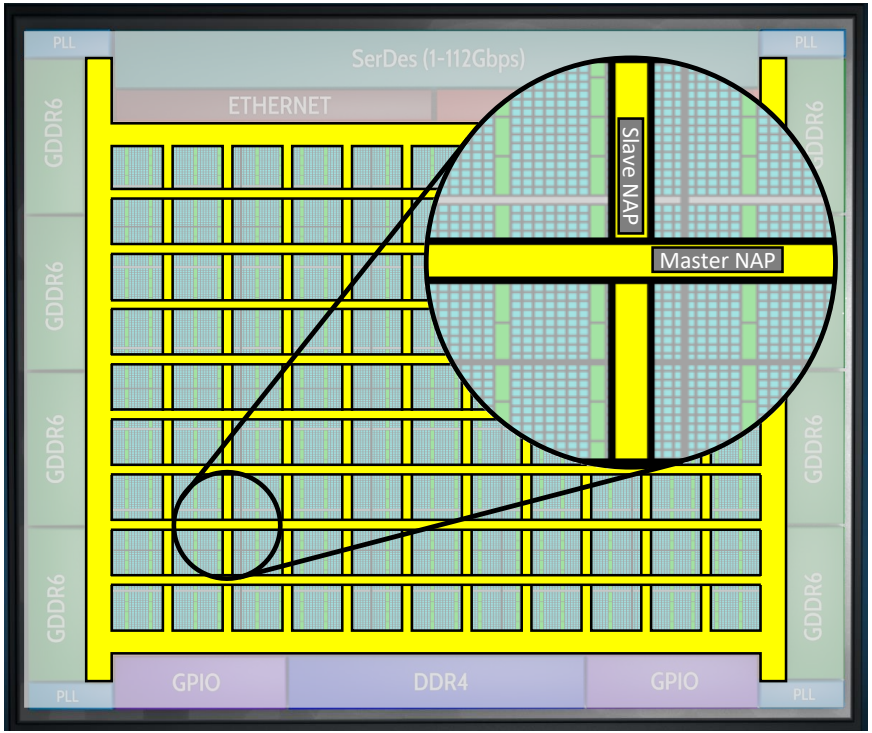
- Large contiguous FPGA core
- Dedicated controllers for high-speed connections
- Tied together with NoC
  - Packet based
  - Independent of FPGA routing fabric



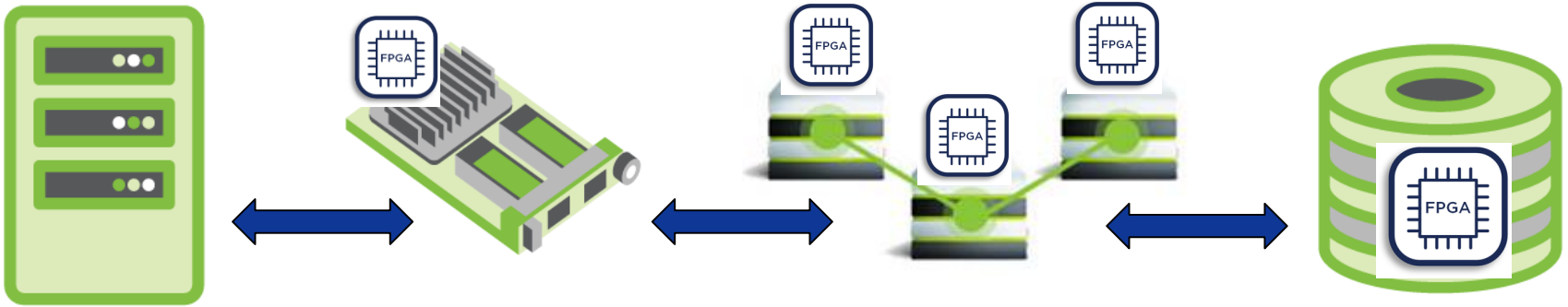
FPGA NoC for Converged Solutions

2-Dimensional NoC

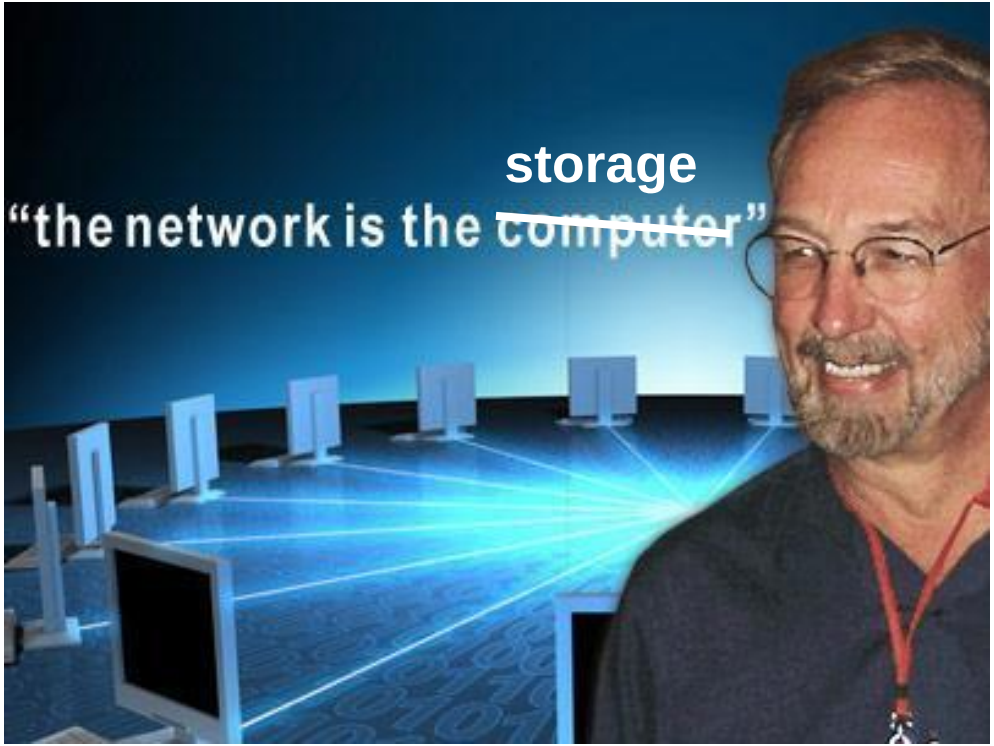
- Outer ring for traffic not involving FPGA
- Inner 2D mesh with 160 access points into the FPGA fabric
- 20Tbps bisectional bandwidth



Converge Compute/Network/Storage



Enabled by FPGA with efficient on-chip bandwidth to keep up with line rate scaling throughout the entire system



John Gage, former VP at Sun Microsystems

- Need efficient dataplane acceleration throughput
- FPGAs can enable the next generation of converged solutions